

# BLC10G18XS-360AVT

Power LDMOS transistor

Rev. 1 — 30 November 2017

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

360 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 1880 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$  in an asymmetrical Doherty demo circuit.  $V_{DS} = 28\text{ V}$ ;  $I_{DQ} = 650\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.6\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	28	56	17.0	50.5	-29.5 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

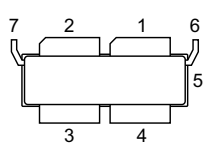
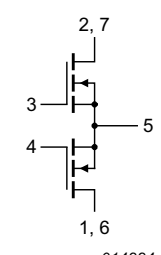
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1880 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source <sup>[1]</sup>		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G18XS-360AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-6	+9	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<sup>[1]</sup>	-	225	°C
$T_{case}$	case temperature	operating <sup>[1]</sup>	-40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 28 \text{ V}$ ; $I_{DQ} = 750 \text{ mA}$ (main); $V_{GS(amp)peak} = 0,65 \text{ V}$ ; $T_{case} = 80 \text{ °C}$		
		$P_L = 56 \text{ W}$	0.32	k/W
		$P_L = 74 \text{ W}$	0.29	k/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 120\text{ mA}$	1.5	2.0	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 600\text{ mA}$	-	2.2	-	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	20	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 9\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 6.0\text{ A}$	-	11.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 4.2\text{ A}$	-	120	148	$\text{m}\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.36\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 236\text{ mA}$	1.5	2.0	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 1500\text{ mA}$	-	2.2	-	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	38	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 9\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 11.8\text{ A}$	-	20.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 8.26\text{ A}$	-	70	88	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF;  
 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 1807.5\text{ MHz}$ ;  $f_2 = 1877.5\text{ MHz}$ ; RF performance at  
 $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 600\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in  
 an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 56\text{ W}$	14.6	15.4	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 56\text{ W}$	-	-12	-7	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 56\text{ W}$	46	50	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 56\text{ W}$	-	-30	-26	dBc

**Table 8. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF;  
 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 1807.5\text{ MHz}$ ;  $f_2 = 1877.5\text{ MHz}$ ; RF performance at  
 $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 600\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in  
 an asymmetrical Doherty production test circuit at a frequency of 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$PAR_O$	output peak-to-average ratio	$P_{L(AV)} = 56\text{ W}$	6.2	6.6	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)} = 56\text{ W}$	368	410	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLC10G18XS-360AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 32$  V;  $I_{DQ} = 600$  mA;  $V_{GS(amp)peak} = 0.5$  V;  $f = 1807.5$  MHz;  $P_L = 117$  W (5.5 dB OBO); 1-carrier W-CDMA, 100 % clipping.

### 7.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{DQ} = 670$  mA (main);  $V_{DS} = 28$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	$\eta_D$ [2]	G <sub>p</sub> [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
<b>Maximum power load</b>					
1800	1.0 – j4.5	1.3 – j2.7	190	63.4	16.8
1845	1.3 – j4.9	1.2 – j2.7	190	60.2	16.5
1880	1.6 – j5.3	1.2 – j2.9	190	59.1	16.4
<b>Maximum drain efficiency load</b>					
1805	1.0 – j4.5	2.0 – j2.0	155	71.5	18.5
1840	1.3 – j4.9	2.0 – j1.9	145	71.0	18.7
1880	1.6 – j5.3	2.1 – j1.8	135	70.0	19.0

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.

**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{DQ} = 1320$  mA (peak);  $V_{DS} = 28$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]	$\eta_D$ [2]	G <sub>p</sub> [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
<b>Maximum power load</b>					
1800	1.9 – j5.6	1.4 – j2.2	330	61.7	17.9
1845	2.9 – j6.4	1.4 – j2.3	330	60.6	18.0
1880	4.3 – j7.0	1.4 – j2.3	325	59.4	18.0
<b>Maximum drain efficiency load</b>					
1800	1.9 – j5.6	1.9 – j1.3	260	67.4	19.5
1845	2.9 – j6.4	2.9 – j6.4	260	67.3	19.7
1880	4.3 – j7.0	4.3 – j7.0	260	66.6	19.7

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.

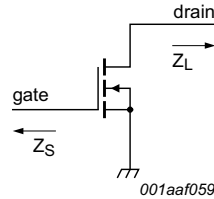


Fig 1. Definition of transistor impedance

### 7.3 Recommended impedances for Doherty design

**Table 11. Typical impedance of main at 1 : 1 load**

Measured load-pull data of main device;  $I_{DQ} = 670$  mA (main);  $V_{DS} = 28$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	$Z_S$ [1]	$Z_L$ [1]	$P_{L(3dB)}$ [2]	$\eta_D$ [2]	$G_p$ [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
1800	$1.3 - j4.1$	$1.5 - j3.2$	165	37.5	19.9
1845	$1.5 - j4.2$	$1.5 - j2.9$	170	38.0	19.9
1880	$1.7 - j4.5$	$1.5 - j2.6$	170	39.0	20.0

[1]  $Z_S$  and  $Z_L$  defined in Figure 1.

[2] At  $P_{L(AV)} = 56$  W.

**Table 12. Typical impedance of main device at 1 : 2.5 load**

Measured load-pull data of main device;  $I_{DQ} = 670$  mA (main);  $V_{DS} = 28$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	$Z_S$ [1]	$Z_L$ [1]	$P_{L(3dB)}$ [2]	$\eta_D$ [2]	$G_p$ [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
1800	$1.3 - j4.1$	$3.3 - j1.6$	100	55.9	22.6
1845	$1.5 - j4.2$	$3.3 - j1.4$	90	57.1	23.2
1880	$1.7 - j4.5$	$3.3 - j1.1$	85	57.5	23.5

[1]  $Z_S$  and  $Z_L$  defined in Figure 1.

[2] At  $P_{L(AV)} = 56$  W.

**Table 13. Typical impedance of peak device at 1 : 1 load**

Measured load-pull data of peak device;  $I_{DQ} = 1320$  mA (peak);  $V_{DS} = 28$  V; pulsed CW ( $t_p = 100$   $\mu$ s;  $\delta = 10$  %).

f	$Z_S$ [1]	$Z_L$ [1]	$P_{L(3dB)}$ [2]	$\eta_D$ [2]	$G_p$ [2]
(MHz)	( $\Omega$ )	( $\Omega$ )	(W)	(%)	(dB)
1800	$2.1 - j5.0$	$1.5 - j2.5$	275	26.0	21.5
1845	$2.9 - j5.6$	$1.4 - j2.3$	300	26.5	20.7
1880	$3.9 - j6.1$	$1.4 - j2.1$	295	27.4	21.2

[1]  $Z_S$  and  $Z_L$  defined in Figure 1.

[2] At  $P_{L(AV)} = 56$  W.

Table 14. Off-state impedances of peak device

f (MHz)	Z <sub>off</sub> (Ω)
1800	0.7 – j5.4
1845	0.9 – j6.1
1880	1.3 – j7.0

## 7.4 Test circuit

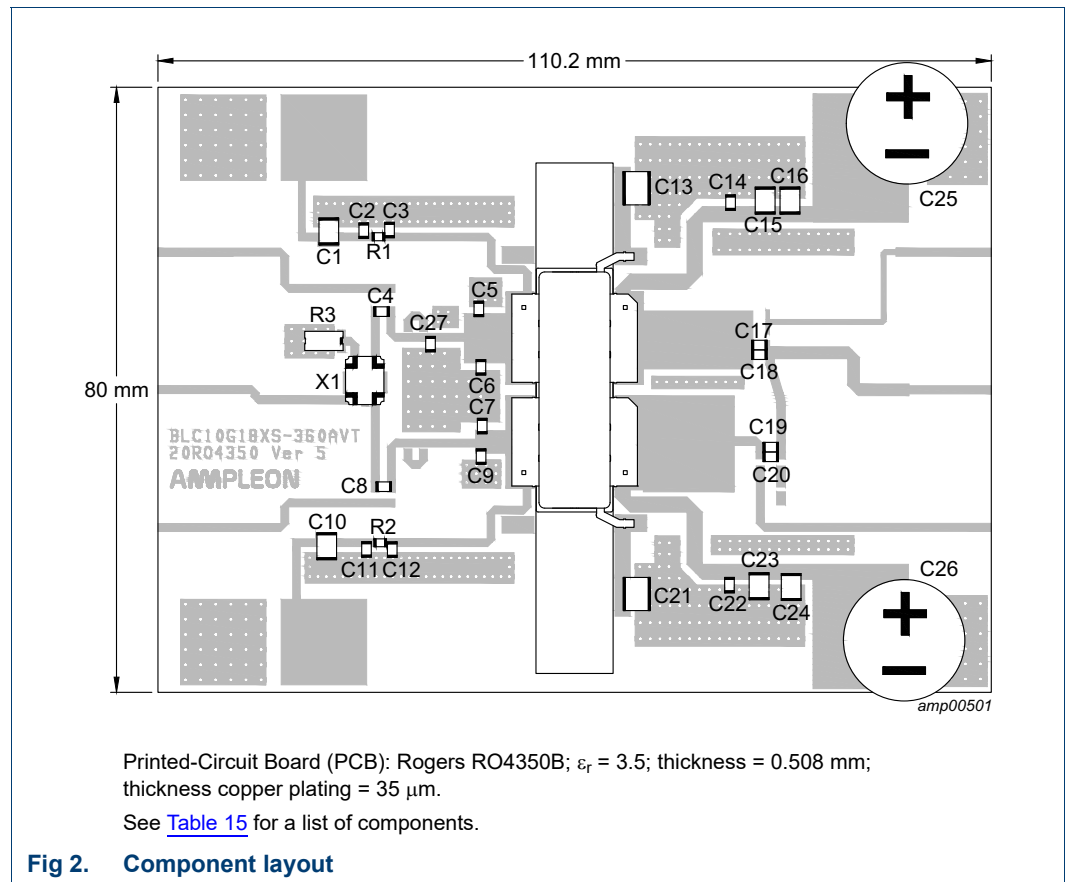


Table 15. List of components

See [Figure 2](#) for component layout.

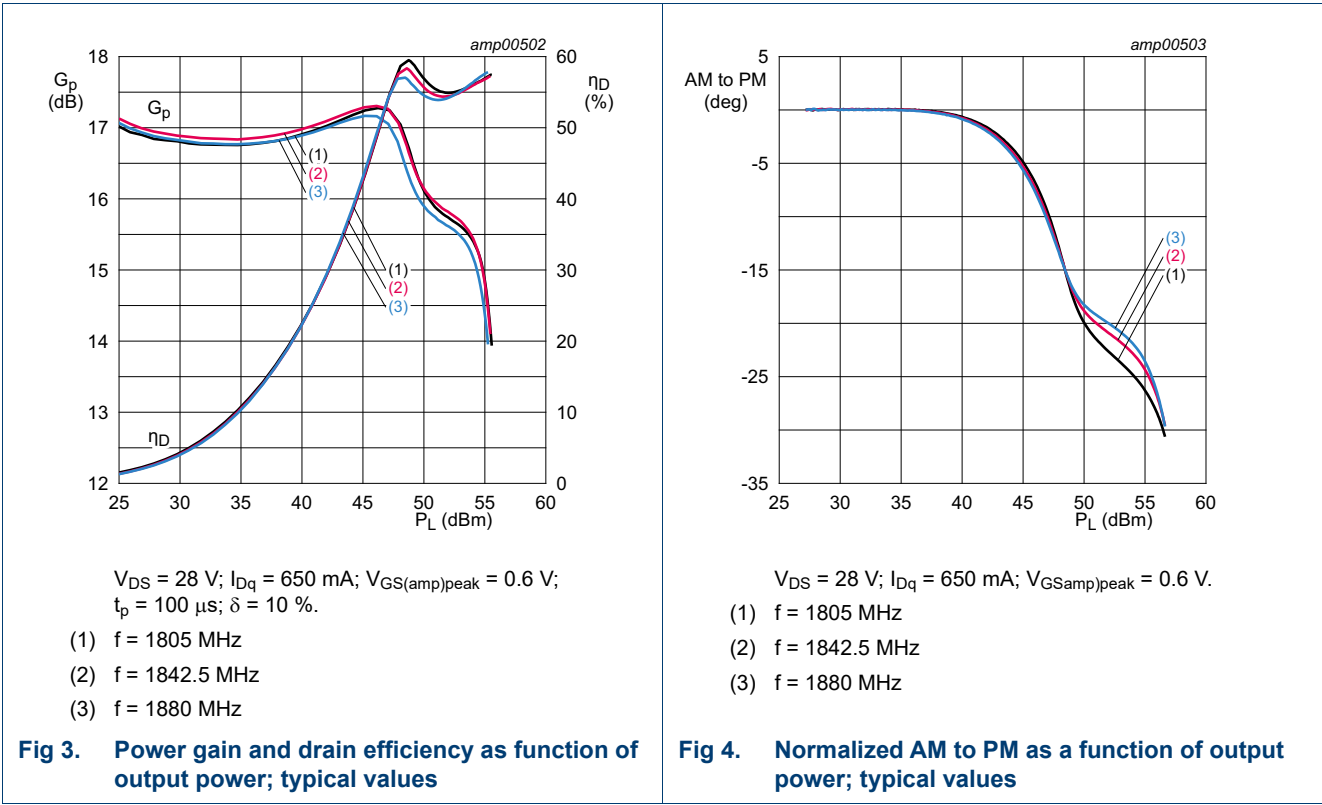
Component	Description	Value	Remarks
C1, C10, C15, C16, C23, C24	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	SMD 1210, Murata: GRM32ER71H475KA88L
C2, C11	multilayer ceramic chip capacitor	100 nF, 50 V	SMD 0805, Murata Hi-Q
C3, C4, C8, C12, C14, C19, C20, C22	multilayer ceramic chip capacitor	10 pF	SMD 0805, Murata Hi-Q
C5	multilayer ceramic chip capacitor	2.4 pF	SMD 0805, Murata Hi-Q
C6	multilayer ceramic chip capacitor	2.7 pF	SMD 0805, Murata Hi-Q
C7	multilayer ceramic chip capacitor	2.4 pF	SMD 0805, Murata Hi-Q
C9	multilayer ceramic chip capacitor	2.2 pF	SMD 0805, Murata Hi-Q
C13, C21	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	TDK: C5750X7R2A475KT/A

Table 15. List of components ...continued  
See Figure 2 for component layout.

Component	Description	Value	Remarks
C17, C18	multilayer ceramic chip capacitor	2.0 pF	SMD 0805, Murata Hi-Q
C25, C26	electrolytic capacitor	470 μF, 63 V	
C27	multilayer ceramic chip capacitor	1.2 pF	SMD 0805, Murata Hi-Q
R1, R2	resistor	4.7 Ω, 1 %	SMD 0805
R3	resistor	50 Ω, 25 W	Anaren: C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren Xinger III: X3C20F1-02

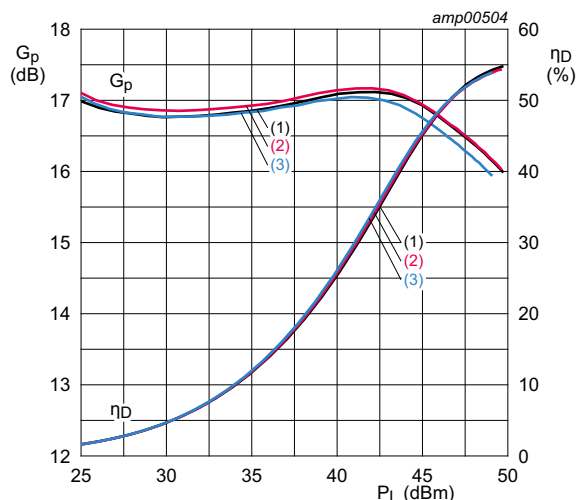
7.5 Graphical data

7.5.1 Pulsed CW



## 7.5.2 1-Carrier W-CDMA

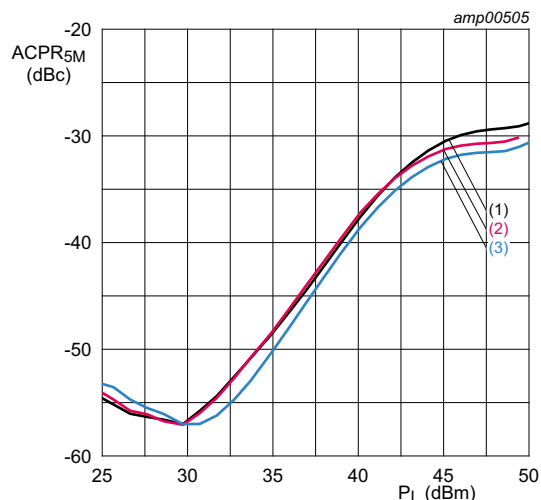
Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



$V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 650 \text{ mA}$ ;  $V_{GS(amp)peak} = 0.6 \text{ V}$ .

- (1)  $f = 1805 \text{ MHz}$
- (2)  $f = 1842.5 \text{ MHz}$
- (3)  $f = 1880 \text{ MHz}$

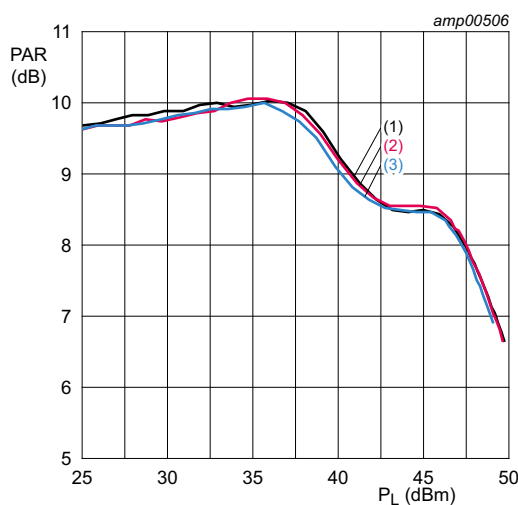
**Fig 5. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 650 \text{ mA}$ ;  $V_{GS(amp)peak} = 0.6 \text{ V}$ .

- (1)  $f = 1805 \text{ MHz}$
- (2)  $f = 1842.5 \text{ MHz}$
- (3)  $f = 1880 \text{ MHz}$

**Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values**



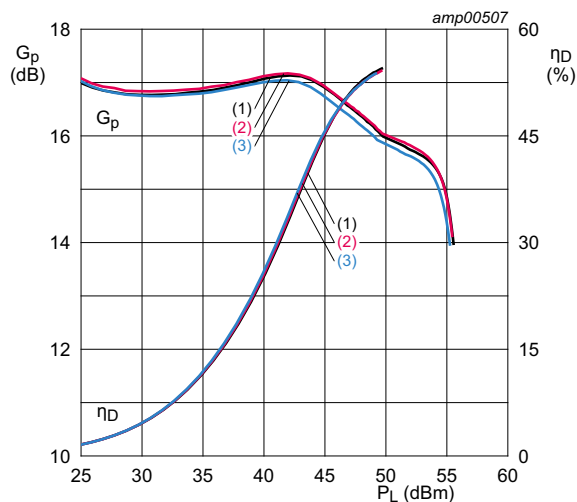
$V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 650 \text{ mA}$ ;  $V_{GS(amp)peak} = 0.6 \text{ V}$ .

- (1)  $f = 1805 \text{ MHz}$
- (2)  $f = 1842.5 \text{ MHz}$
- (3)  $f = 1880 \text{ MHz}$

**Fig 7. Peak-to-average power ratio as a function of output power; typical values**

### 7.5.3 2-Carrier W-CDMA

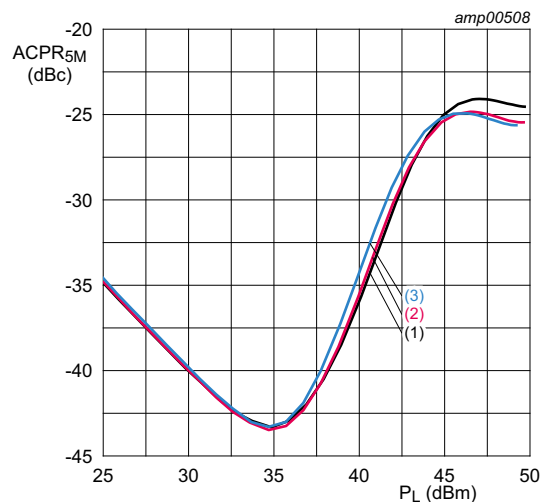
Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



$V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 650 \text{ mA}$ ;  $V_{GS(amp)peak} = 0.6 \text{ V}$ .

- (1)  $f = 1805 \text{ MHz}$
- (2)  $f = 1842.5 \text{ MHz}$
- (3)  $f = 1880 \text{ MHz}$

**Fig 8. Power gain and drain efficiency as function of output power; typical values**

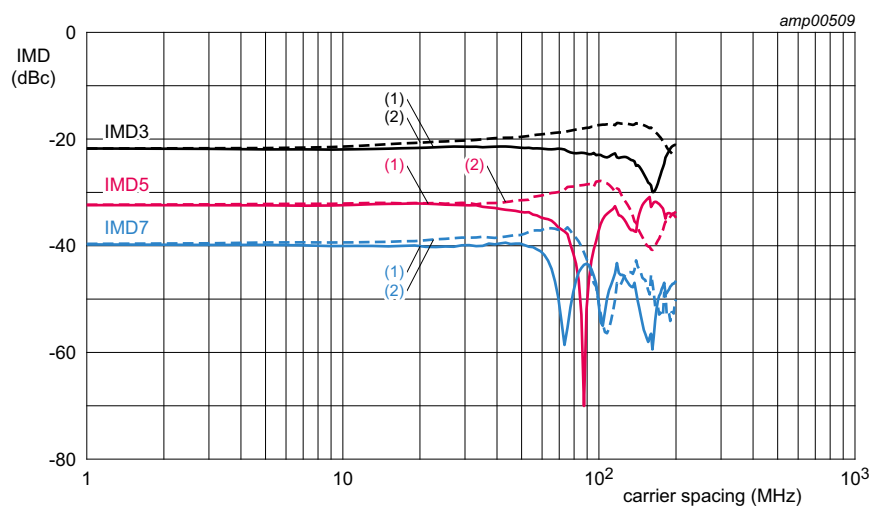


$V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 650 \text{ mA}$ ;  $V_{GS(amp)peak} = 0.6 \text{ V}$ .

- (1)  $f = 1805 \text{ MHz}$
- (2)  $f = 1842.5 \text{ MHz}$
- (3)  $f = 1880 \text{ MHz}$

**Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values**

### 7.5.4 2-Tone VBW

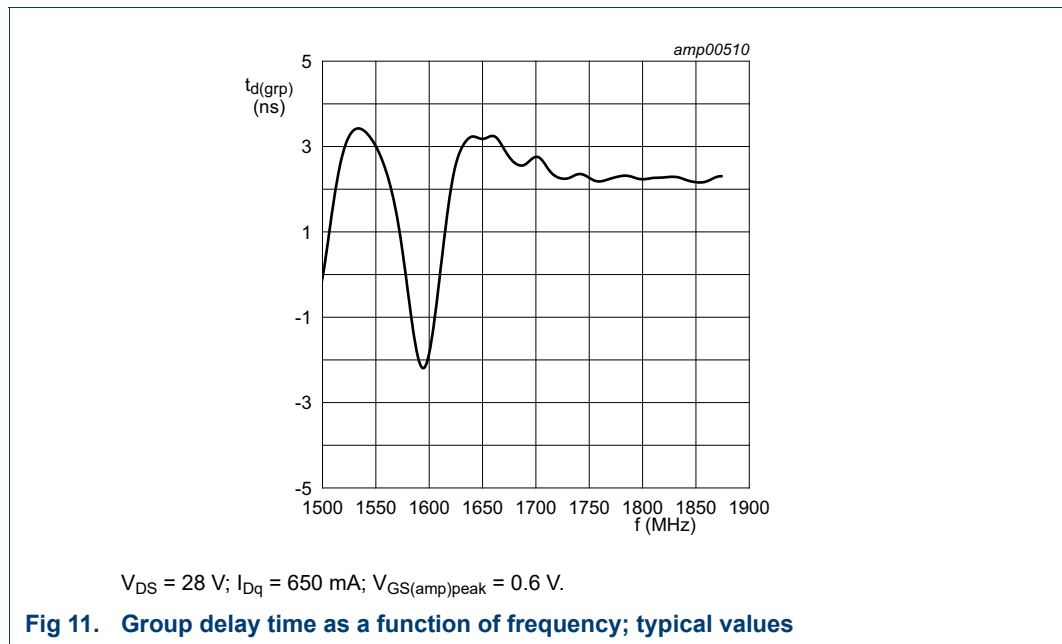


$V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 650 \text{ mA}$ ;  $V_{GS(amp)peak} = 0.6 \text{ V}$ .

- (1) IMD low
- (2) IMD high

**Fig 10. VBW capability**

### 7.5.5 Group delay



## 8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-4

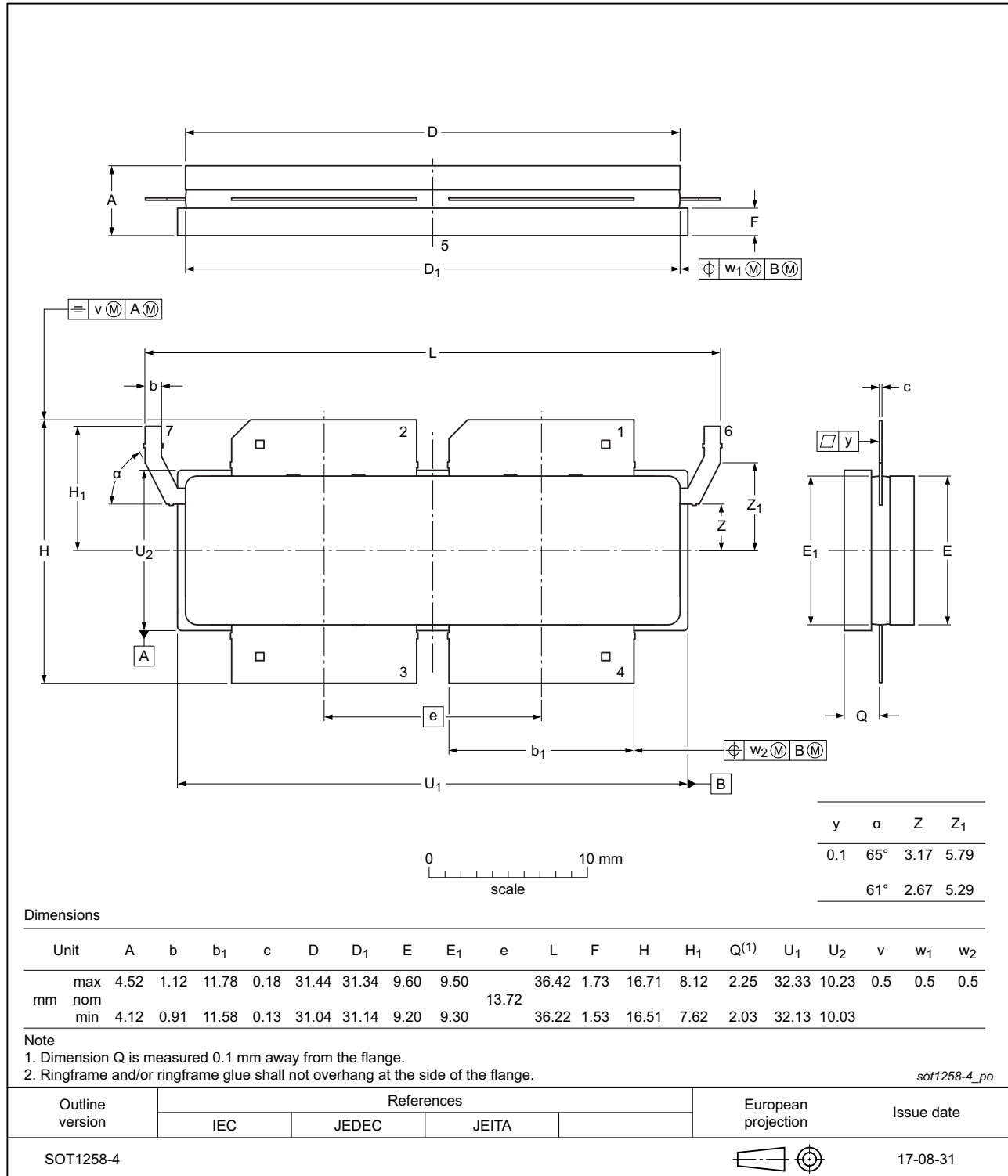


Fig 12. Package outline SOT1258-4

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G18XS-360AVT v.1	20171130	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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