

FEATURES

- 205 MSPS maximum conversion rate**
- 500 MHz programmable analog bandwidth**
- 0.5 V to 1.0 V analog input range**
- Less than 450 ps p-p PLL clock jitter @ 205 MSPS**
- 3.3 V power supply**
- Full sync processing**
- Sync detect for "hot plugging"**
- 2:1 analog input mux**
- 4:2:2 output format mode**
- Midscale clamping**
- Power-down mode**
- Low power: <1 W typical @ 205 MSPS**

APPLICATIONS

- RGB graphics processing**
- LCD monitors and projectors**
- Plasma display panels**
- Scan converters**
- Microdisplays**
- Digital TV**

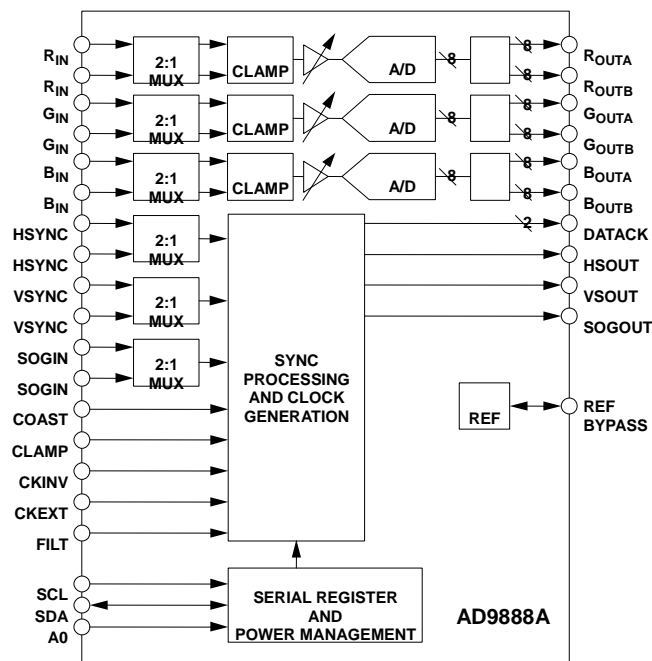


Figure 1.

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD9888A is a complete 7-bit 205 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 205 MSPS encode rate capability and full-power analog bandwidth of 500 MHz supports resolutions up to 1600 × 1200 (UXGA) at 75 Hz.

For ease of design and to minimize cost, the AD9888A is a fully integrated interface solution for flat panel displays. The AD9888A includes an analog interface with a 205 MHz triple ADC with an internal 1.25 V reference, PLL to generate a pixel clock from HSYNC and COAST, midscale clamping, and programmable gain, offset, and clamp controls. The user provides only a 3.3 V power supply, analog input, and HSYNC and COAST signals. Three-state CMOS outputs can be powered from 2.5 V to 3.3 V.

The AD9888A's on-chip PLL generates a pixel clock from HSYNC and COAST inputs. Pixel clock output frequencies range from 10 MHz to 205 MHz. PLL clock jitter is typically less

than 450 ps p-p at 205 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A sampling phase adjustment is provided. Data, HSYNC, and clock output phase relationships are maintained. The PLL can be disabled, and an external clock input can be provided as the pixel clock. The AD9888A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This device is fully programmable via a 2-wire serial port.

Fabricated in an advanced CMOS process, the AD9888A is provided in a space-saving 128-lead MQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range. The AD9888A is also available in a Pb-free package.

Rev. 0

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REVISION HISTORY

Rev.0 8/2011

AD9888A

SPECIFICATIONS

$V_D = 3.3\text{ V}$, $V_{DD} = 3.3\text{ V}$, ADC clock = maximum conversion rate.

Table 1.

| Parameter | Temp | Test Level | AD9888AKS-205 | | | Unit |
|-------------------------------|------|------------|---------------|------------|-------------------|--------|
| | | | Min | Typ | Max | |
| RESOLUTION | | | | 7 | | Bits |
| DC ACCURACY | | | | | | |
| Differential Nonlinearity | 25°C | I | | ±0.4 | +0.75/ −1.0 | LSB |
| | Full | VI | | | +0.9/ −1.0 | LSB |
| Integral Nonlinearity | 25°C | I | | ±0.5 | ±1.9 | LSB |
| | Full | VI | | | ±2.3 | LSB |
| No Missing Codes | 25°C | I | | Guaranteed | | |
| ANALOG INPUT | | | | | | |
| Input Voltage Range | | | | | | |
| Minimum | 25°C | I | | | 0.5 | V p-p |
| Maximum | 25°C | I | 1.0 | | | V p-p |
| Gain Tempco | 25°C | V | | 100 | | ppm/°C |
| Input Bias Current | 25°C | IV | | | 1 | μA |
| | Full | IV | | | 2 | μA |
| Input Capacitance | Full | V | | 3 | | pF |
| Input Resistance | Full | IV | 1 | | | M |
| Input Offset Voltage | Full | VI | | 7 | 90 | mV |
| Input Full-Scale Matching | Full | VI | | 2.5 | 9.0 | % FS |
| Offset Adjustment Range | Full | VI | 44 | 49 | 53 | % FS |
| REFERENCE OUTPUT | | | | | | |
| Output Voltage | Full | VI | 1.20 | 1.25 | 1.30 | V |
| Temperature Coefficient | Full | V | | ±50 | | ppm/°C |
| SWITCHING PERFORMANCE | | | | | | |
| Maximum Conversion Rate | Full | VI | 205 | | | MSPS |
| Minimum Conversion Rate | Full | IV | | | 10 | MSPS |
| Clock to Data Skew t_{skew} | Full | IV | −1.25 | | +1.25 | ns |
| t_{BUFF}^1 | Full | VI | 4.7 | | | μs |
| t_{STAH}^1 | Full | VI | 4.0 | | | μs |
| t_{DHO}^1 | Full | VI | 250 | | | ns |
| t_{DAL}^1 | Full | VI | 4.7 | | | μs |
| t_{DAH}^1 | Full | VI | 4.0 | | | μs |
| t_{DSU}^1 | Full | VI | 250 | | | ns |
| t_{STASU}^1 | Full | VI | 4.7 | | | μs |
| t_{STOSU}^1 | Full | VI | 4.0 | | | μs |
| HSYNC Input Frequency | Full | IV | 15 | | 110 | kHz |
| Maximum PLL Clock Rate | Full | VI | 205 | | | MHz |
| Minimum PLL Clock Rate | Full | IV | | | 10 | MHz |
| PLL Jitter | 25°C | IV | | 440 | 700 ⁴ | ps p-p |
| | Full | IV | | | 1000 ⁴ | ps p-p |
| Sampling Phase Tempco | Full | IV | | 15 | | ps/°C |

| | | | | | |
|----------------|------|--|--|--|--|
| DIGITAL INPUTS | Full | | | | |
|----------------|------|--|--|--|--|

| Parameter | Temp | Test Level | AD9888AKS-205 | | | Unit |
|---|------|------------|---------------|--------|------|------|
| | | | Min | Typ | Max | |
| Input Voltage, High (V_{IH}) | Full | VI | 2.5 | | | V |
| Input Voltage, Low (V_{IL}) | Full | VI | | | 0.8 | V |
| Input Current, High (I_{IH}) | Full | IV | | | −1.0 | μA |
| Input Current, Low (I_{IL}) | Full | IV | | | +1.0 | μA |
| Input Capacitance | 25°C | V | | 3 | | pF |
| DIGITAL OUTPUTS | | | | | | |
| Output Voltage, High (V_{OH}) | Full | VI | $V_D - 0.1$ | | | V |
| Output Voltage, Low (V_{OL}) | Full | VI | | | | V |
| Duty Cycle | Full | IV | 44 | 49 | 55 | % |
| DATAACK, $\overline{\text{DATAACK}}$ | Full | IV | | | | |
| Output Coding | Full | IV | | Binary | | |
| POWER SUPPLY | | | | | | |
| V_D Supply Voltage | Full | IV | 3.0 | 3.3 | 3.6 | V |
| V_{DD} Supply Voltage | Full | IV | 2.2 | 3.3 | 3.6 | V |
| P_{VD} Supply Voltage | Full | IV | 3.0 | 3.3 | 3.6 | V |
| I_D Supply Current (V_D) | 25°C | | | 230 | | mA |
| I_{DD} Supply Current (V_{DD}) ² | 25°C | | | 60 | | mA |
| I_{PVD} Supply Current (P_{VD}) | 25°C | | | 10 | | mA |
| Total Power Dissipation | Full | VI | | 990 | 1250 | mW |
| Power-Down Supply Current | Full | VI | | 12 | 20 | mA |
| Power-Down Dissipation | Full | VI | | 40 | 66 | mW |
| DYNAMIC PERFORMANCE | | | | | | |
| Analog Bandwidth, Full Power ³ | 25°C | V | | 500 | | MHz |
| Transient Response | 25°C | V | | 2 | | ns |
| Overvoltage Recovery Time | 25°C | V | | 1.5 | | ns |
| Signal-to-Noise Ratio (SNR) ⁴ | 25°C | IV | 40 | 42 | | dB |
| (Without Harmonics) | Full | V | | 41 | | dB |
| $f_{IN} = 40.7$ MHz | | | | | | |
| Crosstalk | Full | V | | 50 | | dBc |
| THERMAL CHARACTERISTICS | | | | | | |
| θ_{JC} —Junction-to-Case Thermal Resistance | | V | | 8.4 | | °C/W |
| θ_{JA} —Junction-to-Ambient Thermal Resistance | | V | | 35 | | °C/W |

¹ See Figure 25.² DEMUX = 1, DATAACK and $\overline{\text{DATAACK}}$ Load = 15 pF, data load = 5 pF.³ Maximum bandwidth setting. Bandwidth can also be programmed to 300 MHz, 150 MHz, and 75 MHz.⁴ Using external pixel clock.

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|------------------------------|-----------------|
| V_D | 3.6 V |
| V_{DD} | 3.6 V |
| Analog Inputs | V_D to 0.0 V |
| VREF IN | V_D to 0.0 V |
| Digital Inputs | 5 V to 0.0 V |
| Digital Output Current | 20 mA |
| Operating Temperature | –25°C to +85°C |
| Storage Temperature | –65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Maximum Case Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C; sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

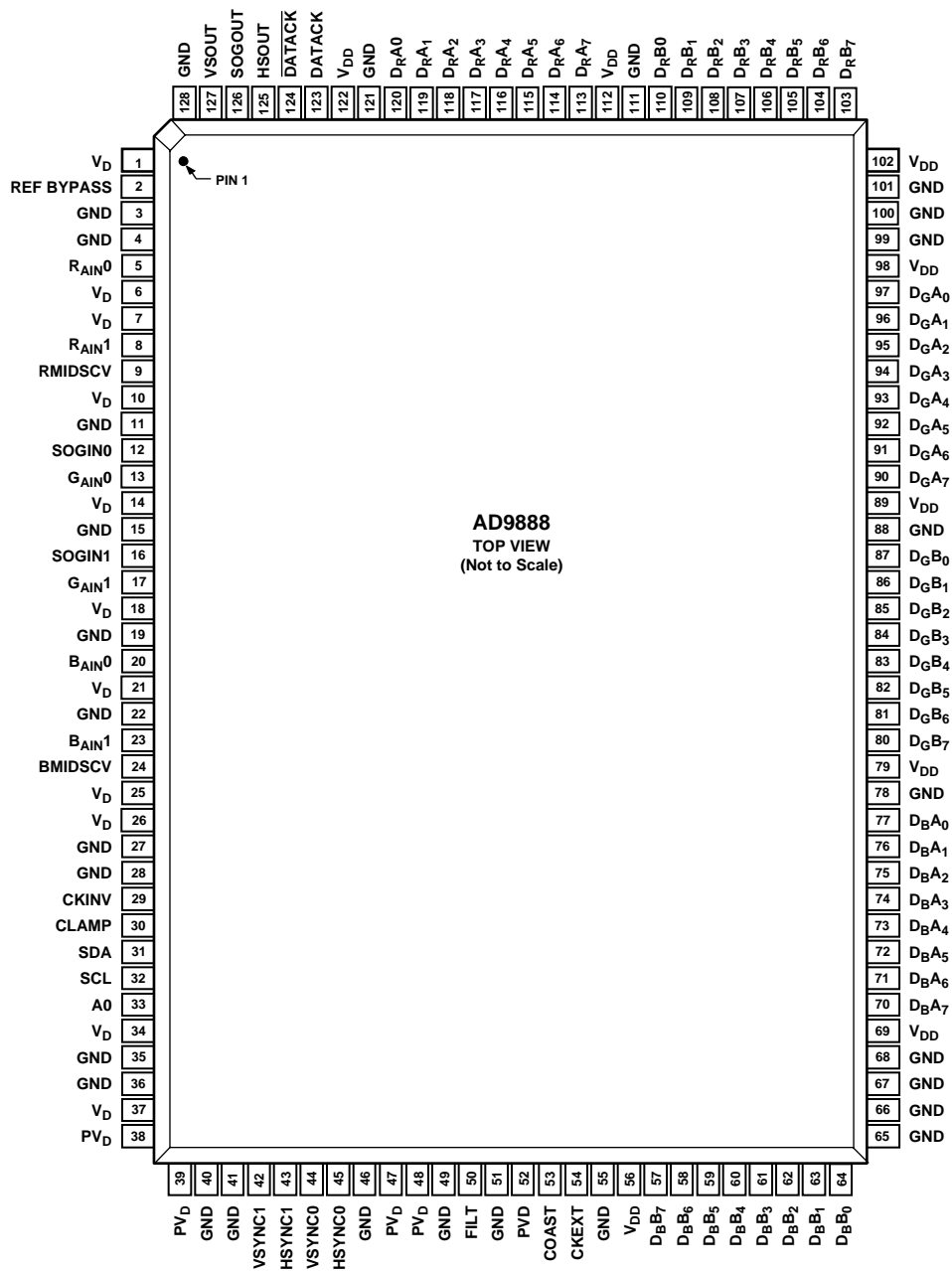


Figure 2. Pin Configuration

Table 3. Complete Pinout List

| Pin Type | Mnemonic | Description | Value | Pin No. |
|--|-----------------------------|---|----------------|------------|
| Analog Video Inputs | R _{AIN} 0 | Channel 0 Analog Input for Converter R. | 0.0 V to 1.0 V | 5 |
| | G _{AIN} 0 | Channel 0 Analog Input for Converter G. | 0.0 V to 1.0 V | 13 |
| | B _{AIN} 0 | Channel 0 Analog Input for Converter B. | 0.0 V to 1.0 V | 20 |
| | R _{AIN} 1 | Channel 1 Analog Input for Converter R. | 0.0 V to 1.0 V | 8 |
| | G _{AIN} 1 | Channel 1 Analog Input for Converter G. | 0.0 V to 1.0 V | 17 |
| | B _{AIN} 1 | Channel 1 Analog Input for Converter B. | 0.0 V to 1.0 V | 23 |
| Sync/Clock Inputs | HSYNC0 | Channel 0 Horizontal SYNC Input. | 3.3 V CMOS | 45 |
| | VSYNC0 | Channel 0 Vertical SYNC Input. | 3.3 V CMOS | 44 |
| | SOGIN0 | Channel 0 Sync-on-Green Input. | 0.0 V to 1.0 V | 12 |
| | HSYNC1 | Channel 1 Horizontal SYNC Input. | 3.3 V CMOS | 43 |
| | VSYNC1 | Channel 1 Vertical SYNC Input. | 3.3 V CMOS | 42 |
| | SOGIN1 | Channel 1 Sync-on-Green Input. | 0.0 V to 1.0 V | 16 |
| | CLAMP | Clamp Input (external CLAMP signal). | 3.3 V CMOS | 30 |
| | COAST | PLL Coast Signal Input. | 3.3 V CMOS | 53 |
| | CKEXT | External Pixel Clock Input (to bypass the PLL), or 10 kΩ to ground. | 3.3 V CMOS | 54 |
| | CKINV | ADC Sampling Clock Invert. | 3.3 V CMOS | 29 |
| Sync Outputs | HSOUT | HSYNC Output Clock (phase-aligned with DATAACK). | 3.3 V CMOS | 125 |
| | VSOUT | VSYNC Output Clock (phase-aligned with DATAACK). | 3.3 V CMOS | 127 |
| | SOGOUT | Sync-on-Green Slicer Output. | 3.3 V CMOS | 126 |
| | REF BYPASS | Internal Reference Bypass (bypass with 0.1 μF to ground). | 1.25 V ± 10% | 2 |
| Voltage Clamp Voltages | RMIDSCV | Red Channel Midscale Clamp Voltage Bypass. | | 9 |
| | BMIDSCV | Blue Channel Midscale Clamp Voltage Bypass. | | 24 |
| PLL Filter | FILT | Connection for External Filter Components for Internal PLL. | | 50 |
| Power Supply | V _D | Analog Power Supply. | 3.3 V ± 10% | |
| | V _{DD} | Output Power Supply. | 3.3 V ± 10% | |
| | PV _D | PLL Power Supply. | 3.3 V ± 10% | |
| | GND | Ground. | 0 V | |
| Serial Port (2-Wire Serial Interface) | SDA | Serial Port Data I/O. | 3.3 V CMOS | 31 |
| | SCL | Serial Port Data Clock. | 3.3 V CMOS | 32 |
| | A0 | Serial Port Address Input 1. | 3.3 V CMOS | 33 |
| Data Outputs | Red A[7:0] | Port A Outputs of Converter Red. Bit 7 is the MSB. | 3.3 V CMOS | 113 to 119 |
| | Red B[7:0] | Port B Outputs of Converter Red. Bit 7 is the MSB. | 3.3 V CMOS | 103 to 109 |
| | Green A[7:0] | Port A Outputs of Converter Green. Bit 7 is the MSB. | 3.3 V CMOS | 90 to 96 |
| | Green B[7:0] | Port B Outputs of Converter Green. Bit 7 is the MSB. | 3.3 V CMOS | 80 to 86 |
| | Blue A[7:0] | Port A Outputs of Converter Blue. Bit 7 is the MSB. | 3.3 V CMOS | 70 to 76 |
| | Blue B[7:0] | Port B Outputs of Converter Blue. Bit 7 is the MSB. | 3.3 V CMOS | 57 to 63 |
| Data Clock Output | DATAACK | Data Output Clock. | 3.3 V CMOS | 123 |
| | $\overline{\text{DATAACK}}$ | Data Output Clock Complement. | 3.3 V CMOS | 124 |

Table 4. Pin Function Descriptions

| Mnemonic | Description |
|---------------------|---|
| Inputs | |
| R _{AIN} 0 | Channel 0 Analog Input for Red. |
| G _{AIN} 0 | Channel 0 Analog Input for Green. |
| B _{AIN} 0 | Channel 0 Analog Input for Blue. |
| R _{AIN} 1 | Channel 1 Analog Input for Red. |
| G _{AIN} 1 | Channel 1 Analog Input for Green. |
| B _{AIN} 1 | Channel 1 Analog Input for Blue. |
| | These high impedance inputs accept red, green, and blue channel graphics signals, respectively. The six channels are identical and can be used for any color; colors are assigned for convenient reference. They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation. |
| HSYNC0 | Channel 0 Horizontal Sync Input. |
| HSYNC1 | Channel 1 Horizontal Sync Input. |
| | These inputs receive a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by Serial Register 0x0E, Bit 6 (Hsync polarity). Only the leading edge of Hsync is used by the PLL. The trailing edge is used for clamp timing only. When HSPOL = 0, the falling edge of Hsync is used. When HSPOL = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V. |
| VSYNC0 | Channel 0 Vertical Sync Input. |
| VSYNC1 | Channel 1 Vertical Sync Input. |
| | These are the inputs for vertical sync. |
| SOGIN0 | Channel 0 Sync-on-Green Input. |
| SOGIN1 | Channel 1 Sync-on-Green Input. |
| | This input is provided to assist with processing signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated, variable threshold level, which is nominally set to 0.15 V above the negative peak of the input signal. When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT. This is usually a composite sync signal, containing both vertical and horizontal sync information. When not used, this input should be left unconnected. For more details on this function and how it should be configured, see the Sync-on-Green Input section. |
| CLAMP | External Clamp Input. |
| | This logic input can be used to define the time during which the input signal is clamped to the reference dc level (to ground for RGB or to midscale for YUV). It should be used when the reference dc level is known to be present on the analog input channels, typically during a period following Hsync called the back porch. The CLAMP pin is enabled by setting the external clamp control (Register 0x0F, Bit 7) to 1 (default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the HSYNC input. The logic sense of this pin is controlled by the clamp polarity control (Register 0x0F, Bit 6). When not used, this pin should be grounded and the external clamp should be programmed to 0. |
| COAST | Clock Generator Coast Input (optional). |
| | This input can be used to stop the pixel clock generator from synchronizing with HSYNC while continuing to produce a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval or that include equalization pulses. The coast signal is usually not required for PC-generated signals. The logic sense of this pin is controlled by Register 0x0F, Bit 3 (coast polarity). When not used, either ground this pin and program the coast polarity to 1, or tie the pin high (to V _D through a 10 kΩ resistor) and program the coast polarity to 0. The coast polarity register bit defaults to 1 at power-up. |
| CKEXT | External Clock Input (Optional). |
| | This pin can be used to provide an external clock to the AD9888A in place of the clock internally generated from HSYNC. It is enabled by programming the external clock register to 1 (Register 0x15, Bit 0). When an external clock is used, all other internal functions operate normally. When unused, this pin should be tied through a 10 kΩ resistor to ground, and the external clock register should be programmed to 0. The clock phase adjustment still operates when an external clock source is used. |
| CKINV | Sampling Clock Inversion (optional). |
| | This pin can be used to invert the pixel sampling clock, which has the effect of shifting the sampling phase 180°. This supports the alternate pixel sampling mode, wherein higher frequency input signals (up to 410 MSPS) can be captured by first sampling the odd pixels, and then capturing the even pixels on the subsequent frame. This pin should be used only during blanking intervals (typically vertical blanking), because it might produce several samples of corrupted data during the phase shift. CKINV should be grounded when not used. |
| Outputs | |
| D _{RA} 6-0 | Data Output, Red Channel, Port A. |
| D _{RB} 6-0 | Data Output, Red Channel, Port B. |
| D _{GA} 6-0 | Data Output, Green Channel, Port A. |
| D _{GB} 6-0 | Data Output, Green Channel, Port B. |
| D _{BA} 6-0 | Data Output, Blue Channel, Port A. |
| D _{BB} 6-0 | Data Output, Blue Channel, Port B. |

AD9888A

| Mnemonic | Description |
|--|--|
| | Each channel has two ports. When the part is operated in single-channel mode (channel mode bit (Register 0x15, Bit 7) = 0), all data is presented to Port A, and Port B is placed in a high impedance state. Programming the channel mode bit to 1 establishes dual-channel mode, wherein alternate pixels are presented to Port A and Port B of each channel. These appear simultaneously; two pixels are presented at the time of every second input pixel when the output mode bit (Register 0x15, Bit 6) is set to 1 (parallel mode). When the output mode bit is set to 0, pixel data appear alternately on the two ports, one new sample with each incoming pixel (interleaved mode). In dual-channel mode, the first pixel after HSYNC is routed to Port A. The second pixel goes to Port B, the third to A, and so on. This can be reversed by setting the A/B invert bit to 1 (Register 0x15, Bit 5). The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATA _{CK} , $\overline{\text{DATA}}_{\text{CK}}$, and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. |
| DATA _{CK} , $\overline{\text{DATA}}_{\text{CK}}$ | Data Output Clock, Data Output Clock Complement. These are differential data clock output signals to be used to strobe the output data and HSOUT into external logic. They are produced by the internal clock generator and are synchronous with the internal pixel sampling clock. When the AD9888A is operated in single-channel mode, the output frequency is equal to the pixel sampling frequency. When operated in dual-channel mode, the clock frequency is half the pixel frequency, as is the output data frequency. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATA _{CK} , $\overline{\text{DATA}}_{\text{CK}}$, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained. Either or both signals can be used, depending on the timing mode and interface design used. |
| HSOUT | Horizontal Sync Output. This is a reconstructed, phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATA _{CK} , $\overline{\text{DATA}}_{\text{CK}}$, and Data, data timing with respect to horizontal sync can always be determined. |
| SOGOUT | Sync-on-Green Slicer Output. This pin can be programmed to output either the sync-on-green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Processing Block Diagram (Figure 27) to view how this pin is connected. Note that other than slicing off SOG, the output from this pin gets no other additional processing on the AD9888A. Vsync separation is performed via the sync separator. |
| REF BYPASS | Internal Reference BYPASS. The absolute accuracy of this reference is $\pm 4\%$, and the temperature coefficient is ± 50 ppm, which is adequate for most AD9888A applications. If higher accuracy is required, an external reference may be employed instead. |
| RMIDSCV | Red Channel Midscale Voltage Bypass. |
| BMIDSCV | Blue Channel Midscale Voltage Bypass. These bypasses for the internal midscale voltage references should each be connected to ground through 0.1 μF capacitors. The exact voltage varies with the gain setting of the blue channel. |
| FILT | External Filter Connection. For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node. |
| Power Supply | |
| V _D | Main Power Supply. These pins supply power to the main elements of the circuit. It should be as quiet and filtered as possible. |
| V _{DD} | Digital Output Power Supply. A large number of output pins (up to 52) switching at high speed (up to 110 MHz) generate significant power supply transients (noise). These supply pins are identified separately from the V _D pins, so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9888A is interfacing with lower voltage logic, V _{DD} can be connected to a lower supply voltage (as low as 2.5 V) for compatibility. |
| PV _D | Clock Generator Power Supply. The most sensitive portion of the AD9888A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide noise-free power to these pins. |
| GND | Ground. The ground return for all circuitry on the chip. It is recommended that the AD9888A be assembled on a single solid ground plane, with careful attention paid to ground current paths. |
| Serial Port (2-Wire) | For a full description of the 2-wire serial register and how it works, refer to the 2-Wire Serial Control Port section. |
| SDA | Serial Port Data I/O. |
| SCL | Serial Port Data Clock. |
| A0 | Serial Port Address Input 1 |

DESIGN GUIDE

GENERAL DESCRIPTION

The AD9888A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for HDTV monitors or for serving as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 205 MHz, or up to 340 MHz with an alternate pixel sampling mode.

The AD9888A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 650 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

INPUT SIGNAL HANDLING

The AD9888A has six high impedance analog input pins for the red, green, and blue channels. They accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or BNC connectors. The AD9888A should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At this point, the signal should be resistively terminated (to the signal ground return) and capacitively coupled to the AD9888A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance would be obtained with the widest possible signal bandwidth. The ultra wide bandwidth inputs of the AD9888A (500 MHz) would track the input signal continuously as it moved from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. The AD9888A can digitize graphics signals over a very wide range of frequencies (10 MHz to 205 MHz). Often characteristics that are beneficial at one frequency can be detrimental at another. Analog bandwidth is one such characteristic. For UXGA resolutions (up to 205 MHz), a very high analog bandwidth is desirable because of the fast input

signal slew rates. For VGA and lower resolutions (down to 12.5 MHz), a very high bandwidth is not desirable because it allows excess noise to pass through. To accommodate these varying needs, the AD9888A includes variable analog bandwidth control. Four settings are available (75 MHz, 150 MHz, 300 MHz, and 500 MHz), allowing the analog bandwidth to be matched with the resolution of the incoming graphics signal

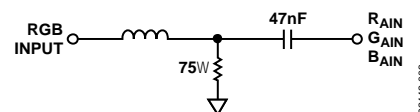


Figure 3. Analog Input Interface Circuit

SYNC PROCESSING OVERVIEW

The AD9888A circuitry enables it to accept composite sync inputs, such as sync-on-green or the trilevel sync inputs found in digital TV signals. A complete description of the sync processing functionality is found in the Sync Slicer and the Sync Separator sections.

HSYNC AND VSYNC INPUTS

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. It is possible to operate the AD9888A without applying Hsync (using an external clock, external clamp, and single port output mode), but a number of features of the chip will be unavailable; it is recommended that Hsync be provided. This can be either a sync signal directly from the graphics source, or a preprocessed TTL- or CMOS-level signal.

The Hsync input includes a Schmitt-trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphics systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required or desired.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

OUTPUT SIGNAL HANDLING

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

CLAMPING

RGB Clamping

To digitize the incoming signal properly, the dc offset of the

input must be adjusted to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground, black is at 300 mV, and white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9888A.

The key to clamping is to identify a time when the graphic system is known to be producing black. An offset is then introduced, which results in the ADCs producing a black output (Code 0x00) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most graphics systems, black is transmitted between active video lines. In CRT displays, when the electron beam has completed writing a horizontal line on the right side of the screen, the beam is deflected quickly to the left side of the screen (called horizontal retrace), and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is almost always a period following Hsync, called the back porch, when a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with External Clamp = 1). The polarity of this signal is set by the clamp polarity bit (Register 0x0F, Bit 6).

A simpler method of clamp timing employs the AD9888A internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration, Register 0x06) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync, because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to Register 0x08 (providing eight pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to Register 0x14 (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this

capacitor affects the performance of the clamp. If it is too small, there is a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it takes an excessively long time for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1/2 LSB in 10 lines with a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping

YUV graphics signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the video signal rather than at the bottom. For these signals it might be necessary to clamp to the midscale range of the ADC range (Register 0x80) rather than to bottom of the ADC range (Register 0x00).

Clamping to midscale rather than to ground can be accomplished by setting the clamp select bits in the series bus register. The red and blue channels each have their own selection bit so that they can be clamped to either midscale or ground independently. The clamp controls are located in Register 0x10, Bits 1 and 2. The midscale reference voltage that each ADC clamps to is provided independently on the RMIDSCV and BMIDSCV pins. These two pins should be bypassed to ground with a 0.1 μ F capacitor, even if midscale clamping is not required.

GAIN AND OFFSET CONTROL

The AD9888A can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain; Registers 0x08, 0x09, and 0x10, respectively). Increasing the gain setting results in an image with less contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (Red Offset, Green Offset, Blue Offset; Registers 0x0B, 0x0C, and 0x0D, respectively) provide independent settings for each channel.

The offset controls provide a ± 63 LSB adjustment range. This range is connected with the full-scale range. Therefore, if the input range is doubled (from 0.5 V to 1.0 V), the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 4 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale range is not affected, but the full-scale level is shifted by the same amount as the zero-scale level.

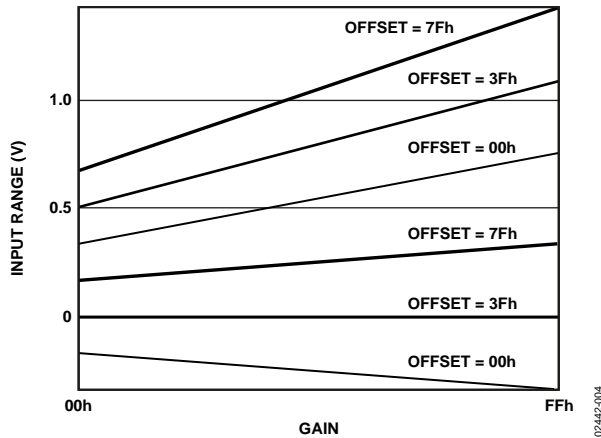


Figure 4. Gain and Offset Control

SYNC-ON-GREEN INPUT

The sync-on-green input operates in two steps. First, with the aid of a negative peak detector, it sets a baseline clamp level from the incoming video signal. Second, it sets the sync trigger level (nominally 150 mV above the negative peak). The exact trigger level is variable and can be programmed via Register 0x11. The sync-on-green input must be ac-coupled to the green analog input through its own capacitor, as shown in Figure 5. The value of the capacitor must be $1 \text{ nF} \pm 20\%$. If sync-on-green input is not used, this connection is not required and the SOGIN pin should be left unconnected. (Note that the sync-on-green signal is always negative polarity.) For more details, see the Sync Processing Overview section.

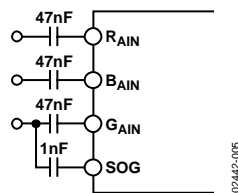


Figure 5. Typical Clamp Configuration for RGB/YUV Applications

CLOCK GENERATION

A phase-locked loop (PLL) is employed to generate the pixel clock. The Hsync input provides a reference frequency to the PLL. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (Registers 0x01 and 0x02) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is very important for providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling to a new value. Then, the input voltage is stable until the signal slews to a new value (Figure 6). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC, the bandwidth of the transmission system (cable and termination), and the overall

pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling times are likewise fixed. These times must be subtracted from the total pixel period to determine the stable period. At higher pixel frequencies, both the total cycle time and stable pixel time are shorter.

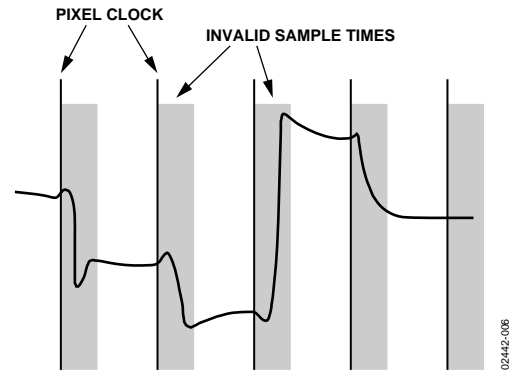


Figure 6. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined, and must be subtracted from the stable pixel time. The AD9888A's clock generation circuit is designed to minimize jitter to less than 9% of the total pixel time in all operating modes, making its effect on valid sampling time negligible (see Figure 7).

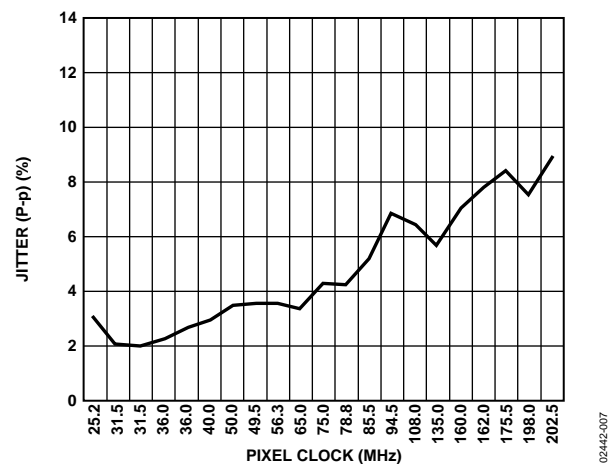


Figure 7. Pixel Clock Jitter vs. Frequency

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is illustrated in Figure 8.

Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table 5.

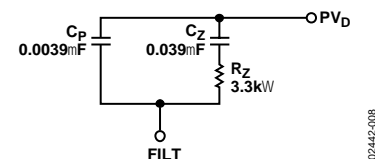


Figure 8. PLL Loop Filter Detail

Table 5. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

| Standard | Resolution | Refresh Rate (Hz) | Horizontal Frequency (kHz) | Pixel Rate (MHz) | VCORNGE | Current |
|----------|-------------|-------------------|----------------------------|----------------------|---------|---------|
| VGA | 640 × 480 | 60 | 31.5 | 25.175 | 00 | 010 |
| | | 72 | 37.7 | 31.500 | 00 | 100 |
| | | 75 | 37.5 | 31.500 | 00 | 100 |
| | | 85 | 43.3 | 36.000 | 00 | 100 |
| SVGA | 800 × 600 | 56 | 35.1 | 36.000 | 00 | 100 |
| | | 60 | 37.9 | 40.000 | 00 | 101 |
| | | 72 | 48.1 | 50.000 | 01 | 011 |
| | | 75 | 46.9 | 49.500 | 01 | 011 |
| | | 85 | 53.7 | 56.250 | 01 | 011 |
| XGA | 1024 × 768 | 60 | 48.4 | 65.000 | 01 | 100 |
| | | 70 | 56.5 | 75.000 | 01 | 100 |
| | | 75 | 60.0 | 78.750 | 01 | 101 |
| | | 80 | 64.0 | 85.500 | 10 | 011 |
| | | 85 | 68.3 | 94.500 | 10 | 011 |
| SXGA | 1280 × 1024 | 64.0 | 64.0 | 108.000 | 10 | 011 |
| | | 80.0 | 80.0 | 135.000 | 10 | 100 |
| | | 91.1 | 91.1 | 157.500 | 11 | 100 |
| UXGA | 1600 × 1200 | 60 | 75.0 | 162.000 | 11 | 100 |
| | | 65 | 81.3 | 175.000 | 11 | 100 |
| | | 70 | 87.5 | 189.000 | 11 | 101 |
| | | 75 | 93.8 | 202.500 | 11 | 101 |
| | | 85 | 106.3 | 229.500 ¹ | 10 | 110 |
| QXGA | 2048 × 1536 | 60 | 96.8 | 260.000 ¹ | 11 | 100 |
| | 2048 × 1536 | 75 | 120.0 | 315.000 ¹ | 11 | 100 |
| TV Modes | 480i | 60 | 15.75 | 13.510 | 00 | 000 |
| | 480p | 60 | 31.47 | 27.000 | 00 | 011 |
| | 720p | 60 | 45.0 | 74.250 | 01 | 011 |
| | 1080i | 60 | 33.75 | 74.250 | 01 | 011 |
| | 1080p | 60 | 33.75 | 148.500 | 10 | 011 |

¹ Graphics sampled at half the incoming pixel rate using Alternate Pixel Sampling mode.

Four programmable registers are provided to optimize the performance of the PLL:

1. The 12-Bit Divisor Registers. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 10 MHz to 205 MHz. The Divisor register controls the exact multiplication factor. This register can be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-Bit VCO Range Register. To lower the sensitivity of the output frequency to noise on the control signal, the VCO operating frequency range is divided into four overlapping regions. The VCO Range register sets this operating range. Because there are only four possible regions, only the two least significant bits of the VCO Range register are used. The frequency ranges for the lowest and highest regions are shown in Table 6.

Table 6. VCO Frequency Ranges

| PV1 | PV0 | Pixel Clock Range (MHz) | KVCO Gain (MHz/V) |
|-----|-----|-------------------------|-------------------|
| 0 | 0 | 10 to 41 | 150 |
| 0 | 1 | 41 to 82 | 150 |
| 1 | 0 | 82 to 150 | 150 |
| 1 | 1 | 150+ | 180 |

3. The 3-Bit Charge Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table 7.

Table 7. Charge Pump Current/Control Bits

| Ip2 | Ip1 | Ip0 | Current(μA) |
|-----|-----|-----|-------------|
| 0 | 0 | 0 | 50 |
| 0 | 0 | 1 | 100 |
| 0 | 1 | 0 | 150 |
| 0 | 1 | 1 | 250 |
| 1 | 0 | 0 | 350 |
| 1 | 0 | 1 | 500 |
| 1 | 1 | 0 | 750 |
| 1 | 1 | 1 | 1500 |

4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjustment is still available if the pixel clock is being provided externally.

The COAST pin is used to allow the PLL to continue to run at the same frequency in the absence of the incoming Hsync signal. This can be used during the vertical sync period, or any other time that the Hsync signal is unavailable. The polarity of the COAST signal can be set through the COAST Polarity register. Also, the polarity of the Hsync signal can be set through the Hsync Polarity register.

ALTERNATE PIXEL SAMPLING MODE

A Logic 1 input on Clock Invert (CKINV, Pin 29) inverts the nominal ADC clock. CKINV can be switched between frames to implement the alternate pixel sampling mode. This allows higher effective image resolution to be achieved at lower pixel rates, but with lower frame rates.

On one frame, only even pixels are digitized. On the subsequent frame, odd pixels are sampled. By reconstructing the entire frame in the graphics controller, a complete image can be reconstructed. This is similar to the interlacing process employed in broadcast television systems, but the interlacing is vertical instead of horizontal. The frame data is still presented to the display at the full desired refresh rate (usually 60 Hz), so there are no flicker artifacts added.

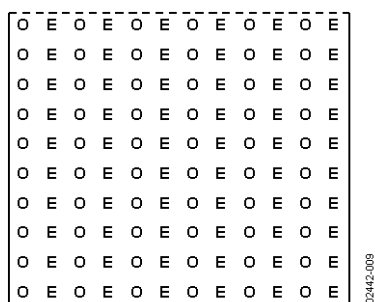


Figure 9. Odd and Even Pixels in a Frame

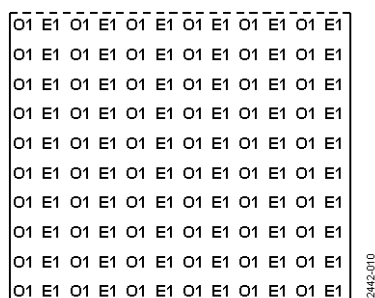


Figure 10. Odd Pixels from Frame 1

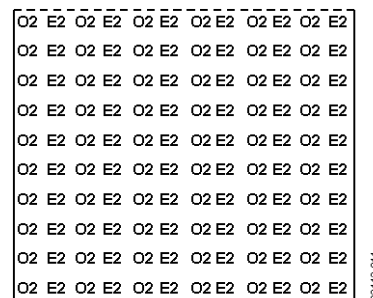


Figure 11. Even Pixels from Frame 2



Figure 12. Combined Frame Output from Graphics



Figure 13. Subsequent Frame from Controller

TIMING

Figures 15 through 24 show the operation of the AD9888A analog interface in all clock modes. The part establishes timing by sending the pixel corresponding with the leading edge of Hsync to the A data port. In dual-channel mode, the next sample is to the B port. Subsequent samples are alternated between the A and B data ports. In single-channel mode, data is sent only to the A data port, and the B port is placed in a high impedance state. The output data clock signal is created so that its rising edge always occurs between transitions of the A port data, and can be used to latch the output data externally.

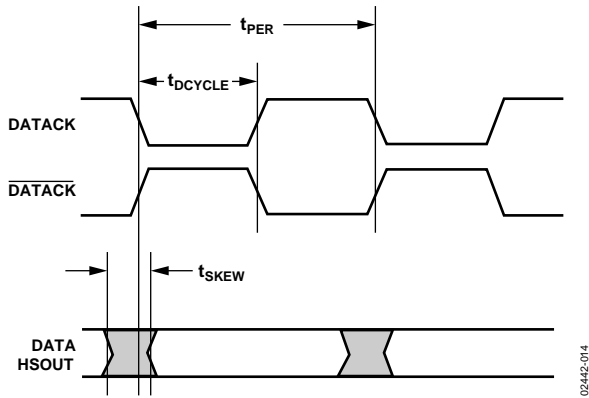


Figure 14. Output Timing

Hsync Timing

Horizontal sync is processed in the AD9888A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted with respect to Hsync through a full 360° in 32 steps via the Phase Adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOULT) and data clock (DATAACK).

Three things happen to horizontal sync in the AD9888A. First, the polarity of Hsync input is determined and thus has a known output polarity. The known output polarity can be programmed

either active high or active low (Register 0x0E, Bit 5). Second, HSOULT is aligned with DATAACK and data outputs. Third, the duration of HSOULT (in pixel clocks) is set via Register 0x07. HSOULT is the sync signal that should be used to drive the rest of the display system.

COAST Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used. In some systems, however, Hsync is disturbed during the vertical sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ composite sync (Csync) or embedded sync-on-green (SOG) signals, Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock to this new frequency and changes frequency by the end of the Vsync period. It then requires a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a “tearing” of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and holds the clock at its current frequency. The PLL can operate in this manner for several lines without significant frequency drift.

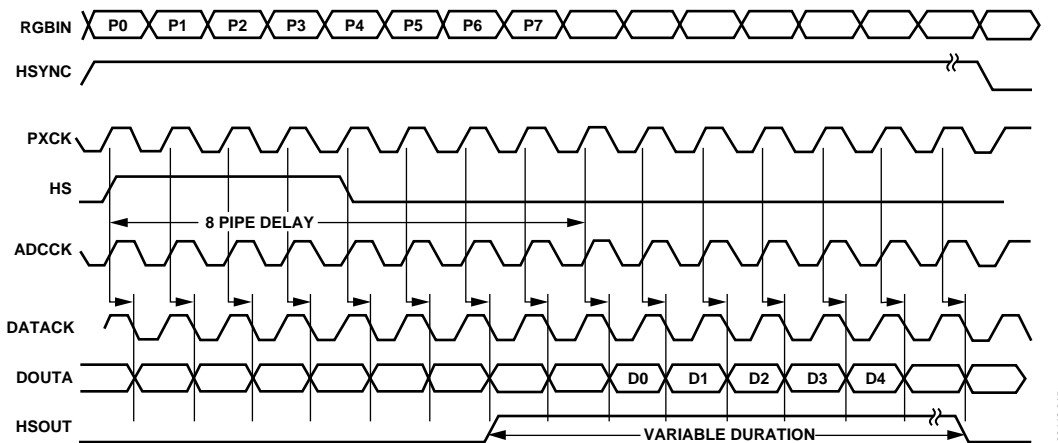


Figure 15. Single-Channel Mode

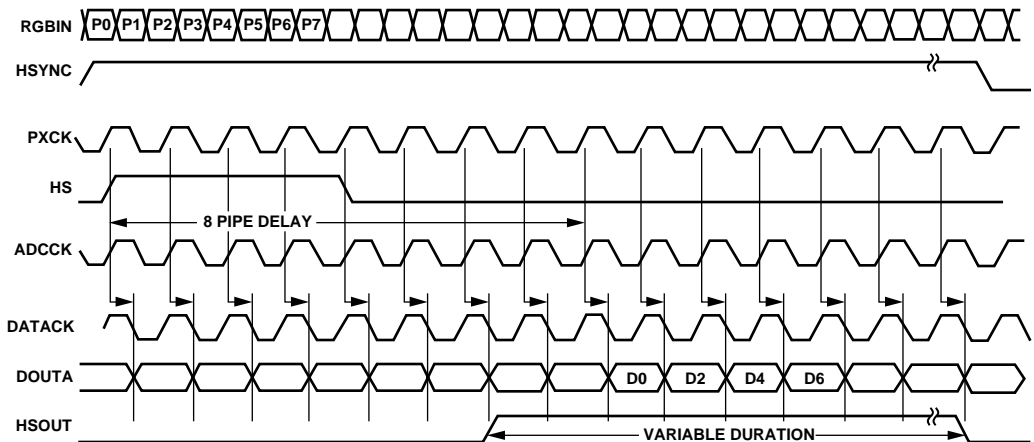


Figure 16. Single-Channel Mode, Two Pixels/Clock (Even Pixels)

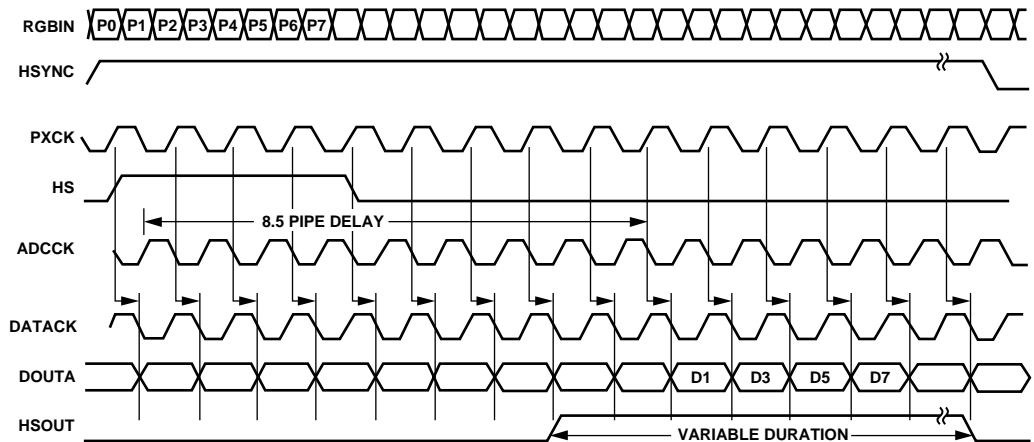


Figure 17. Single-Channel Mode, Two Pixels/Clock (Odd Pixels)

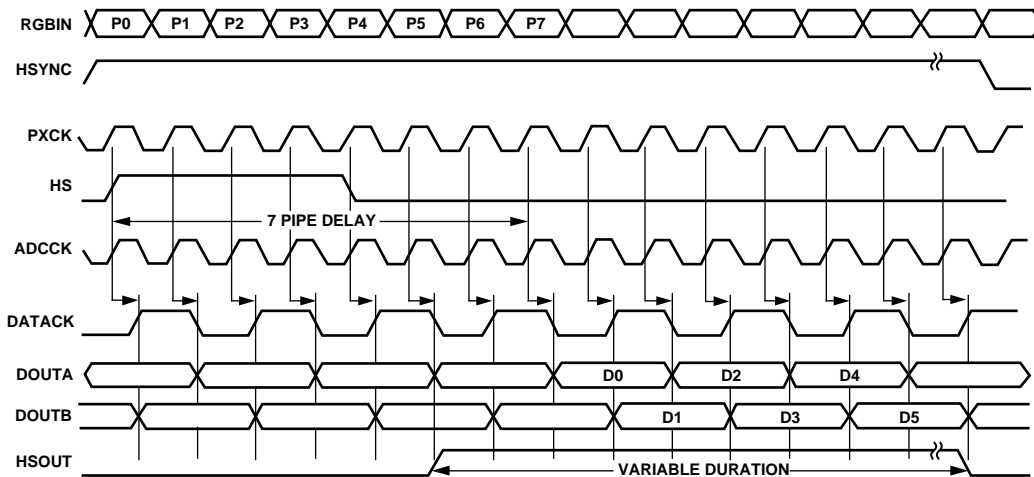


Figure 18. Dual-Channel Mode, Interleaved Outputs

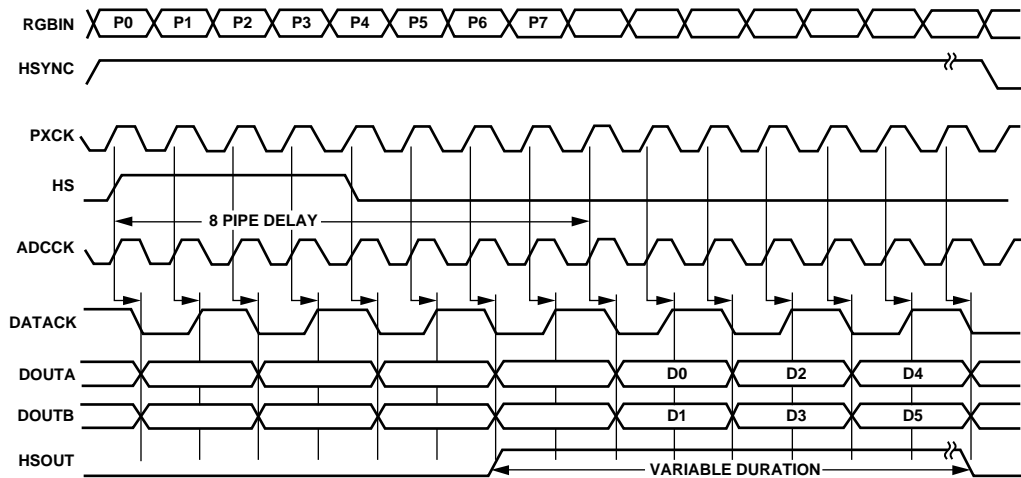


Figure 19. Dual-Channel Mode, Parallel Outputs

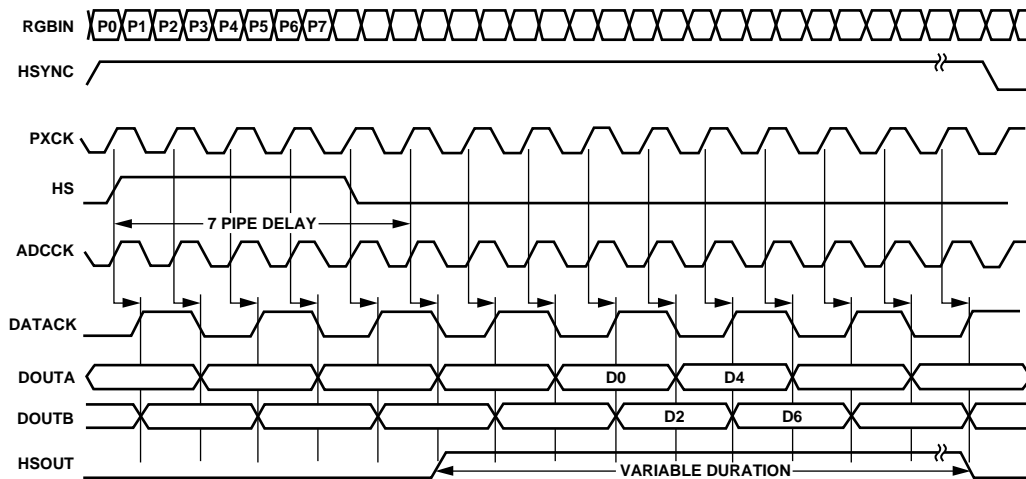


Figure 20. Dual-Channel Mode, Interleaved Outputs, Two Pixels/Clock (Even Pixels)

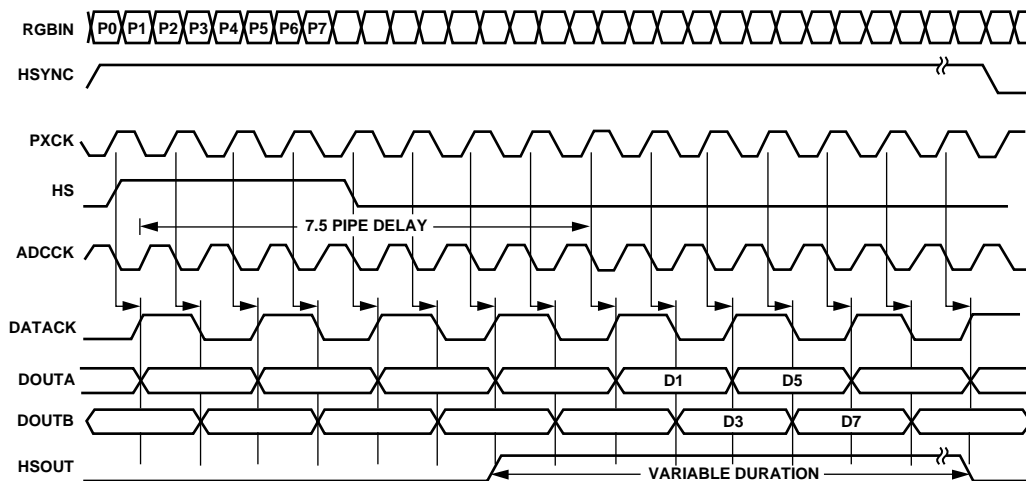


Figure 21. Dual-Channel Mode, Interleaved Outputs, Two Pixels/Clock (Odd Pixels)

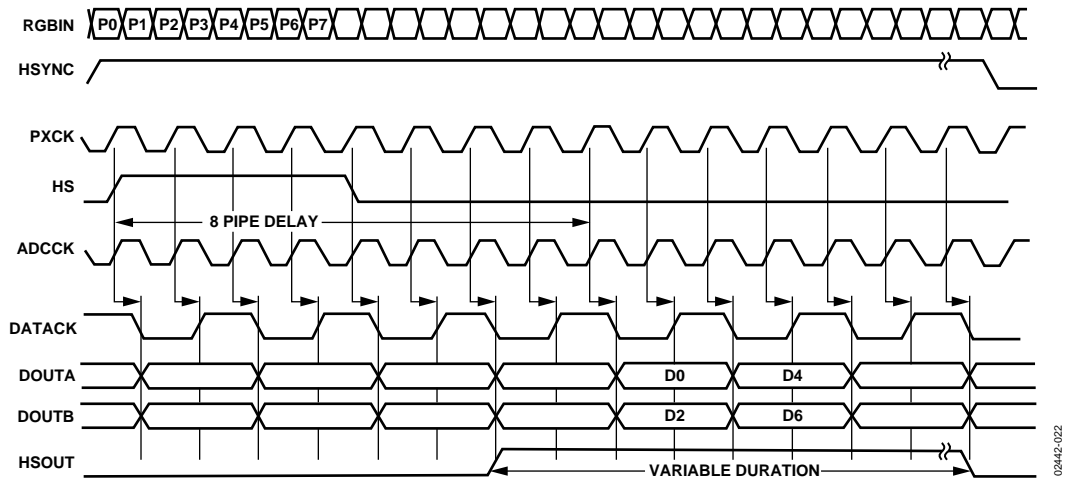


Figure 22. Dual-Channel Mode, Parallel Outputs, Two Pixels/Clock (Even Pixels)

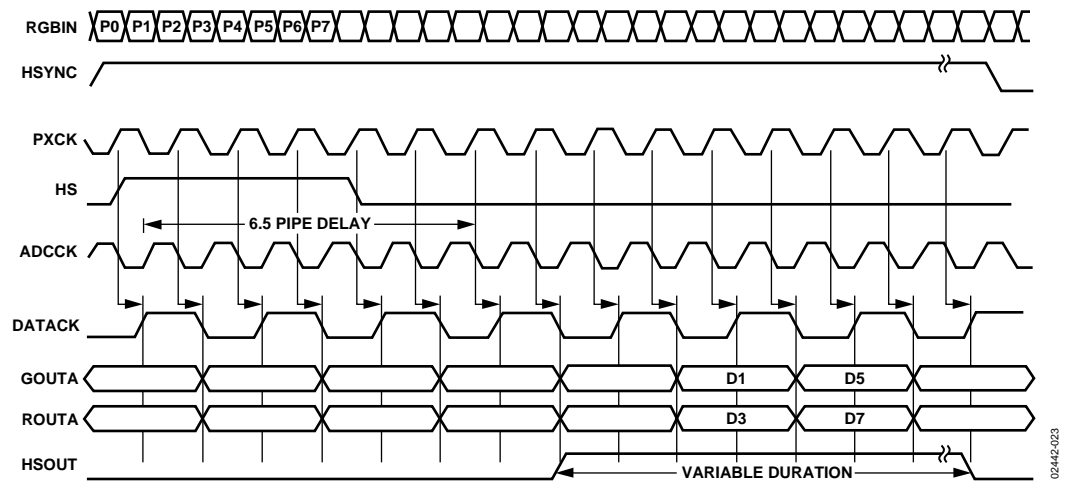


Figure 23. Dual-Channel Mode, Parallel Outputs, Two Pixels/Clock (Odd Pixels)

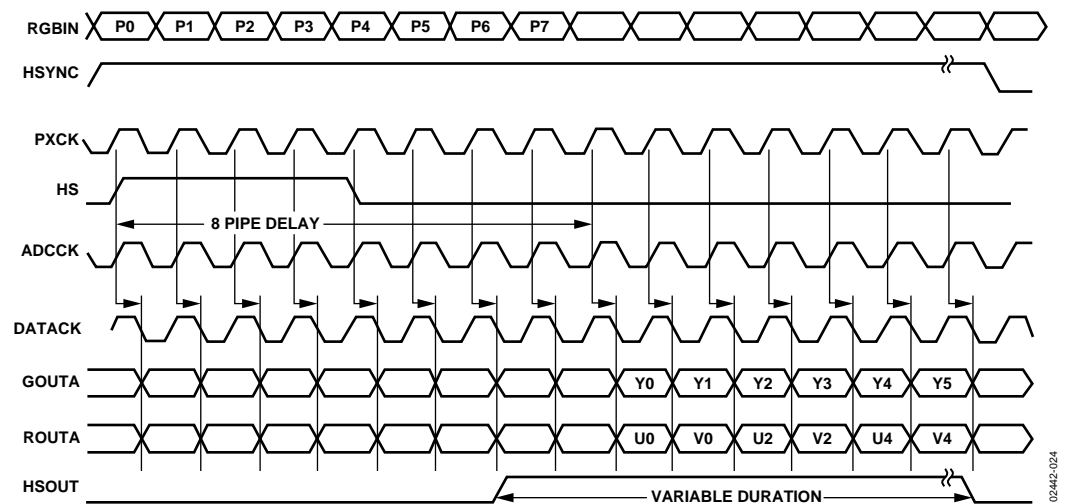


Figure 24. 4:2:2 Output Mode

2-WIRE SERIAL REGISTER MAP

The AD9888A is initialized and controlled by a set of registers that determine the operating modes. An external controller is employed to write and read the Control registers through the 2-line serial interface port.

Table 8. Control Register Map

| Hex Address | Read and Write, or Read Only | Bit | Default Value | Register Name | Function |
|-------------|------------------------------|-----|--|--------------------------|---|
| 0x00 | RO | 7:0 | | Chip Revision | An 8-bit register that represents the silicon revision level. |
| 0x01 | R/W | 7:0 | 01101001 | PLL Div MSB | This register is for Bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. This gives the PLL more time to lock. ¹ |
| 0x02 | R/W | 7:4 | 1101**** | PLL Div LSB | Bits [7:4] LSBs of the PLL divider word. ¹ |
| 0x03 | R/W | 7:2 | 01***** **001*** | VCO/CPMP | Bits [7:6] VCO Range. Selects VCO frequency range. See PLL description. Bits [5:3] Charge Pump Current. Varies the current that drives the low-pass filter. See PLL description. |
| 0x04 | R/W | 7:3 | 10000*** | Phase Adjust | ADC Clock phase adjustment. Larger values mean more delay. (1 LSB = T/32) |
| 0x05 | R/W | 7:0 | 00001000 | Clamp Placement | Places the Clamp signal an integer number of clock periods after the trailing edge of the Hsync signal. |
| 0x06 | R/W | 7:0 | 00010100 | Clamp Duration | Number of clock periods that the Clamp signal is actively clamping. |
| 0x07 | R/W | 7:0 | 00100000 | Hsync Output Pulse Width | Sets the number of pixel clocks that HSOUT remains active. |
| 0x08 | R/W | 7:0 | 10000000 | Red Gain | Controls ADC input range (contrast) of each respective channel. Bigger values give less contrast. |
| 0x09 | R/W | 7:0 | 10000000 | Green Gain | See Red Gain |
| 0x0A | R/W | 7:0 | 10000000 | Blue Gain | See Red Gain |
| 0x0B | R/W | 7:1 | 1000000* | Red Offset | Controls dc offset (brightness) of each respective channel. Bigger values decrease brightness. |
| 0x0C | R/W | 7:1 | 1000000* | Green Offset | See Red Offset |
| 0x0D | R/W | 7:1 | 1000000* | Blue Offset | See Red Offset |
| 0x0E | R/W | 7:0 | 0***** *1***** **0***** ***0**** ****0*** *****0** *****0* *****0 | Sync Control | Bit 7—Hsync Polarity Override. Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 6 in Register 0x0E. Bit 6—Hsync Input Polarity. Indicates to the PLL the polarity of the incoming Hsync signal. Logic 0 = active low, Logic 1 = active high. Bit 5—Hsync Output Polarity. Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync. Bit 4—Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 3. If set to Logic 0, the active interface is selected via Bit 6 in Register 0x14. Bit 3—Active Hsync Select. Logic 0 selects Hsync as the active sync. Logic 1 selects sync-on-green as the active sync. Note that the indicated Hsync is used only if Bit 4 is set to Logic 1 or if both syncs are active (Bits 1, 7 = Logic 1 in Register 0x14). Bit 2—Vsync Output Invert. Logic 0 = Invert, Logic 1 = No Invert. Bit 1—Active Vsync Override. If set to Logic 1, the user can select the Vsync to be used via Bit 0. If set to Logic 0, the active interface is selected via Bit 3 in Register 0x14. Bit 0—Active Vsync Select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note that the indicated Vsync is used only if Bit 1 is set to Logic 1. |

| Hex Address | Read and Write, or Read Only | Bit | Default Value | Register Name | Function |
|-------------|------------------------------|-----|--|--------------------------|--|
| 0x0F | R/W | 7:1 | 0***** *1***** **0***** ***0**** ****1*** *****1** *****1* | | <p>Bit 7—Clamp Function. Chooses between Hsync and another external signal to be used for clamping. Logic 0 = Hsync, Logic 1 = Clamp.</p> <p>Bit 6—Clamp Polarity. Valid only with external Clamp signal. Logic 0 = active high, Logic 1 = active low.</p> <p>Bit 5—COAST Select. Logic 0 = the coast input pin is used for the PLL coast, Logic 1 = Vsync is used for the PLL coast.</p> <p>Bit 4—COAST Polarity Override. Logic 0 = polarity determined by chip, Logic 1 = polarity set by Bit 3 in Register 0x0F.</p> <p>Bit 3—COAST Polarity. Changes polarity of external COAST signal. Logic = 0 = active low, Logic 1 = active high.</p> <p>Bit 2—Seek Mode Override. Logic 1 = allow low-power mode, Logic 0 = disallow low power mode.</p> <p>Bit 1—PWRDN. Full chip power-down, active low. Logic 0 = full chip power-down, Logic 1 = normal.</p> |
| 0x10 | R/W | 7:3 | 01111*** *****0** *****0* *****0 | Sync-on-Green Threshold | <p>Sync-on-Green Threshold. Sets the voltage level of the sync-on-green slicer comparator.</p> <p>Bit 2—Red Clamp Select. Logic 0 = clamp to ground, Logic 1 = clamp to midscale [voltage at Pin 9].</p> <p>Bit 1—Blue Clamp Select. Logic 0 = clamp to ground, Logic 1 = clamp to midscale [voltage at Pin 24].</p> <p>Bit 0—Must be set to 1 for proper operation.</p> |
| 0x11 | R/W | 7:0 | 00100000 | Sync Separator Threshold | Sync Separator Threshold. Sets how many internal 5 MHz clock periods the sync separator counts before toggling high or low. This should be set to a number greater than the maximum Hsync or equalization pulse width. |
| 0x12 | R/W | 7:0 | 00000000 | Pre-COAST | Pre-COAST. Sets the number of Hsync periods before which coast becomes active prior to Vsync. |
| 0x13 | R/W | 7:0 | 00000000 | Post-COAST | Post-COAST. Sets the number of Hsync periods before which coast stays active following Vsync. |
| 0x14 | RO | 7:0 | | Sync Detect | <p>Bit 7—Hsync Detect. It is set to Logic 1 if Hsync is present on the analog interface; otherwise, it is set to Logic 0.</p> <p>Bit 6—Active Hsync (AHS). This bit indicates which analog Hsync is being used. Logic 0 = Hsync input pin, Logic 1 = Hsync from sync-on-green.</p> <p>Bit 5—Input Hsync Polarity Detect. Logic 0 = active low, Logic 1 = active high.</p> <p>Bit 4—Vsync detect. It is set to Logic 1 if Vsync is present on the analog interface; otherwise, it is set to Logic 0.</p> <p>Bit 3—Active Vsync (AVS). This bit indicates which analog Vsync is being used. Logic 0 = Vsync input pin, Logic 1 = Vsync from sync separator.</p> <p>Bit 2—Output Vsync Polarity Detect. Logic 0 = active high, Logic 1 = active low.</p> <p>Bit 1—Sync-on-Green Detect. It is set to Logic 1 if sync is present on the green video input; otherwise, it is set to 0.</p> <p>Bit 0—Input COAST Polarity Detect. Logic 0 = active low, Logic 1 = active high.</p> |

AD9888A

| Hex Address | Read and Write, or Read Only | Bit | Default Value | Register Name | Function |
|-------------|------------------------------|-----|---|---------------|---|
| 0x15 | R/W | 7:0 | 1***** *1***** **0***** ***0**** ****0*** *****11* *****0 | | Bit 7—Channel Mode. Determines single-channel or dual-channel output mode. Logic 0 = single-channel mode, Logic 1 = dual-channel mode. Bit 6—Output Mode. Determines interleaved or parallel output mode. Logic 0 = interleaved mode, Logic 1 = parallel mode. Bit 5—A/B Invert. Determines which port outputs the first data byte after Hsync. Logic 0 = A port, Logic 1 = B port. Bit 4—4:2:2 Output Formatting Mode. Bit 3—Input Mux Control. Bits [2:1]—Input Bandwidth. Bit 0—External Clock. Shuts down PLL and allows external clock to drive the part. Logic 0 = use internal PLL, Logic 1 = bypassing of the internal PLL. |
| 0x16 | R/W | 7:0 | 11111111 | Test Register | Must be set to 11111110 for proper operation. |
| 0x17 | R/W | 7:3 | 00000000 | Test Register | Must be set to default for proper operation. |
| 0x18 | RO | 7:0 | | Test Register | |
| 0x19 | RO | 7:0 | | Test Register | |

¹ The AD9888A only updates the PLL divide ratio when the LSBs are written to (Register 0x02).

2-WIRE SERIAL CONTROL REGISTER DETAIL

CHIP IDENTIFICATION

00 7-0 Chip Revision

An 8-bit register that represents the silicon revision.

PLL DIVIDER CONTROL

01 7-0 PLL Divide Ratio MSBs

The 8 MSBs of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The PLL derives a master clock from an incoming Hsync signal. The master clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established standard timing specifications that assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table 5). However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV usually produces one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

The AD9888A only updates the full divide ratio when the LSBs are changed. Writing to this register by itself will not trigger an update.

02 7-4 PLL Divide Ratio LSBs

The 4 LSBs of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

The AD9888A updates the full divide ratio only when this register is written to.

CLOCK GENERATOR CONTROL

03 7-6 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL provides the best jitter performance at high frequencies. To output low pixel rates while minimizing jitter, the PLL actually operates at a higher frequency and then divides down the clock rate afterwards. Table 9 shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table 9. VCO Ranges

| VCORNGE | Pixel Rate Range |
|---------|------------------|
| 00 | 10 to 41 |
| 01 | 41 to 82 |
| 10 | 82 to 150 |
| 11 | 150+ |

The power-up default is 01.

03 5-3 Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table 10. Charge Pump Currents

| CURRENT | Current (mA) |
|---------|--------------|
| 000 | 50 |
| 001 | 100 |
| 010 | 150 |
| 011 | 250 |
| 100 | 350 |
| 101 | 500 |
| 110 | 750 |
| 111 | 1500 |

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default is CURRENT = 001.

04 7-3 Clock Phase Adjust

A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default value is 16.

CLAMP TIMING

05 7-0 Clamp Placement

An 8-bit register that sets the position of the internally generated clamp.

When the external clamp control bit is set to 0, a clamp signal is generated internally at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (clamp placement) pixel periods after the trailing edge of Hsync. The clamp placement can be programmed to any value up to 255, except 0.

The clamp should be placed during a time when the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When the external clamp control bit is set to 1, this register is ignored.

06 7-0 Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp.

When the external clamp control bit is set to 0, a clamp signal is generated internally at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started [clamp placement] pixel periods after the trailing edge of Hsync, and continues for [clamp duration] pixel periods. The clamp duration may be programmed to any value between 1 and 255. A value of 0 is not supported.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen and a slow recovery from large changes in the average picture level (APL), or brightness.

When the external clamp control bit is set to 1, this register is ignored.

HSYNC PULSE WIDTH

07 7-0 Hsync Output Pulse Width

An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9888A then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase-adjusted.

INPUT GAIN

08 7-0 Red Channel Gain Adjust (REDGAIN)

An 8-bit word that sets the gain of the red channel.

The AD9888A can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting REDGAIN to 255 corresponds to an input range of 1.0 V. A REDGAIN of 0 establishes an input range of 0.5 V. Note that increasing REDGAIN results in the picture having less contrast, because the input signal uses fewer of the available converter codes. See Figure 4

09 7-0 Green Channel Gain Adjust

An 8-bit word that sets the gain of the green channel. See REDGAIN (08).

0A 7-0 Blue Channel Gain Adjust

An 8-bit word that sets the gain of the blue channel. See REDGAIN (08).

Input Offset

0B 7-1 Red Channel Offset Adjust (REDOFST)

A 7-bit offset binary word that sets the dc offset of the red channel.

One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel changes. A nominal setting of 63 results in the channel nominally clamping to Code 00 during the back porch clamping interval. An offset setting of 127 results in the channel clamping to Code 64 of the ADC. An offset setting of 0 clamps to Code -63 (off the bottom of the range). Increasing the value of red offset decreases the brightness of the channel.

0C 7-1 Green Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the green channel. See REDOFST (0B).

0D 7-1 Blue Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the blue channel. See REDOFST (0B).

0E 7 Hsync Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table 11. Hsync Input Polarity Override Settings

| Override Bit | Result |
|--------------|-----------------------------------|
| 0 | Hsync polarity determined by chip |
| 1 | Hsync polarity determined by user |

The default for Hsync polarity override is 0 (polarity determined by chip).

0E 6 HSPOL Hsync Input Polarity

A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table 12. Hsync Input Polarity Settings

| HSPOL | Function |
|-------|-------------|
| 0 | Active low |
| 1 | Active high |

Active low means the leading edge of the Hsync pulse is negative-going. All timing is based on the leading edge of Hsync, which is the falling edge. The rising edge has no effect.

Active high means the leading edge of the Hsync pulse is positive-going. This means that timing is based on the leading edge of Hsync, which is now the rising edge.

The device operates if this bit is set incorrectly, but the internally generated clamp position, as established by the clamp placement (Register 0x05), will not be placed as expected, which could generate clamping errors.

The power-up default is HSPOL = 1.

0E 5 Hsync Output Polarity

One bit that determines the polarity of the Hsync output and the SOG output. Table 13 shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table 13. Hsync Output Polarity Settings

| Setting | SYNC |
|---------|-----------------------------|
| 0 | Logic 1 (positive polarity) |
| 1 | Logic 0 (negative polarity) |

The default setting for this register is 0.

This bit is used to override the automatic Hsync selection. To initiate this, set this bit to Logic 1. When overriding the automatic Hsync selection, the active Hsync is set via Bit 3 in this register.

Table 14. Active Hsync Override Settings

| Override | Result |
|----------|--|
| 0 | Auto determines the active interface. |
| 1 | Override, Bit 3 determines the active interface. |

The default for this register is 0.

0E 3 Active Hsync Select

This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternatively, it is used to determine the active Hsync when the override bit is not set but both Hsyncs are detected.

Table 15. Active Hsync Select Settings

| Select | Result |
|--------|---------------------|
| 0 | Hsync input |
| 1 | Sync-on-green input |

The default for this register is 0.

0E 2 Vsync Output Invert

A bit that inverts the polarity of the Vsync output. Table 16 shows the effect of this option.

Table 16. Vsync Output Polarity Settings

| Setting | SYNC |
|---------|---------------|
| 0 | Invert |
| 1 | Do not invert |

The default setting for this register is 0.

0E 1 Active Vsync Override

This bit is used to override the automatic Vsync selection. To initiate this, set this bit to Logic 1. When overriding the automatic Vsync selection, the active interface is set via Bit 0 in this register.

Table 17. Active Vsync Override Settings

| Override | Result |
|----------|--|
| 0 | Autodetermines the active Vsync. |
| 1 | Override, Bit 0 determines the active Vsync. |

The default for this register is 0.

0E 4 Active Hsync Override

0E 0 Active Vsync Select

This bit is used to select the active Vsync when the override bit is set (Bit 1).

Table 18. Active Vsync Select Settings

| Select | Result |
|--------|-----------------------|
| 0 | Vsync input |
| 1 | Sync separator output |

The default for this register is 0.

0F 7 Clamp Input Signal Source

A bit that determines the source of clamp timing.

Table 19. Clamp Input Signal Source Settings

| External Clamp | Function |
|----------------|----------------------------------|
| 0 | Internally generated clamp |
| 1 | Externally provided clamp signal |

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the trailing edge of Hsync.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the Clamp Polarity bit (Register 0x0F, Bit 6).

The power-up default is External Clamp = 0.

0 6 Clamp Input Signal Polarity

A bit that determines the polarity of the externally provided CLAMP signal.

Table 20. Clamp Input Signal Polarity Settings

| Clamp Polarity | Function |
|----------------|-------------|
| 1 | Active low |
| 0 | Active high |

A Logic 1 means the circuit clamps when CLAMP is low and passes the signal to the ADC when CLAMP is high.

A Logic 0 means the circuit clamps when CLAMP is high and passes the signal to the ADC when CLAMP is low.

The power-up default is Clamp Polarity = 1.

This bit is used to select the active coast source. The choices are the coast input pin or Vsync. If Vsync is selected, users must decide whether to use the VSYNC input pin or the output from the sync separator (Register 0x0E, Bits 1 and 0).

Table 21. COAST Source Selection Settings

| Select | Result |
|--------|------------------------|
| 0 | COAST input pin |
| 1 | Vsync (see above text) |

The default for this register is 0.

0F 4 COAST Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL.

Table 22. COAST Input Polarity Override Settings

| Override Bit | Result |
|--------------|-----------------------------------|
| 0 | COAST polarity determined by chip |
| 1 | COAST polarity determined by user |

The default for coast polarity override is 0.

0F 3 COAST Input Polarity

A bit to indicate the polarity of the COAST signal that is applied to the PLL COAST input.

Table 23. COAST Input Polarity Settings

| CSTPOL | Function |
|--------|-------------|
| 0 | Active low |
| 1 | Active high |

Active low means that the clock generator ignores Hsync inputs when COAST is low and continues operating at the same nominal frequency until COAST goes high.

Active high means that the clock generator ignores Hsync inputs when COAST is high and continues operating at the same nominal frequency until COAST goes low.

This function needs to be used along with the COAST Polarity Override bit (Bit 4).

The power-up default is CSTPOL = 1.

0F 5 COAST Select

0F 2 Seek Mode Override

This bit is used to either allow or disallow the low power mode. The low power mode (seek mode) occurs when there are no signals on any of the sync inputs.

Table 24. Seek Mode Override Settings

| Select | Result |
|--------|--------------------|
| 1 | Allow seek mode |
| 0 | Disallow seek mode |

The default for this register is 1.

0F 1 $\overline{\text{PWRDN}}$

This bit is used to put the chip in power-down mode. In this mode, the chip's power dissipation is reduced to a fraction of the typical power (see the Specifications in Table 1 for exact power dissipation). When in power-down, the HSOUT, VSOUT, DATAACK, $\overline{\text{DATAACK}}$, and all 48 of the data outputs are put into a high impedance state. Note that the SOGOUT output is not put into high impedance. Circuit blocks that continue to be active during power-down include the voltage references, sync processing, sync detection, and the serial register. These blocks facilitate a fast startup from power-down.

Table 25. Power-Down Settings

| Select | Result |
|--------|------------------|
| 0 | Power-down |
| 1 | Normal operation |

The default for this register is 1.

10 7-3 Sync-on-Green Slicer Threshold

This register allows the comparator threshold of the sync-on-green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting of 10 mV and the maximum setting of 330 mV.

The default setting is 15, which corresponds to a threshold value of 0.16 V.

10 2 Red Clamp Select

A bit that determines whether the red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YCbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 9.

Table 26. Red Clamp Select Settings

| Clamp | Function |
|-------|---------------------------|
| 0 | Clamp to ground |
| 1 | Clamp to midscale (Pin 9) |

The default setting for this register is 0.

10 1 Blue Clamp Select

A bit that determines whether the blue channel is clamped to ground or to midscale. Clamping to midscale actually clamps to Pin 24.

Table 27. Blue Clamp Select Settings

| Clamp | Function |
|-------|----------------------------|
| 0 | Clamp to ground |
| 1 | Clamp to midscale (Pin 24) |

The default setting for this register is 0.

11 7:0 Sync Separator Threshold

This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to a number greater than the maximum Hsync pulse width. The sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 32.

12 7-0 Pre-COAST

This register allows the COAST signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

13 7-0 Post-COAST

This register allows the COAST signal to be applied following the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

14 7 Hsync Detect

This bit is used to indicate when activity is detected on the selected Hsync input pin. If HSYNC is held high or low, activity is not detected.

Table 28. Hsync Detection Results

| Detect | Function |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

The Sync Processing Block Diagram (Figure 27) shows where this function is implemented.

14 6 Active Hsync (AHS)

This bit indicates which Hsync input source is being used by the PLL (Hsync or sync-on-green input). Bits 7 and 1 in this register determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in Register 0x0E. The user can override this function via Bit 4 in Register 0x0E. If the override bit is set to Logic 1, this bit is forced to the state that Bit 3 is set to in Register 0x0E.

Table 29. Active Hsync Results

| Bit 7 (Hsync Detect) | Bit 1 (SOG Detect) | Bit 4, Reg. 0x0E (Override) | AHS |
|----------------------|--------------------|-----------------------------|---------------|
| 0 | 0 | 0 | Bit 3 in 0x0E |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | Bit 3 in 0x0E |
| X | X | 1 | Bit 3 in 0x0E |

When AHS = 0, use the HSYNC pin input for HSYNC.

When AHS = 1, use the SOG pin input for HSYNC.

The override bit is in Register 0x0E, Bit 4.

14 5 Detected Hsync Input Polarity Status

This bit reports the status of the HSYNC input polarity detection circuit. It can be used to determine the polarity of the HSYNC input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 27).

Table 30. Detected Hsync Input Polarity Status

| HSYNC Polarity Status | Result |
|-----------------------|-----------------------------|
| 0 | Hsync polarity is negative. |
| 1 | Hsync polarity is positive. |

14 4 Vsync Detect

This bit is used to indicate when activity is detected on the selected Vsync input pin. If Vsync is held high or low, activity is not detected.

Table 31. Vsync Detection Results

| Detect | Function |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

The Sync Processing Block Diagram (Figure 27) shows where this function is implemented.

This bit indicates which Vsync source is being used: the Vsync input or the output from the sync separator. Bit 4 in this register determines which is active. If both Vsync and SOG are detected, the user can determine which has priority via Bit 0 in Register 0x0E. The user can override this function via Bit 1 in Register 0x0E. If the override bit is set to Logic 1, this bit is forced to the state that Bit 0 is set to in Register 0x0E.

Table 32. Active Vsync Results

| Bit 5 (Vsync Detect) | Override | AVS |
|----------------------|----------|---------------|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| X | 1 | Bit 0 in 0x0E |

When AVS = 1, the sync separator is used.

When AVS = 0, the Vsync input is used.

The override bit is in Register 0x0E, Bit 1.

14 2 Detected Vsync Output Polarity Status

This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 27).

Table 33. Detected Vsync Input Polarity Status

| Vsync Polarity Status | Result |
|-----------------------|--------------------------------|
| 0 | Vsync polarity is active high. |
| 1 | Vsync polarity is active low. |

14 1 Sync-on-Green Detect

This bit is used to indicate when sync activity is detected on the selected sync-on-green input pin.

Table 34. Sync-on-Green Detection Results

| Detect | Function |
|--------|----------------------|
| 0 | No activity detected |
| 1 | Activity detected |

The Sync Processing Block Diagram (Figure 27) shows where this function is implemented.

14 0 Detected COAST Polarity Status

This bit reports the status of the COAST input polarity detection circuit. It can be used to determine the polarity of the COAST input. The detection circuit's location is shown in Figure 27.

Table 35. Detected COAST Input Polarity Status

| HSYNC Polarity Status | Result |
|-----------------------|-----------------------------|
| 0 | COAST polarity is negative. |
| 1 | COAST polarity is positive. |

14 3 Active Vsync (AVS)

MODE CONTROL 1

15 7 Channel Mode

A bit that determines whether all pixels are presented to a single port (Port A), or alternating pixels are demultiplexed to Ports A and B.

Table 36. Channel Mode Settings

| DEMUX | Function |
|-------|---|
| 0 | All data goes to Port A. |
| 1 | Alternate pixels go to Port A and Port B. |

When DEMUX = 0, Port B outputs are in a high impedance state. The maximum data rate for single-port mode is 110 MHz. The timing diagrams in Figure 15 to Figure 24 show the effects of this option.

The power-up default is 1.

15 6 Output Mode

This bit determines whether all pixels are presented to Port A and Port B simultaneously upon every second DATAACK rising edge, or alternately to Port A and Port B upon successive DATAACK rising edges.

Table 37. Output Mode Settings

| PARALLEL | Function |
|----------|---|
| 0 | Data is interleaved. |
| 1 | Data is simultaneous on every other data clock. |

When in single-port mode (DEMUX = 0), this bit is ignored. The timing diagrams (Figure 21 and Figure 22) show the effects of this option.

The power-up default is PARALLEL = 1.

15 5 Output Port Phase

One bit that determines whether even pixels or odd pixels go to Port A

Table 38. Output Port Phase Settings

| OUTPHASE | First Pixel after Hsync |
|----------|-------------------------|
| 0 | Port A |
| 1 | Port B |

In normal operation (OUTPHASE = 0) when operating in dual-port output mode (DEMUX = 1), the first sample after the Hsync leading edge is presented at Port A. Every subsequent odd sample goes to Port A. All even samples go to Port B.

When OUTPHASE = 1, these ports are reversed and the first sample goes to Port B.

When DEMUX = 0, this bit is ignored because data always comes out of only Port A.

15 4 4:2:2 Output Mode Select

A bit that configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 to 16 for applications using YUV, YCbCr, or YPbPr graphics signals. A timing diagram for this mode is shown in Figure 14. Recommended input and output configurations are shown in Table 40. In 4:2:2 mode, the red and blue channels can be interchanged to help satisfy board layout or timing requirements, but the green channel must be configured for Y.

Table 39. 4:2:2 Output Mode Select

| Select | Output Mode |
|--------|-------------|
| 0 | 4:4:4 |
| 1 | 4:2:2 |

Table 40. 4:2:2 Input/Output Configuration

| Channel | Input Connection | Output Format |
|---------|------------------|----------------|
| Red | V | U/V |
| Green | Y | Y |
| Blue | U | High impedance |

15 3 Input Mux Control

A bit that selects analog inputs from either Channel 0 or 1.

Table 41. Input Mux Control

| Control | Channel Selected |
|---------|------------------|
| 0 | Channel 0 |
| 1 | Channel 1 |

15 2-1 Analog Bandwidth Control

Two bits that select the analog bandwidth.

Table 42. Analog Bandwidth Control

| Bit 2 | Bit 1 | Analog Bandwidth |
|-------|-------|------------------|
| 1 | 1 | 500 MHz |
| 1 | 0 | 300 MHz |
| 0 | 1 | 150 MHz |
| 0 | 0 | 75 MHz |

15 0 External Clock Select

A bit that determines the source of the pixel clock.

Table 43. External Clock Select Settings

| EXTCLK | Function |
|--------|----------------------------------|
| 0 | Internally generated clock |
| 1 | Externally provided clock signal |

A Logic 0 enables the internal PLL that generates the pixel clock from an externally provided HSYNC.

A Logic 1 enables the external CKEXT input pin. In this mode, the PLL divide ratio (PLLDIV) is ignored. The clock phase adjust (PHASE) is still functional.

The power-up default is EXTCLK = 0.

2-WIRE SERIAL CONTROL PORT

A 2-wire serial control interface is provided. Up to two AD9888A devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The AD9888A acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets the action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal compose a 7-bit slave address (the first seven bits) and a single R/W bit (the eighth bit). The R/W bit indicates the direction of data transfer, reading from (1) or writing to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the A_0 input pin in Table 44), the AD9888A acknowledges it by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9888A does not acknowledge it.

Table 44. Serial Port Addresses

| Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
|-------------|-------|-------|-------|-------|-------|-------|
| A_6 | A_5 | A_4 | A_3 | A_2 | A_1 | A_0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 |

DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9888A does not acknowledge the master device during a write sequence, the SDA remains high so that the master can generate a stop signal. If the master device does not acknowledge the AD9888A during a read sequence, the AD9888A interprets this as “end of data.” The SDA remains high so that the master can generate a stop signal.

Writing data to a control register of the AD9888A requires writing to its 8-bit address after the slave address is established. This control register address is the base address for subsequent write operations. The base address auto-increments by 1 for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value of 0x19. Any base address higher than 0x19 does not produce an acknowledge signal.

Data are read from the control registers of the AD9888A in a similar manner. Reading requires two data transfer operations.

The base address must be written with the $\overline{R/W}$ bit of the slave address byte low to set up a sequential read operation.

Reading (with the $\overline{R/W}$ bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9888A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to One Control Register

Start Signal

Slave Address Byte ($\overline{R/W}$ Bit = Low)

Base Address Byte

Data Byte to Base Address

Stop Signal

Write to Four Consecutive Control Registers

Start Signal
 Slave Address Byte ($\overline{R/\overline{W}}$ Bit = Low)
 Base Address Byte
 Data Byte to Base Address
 Data Byte to (Base Address + 1)
 Data Byte to (Base Address + 2)
 Data Byte to (Base Address + 3)
 Stop Signal

Read from One Control Register

Start Signal
 Slave Address Byte ($\overline{R/\overline{W}}$ Bit = Low)
 Base Address Byte
 Start Signal
 Slave Address Byte ($\overline{R/\overline{W}}$ Bit = High)
 Data Byte from Base Address
 Stop Signal

Read from Four Consecutive Control Registers

Start Signal
 Slave Address Byte ($\overline{R/\overline{W}}$ Bit = Low)
 Base Address Byte
 Start Signal
 Slave Address Byte ($\overline{R/\overline{W}}$ Bit = High)
 Data Byte from Base Address
 Data Byte from (Base Address + 1)
 Data Byte from (Base Address + 2)
 Data Byte from (Base Address + 3)
 Stop Signal

SYNC PROCESSING

Table 45. Control of the Sync Block Muxes via the Serial Register

| Mux Number(s) | Serial Bus Control Bit | Control Bit State | Result |
|---------------|------------------------|-------------------|----------------------------|
| 1 and 2 | 0x0E: Bit 3 | 0 | Pass HSYNC |
| | | 1 | Pass sync-on-green |
| 3 | 0x0F: Bit 5 | 0 | Pass COAST |
| | | 1 | Pass Vsync |
| 4 | 0x0E: Bit 0 | 0 | Pass Vsync |
| | | 1 | Pass sync separator signal |
| 5 | 0x15: Bit 3 | 0 | Pass Channel 0 inputs |
| | | 1 | Pass Channel 1 inputs |

SYNC SLICER

The purpose of the sync slicer is to extract the sync signal from the green graphics channel. A sync signal is not present on all graphics signals, only those with sync-on-green. The sync signal is extracted from the green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The “sliced” sync is typically a composite sync signal containing both Hsync and Vsync.

SYNC SEPARATOR

A sync separator extracts the Vsync signal from a composite sync signal by using a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. Therefore, it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulse width and a Vsync pulse width.

The sync separator on the AD9888A is an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. Polarities are determined elsewhere on the chip. The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down, eventually reaching 0 before the next Hsync pulse arrives. The specific value of N varies among video modes, but is always less than 255. For example, with a 1 μ s width Hsync, the counter reaches only 5 (1 μ s/200 ns = 5). When Vsync is present on the composite sync, the counter also counts up. However, because the Vsync signal is much longer, it counts to a higher number, M. For most video modes, M is at least 255. Therefore, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (0x0F).

Once Vsync is detected, there is a similar process to detect when it goes inactive. Upon detection, the counter first resets to 0, then starts counting up when Vsync disappears. Similar to the previous case, it detects the absence of Vsync when the counter reaches the threshold count (T). In this way, it rejects noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

PCB LAYOUT RECOMMENDATIONS

The AD9888A is a high precision, high speed analog device. To optimize its performance, it is important to have a well laid out board. The following is a guide for designing a board using the AD9888A.

ANALOG INTERFACE INPUTS

Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs by placing the AD9888A as close as possible to the graphics (VGA) connector. Long input trace lengths are undesirable because they pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors (see Figure 3) as close to as possible the AD9888A chip. Any additional trace length between the termination resistors and the input of the AD9888A increases the magnitude of reflections, which corrupts the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω increase the chance of reflections.

The AD9888A has very high input bandwidth (500 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it also captures any high frequency noise present. Therefore, it is important to reduce the amount of noise coupled to the inputs. Avoid running any digital traces near the analog inputs.

The AD9888A can digitize graphics signals over a very wide range of frequencies (10 MHz to 205 MHz). Often, characteristics that are beneficial at one frequency can be detrimental at another. Analog bandwidth is one such characteristic. For UXGA resolutions (up to 205 MHz), a very high analog bandwidth is desirable because of the fast input signal slew rates. For VGA and lower resolutions (down to 12.5 MHz), a very high bandwidth is not desirable because it allows excess noise to pass through. To accommodate these varying needs, the AD9888A includes variable analog bandwidth control. Four settings are available (75 MHz, 150 MHz, 300 MHz, and 500 MHz), allowing the analog bandwidth to be matched with the resolution of the incoming graphics signal.

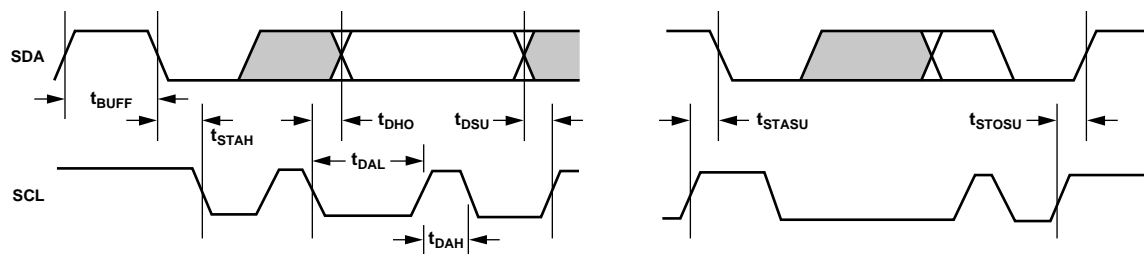


Figure 25. Serial Port Read/Write Timing

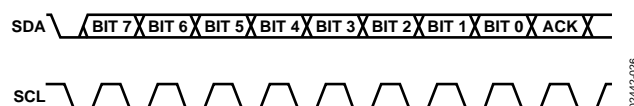
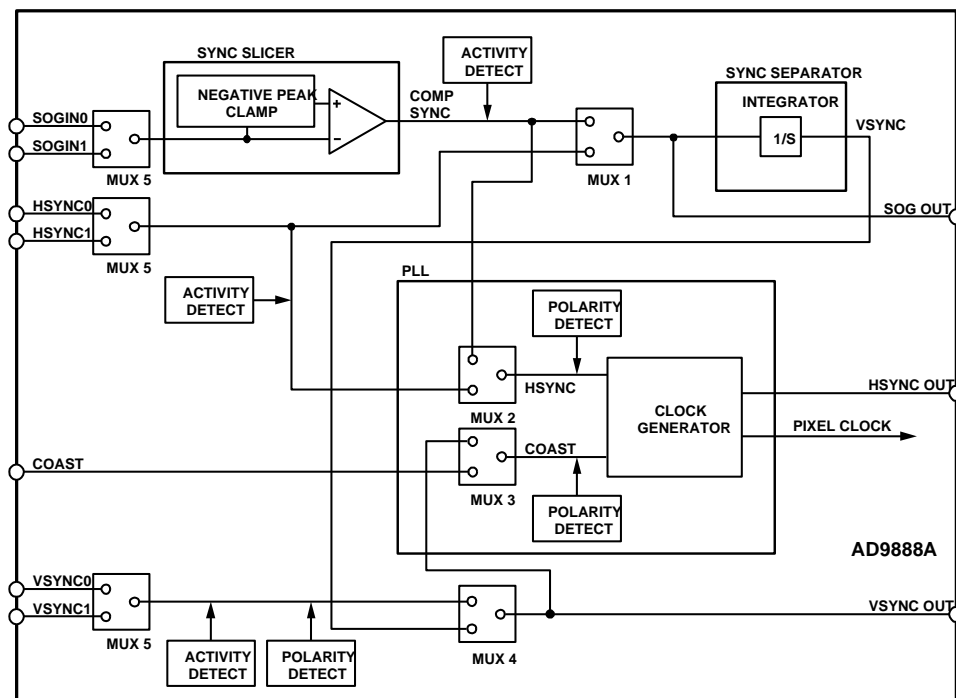


Figure 26. Serial Interface—Typical Byte Transfer



02442-027

Figure 27. Sync Processing Block Diagram

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 μF capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have only one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the side of the PC board opposite from the AD9888A, because this interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful regulation, filtering, and bypassing. It is highly desirable to provide separate, regulated supplies for each of the analog circuitry groups, V_D and PV_D .

Some graphics controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the

regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D , from a different, cleaner power source, for example, from a 12 V supply.

It is also recommended to use a single ground plane for the entire board. Experience shows that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For these cases, it is recommended to at least place a single ground plane under the AD9888A. The location of the split should be at the receiver of the digital outputs, making it is even more important to place components wisely because the current loops will be much longer, and current takes the path of least resistance. An example of a current loop: power plane \rightarrow AD9888A \rightarrow digital output trace \rightarrow digital data receiver \rightarrow digital ground plane \rightarrow analog ground plane.

PLL

Place the PLL loop filter components as close as possible to the FILT pin. Do not place any digital or other high frequency traces near these components. Use the values suggested in the data sheet with 10% tolerances or less.

OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length that the digital outputs must

AD9888A

drive. Longer traces have higher capacitance, requiring more current and causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor with a value of $22\ \Omega$ to $100\ \Omega$ can suppress reflections, reduce EMI, and reduce the current spikes inside the AD9888A. However, if $50\ \Omega$ traces are used on the PCB, the data output should not need these resistors.

A $22\ \Omega$ resistor on the DATAACK output should provide good impedance matching that will reduce reflections. If series resistors are used, place them as close as possible to the AD9888A pins, but avoid adding vias or extra length to the output trace.

If possible, limit the capacitance that each of the digital outputs drives to less than $10\ \text{pF}$. This can easily be accomplished by keeping traces short and connecting the outputs to only one device. Loading the outputs with excessive capacitance increases

the current transients inside of the AD9888A, creating more digital noise on its power supplies.

DIGITAL INPUTS

The digital inputs on the AD9888A were designed to work with $3.3\ \text{V}$ signals, but are tolerant of $5.0\ \text{V}$ signals. Therefore, no extra components are needed when using $5.0\ \text{V}$ logic.

Any noise in the Hsync input trace produces jitter in the system. Therefore, minimize the trace length, and do not run any digital or other high frequency traces near it.

VOLTAGE REFERENCE

The voltage reference should be bypassed with a $0.1\ \mu\text{F}$ capacitor. Place it as close as possible to the AD9888A pin. Make the ground connection as short as possible.

OUTLINE DIMENSIONS

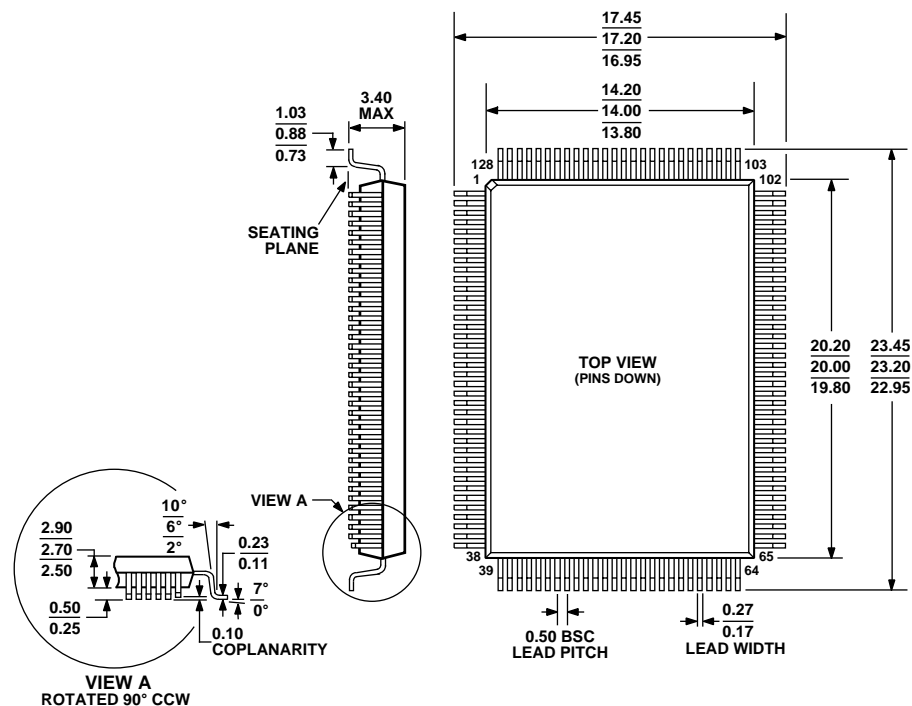


Figure 28. 128-Lead Metric Quad Flat Package [MQFP]
(S-128-1)
Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Option |
|--|-------------------|----------------|
| AD9888AKSZ-205Error! Bookmark not defined. | 0°C to 70°C | S-128-1 |
| AD9888/PCB | 25°C | Evaluation Kit |

Error! Bookmark not defined. Z = Pb-free part.