Precision Low Noise, Low Input Bias Current Operational Amplifiers

Preliminary Technical Data

ADA4077-2

FEATURES

Low offset voltage:
- **B-Grade: 25 µV max (SOIC)**
- **A-Grade: 50 µV max (SOIC), 125 µV max (MSOP)**

Very low offset voltage drift:
- **B-Grade: 0.25 µV/°C max (SOIC)**
- **A-Grade: 0.55 µV/°C max (SOIC), 1.2 µV/°C max (MSOP)**

Low input bias current: <1.0 nA maximum
Low noise: 8 nV/√Hz typical
CMRR, PSRR, and A_{VO} > 120 dB minimum
Low supply current: 400 µA per amplifier
Wide Bandwidth: 3.9 MHz
Dual supply operation: ±2.5 V to ±15 V
Unity-gain stable
No phase reversal

APPLICATIONS

Wireless base station control circuits
Optical network control circuits
Instrumentation
Sensors and controls
- **Thermocouples**
- **Resistor thermal detectors (RTDs)**
- **Strain bridges**
- **Shunt current measurements**

Precision filters

PIN CONFIGURATIONS

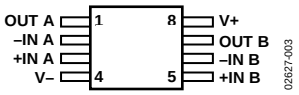

Figure 1. 8-Lead MSOP (RM Suffix)

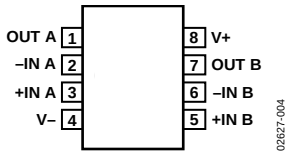

Figure 2. 8-Lead SOIC_N (R Suffix)

GENERAL DESCRIPTION

The ADA4077 family consists of very high precision, single, dual, and quad amplifiers featuring extremely low offset voltage and drift, low input bias current, low noise, and low power consumption. Outputs are stable with capacitive loads of over 1000 pF with no external compensation. Supply current is less than 500 µA per amplifier at 30 V.

Applications for these amplifiers include precision diode power measurement, voltage and current level setting, and level detection in optical and wireless transmission systems. Additional applications include line-powered and portable instrumentation and controls—thermocouple, RTD, strain-bridge, precision filters, and other sensor signal conditioning.

The ADA4077 family is fully specified for operation from −40°C to +125°C for the most demanding operating environments. The ADA4077-2 is a dual available in 8-lead SOIC and MSOP packages. The B Grade is only available in the ADA4077-2 in the SOIC package.

ADI's 30V, Precision, Bipolar OP07 Op Amp Generations						
	1st	2nd	3rd	4th	5th	6th
Single	OP07	OP77	OP177	OP1177	AD8677	
Dual				OP2177		ADA4077-2
Quad				OP4177		

Rev. PrB

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted. **B Grade Specifications are targets only.**

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B-Grade, SOIC)[1]	V_{OS}			10	25	µV
		−40°C < T_A < +125°C			TBD	µV
Offset Voltage Drift (B-Grade, SOIC)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.1	0.25	µV/°C
Offset Voltage (A-Grade)[1]	V_{OS}					
SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
MSOP				50	110	µV
		−40°C < T_A < +125°C			230	µV
Offset Voltage Drift (A-Grade)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
SOIC				0.25	0.55	µV/°C
MSOP				0.5	1.2	µV/°C
Offset Voltage Drift with Time	$\Delta V_{OS}/\Delta Time$			TBD		µV/mon
Input Bias Current	I_B		−1	TBD	+1	nA
		−40°C < T_A < +125°C	-1.5		+1.5	nA
Input Offset Current	I_{OS}		−1	TBD	+1	nA
		−40°C < T_A < +125°C	-1.5		+1.5	
Input Voltage Range			−3.8		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.8 V to +3V	122	130		dB
		−40°C < T_A < +125°C	120			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −3.0 V to +3.0 V	121	130		dB
		−40°C < T_A < +125°C	118			dB
Input Capacitance	C_{INDM}	Differential Mode		TBD		pF
	C_{INCM}	Common Mode		TBD		pF
Input Resistance	R_{IN}			TBD		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	+4.1			V
		−40°C < T_A < +125°C	+4			
Output Voltage Low	V_{OL}	I_L = 1 mA			-3.5	V
		−40°C < T_A < +125°C			-3.2	
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
Short Circuit Current	I_{SC}	T_A = 25°C		TBD		mA
Closed Loop Output Impedance	Z_{OUT}			TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±15 V (A-Grade)	123	128		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	450	µA
		−40°C < T_A < +125°C			660	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1		V/µs
Settling Time to 0.01%	t_s	V_{IN} =1V step, C_L = TBD, R_L = TBD, A_V = TBD		TBD		µs
Settling Time to 0.1%	t_s	V_{IN} =1V step, C_L = TBD, R_L = TBD, A_V = TBD		TBD		µs
Gain Bandwidth Product	GBP			4.0		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		µV p-p

Voltage Noise Density	e_n	f = 100 Hz	TBD	TBD	nV/√Hz
		f = 1 kHz	8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz	0.1		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	DC	0.01		µV/V
		f = 100 kHz	−120		dB

1. Vos does not include SHR effect

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted. **B Grade Specifications are targets only.**

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B-Grade, SOIC)[1]	V_{OS}			10	25	µV
		−40°C < T_A < +125°C			TBD	µV
Offset Voltage Drift (B-Grade, SOIC)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		0.1	0.25	µV/°C
Offset Voltage (A-Grade)[1]	V_{OS}					
SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
MSOP				50	110	µV
		−40°C < T_A < +125°C			230	µV
Offset Voltage Drift (A-Grade)	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
SOIC				0.2	0.55	µV/°C
MSOP				0.5	1.2	µV/°C
Offset Drift	$\Delta V_{OS}/\Delta$Time			TBD		µV/mon
Input Bias Current	I_B		−1	TBD	+1	nA
		−40°C < T_A < +125°C	-1.5		+1.5	nA
Input Offset Current	I_{OS}		−1		+1	nA
		−40°C < T_A < +125°C	-1.5	TBD	+1.5	nA
Input Voltage Range			−13.8		+13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.8 V to +13 V	132	140		dB
		−40°C < T_A < +125°C	130			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −13.0 V to +13.0V	125	130		dB
		−40°C < T_A < +125°C	122			dB
Input Capacitance	C_{INDM}	Differential Mode		TBD		pF
	C_{INCM}	Common Mode		TBD		pF
Input Resistance	R_{IN}			TBD		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	+14.1			V
		−40°C < T_A < +125°C	+14			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−13.5	V
		−40°C < T_A < +125°C			-13.2	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
Short Circuit Current	I_{SC}	T_A = 25ºC		TBD		mA
Closed Loop Output Impedance	Z_{OUT}			TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±15 V	123	128		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	500	µA
		−40°C < T_A < +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1		V/µs
Settling Time to 0.01%	t_s	V_{IN} =1V step, C_L = TBD, R_L = TBD, A_V = TBD		TBD		µs
Settling Time to 0.1%	t_s	V_{IN} =1V step, C_L = TBD, R_L = TBD, A_V = TBD		TBD		µs
Gain Bandwidth Product	GBP			3.9		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.25		µ$V_{p\text{-}p}$
Voltage Noise Density	e_n	f = 100 Hz		TBD	TBD	nV/√Hz
		f = 1 kHz		8		nV/√Hz

Current Noise Density	i_n	f = 1 kHz	0.1	pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	CS	DC f = 100 kHz	0.01 −120	µV/V dB

1. Vos does not include SHR effect

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_{S-} to V_{S+}
Differential Input Voltage	±Supply Voltage
Storage Temperature Range	
R and RM Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	
R, RM, RJ, and RU Packages	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	190	44	°C/W
8-Lead SOIC_N (R-8)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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