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- ADL5310 Evaluation Board

DOCUMENTATION

Application Notes

- AN-643: Closed-Loop Control Circuit Implementation of the ADuC832 MicroConverter®IC and the AD8305 Logarithmic Converter in a Digital Variable Optical Attenuator

Data Sheet

- ADL5310: 120dB-range (3 nA - 3 mA) Dual Logarithmic Converter Data Sheet

REFERENCE DESIGNS

- CN0056
- CN0057

REFERENCE MATERIALS

Informational

- Optical and High Speed Networking ICs

Technical Articles

- Design a Logamp RF Pulse Detector
- Log Amps and Directional Couplers Enable VSWR Detection
- Logarithmic Processing Applied to Network Power Monitoring

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REVISION HISTORY

9/04—Data Sheet Changed from Rev. 0 to Rev. A	
Changes to Ordering Guide	20
11/03—Revision 0: Initial Version	

SPECIFICATIONS

$V_P = 5\text{ V}$, $V_N = 0\text{ V}$, $T_A = 25^\circ\text{C}$, $R_{REF} = 665\text{ k}\Omega$, and VRDZ connected to VREF, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT INTERFACE					
Specified Current Range, I_{PD}	Pins 1 to 6: INP1 and INP2, IRF1 and IRF2, VSUM Flows toward INP1 pin or INP2 pin	3 n		3 m	A
Input Current Min/Max Limits	Flows toward INP1 pin or INP2 pin			10 m	A
Reference Current, I_{REF} , Range	Flows toward IRF1 pin or IRF2 pin	3 n		3 m	A
Summing Node Voltage	Internally preset; user alterable	0.46	0.5	0.54	V
Temperature Drift	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.030		mV/ $^\circ\text{C}$
Input Offset Voltage	$V_{IN} - V_{SUM}$, $V_{IREF} - V_{SUM}$	-20		+20	mV
LOGARITHMIC OUTPUTS					
Logarithmic Slope	Pin 15 and Pin 16: LOG1 and LOG2 $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	190	200	210	mV/dec
Logarithmic Intercept ¹	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	185		215	mV/dec
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	165	300	535	pA
	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	40		1940	pA
Law Conformance Error	$10\text{ nA} < I_{PD} < 1\text{ mA}$		0.1	0.4	dB
	$3\text{ nA} < I_{PD} < 3\text{ mA}$		0.3	0.6	dB
Wideband Noise ²	$I_{PD} > 3\text{ }\mu\text{A}$; output referred		0.5		$\mu\text{V}/\sqrt{\text{Hz}}$
Small Signal Bandwidth	$I_{PD} = 3\text{ }\mu\text{A}$		1.5		MHz
Maximum Output Voltage			1.7		V
Minimum Output Voltage	Limited by $V_N = 0\text{ V}$		0.10		V
Output Resistance		4.375	5	5.625	k Ω
REFERENCE OUTPUT					
Voltage wrt Ground	Pin 7 and Pin 24 (internally shorted): VREF $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	2.45	2.5	2.55	V
		2.42		2.58	V
Maximum Output Current	Sourcing (grounded load)		20		mA
Incremental Output Resistance	Load current $< 10\text{ mA}$		4		Ω
OUTPUT BUFFERS					
Input Offset Voltage	Pins 12 to 14 and 17 to 19: OUT2, SCL2, BIN2, BIN1, SCL1, and OUT1	-20		+20	mV
Input Bias Current	Flowing out of Pins 13, 14, 17, and 18		0.4		μA
Incremental Input Resistance			35		M Ω
Incremental Output Resistance	Load current $< 10\text{ mA}$; gain = 1		0.5		Ω
Output High Voltage	$R_L = 1\text{ k}\Omega$ to ground		$V_P -$ 0.1		V
Output Low Voltage	$R_L = 1\text{ k}\Omega$ to ground		0.10		V
Peak Source/Sink Current			30		mA
Small-Signal Bandwidth	Gain = 1		15		MHz
Slew Rate	0.2 V to 4.8 V output swing		15		V/ μs
POWER SUPPLY					
Positive Supply Voltage	Pins 8 and 9: VPOS; Pins 10, 11, and 20: VNEG $(V_P - V_N) \leq 12\text{ V}$	3	5	12	V
Quiescent Current	Input currents $< 10\text{ }\mu\text{A}$		9.5	11.5	mA
Negative Supply Voltage (Optional)	$(V_P - V_N) \leq 12\text{ V}$	-5.5	0		V

¹ Other values of logarithmic intercept can be achieved by adjustment of R_{REF} .

² Output noise and incremental bandwidth are functions of input current; measured using output buffer connected for GAIN = 1.

ABSOLUTE MAXIMUM RATINGS

Table 2.

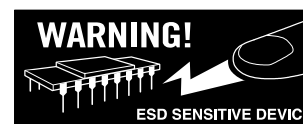
Parameter	Rating
Supply Voltage $V_P - V_N$	12 V
Input Current	20 mA
Internal Power Dissipation θ_{JA}	500 mW 35°C/W ¹
Maximum Junction Temperature	125°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

¹ With paddle soldered down.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

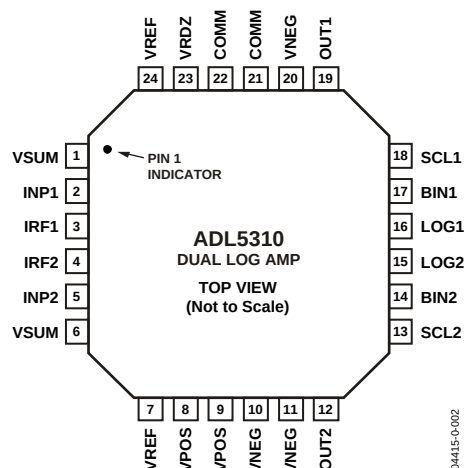


Figure 2. 24-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 6	VSUM	Guard Pin. Used to shield the INP1 and INP2 input current lines, and for optional adjustment of the input summing node potentials. Pin 1 and Pin 6 are internally shorted.
2	INP1	Channel 1 Numerator Input. Accepts (sinks) photodiode current I_{PD1} . Usually connected to photodiode anode such that photocurrent flows into INP1.
3	IRF1	Channel 1 Denominator Input. Accepts (sinks) reference current, I_{RF1} .
4	IRF2	Channel 2 Denominator Input. Accepts (sinks) reference current, I_{RF2} .
5	INP2	Channel 2 Numerator Input. Accepts (sinks) photodiode current I_{PD2} . Usually connected to photodiode anode such that photocurrent flows into INP2.
7, 24	VREF	Reference Output Voltage of 2.5 V. Pin 7 and Pin 24 are internally shorted.
8, 9	VPOS	Positive Supply, $(V_P - V_N) \leq 12$ V. Both pins must be connected externally.
10, 11, 20	VNEG	Optional Negative Supply, V_N . These pins are usually grounded. For more details, see the General Structure and Applications sections. All VNEG pins must be connected externally.
12	OUT2	Buffer Output for Channel 2.
13	SCL2	Buffer Amplifier Inverting Input for Channel 2.
14	BIN2	Buffer Amplifier Noninverting Input for Channel 2.
15	LOG2	Output of the Logarithmic Front End for Channel 2.
16	LOG1	Output of the Logarithmic Front End for Channel 1.
17	BIN1	Buffer Amplifier Noninverting Input for Channel 1.
18	SCL1	Buffer Amplifier Inverting Input for Channel 1.
19	OUT1	Buffer Output for Channel 1.
21, 22	COMM	Analog Ground. Pin 21 and Pin 22 are internally shorted.
23	VRDZ	Intercept Shift Reference Input. The top of a resistive divider network that offsets VLOG to position the intercept. Normally connected to VREF; may also be connected to ground when bipolar outputs are to be provided.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_P = 5\text{ V}$, $V_N = 0\text{ V}$, $R_{REF} = 665\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

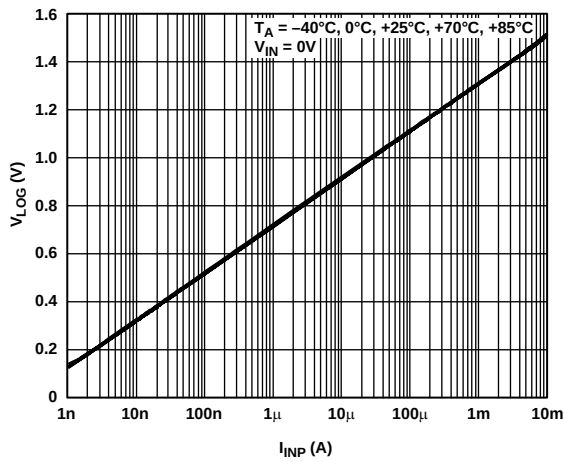


Figure 3. V_{LOG} vs. I_{INP} for Multiple Temperatures

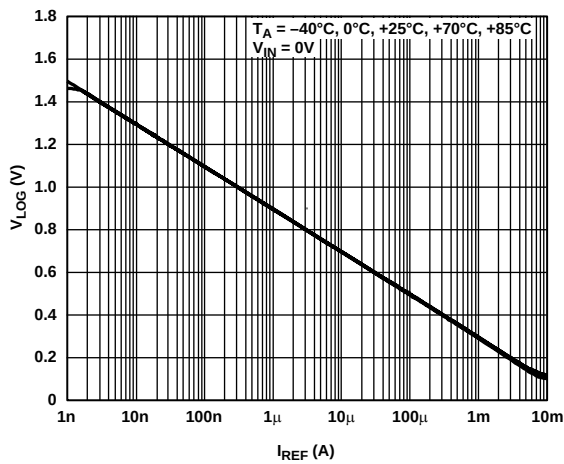


Figure 4. V_{LOG} vs. I_{REF} for Multiple Temperatures ($I_{INP} = 3\text{ }\mu\text{A}$)

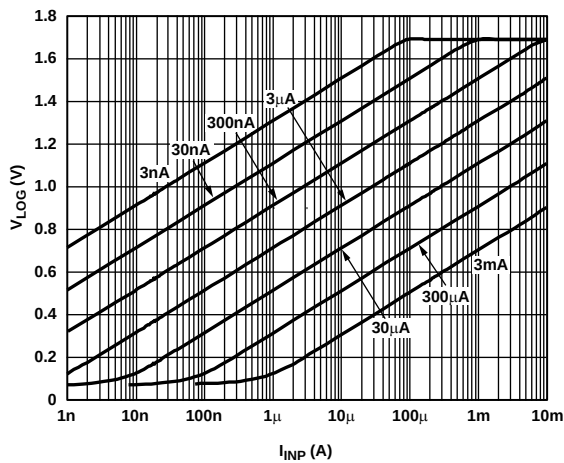


Figure 5. V_{LOG} vs. I_{INP} for Multiple Values of I_{REF} , Decade Steps from 3 nA to 3 mA

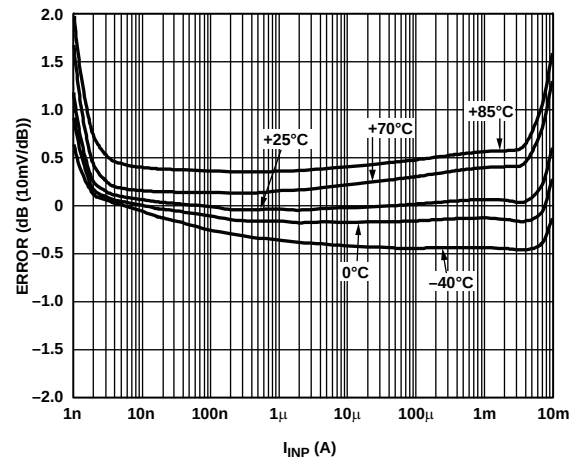


Figure 6. Law Conformance Error vs. I_{INP} for Multiple Temperatures, Normalized to 25°C

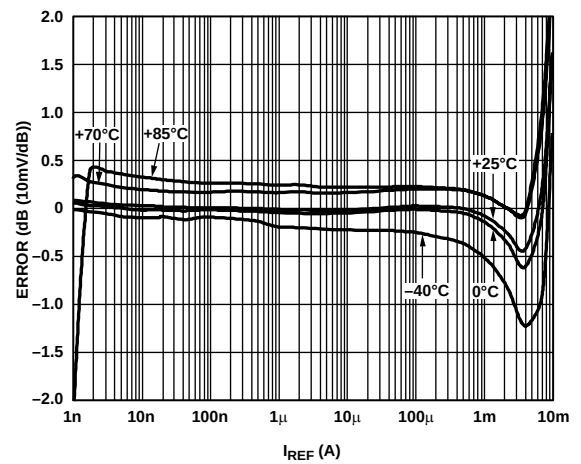


Figure 7. Law Conformance Error vs. I_{REF} for Multiple Temperatures, Normalized to 25°C ($I_{INP} = 3\text{ }\mu\text{A}$)

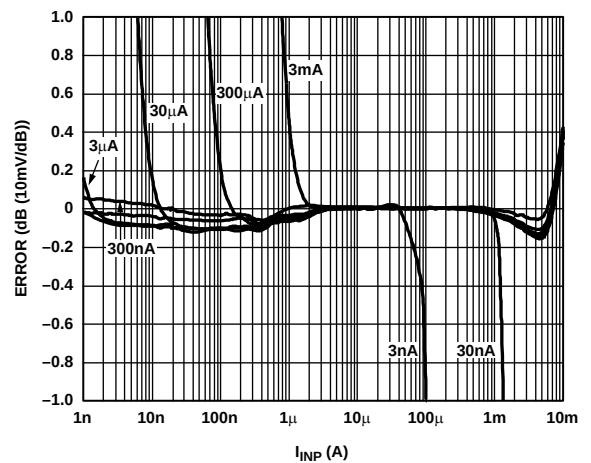


Figure 8. Law Conformance Error vs. I_{INP} for Multiple Values of I_{REF} , Decade Steps from 3 nA to 3 mA

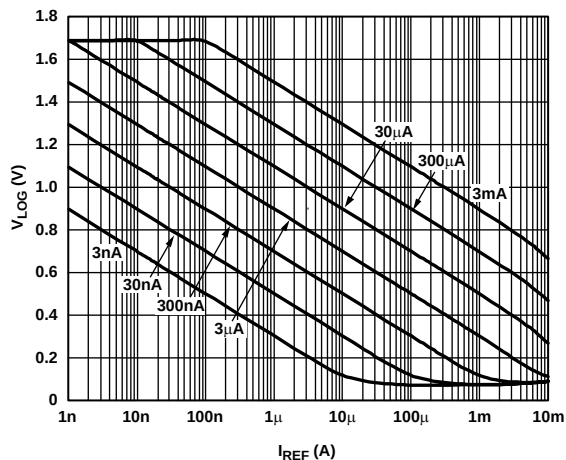


Figure 9. V_{LOG} vs. I_{REF} for Multiple Values of I_{INP} , Decade Steps from 3 nA to 3 mA

04415-0-009

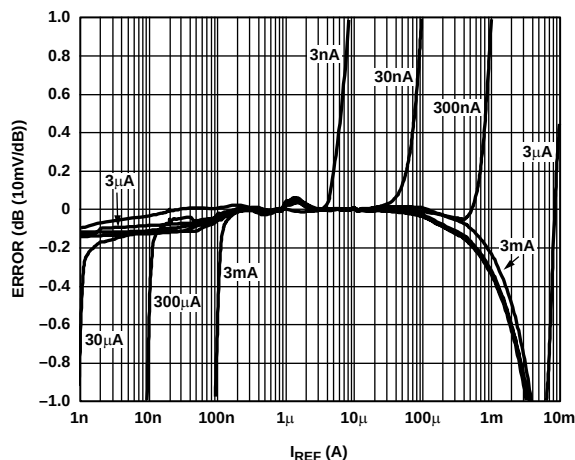


Figure 12. Law Conformance Error vs. I_{REF} for Multiple Values of I_{INP} , Decade Steps from 3 nA to 3 mA

04415-0-012

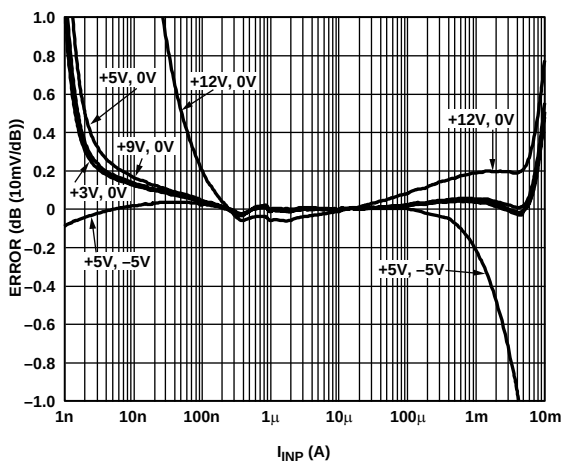


Figure 10. Law Conformance Error vs. I_{INP} for Various Supply Conditions

04415-0-010

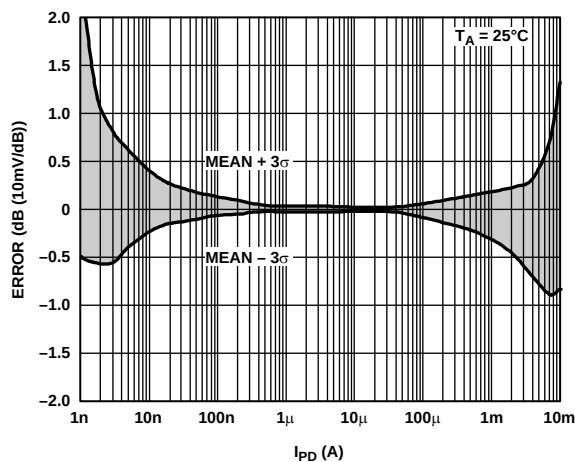


Figure 13. Law Conformance Error Distribution (3σ to Either Side of Mean)

04415-0-013

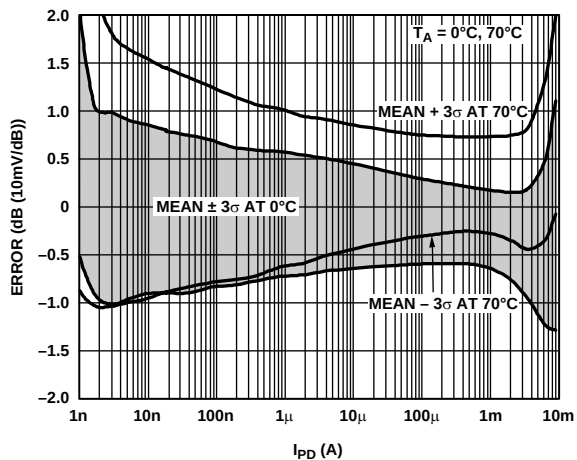


Figure 11. Law Conformance Error Distribution (3σ to Either Side of Mean)

04415-0-011

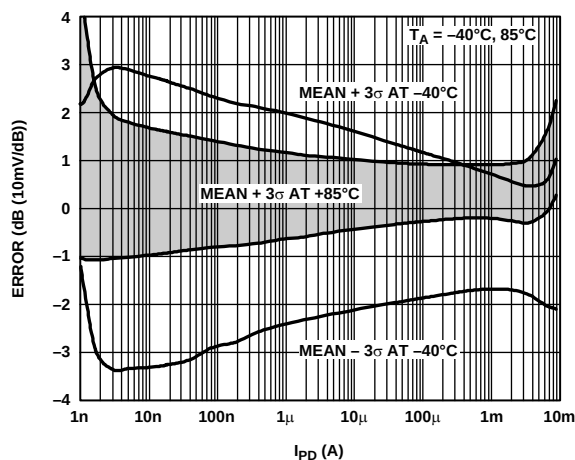


Figure 14. Law Conformance Error Distribution (3σ to Either Side of Mean)

04415-0-014

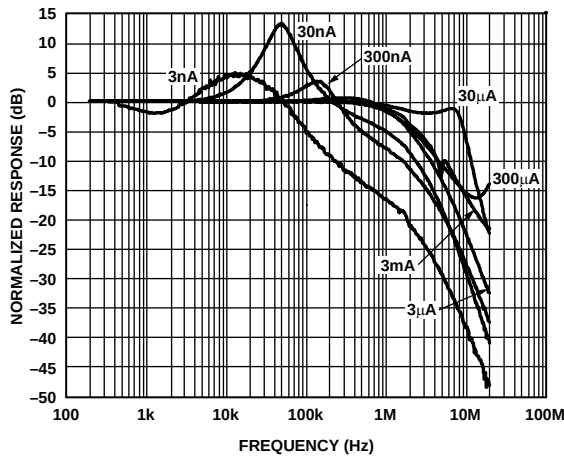


Figure 15. Small Signal AC Response, I_{INP} to V_{OUT} ($A_V = 1$) (5% Sine Modulation, Decade Steps from 3 nA to 3 mA)

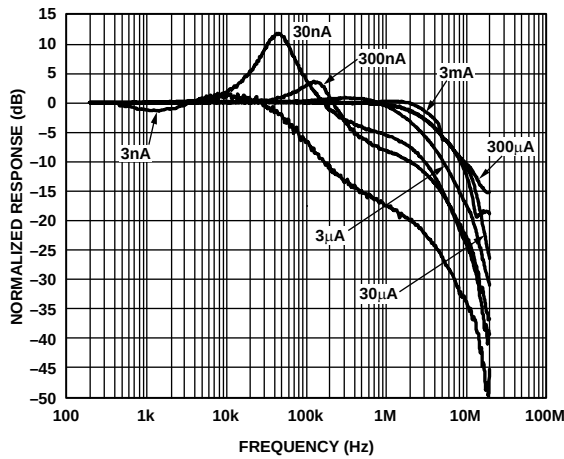


Figure 16. Small Signal AC Response, I_{REF} to V_{OUT} ($A_V = 1$) (5% Sine Modulation, Decade Steps from 3 nA to 3 mA)

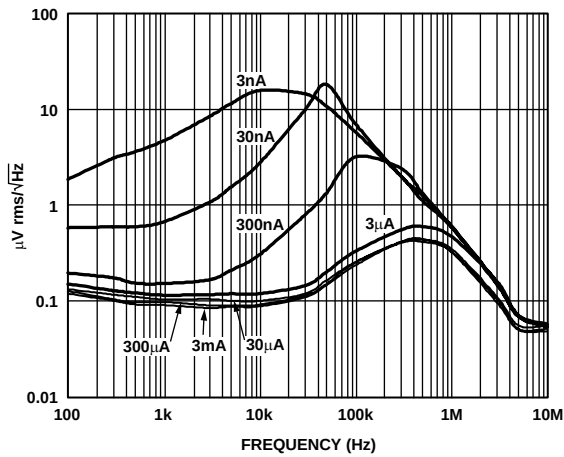


Figure 17. Spot Noise Spectral Density at V_{OUT} vs. Frequency ($A_V = 1$) for I_{INP} in Decade Steps from 3 nA to 3 mA

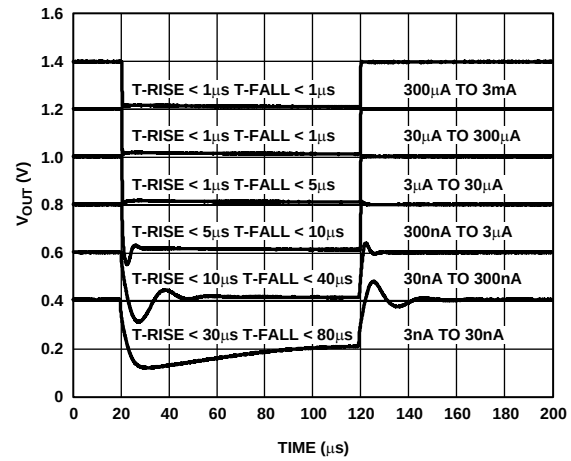


Figure 18. Pulse Response— I_{INP} to V_{OUT} ($A_V = 1$) in Consecutive 1-Decade Steps

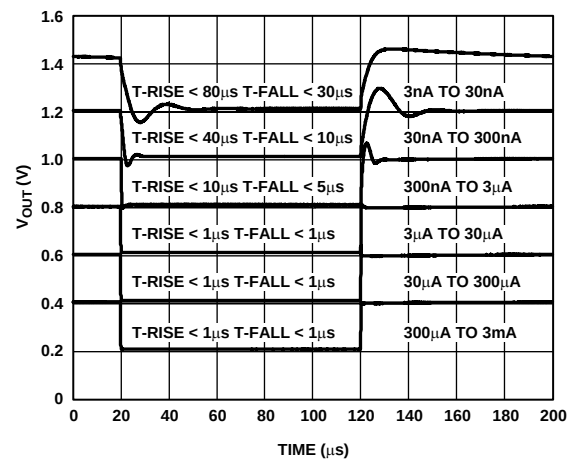


Figure 19. Pulse Response— I_{REF} to V_{OUT} ($A_V = 1$) in Consecutive 1-Decade Steps

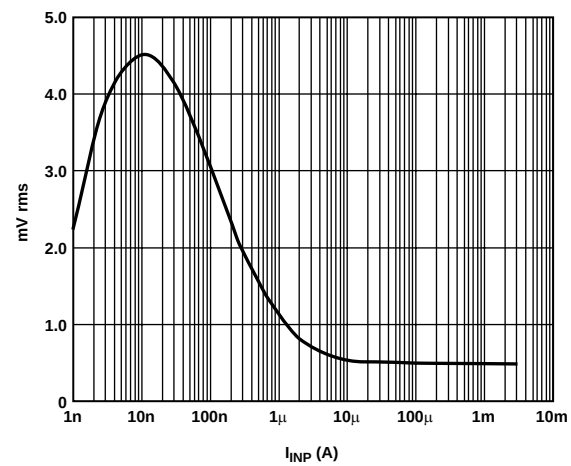


Figure 20. Total Wideband Noise Voltage at V_{OUT} vs. I_{INP} ($A_V = 1$)

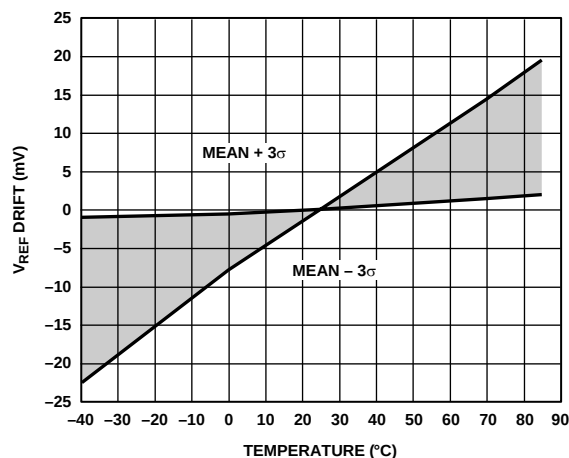


Figure 21. V_{REF} Drift vs. Temperature (3σ to Either Side of Mean) Normalized to 25°C

04415-0-021

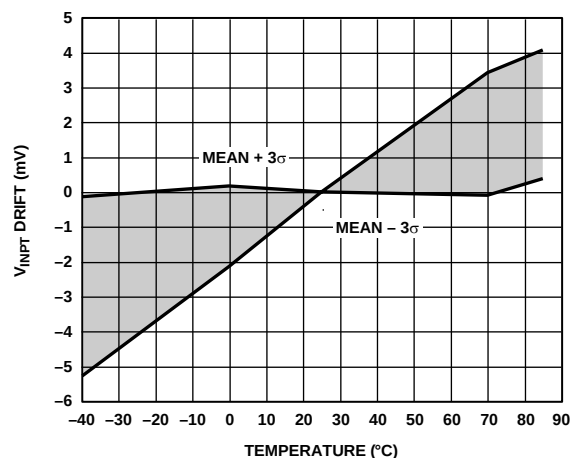


Figure 24. V_{INPT} Drift vs. Temperature (3σ to Either Side of Mean) Normalized to 25°C

04415-0-024

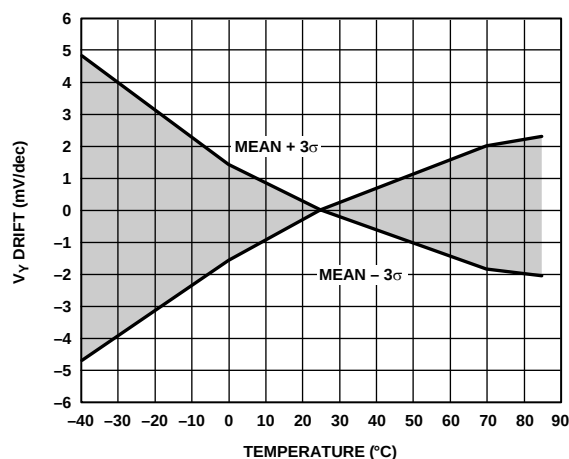


Figure 22. Slope Drift vs. Temperature (3σ to Either Side of Mean) Normalized to 25°C

04415-0-022

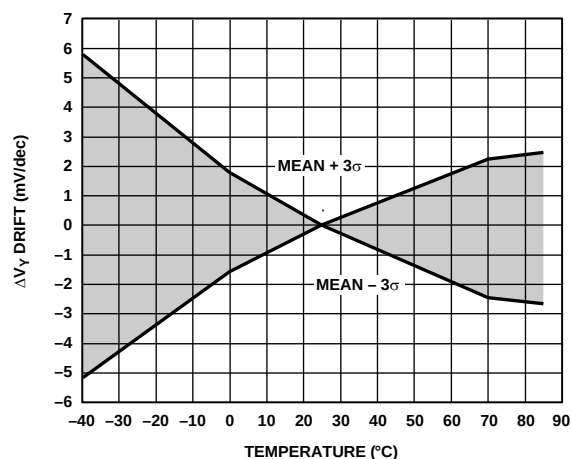


Figure 25. Slope Mismatch Drift vs. Temperature ($V_{Y1} - V_{Y2}$, 3σ to Either Side of Mean) Normalized to 25°C

04415-0-025

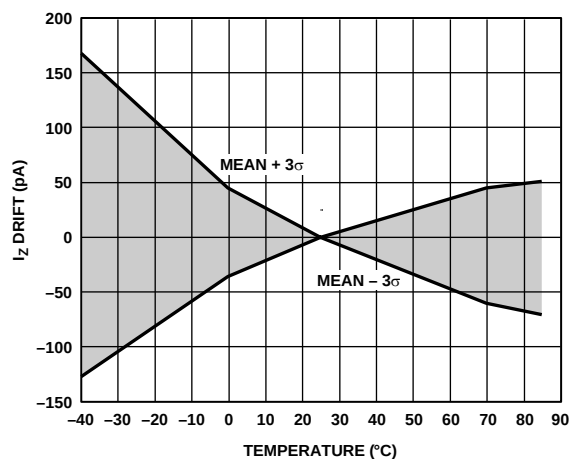


Figure 23. Intercept Drift vs. Temperature (3σ to Either Side of Mean) Normalized to 25°C

04415-0-023

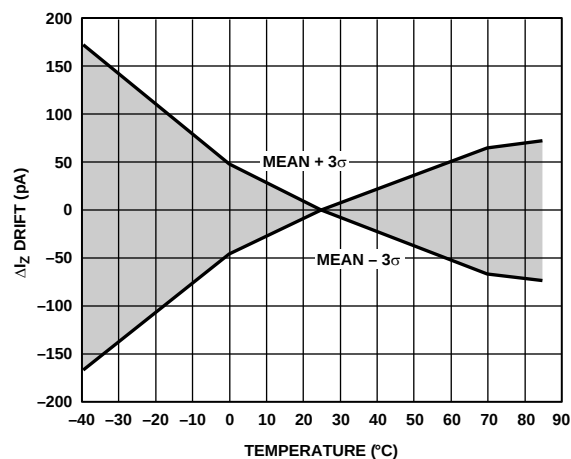


Figure 26. Intercept Mismatch Drift vs. Temperature ($I_{Z1} - I_{Z2}$, 3σ to Either Side of Mean) Normalized to 25°C

04415-0-026

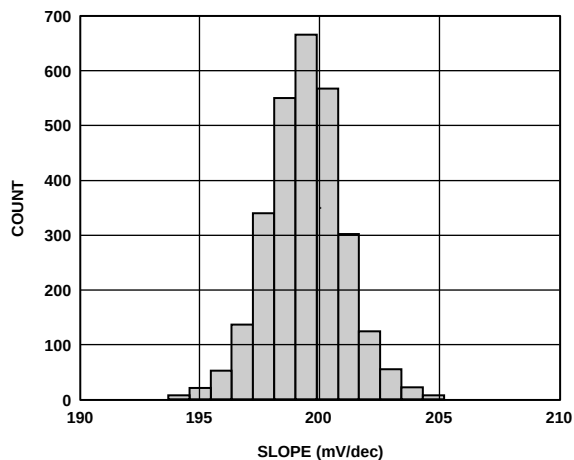
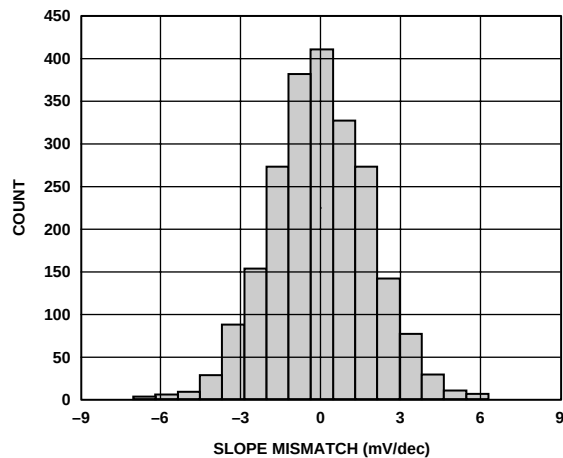


Figure 27. Distribution of Logarithmic Slope

04415-0-027

Figure 30. Distribution of Channel-to-Channel Slope Mismatch ($V_{I1} - V_{I2}$)

04415-0-030

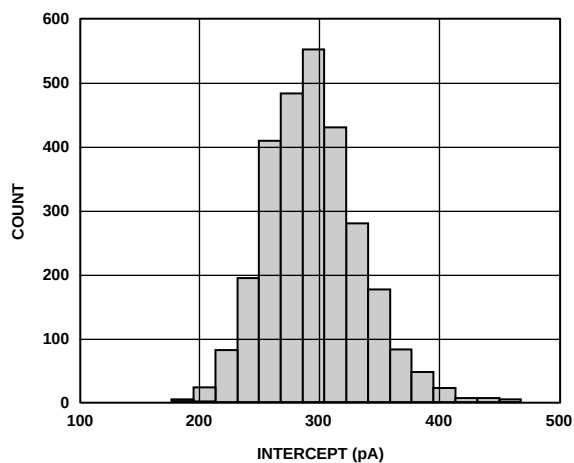
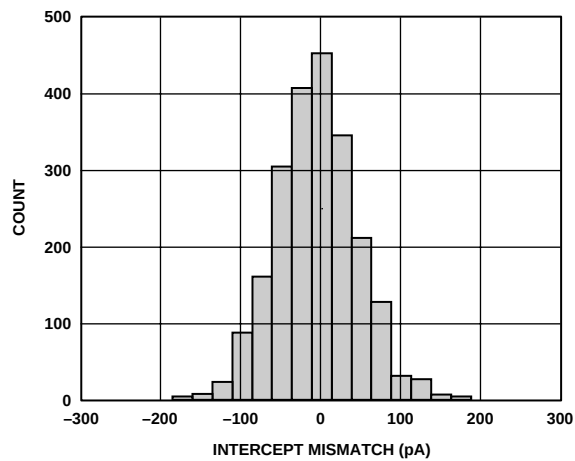
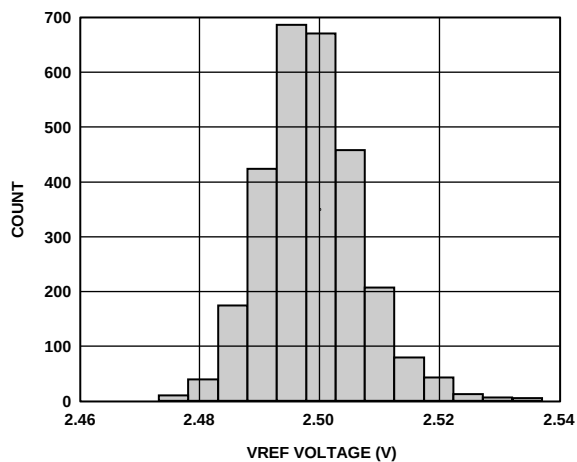


Figure 28. Distribution of Logarithmic Intercept

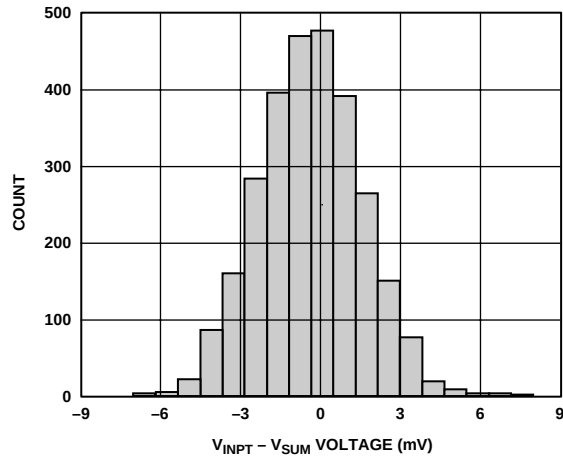
04415-0-028

Figure 31. Distribution of Channel-to-Channel Intercept Mismatch ($I_{I1} - I_{I2}$)

04415-0-031

Figure 29. Distribution of V_{REF} ($R_L = 100\text{ k}\Omega$)

04415-0-029

Figure 32. Distribution of Offset Voltage ($V_{INPT} - V_{SUM}$)

04415-0-032

The voltage V_{LOG} is generated by applying I_{LOG} to an internal resistance of 4.55 k Ω , formed by the parallel combination of a 6.69 k Ω resistor to ground and a 14.2 k Ω resistor to Pin VRDZ (typically tied to the 2.5 V reference, VREF). At the LOG1 (LOG2) pin, the output current I_{LOG} generates a voltage of

$$\begin{aligned} V_{LOG} &= I_{LOG} \times 4.55 \text{ k}\Omega \\ &= 44 \mu\text{A} \times 4.55 \text{ k}\Omega \times \log_{10}(I_{PD}/I_{INTC}) \\ &= V_Y \log_{10}(I_{PD}/I_{INTC}) \end{aligned} \quad (5)$$

where $V_Y = 200 \text{ mV/decade}$ or 10 mV/dB . Note that any resistive loading on LOG1 (LOG2) lowers this slope and results in an overall scaling uncertainty. This is due to the variability of the on-chip resistors compared to the off-chip load. As a consequence, this practice is not recommended.

V_{LOG} may also swing below ground when dual supplies (V_P and V_N) are used. When $V_N = -0.5 \text{ V}$ or larger, the input Pins INP1 (INP2) and IRF1 (INP2) may be positioned at ground level simply by grounding VSUM. Care must be taken to limit the power consumed by the input BJT devices when using a larger negative supply, because self-heating degrades the accuracy at higher currents.

MANAGING INTERCEPT AND SLOPE

When using a single supply, VRDZ should be directly connected to VREF to allow operation over the entire 6-decade input current range. As noted in the Theory section, this introduces an accurate offset voltage of 0.8 V at the LOG1 and LOG2 pins, equivalent to four decades, resulting in a logarithmic transfer function that can be written as

$$\begin{aligned} V_{LOG} &= V_Y \log_{10}(10^4 \times I_{PD}/I_{REF}) \\ &= V_Y \log_{10}(I_{PD}/I_{INTC}) \end{aligned} \quad (6)$$

where $I_{INTC} = I_{REF}/10^4$.

Thus, the effective intercept current I_{INTC} is only one ten-thousandth of I_{REF} , corresponding to 300 pA when using the recommended value of $I_{REF} = 3 \mu\text{A}$.

The slope can be reduced by attaching a resistor between the log amp output pin, LOG1 or LOG2, and ground. This is strongly discouraged given that the on-chip resistors do not ratio correctly to the added resistance. Also, it is rare that one would wish to lower the basic slope of 10 mV/dB; if this is needed, it should be effected at the low impedance output of the buffer amps, which are provided to avoid such miscalibration and to allow higher slopes to be used.

Each of the ADL5310's buffers is essentially an uncommitted operational amplifier with rail-to-rail output swing, good load-driving capabilities, and a typical unity-gain bandwidth of 15 MHz. In addition to allowing the introduction of gain, using standard feedback networks and thereby increasing the slope voltage V_Y , the buffer can be used to implement multipole, low-pass filters, threshold detectors, and a variety of other functions. Further details on these applications can be found in the AD8304 data sheet.

RESPONSE TIME AND NOISE CONSIDERATIONS

The response time and output noise of the ADL5310 are fundamentally a function of the signal current, I_{PD} . For small currents, the bandwidth is proportional to I_{PD} , as shown in Figure 15. The output low frequency voltage-noise spectral-density is a function of I_{PD} (see Figure 17) and also increases for small values of I_{REF} . Details of the noise and bandwidth performance of translinear log amps can be found in the AD8304 data sheet.

APPLICATIONS

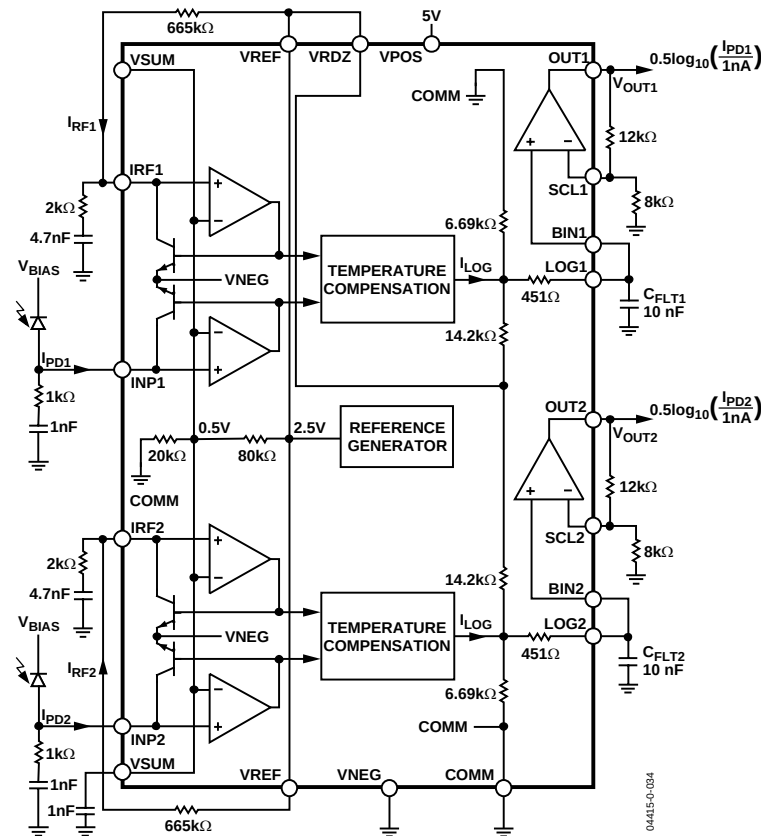


Figure 34. Basic Connections for Fixed Intercept Use

The ADL5310 is easy to use in optical supervisory systems and in similar situations where a wide-ranging current is to be converted to its logarithmic equivalent—that is, represented in decibel terms. Basic connections for measuring a single current at each input are shown in Figure 34, which also includes various nonessential components, as explained next.

The 2 V difference in voltage between the VREF and Input Pins INP1 and INP2, in conjunction with the external 665 kΩ resistors R_{RF1} and R_{RF2} , provides 3 μA reference currents I_{RF1} and I_{RF2} into Pins IRF1 and IRF2. Connecting VRDZ to VREF raises the voltage at LOG1 and LOG2 by 0.8 V, effectively lowering each intercept current I_{INTC} by a factor of 10^4 to position it at 300 pA. A wide range of other values for I_{REF} , from 3 nA to 3 mA, may be used. The effect of such changes is shown in Figure 5 and Figure 8.

Any temperature variation in R_{RF1} (R_{RF2}) must be taken into account when estimating the stability of the intercept. Also, the overall noise increases when using very low values of I_{RF1} (I_{RF2}). In fixed-intercept applications there is little benefit in using a large reference current, because doing so only compresses the low-current-end of the dynamic range when operated from a single supply. The capacitor between VSUM and ground is

strongly recommended to minimize the noise on this node, to reduce channel-to-channel crosstalk, and to help provide clean reference currents.

In addition, each input and reference pin (INP1, INP2, IRF1, and IRF2) has a compensation network made up of a series resistor and capacitor. The junction capacitance of the photodiode along with the network capacitance of the board artwork around the input system creates a pole that varies widely with input current. The RC network stabilizes the system by simultaneously reducing this pole frequency and inserting a zero to compensate an additional pole inherent in the input system. In general, the 1 nF, 1 kΩ network handles almost any photodiode interface. In situations where larger active area photodiodes are used, or when long input traces are used, the capacitor value may need to be increased to ensure stability. Although the signal and reference input systems are similar, additional care is required to ensure stable operation of the reference inputs at temperature extremes across the full current range of I_{RF1} (I_{RF2}). It is recommended that filter components of 4.7 nF and 2 kΩ should be used from Pin IRF1 (IRF2) to ground. Temperature-stable components should always be used in critical locations such as the compensation networks; Y5V-type chip capacitors are to be avoided due to their poor temperature stability.

The optional capacitor from LOG1 (LOG2) to ground forms a single-pole, low-pass filter in combination with the 5 kΩ resistance at this pin. For example, when using a C_{FLT} of 10 nF, the 3 dB corner frequency is 3.2 kHz. Such filtering is useful in minimizing the output noise, particularly when I_{PD} is small. Multipole filters are more effective in reducing the total noise; examples are provided in the AD8304 data sheet.

Because the basic scaling at LOG1 (LOG2) is 0.2 V/decade, and thus a 4 V swing at the buffer output would correspond to 20 decades, it is often useful to raise the slope to make better use of the rail-to-rail voltage range. For illustrative purposes, both channels in Figure 34 provide a 0.5 V/decade overall slope (25 mV/dB). Thus, using $I_{REF} = 3 \mu A$, V_{LOG} runs from 0.2 V at $I_{PD} = 3 \text{ nA}$ to 1.4 V at $I_{PD} = 3 \text{ mA}$; the buffer output runs from 0.5 V to 3.5 V, corresponding to a dynamic range of 120 dB (electrical, that is, 60 dB optical power).

Further information on adjusting the slope and intercept, using a negative supply, and additional operations can be found in the AD8305 data sheet.

CALIBRATION

Each channel of the ADL5310 has a nominal slope and intercept at LOG1 (LOG2) of 200 mV/decade and 300 pA, respectively, when configured as shown in Figure 34. These values are untrimmed and the slope alone may vary by as much as 7.5% over temperature. For this reason, it is recommended that a simple calibration be done to achieve increased accuracy. While the ADL5310 offers improved slope and intercept matching compared to a randomly selected pair of AD8305 log amps, the specified accuracy can only be achieved by calibrating each channel individually.

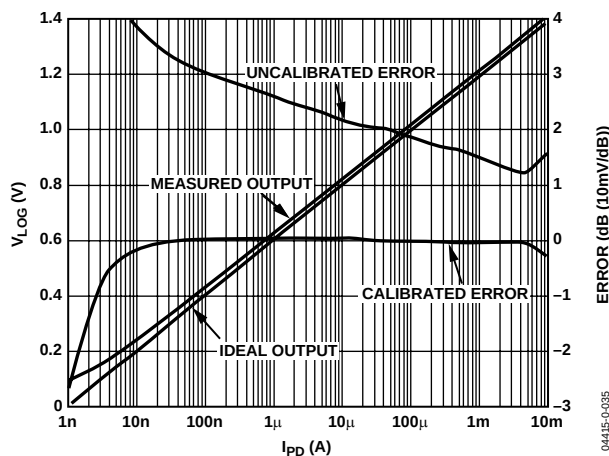


Figure 35. Using 2-Point Calibration to Increase Measurement Accuracy

Figure 35 shows the improvement in accuracy when using a 2-point calibration method. To perform this calibration, apply two known currents, I_1 and I_2 , in the linear operating range between 10 nA and 1 mA. Measure the resulting output, V_1 and V_2 , respectively, and calculate the slope m and the intercept b :

$$m = (V_1 - V_2) / [\log_{10}(I_1) - \log_{10}(I_2)] \quad (7)$$

$$b = V_1 - m \times \log_{10}(I_1) \quad (8)$$

The same calibration could be performed with two known optical powers, P_1 and P_2 . This allows for calibration of the entire measurement system while providing a simplified relationship between the incident optical power and V_{LOG} voltage:

$$m = (V_1 - V_2) / (P_1 - P_2) \quad (9)$$

$$b = V_1 - m \times P_1 \quad (10)$$

The uncalibrated error line in Figure 35 was generated assuming that the slope of the measured output was 200 mV/decade when in fact it was actually 194 mV/decade. Correcting for this discrepancy decreased measurement error up to 3 dB.

MINIMIZING CROSSTALK

Combining two high-dynamic-range logarithmic converters in one IC carries potential pitfalls concerning channel-to-channel isolation. Special care must be taken in several areas to ensure acceptable crosstalk performance, particularly when one or both channels may operate at very low input currents. Fastidious supply bypassing—also necessary for overall stability—and careful board layout are important first steps for minimizing crosstalk.

While the shared bias circuitry improves channel-to-channel matching and reduces power consumption, it is also a source of crosstalk that must be mitigated. The VSUM pins, which are internally shorted, should be bypassed with at least 1 nF to ground, and 20 nF is recommended for operation at the lowest currents (<30 nA). VSUM is of particular importance because it acts as a reference voltage input for each input system, but without the bandwidth limitation at low currents that the primary inputs incur. Disturbances at the VSUM pin that are well within the bandwidth of the input are tracked by the loop and do not generate disturbances at the output (aside from the generally minor perturbation in reference currents caused by voltage variations at IRF1 and IRF2).

For this reason, the pole frequency at VSUM, which has a 16 kΩ typical source resistance, should be set below the minimum input system bandwidth for the lowest input current to be encountered. Because the low frequency noise at VSUM is also tracked by the loop within its available bandwidth, this is also a criterion for reducing the noise contribution at the output from the thermal noise of the 16 kΩ source resistance at VSUM.

The solution in Figure 37 is no longer subject to potential channel mismatch issues. Individual channel slope and intercept characteristics can be calibrated independently. The accuracy was verified using a pair of calibrated current sources. The performance of the circuit depicted in Figure 37 is shown in Figure 38 and Figure 39. Multiple transfer functions and error plots are provided for various power levels. The accuracy is better than 0.1 dB over a 5-decade range. The dynamic range is slightly reduced for strong I_{IN} input currents. This is due to the limited available swing of the VLOG pin and can be recovered through careful selection of input and output optical tap coupling ratios.

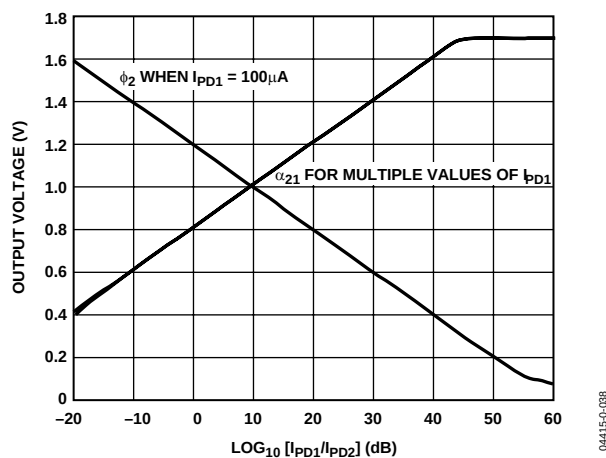


Figure 38. Absorbance and Absolute Power Transfer Functions for Wilson Mirror ADL5310 Combination

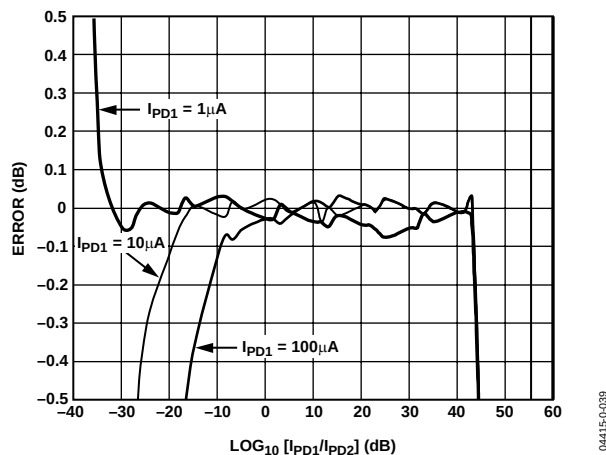


Figure 39. Log Conformance for Wilson Mirror ADL5310 Combination, Normalized to 10 mA Channel 1 Input Current, I_{IN1}

CHARACTERIZATION METHODS

During the characterization of the ADL5310, the device was treated as a precision current-input logarithmic converter, because it is impractical to generate accurate photocurrents by illuminating a photodiode. The test currents were generated by using either a well-calibrated current source, such as the Keithley 236, or a high value resistor from a voltage source to the input pin. Great care is needed when using very small input currents. For example, the triax output connection from the current generator was used with the guard tied to VSUM. The input trace on the PC board was guarded by connecting adjacent traces to VSUM.

These measures are needed to minimize the risk of leakage current paths. With 0.5 V as the nominal bias on the INP1 (INP2) pin, a leakage-path resistance of 1 G Ω to ground would subtract 0.5 nA from the input, which amounts to a -1.6 dB error for a 3 nA source current. Additionally, the very high sensitivity at the input pins and the long cables commonly needed during characterization allow 60 Hz and RF emissions to introduce substantial measurement errors. Careful guarding techniques are essential to reducing the pickup of these spurious signals.

Additional information, including test setups, can be found in the AD8305 and ADL5306 data sheets.

EVALUATION BOARD

An evaluation board is available for the ADL5310 (Figure 40 shows the schematic). It can be configured for a wide variety of experiments. The gain of each buffer amp is factory-set to unity, providing a slope of 200 mV/dec, and the intercept is set to 300 pA. Table 4 describes the various configuration options.

Table 4. Evaluation Board Configuration Options

Component	Function	Default Condition
P1	Supply Interface. Provides access to the Supply Pins VNEG, COMM, and VPOS.	P1 = installed
P2, R1, R3, R8, R9, R17, R22, R25, R30	Monitor Interface. By adding 0 Ω resistors to R1, R3, R8, R9, R17, R22, and R25, the VRDZ, VREF, VSUM, BIN1, BIN2, OUT1, and OUT2 pin voltages can be monitored using a high impedance probe. VBIAS allows for the external bias voltages to be applied to J1 and J2. If R30 = 0 Ω , VBIAS = VREF.	P2 = not installed R1 = R3 = R8 = open (size 0402) R9 = R17 = open (size 0402) R22 = R25 = R30 = open (size 0402)
R5, R6, R7, R16, R18, R19, R20, R21, R31, R32, C4, C14, C15, C16, C19, C20	Buffer Amplifier/Output Interface. The logarithmic slopes of the ADL5310 can be altered using each buffer's gain-setting resistors, R5 and R6, and R18 and R19. R7, R16, R31, R32, C19, and C20 allow for variation in the buffer loading. R20, R21, C4, C14, C15, and C16 are provided for a variety of filtering applications.	R5 = R19 = 0 Ω (size 0402) R7 = R16 = 0 Ω (size 0402) R20 = R21 = 0 Ω (size 0402) R6 = R18 = open (size 0402) R31 = R32 = open (size 0402) C4 = C14 = open (size 0402) C19 = C20 = open (size 0402) C15 = C16 = open (size 0402) LOG1 = OUT1 = installed LOG2 = OUT2 = installed
R2, R28, R29	Intercept Adjustment. The voltage dropped across Resistors R28 and R29 determines the intercept reference current for each log amp, nominally set to 3 μ A using a 665 k Ω 1% resistor. R2 can be used to adjust the output offset voltage at the LOG1 and LOG2 outputs.	R28 = R29 = 665 k Ω (size 0402) R2 = 0 Ω (size 0402)
R4, R10, R11, C2, C3, C5, C6, C8, C9	Supply Decoupling.	C2 = C5 = C9 = 100 pF (size 0402) C3 = C6 = C8 = 0.01 μ F (size 0402) R4 = R10 = R11 = 0 Ω (size 0402)
C1, C7 R12, R13, R14, R15, C10, C11, C12, C13	Filtering VSUM. Input Compensation. Provides essential HF compensation at the Input Pins INP1, INP2, IRF1, and IRF2.	C1 = C7 = 0.01 μ F (size 0402) R12 = R15 = 1 k Ω (size 0402) R13 = R14 = 2 k Ω (size 0402) C10 = C13 = 1 nF (size 0402) C11 = C12 = 4.7 nF (size 0402)
IREF, INPT	Input Interface. The test board is configured to accept current through the SMA connectors labeled INP1 and INP2. Through-holes are provided to connect photodiodes in place of the INP1 and INP2 SMAs for optical interfacing. By removing R28 (R29 for INP2), a second current can be applied to the IRF1 (IRF2 for INP2) input (also SMA) for evaluating the ADL5310 in log ratio applications.	IREF = INPT = installed
J1, J2	SC-Style Photodiode. Provides for the direct mounting of SC-style photodiodes.	J1 = J2 = open

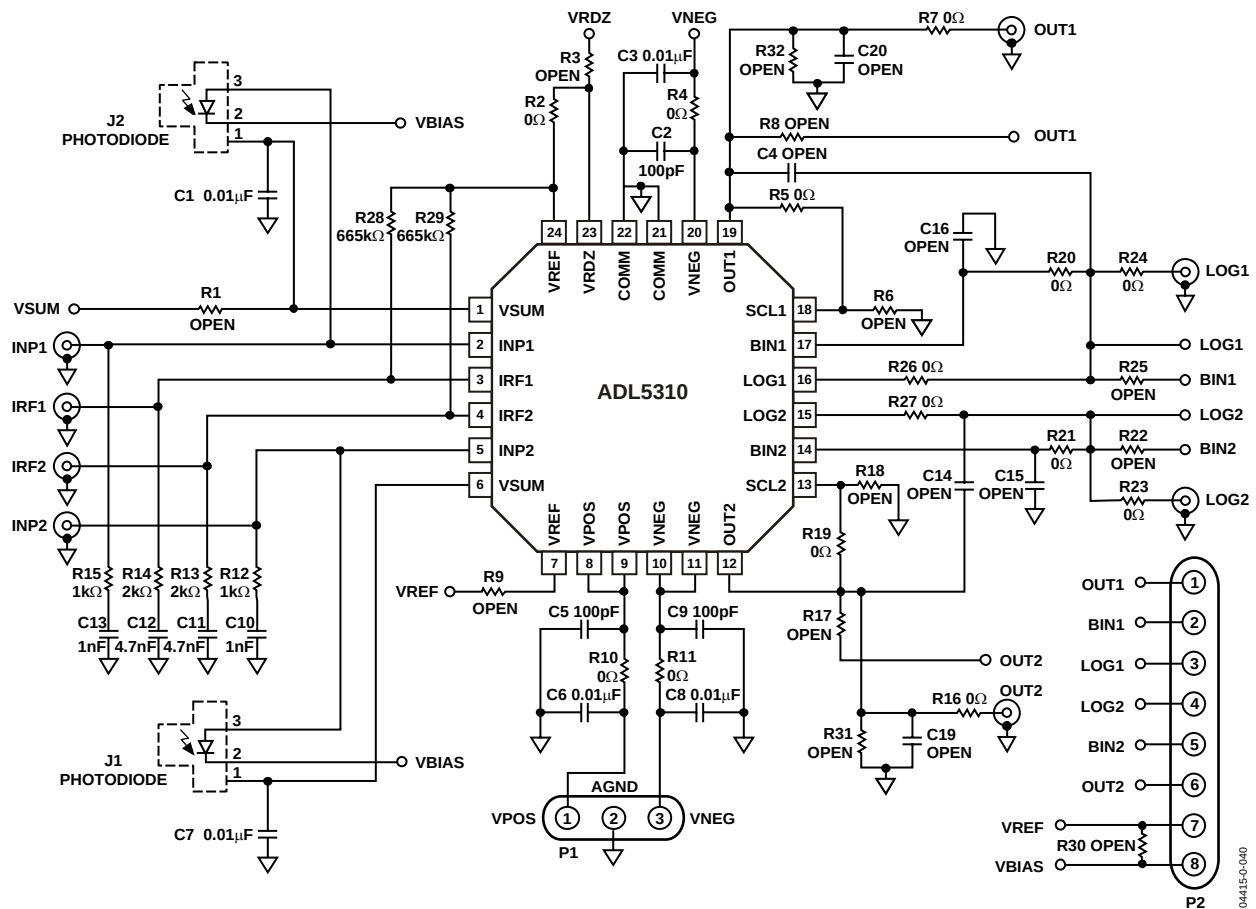


Figure 40. Evaluation Board Schematic

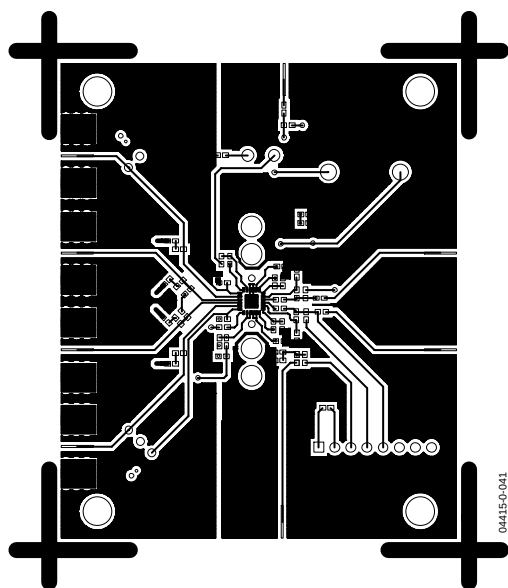


Figure 41. Component-Side Layout

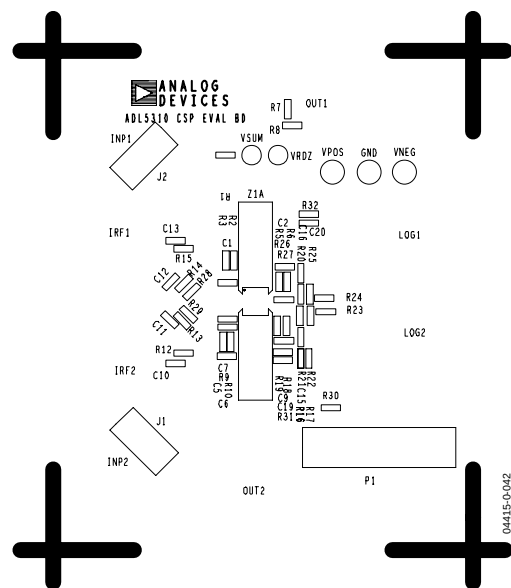
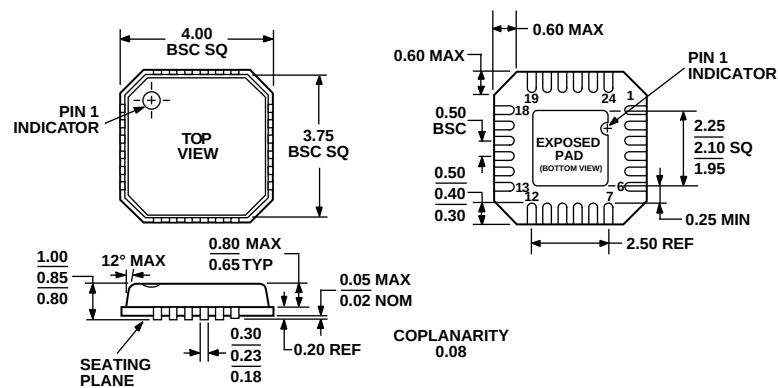


Figure 42. Component-Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2

Figure 43. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding ¹
ADL5310ACP-R2	–40°C to +85°C	24-Lead LFCSP	CP-24-1	JQA
ADL5310ACP-REEL7	–40°C to +85°C	24-Lead LFCSP	CP-24-1	JQA
ADL5310-EVAL		Evaluation Board		

¹ Branding is as follows:
Line 1 — JQA
Line 2 — Lot Code
Line 3 — (Date Code) Date Code is in YYWW format