

Evaluating the **ADMV4420**, K Band Downconverter with Integrated Fractional-N PLL and VCO

FEATURES

Full feature evaluation board for the **ADMV4420**

On-board **SDP-5** connector for SPI control

5 V operation

ACE software interface for SPI control

EVALUATION KIT CONTENTS

ADMV4420-EVALZ

EQUIPMENT NEEDED

5 V dc power supply

SDP-5 controller board

USB cable

RF signal generator

Spectrum analyzer

50 Ω SMA female to 75 Ω Type F male adapter

DOCUMENTS NEEDED

ADMV4420 data sheet

ADMV4420-EVALZ user guide

SOFTWARE NEEDED

Analysis, Control, Evaluation (ACE) software

GENERAL DESCRIPTION

The **ADMV4420** is a highly integrated, double balanced, active mixer with integrated fractional-N synthesizer, ideally suited for next generation K band satellite communications.

The radio frequency (RF) front end consists of an integrated RF balun and a low noise amplifier (LNA) for optimum 7 dB, single sideband noise figure while minimizing external components. Additionally, the high dynamic range intermediate frequency (IF) output amplifier provides a nominal conversion gain of 36 dB.

An integrated, low phase noise, fractional-N phase-locked loop (PLL) with a multicore voltage controlled oscillator (VCO) and an internal $\times 2$ multiplier generates the necessary on-chip local oscillator (LO) signal for the double balanced mixer, eliminating the need for external frequency synthesis. The multicore VCO

EVALUATION BOARD PHOTOGRAPH



Figure 1.

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uses an internal autocalibration routine that allows the PLL to select the necessary settings and lock in approximately 400 μ s.

The reference input to the PLL employs a differentially excited 50 MHz crystal oscillator on the evaluation board. Alternatively, the reference input can be driven by an external single-ended reference source. The phase frequency detector (PFD) comparison frequency of the PLL operates up to 50 MHz.

The **ADMV4420** is fabricated on a silicon germanium (SiGe), bipolar complementary metal-oxide semiconductor (BiCMOS) process and is available in a 32-lead, RoHS compliant, 5 mm \times 5 mm LFCSP with an exposed pad. The device is specified over the -40°C to $+85^{\circ}\text{C}$ temperature range on a 5 V power supply.

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REVISION HISTORY

10/2018—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADMV4420-EVALZ comes with an [ADMV4420](#) chip. Figure 4 shows the location of this chip on the evaluation board and the block diagram of the [ADMV4420](#).

When evaluating the device, connect the RF input to an RF signal generator. The ADMV4420-EVALZ runs on a 5 V dc supply. Figure 2 shows the top side of the ADMV4420-EVALZ and is intended for evaluation purposes only.

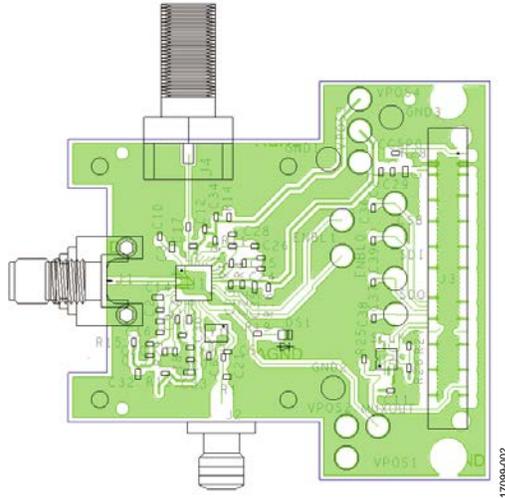


Figure 2. Top View of the ADMV4420-EVALZ

Connect the 5 V dc to the VPOS1 test point and ground to the GND2 test point on the ADMV4420-EVALZ. Connect a 50 Ω SMA female to a 75 Ω Type F male adapter to J4 (IF output). Connect the output of the adapter to a spectrum analyzer. The ADMV4420-EVALZ has 50 MHz crystal on board. Optionally, the user can connect a reference signal from a low phase signal generator to the J2 SMA connector. If the user wants to use an external reference, depopulate Y1, C5, and C6 and then install a 0.01 μF capacitor at C21, a 1 nF capacitor at C6, and 50 Ω at R21. See Figure 5 for ADMV4420-EVALZ lab connections. Figure 3 shows the block diagram of the [ADMV4420](#) lab bench setup.

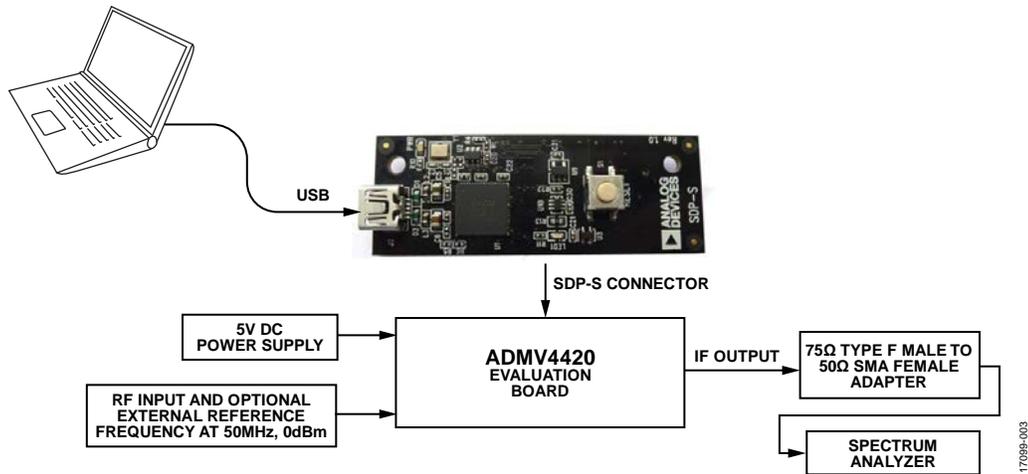


Figure 3. Block Diagram of the ADMV4420-EVALZ Lab Bench Setup

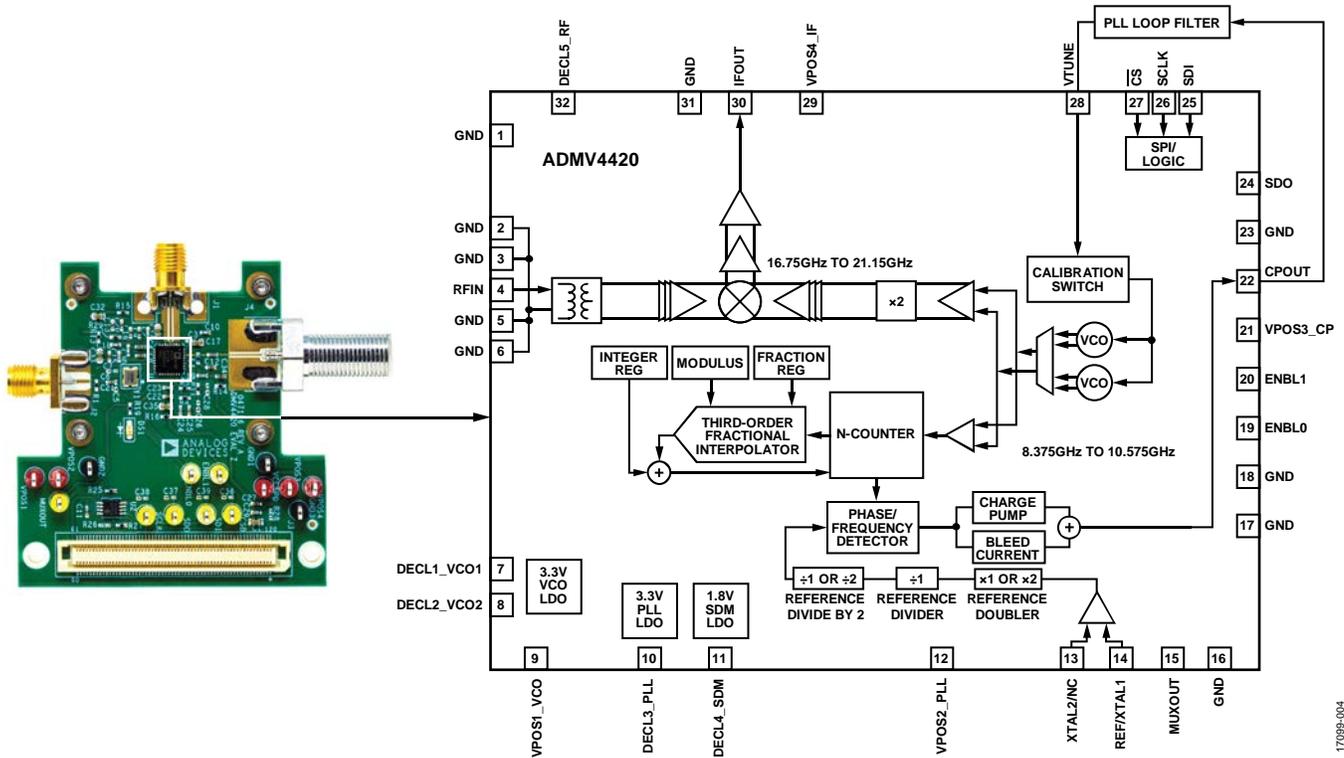


Figure 4. Evaluation Board Configuration

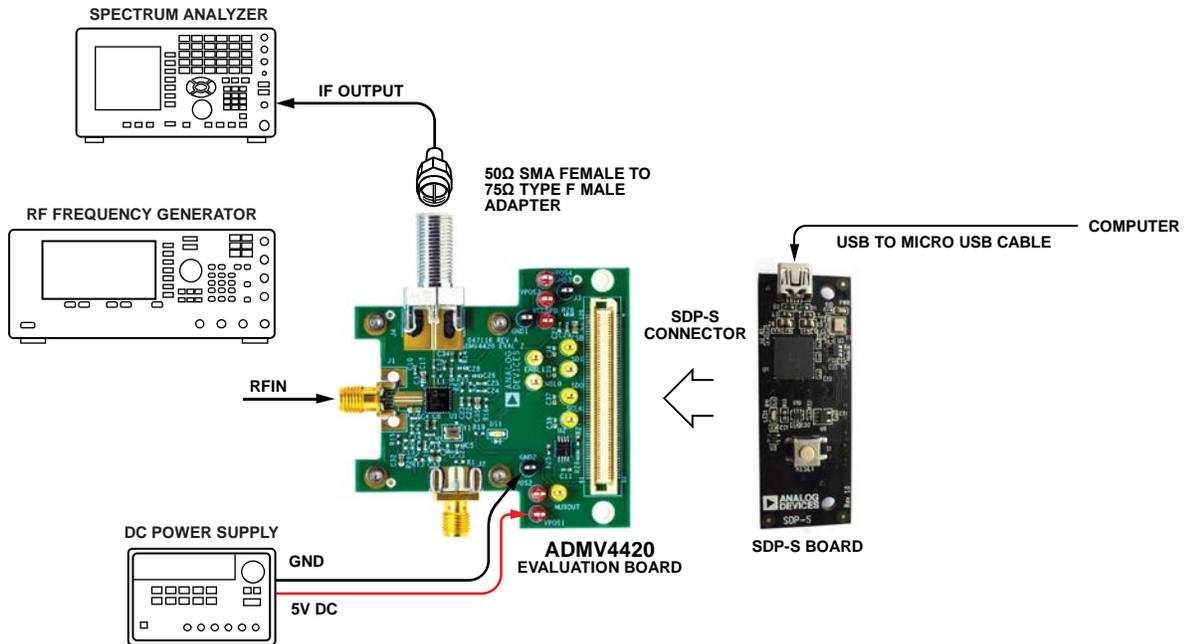


Figure 5. ADMV4420-EVALZ Lab Connections

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND ADMV4420 PLUG-INS AND DRIVERS

The ADMV4420-EVALZ software uses the Analog Devices, Inc., [Analysis, Control, Evaluation \(ACE\)](#) software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

If the ACE software has already been installed on the PC, ensure that it is the latest version as listed on www.analog.com/ACE. When installing the ACE software, ensure that during installation that the **SDP Drivers**, **LRF Drivers**, and **.Net 40 Client** driver installations are checked as well (see Figure 6).

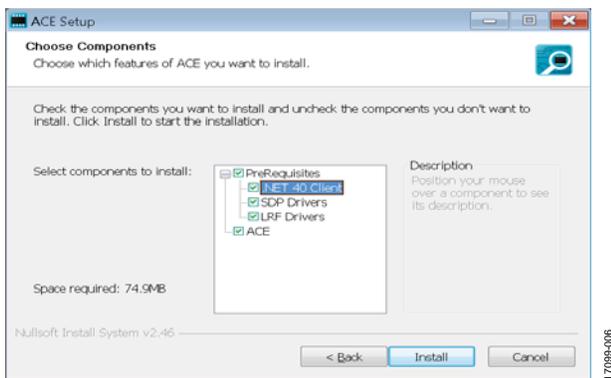


Figure 6. Drivers That Must be Installed Along with ACE

After the ACE software is installed, download the **Board.ADMV4420.acezip** file from the [ADMV4420](#) product page.

After the download is finished, double click on the **Board.ADMV4420.acezip** file and the [ADMV4420](#) is then installed on ACE.

Alternatively, on the main ACE window, click on **Tools > Manage Plug-ins > Available Plug-ins** and then search for **Board.ADMV4420**. Highlight the search result and click on the **Install Selected** button (see Figure 7).

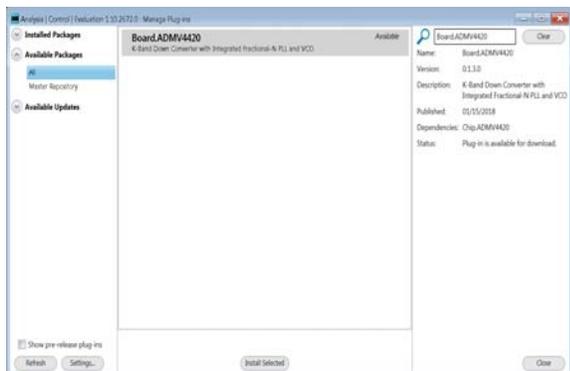


Figure 7. Installing the ADMV4420 Plug-In from ACE

After the installations finish, the ADMV4420-EVALZ plug-in appears when the ACE software opens (see Figure 8).

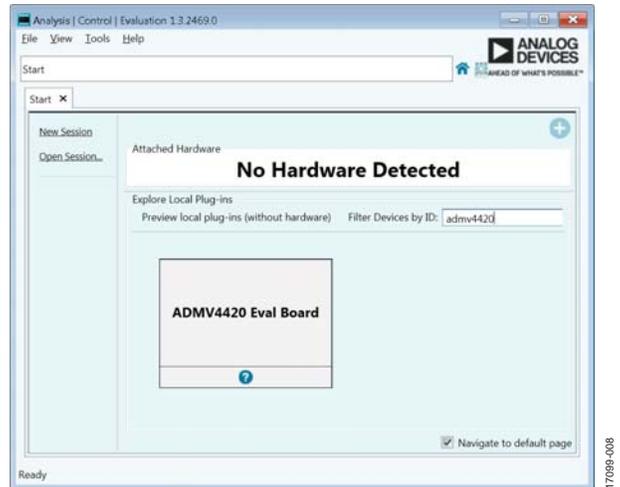


Figure 8. ADMV4420-EVALZ Plug-In Window after the ACE Software Opens

INITIAL SETUP

To set up the ADMV4420-EVALZ, take the following steps:

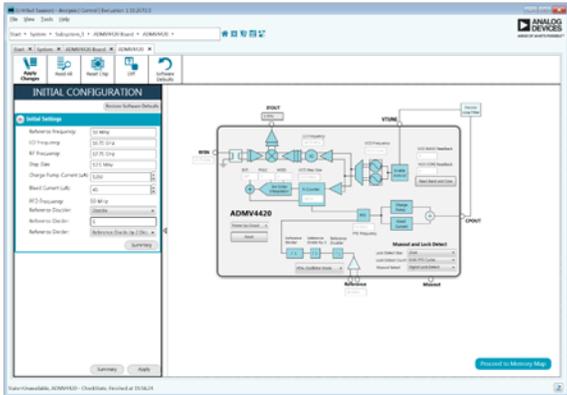
1. Connect a USB cable to the PC and then to the USB connector of the system development platform (SDP-S) controller board. Connect the SDP-S board to the ADMV4420-EVALZ through the on-board SDP-S connector on the ADMV4420-EVALZ.
2. Power up the ADMV4420-EVALZ with a 5 V dc supply. When the USB cable is connected to the PC, the green LED lights up. The PC recognizes the ADMV4420-EVALZ/SDP-S connector.
3. Open the ACE software. The ADMV4420-EVALZ appears in the **Attached Hardware** section (see Figure 9). Double-click on the evaluation board plug-in. If the device is turned off and turned back on, or if the USB cable is unplugged and plugged back in again, while the ACE software is open, the user may lose contact with the ADMV4420-EVALZ. If this happens, click **System**, the USB symbol on the [ADMV4420](#) subsystem, and **Acquire** to talk to the ADMV4420-EVALZ again. In some cases, this may not work, and the ACE session must be closed by clicking on **File < Close Session**.



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Figure 9. Attached Hardware Section When the ADMV4420-EVALZ Connects

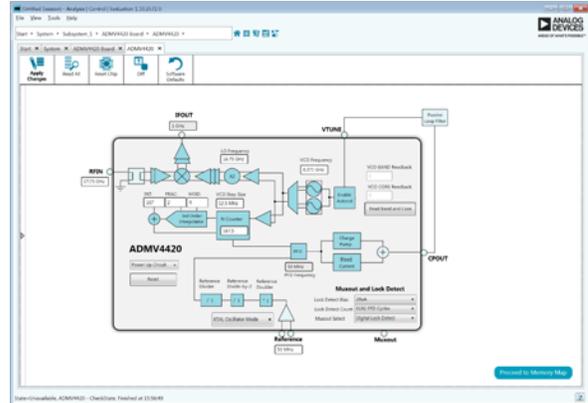
4. The **ADMV4420 Block Diagram** then opens with the **INITIAL CONFIGURATION Initial Settings** menu (see Figure 10).



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Figure 10. ADMV4420-EVALZ with INITIAL CONFIGURATION

5. On the left side of the screen, go to the **INITIAL CONFIGURATION** menu and enter the **Initial Settings**. If nothing is entered, the default settings that appear on the menu are applied to the device and are used for calculations. After entering the **Initial Settings**, click **Apply** at the bottom of the menu. The initial settings must be applied to use the main block diagram.
6. Use the [ADMV4420](#) page with the block diagram in the **ACE** software to interact with the **ADMV4420** device (see Figure 11).



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Figure 11. ADMV4420 Block Diagram in the ACE Software

ADMV4420 BLOCK DIAGRAM AND FUNCTIONS

The ADMV4420 ACE plug-in is conveniently organized to appear similar to the block diagram shown in the ADMV4420 data sheet. In this way, it is easy to correlate the functions on the ADMV4420-EVALZ with the descriptions in the ADMV4420 data sheet. A full description of the settings of each block and its corresponding registers is given in the ADMV4420 data sheet. Some of the blocks and their functions are described as

they pertain to the ADMV4420-EVALZ. The block diagrams with labels are shown in Figure 13 through Figure 16. Table 1 describes the functionality of all the blocks.

Due to ongoing improvements and enhancements to the software, some of the screen images in this user guide may not be the latest versions found in the software.

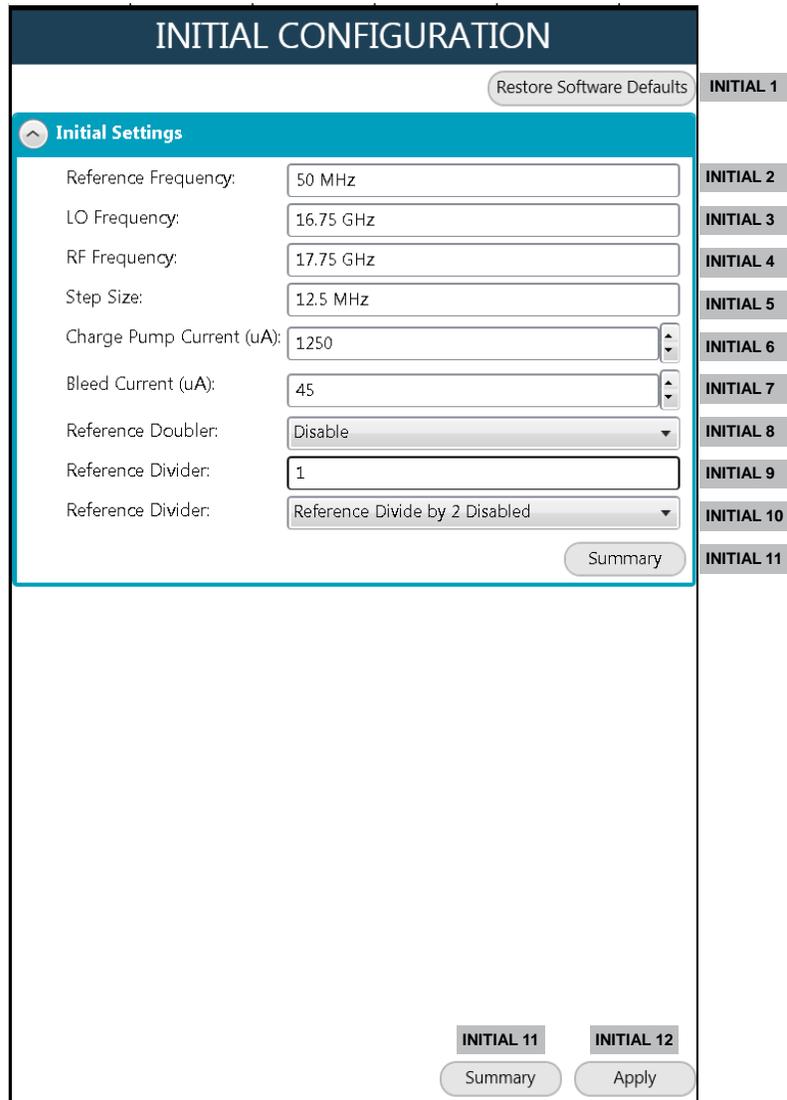


Figure 12. ADMV4420 INITIAL CONFIGURATION Menu with Labels

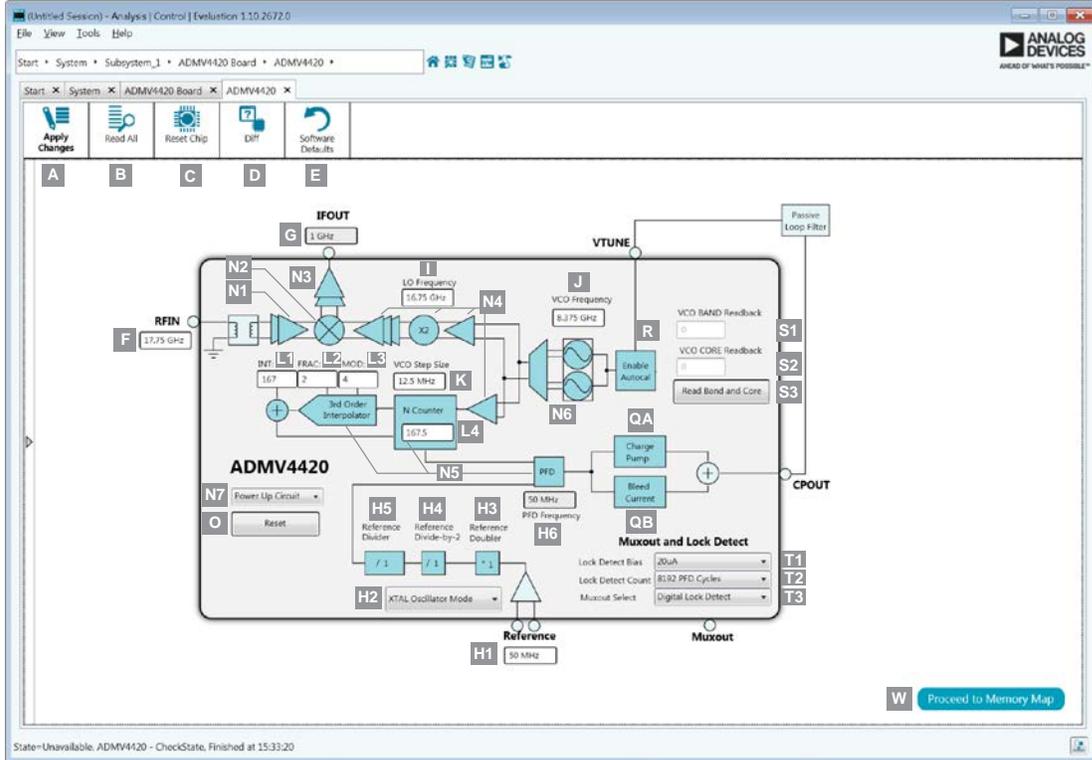


Figure 13. ADMV4420 Main Block Diagram with Labels

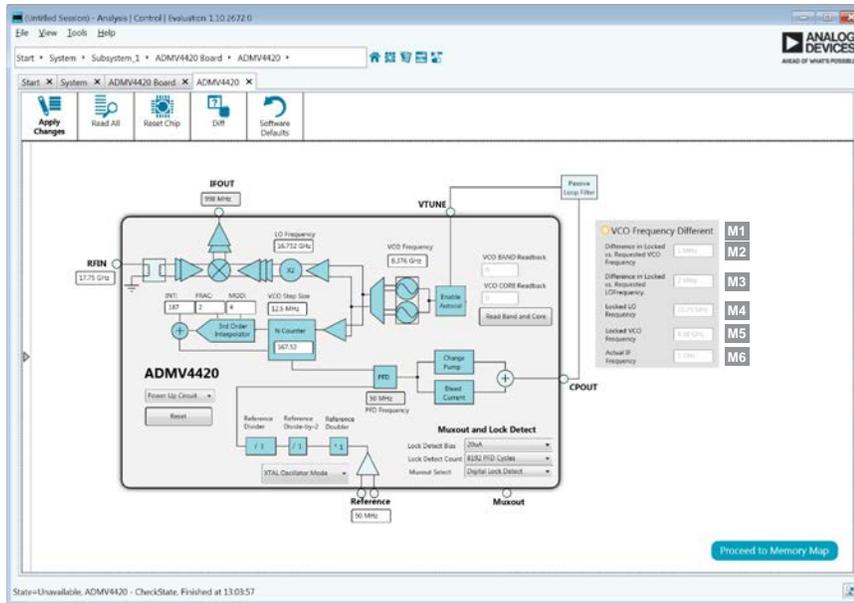


Figure 14. ADMV4420 Block Diagram Labels for VCO Locked Frequency vs. Requested Frequency Difference

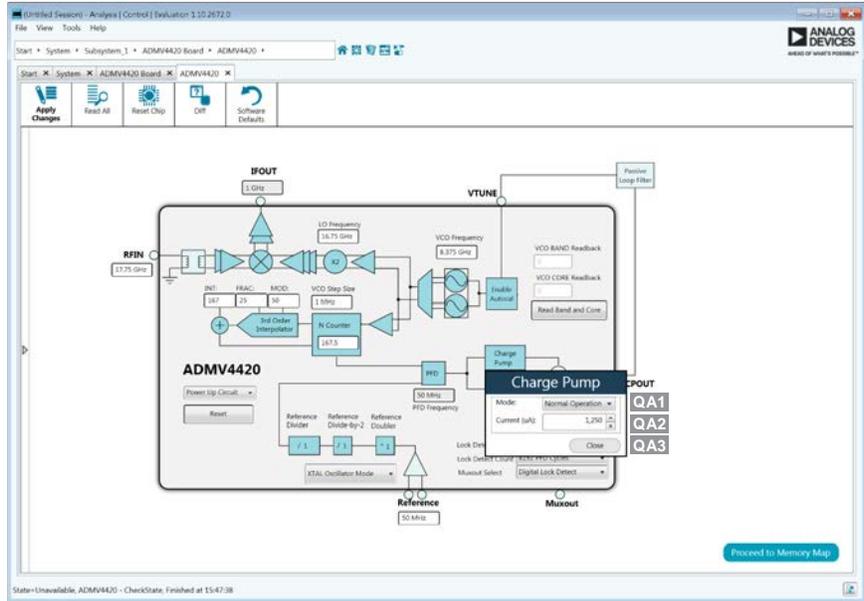


Figure 15. ADMV4420 Block Diagram Labels for Charge Pump

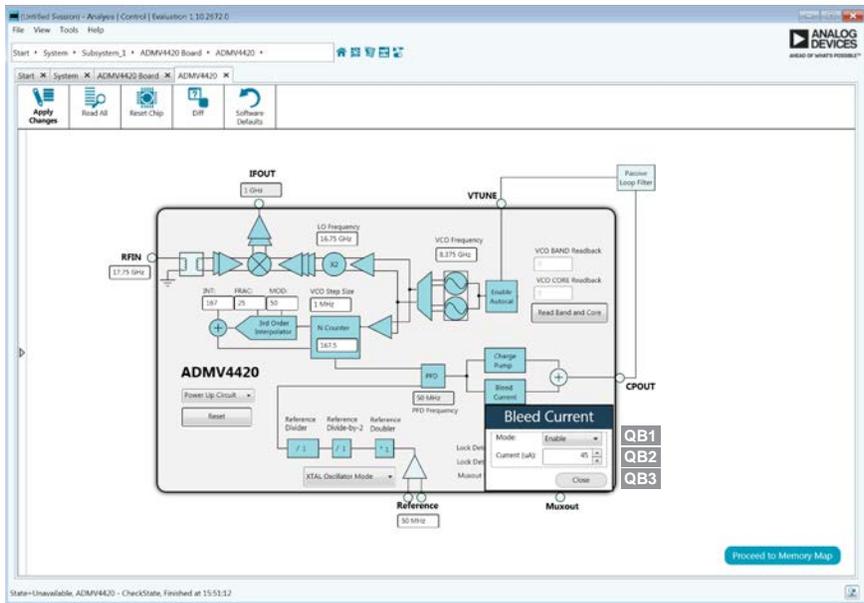


Figure 16. ADMV4420 Block Diagram Labels for Charge Pump Bleed Current

Table 1. ADMV4420 Block Diagram Label Functions (See Figure 12 and Figure 13 Unless Indicated Otherwise)

Label	Function
Initial Configuration Labels	See Figure 12.
Initial 1	Click on Restore Software Defaults to restore the software default values for the initial block labels.
Initial 2	Enter the Reference Frequency here. This value updates the Reference (Label H1) after the Apply button (Label Initial 12) is clicked.
Initial 3	Enter the LO Frequency here. This value updates the LO Frequency (Label I) after the Apply button (Label Initial 12) is clicked.
Initial 4	Enter the RF Frequency here. This value updates the RFIN (Label F) frequency after the Apply button (Label Initial 12) is clicked.
Initial 5	Enter the Step Size here. This value updates the VCO Step Size (Label K) after the Apply button (Label Initial 12) is clicked.

Label	Function
Initial 6	Enter or scroll to the Charge Pump Current here. This value updates the Charge Pump Current (Label QA2), seen in Figure 15, after the Apply button (Label Initial 12) is clicked.
Initial 7	Enter the Bleed Current here. This value updates the Bleed Current (Label QB2), as seen in Figure 16, after the Apply button (Label Initial 12) is clicked.
Initial 8	Click on the Reference Doubler dropdown menu and select whether the doubler is enabled or disabled here. This value updates the Reference Doubler (Label H3) after the Apply button (Label Initial 12) is clicked.
Initial 9	Enter the Reference Divider value here. This value updates the Reference Divider (Label H5) after the Apply button (Label Initial 12) is clicked.
Initial 10	Click on the Reference Divider dropdown menu and select whether the reference divide by 2 is enabled or disabled. This value updates the Reference Divide-by-2 (Label H4) after the Apply button (Label Initial 12) is clicked.
Initial 11	Click on the Summary button to get a list of all the values in the INITIAL CONFIGURATION labels.
Initial 12	Click on the Apply button to input all the initial configuration values to the main block diagram. The main block diagram does not function until the Apply button is clicked.
A	To apply all of the register values to the device, click Apply Changes (Label A). If auto apply is highlighted in the ADMV4420 Board tab, the Apply Changes feature (Label A) and the Read All feature (Label B) continuously run every few seconds, and the Apply Changes (Label A) and Read All (Label B) buttons do not have to be clicked to apply or read back the block diagram settings.
B	To read back all of the serial port interface (SPI) registers of the device, click Read All (Label B). If auto apply is highlighted in the ADMV4420 Board tab, the Apply Changes feature (Label A) and the Read All feature (Label B) continuously run every few seconds, and the Apply Changes (Label A) and Read All (Label B) buttons do not have to be clicked to apply or read back the block diagram settings.
C	Click Reset Chip (Label C) to enable the soft reset bit field in the ADI_SPI_CONFIG_1 register (Register 0x000).
D	Click Diff (Label D) to show registers that are different on the device.
E	Click Software Defaults (Label E) to load the software defaults on to the device, and then click Apply Changes (Label A).
F	Enter the RFIN (Label F) frequency here.
G	The absolute difference between the RFIN (Label F) frequency and the LO Frequency (Label I) is displayed here in the IFOUT frequency label. The IF frequency equation is as follows: $IF\ Frequency = RF\ Input\ Frequency - LO\ Frequency $
H1 to H6	Input reference block.
H1	Enter the reference frequency in the Reference text box and then click Apply Changes (Label A).
H2	Click on the reference type dropdown box to choose the reference type and then click Apply Changes (Label A). The reference type updates the reference register, Register 0x20E, Bit 1, which corresponds to the REF_IN_MODE bit. When REF_IN_MODE is 0, the on-board crystal oscillator is chosen. When REF_IN_MODE is 1, the external reference single-ended mode is chosen. For single-ended operation, populate C21 with R1 and C6 and remove C5 and Y1. See the Bill of Materials section for more information.
H3	Click on the Reference Doubler box and a dropdown menu appears with choices whether to enable the reference doubler or disable the reference doubler. Then, click Apply Changes (Label A). The Reference Doubler updates the reference register, Register 0x20E, Bit 2, which corresponds to the EN_REF_X2 bit. When the reference doubler is enabled, EN_REF_X2 is 1 and vice versa.
H4	Click on the Reference Divide-by-2 box and a dropdown menu appears with choices whether to enable the reference divide by 2 or disable the reference divide by 2. Then, click Apply Changes (Label A). The reference divide by 2 updates the reference register, Register 0x20E, Bit 0, which corresponds to the RDIV2_SEL bit. When the reference divide by 2 is enabled, RDIV2_SEL is 1 and vice versa.
H5	Click on the Reference Divider box and enter the reference divider value, then click Apply Changes (Label A). The reference divider updates the R_DIV_L register (Bits[7:0]) and the R_DIV_H register (Bits[1:0]), which correspond to the R_DIV bits. The R_DIV bits are 10 bits wide, and the reference divider ranges from 1 to 1023.
H6	The PFD Frequency is displayed here. The PFD frequency is calculated based on the following formula: $PFD\ Frequency = Reference\ Frequency \times \frac{Reference\ Doubler}{(Reference\ Divide\ by\ 2 \times Reference\ Divider)}$
I	Enter the LO Frequency on this label and then click Apply Changes (Label A). The LO frequency is twice the VCO Frequency (Label J) based on the following equation: $LO\ Frequency = VCO\ Frequency \times 2$

Label	Function
J	<p>Enter the VCO Frequency on this label and then click Apply Changes (Label A). The VCO frequency is half the LO Frequency (Label I), as seen in the following equation:</p> $VCO\ Frequency = LO\ Frequency \times \frac{1}{2}$ <p>The VCO frequency is also related to the PFD Frequency (Label H6) and the N Counter (Label L4) by the following equation:</p> $VCO\ Frequency = PFD\ Frequency \times N\ Counter$
K	<p>Enter the VCO Step Size on this label and then click Apply Changes (Label A). The step size determines the nearest resolution to which the VCO Frequency (Label J), and therefore the LO Frequency (Label I), locks to. The step size is related to the PFD Frequency (Label H6), MOD (Label L3) and the greatest common denominator (GCD) function by the following equation:</p> $MOD = \frac{PFD\ Frequency}{GCD(PFD\ Frequency, Step\ Size)}$
L1 to L4	<p>INT, FRAC, MOD, and N counter labels.</p>
L1	<p>Enter the INT value on this label and then click Apply Changes (Label A). The INT value updates the 16-bit INT bit field, which is on Register INT_L, Bits[7:0] (Register 0x200) and Register INT_H, Bits[15:8] (Register 0x201). The INT value is automatically updated when the VCO Frequency (Label J), LO Frequency (Label I), or N Counter (Label L4) is changed.</p>
L2	<p>Enter the FRAC value on this label and then click Apply Changes (Label A). The FRAC value updates the 24-bit FRAC bit field, which is on Register FRAC_L, Bits[7:0] (Register 0x202), Register FRAC_M, Bits[15:8] (Register 0x203), and Register FRAC_H, Bits[23:16] (Register 0x204). The FRAC value is automatically updated when the VCO Frequency (Label J), LO Frequency (Label I), VCO Step Size (Label K), or N Counter (Label L4) is changed.</p>
L3	<p>Enter the MOD value on this label and then click Apply Changes (Label A). The MOD value updates the 24-bit MOD bit field, which is on Register MOD_L, Bits[7:0] (Register 0x208), Register MOD_M, Bits[15:8] (Register 0x209), and Register MOD_H, Bits[23:16] (Register 0x20A). The MOD value is automatically updated when the VCO Step Size (Label K) is changed.</p>
L4	<p>Enter the N Counter value on this label and then click Apply Changes (Label A). The N counter value updates the INT (Label L3), FRAC (Label L2), MOD (Label L3), LO Frequency (Label I), and VCO Frequency (Label J).</p> <p>The N counter is related to the VCO Frequency (Label J) and PFD Frequency (Label H6) by the following equation:</p> $N\ Counter = \frac{VCO\ Frequency}{PFD\ Frequency}$ <p>The N counter is related to the INT (Label L1), FRAC (Label L2), and MOD (Label L3) by the following equation:</p> $N\ Counter = INT + \frac{FRAC}{MOD}$ <p>The INT (Label L1) value is calculated from the N counter value using the following equation:</p> $INT = \text{FLOOR}(N\ Counter)$ <p>The FRAC (Label L2) value is calculated from the N counter, INT (Label L1), and MOD (Label L3) value using the following equation:</p> $FRAC = N\ Counter - INT \times MOD$ <p>The MOD (Label L3) value is calculated using the equation in Label K.</p>
M1 to M6	<p>VCO frequency different block. The VCO frequency different block appears on the right of the main block diagram if the requested VCO Frequency (Label J) is different from the actual VCO frequency on the device. This usually happens when the VCO Step Size (Label K) value is not small enough to lock to the desired VCO Frequency (Label J). See Figure 14.</p>
M1	<p>VCO Frequency Different indicator. When the VCO Frequency Different indicator is on, the requested VCO Frequency (Label J) is different from the actual VCO frequency on the device.</p>
M2	<p>The Difference in Locked vs. Requested VCO Frequency shows the difference between the requested VCO Frequency (Label J) and the actual VCO frequency on the device. The Difference in Locked vs. Requested VCO Frequency is calculated using the following equation:</p> $= \left \left(\left(\left(INT\ (Label\ L1) + \frac{FRAC\ (Label\ L2)}{MOD\ (Label\ L3)} \right) \times PFD\ Frequency\ (Label\ H6) \right) - (N\ Counter\ (Label\ L4) \times PFD\ Frequency\ (Label\ H6)) \right) \right $

Label	Function
M3	The Difference in Locked vs. Requested LO Frequency shows the difference between the requested LO Frequency (Label J) and the actual LO frequency on the device. The Difference in Locked vs. Requested LO Frequency is calculated using the following equation: <i>Difference in Locked vs. Requested LO Frequency = 2 × Difference in Locked vs. Requested VCO Frequency (Label M2)</i>
M4	The Locked LO Frequency label shows the actual LO frequency on the device. The Locked LO Frequency is calculated using the following equation: <i>Locked LO Frequency = 2 × Locked VCO Frequency (Label M5)</i>
M5	The Locked VCO Frequency label shows the actual VCO frequency on the device. The Locked VCO Frequency is calculated using the following equation: $\text{Locked VCO Frequency} = \left \left(\text{INT}(\text{Label L1}) + \frac{\text{FRAC}(\text{Label L2})}{\text{MOD}(\text{Label L3})} \right) \times \text{PFD Frequency}(\text{Label H6}) \right $
M6	The Actual IF Frequency out label shows the actual IF frequency on the device as opposed to the IF Frequency (Label G) based on the requested RFIN (Label F) frequency and LO Frequency (Label I). The actual IF frequency out is calculated using the following equation: <i>Actual IF Frequency Out = RF Frequency (Label F) – Locked VCO Frequency (Label M5) </i>
N1 to N7	Enable blocks.
N1	Click LNA Enable Block and click Apply Changes (Label A) to set the EN_LNA bit (Bit 0) in the enables register (Register 0x0103).
N2	Click Mixer Enable Block and click Apply Changes (Label A) to set the EN_MIXER bit (Bit 1) in the enables register (Register 0x0103).
N3	Click IF AMP Enable Block and click Apply Changes (Label A) to set the EN_IFAMP bit (Bit 2) in enables register (Register 0x0103).
N4	Click LO Enable Block and click Apply Changes (Label A) to set the EN_LO bit (Bit 5) in enables register (Register 0x0103).
N5	Click PLL Enable Block and click Apply Changes (Label A) to set the EN_PLL bit (Bit 6) in the enables register (Register 0x0103).
N6	Click VCO Enable Block and click Apply Changes (Label A) to set the EN_VCO bit (Bit 3) in the enables register (Register 0x0103).
N7	Click on the Power Up Circuit dropdown menu and click Apply Changes (Label A) to set or unset N1 to N6 altogether.
O	Click on the Reset button to reset the circuit. This button does a similar function to the Reset Chip (Label C) button.
QA, QA1 to QA3, QB, and QB1 to QB3	Charge pump and charge pump bleed blocks. See Figure 15 and Figure 16.
QA	Click on the Charge Pump block to configure the charge pump current and charge pump mode on the device. The Charge Pump block diagram appears as shown in Figure 15.
QA1	Click on the Charge Pump Mode dropdown menu and choose which mode the charge pump operates and click Apply Changes (Label A). If open loop operation is required, choose Charge Pump Hi-z Operation . For general use, keep the charge pump mode on normal use. The charge pump mode sets the CP_STATE bits (Bits[1:0]) in the CP_STATE register (Register 0x22C).
QA2	Use the scroll button or type in the required Charge Pump Current in microamps. The charge pump current sets the CP_CURRENT bits (Bits[3:0]) in the CP_CURRENT register (Register 0x22E). The charge pump current varies from 312.5 μA to 5000 μA in steps of 312.5 μA.
QA3	Click on the Charge Pump Block Diagram Close button to exit the charge pump block.
QB	Click on the Charge Pump Bleed block to configure the charge pump bleed current and charge pump bleed mode on the device. The Charge Pump Bleed block diagram appears as shown in Figure 16.
QB1	Click on the Charge Pump Bleed Mode dropdown menu and choose which mode the charge pump bleed operates and click Apply Changes (Label A). The charge pump bleed mode sets the EN_BLEED bit (Bit 0) in the CP_BLEED_EN register (Register 0x22D).
QB2	Use the scroll button or type in the required Charge Pump Bleed Current in microamps. The charge pump bleed current sets the BICP bits (Bits[7:0]) in the CP_BLEED register (Register 0x22F). The charge pump bleed current varies from 0 μA to 956.25 μA in steps of 3.75 μA.
QB3	Click on the Charge Pump Bleed Block Diagram Close button to exit the charge pump bleed block.
R	Click Enable Autocal block and click Apply Changes (Label A) to set the EN_AUTOCAL bit (Bit 1) in the AUTOCAL register (Register 0x226).

Label	Function
S1 to S3	Read VCO band and core sequence and label.
S1	The VCO BAND Readback label displays the VCO band when the Read Band and Core (Label S3) button is pressed. This label only updates when S3 is pressed.
S2	The VCO CORE Readback label displays the VCO core when the Read Band and Core (Label S3) button is pressed. This label only updates when S3 is pressed.
S3	Click the Read Band and Core button to update S1 and S2. The VCO Band and Core Readback Sequence section describes how the values for S1 and S2 are obtained.
T1 to T3	MUXOUT and lock detect settings.
T1	Click on the Lock Detect Bias dropdown menu to select the lock detect bias setting and then click Apply Changes (Label A).The lock detect bias sets the LD_BIAS bits (Bits[7:6]) in the LOCK_DETECT register (Register 0x214).
T2	Click on the Lock Detect Count dropdown menu to select the lock detect count setting and then click Apply Changes (Label A).The lock detect count sets the LD_COUNT bits (Bits[5:3]) in the LOCK_DETECT register (Register 0x214).
T3	Click on the Muxout Select dropdown menu to select the MUXOUT pin setting and then click Apply Changes (Label A). The MUXOUT pin sets the PLL_MUX_SEL bits (Bits[7:0]) in the PLL_MUX_SEL register (Register 0x213). The Muxout Select dropdown menu controls the functionality of the MUXOUT pin on the ADMV4420 . When the MUXOUT pin is set to digital lock detect and the PLL is locked, or if the MUXOUT pin is set to logic high, the LED DS1 turns on.
W	Click Proceed to Memory Map (Label W) to open the ADMV4420 memory map (see Figure 17).

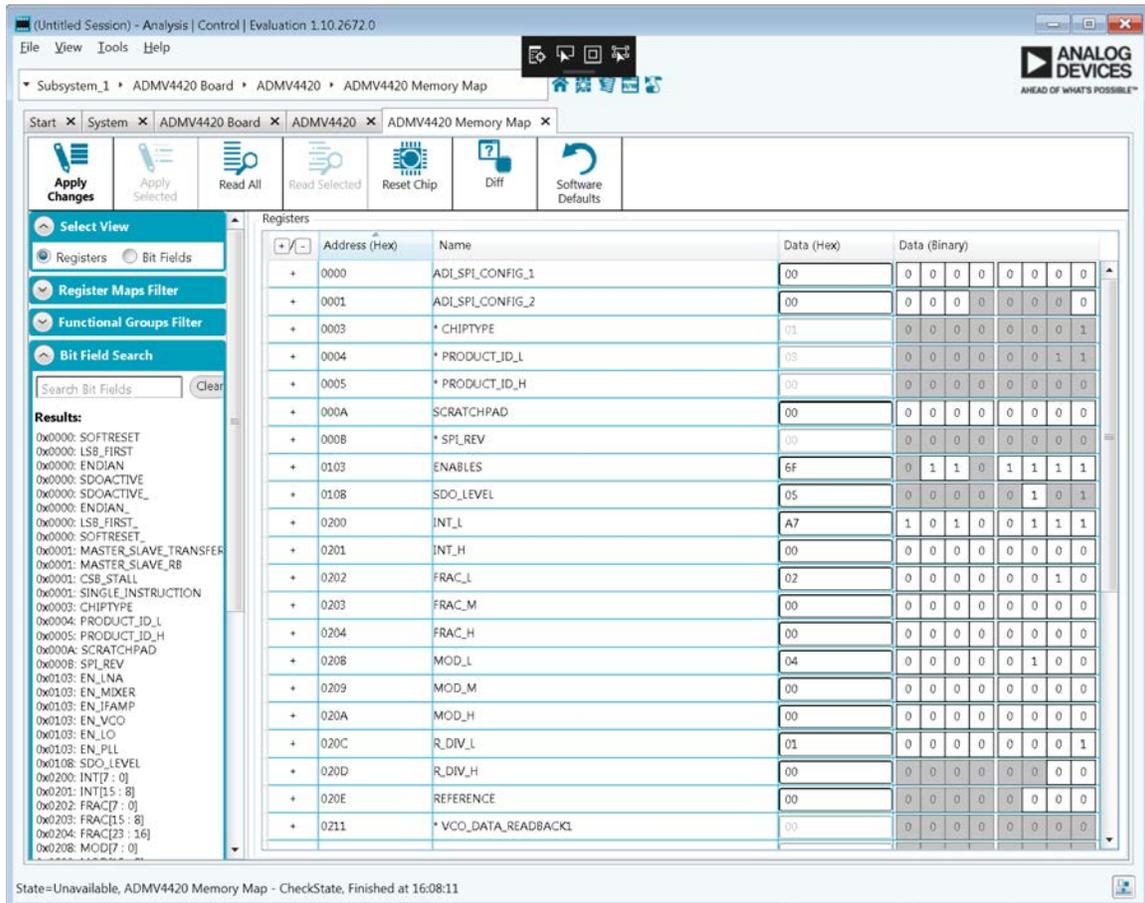


Figure 17. ADMV4420 Memory Map in the ACE Software

VCO BAND AND CORE READBACK SEQUENCE

The read band and core run the following sequence to obtain the values for the VCO core and VCO band:

1. Write 0x04 to VCO_READBACK_SEL bits (Bits[2:0]) in the VCO_READBACK_SEL register (Register 0x21F).
2. Read back Register VCO_DATA_READBACK1 (Register 0x211).
3. The first two bits (Bits[1:0]) equal the VCO core.
4. Write 0x01 to VCO_READBACK_SEL bits (Bits[2:0]) in the VCO_READBACK_SEL register (Register 0x21F).
5. Read back Register VCO_DATA_READBACK1 (Register 0x211).
6. The readback value equals the VCO band.

FREQUENCY UPDATE SEQUENCE

When the VCO frequency or charge pump must be updated, the INT register, MOD register, and FRAC register must be updated in a specific sequence. The ADMV4420 software automatically follows this sequence when the VCO frequency must be updated. When the charge pump must be updated, the CP_CURRENT register is updated before this sequence. The sequence that the ADMV4420 software uses is as follows:

1. Write to FRAC_H register (Register 0x204)
2. Write to FRAC_M register (Register 0x203)
3. Write to FRAC_L register (Register 0x202)
4. Write to MOD_H register (Register 0x20A)
5. Write to MOD_M register (Register 0x209)
6. Write to MOD_L register (Register 0x208)
7. Write to INT_H register (Register 0x201)
8. Write to INT_L register (Register 0x200)
9. Wait 16 SPI clock cycles

RESULTS

When testing the ADMV4420-EVALZ, the following are the expected results for an 18 GHz RF signal at -40 dBm, using the on-board crystal oscillator.

Figure 18 shows the ACE block diagram settings for a 17 GHz LO with an 18 GHz RF signal, and 50 MHz on-board crystal

oscillator. Figure 19 shows the corresponding results on a spectrum analyzer when the RF signal is -40 dBm. Board traces are not de-embedded.

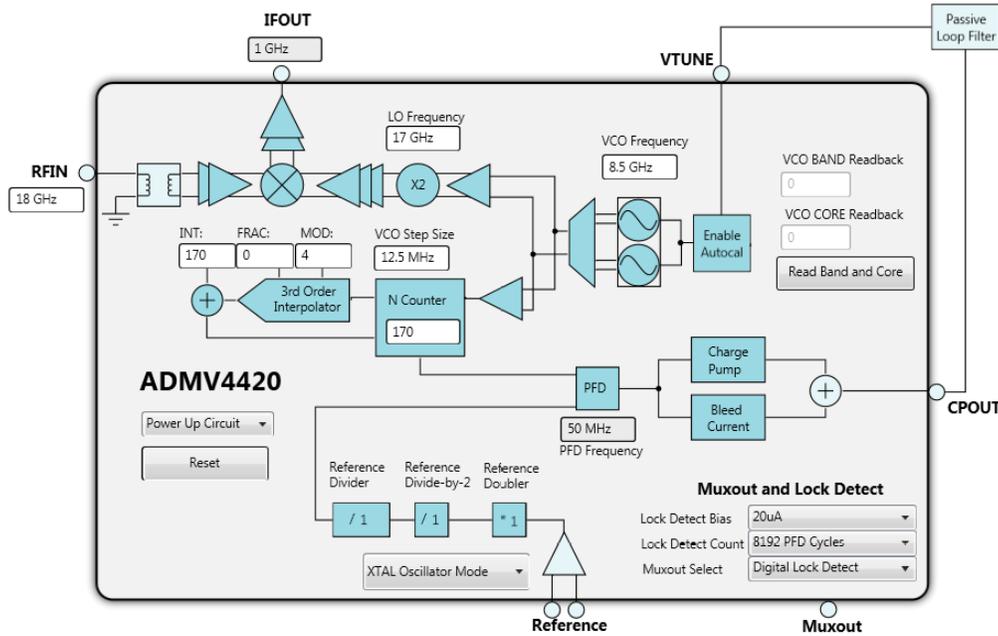


Figure 18. Block Diagram Settings for 18 GHz RF Signal, 17 GHz LO with 50 MHz On-Board Crystal Oscillator

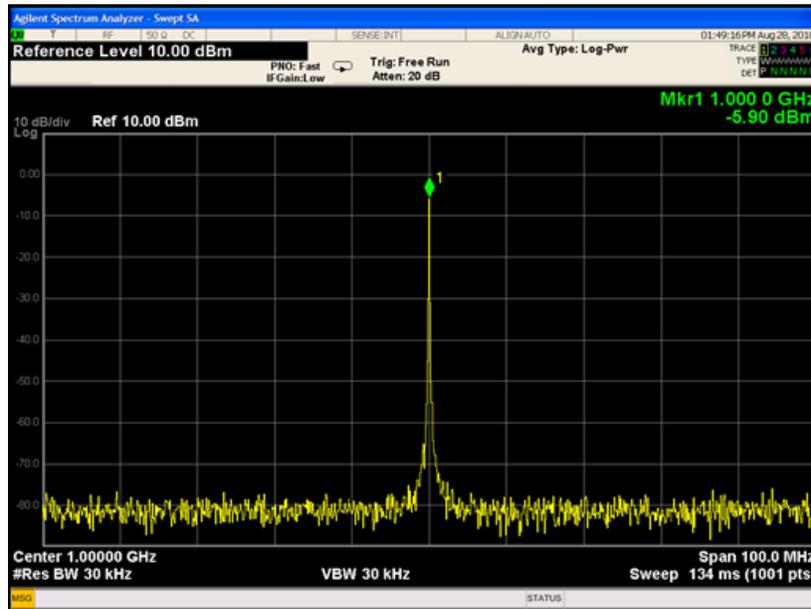


Figure 19. ADMV4420 Results with a 17 GHz LO, 18 GHz RF Signal at -40 dBm, and 50 MHz On-Board Crystal Oscillator

Figure 20 shows the ACE block diagram settings for a 20.2 GHz LO with an 18 GHz RF signal, and 50 MHz on-board crystal oscillator. Figure 21 shows the corresponding results on a

spectrum analyzer when the RF signal is -40 dBm. Board traces are not de-embedded.

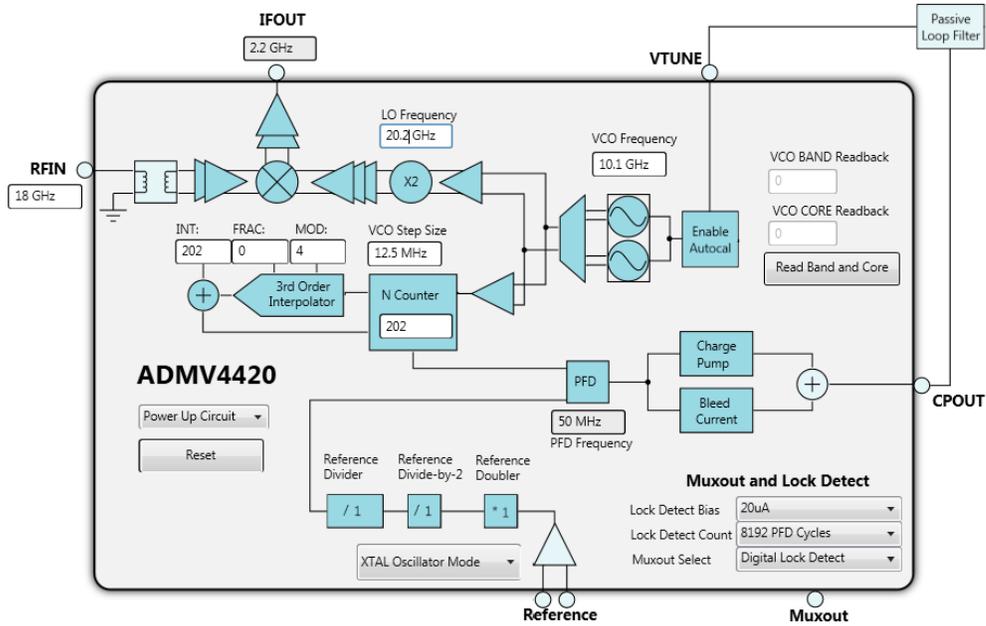


Figure 20. Block Diagram Settings for 18 GHz RF Signal, 20.2 GHz LO with 50 MHz On-Board Crystal Oscillator

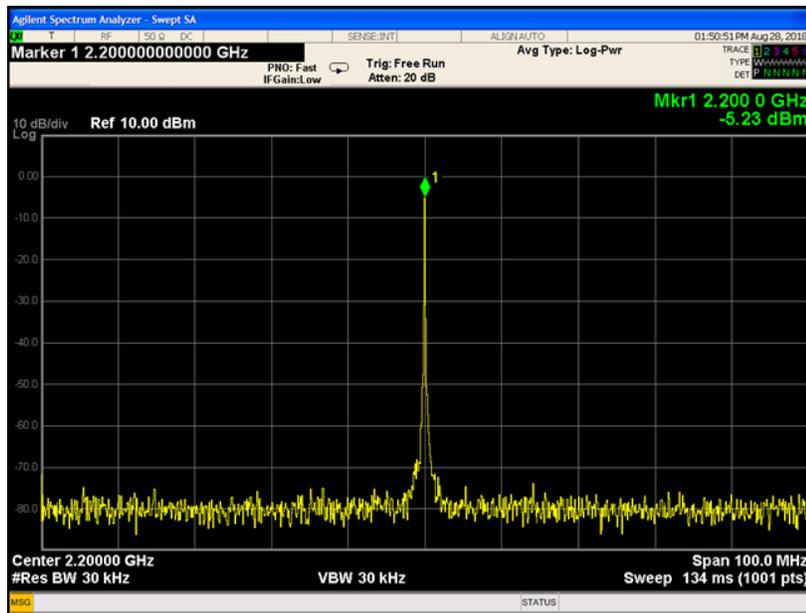


Figure 21. ADMV4420 Results with a 20.2 GHz LO, 18 GHz RF Signal at -40 dBm, and 50 MHz On-Board Crystal Oscillator

EVALUATION BOARD SCHEMATICS AND ARTWORK

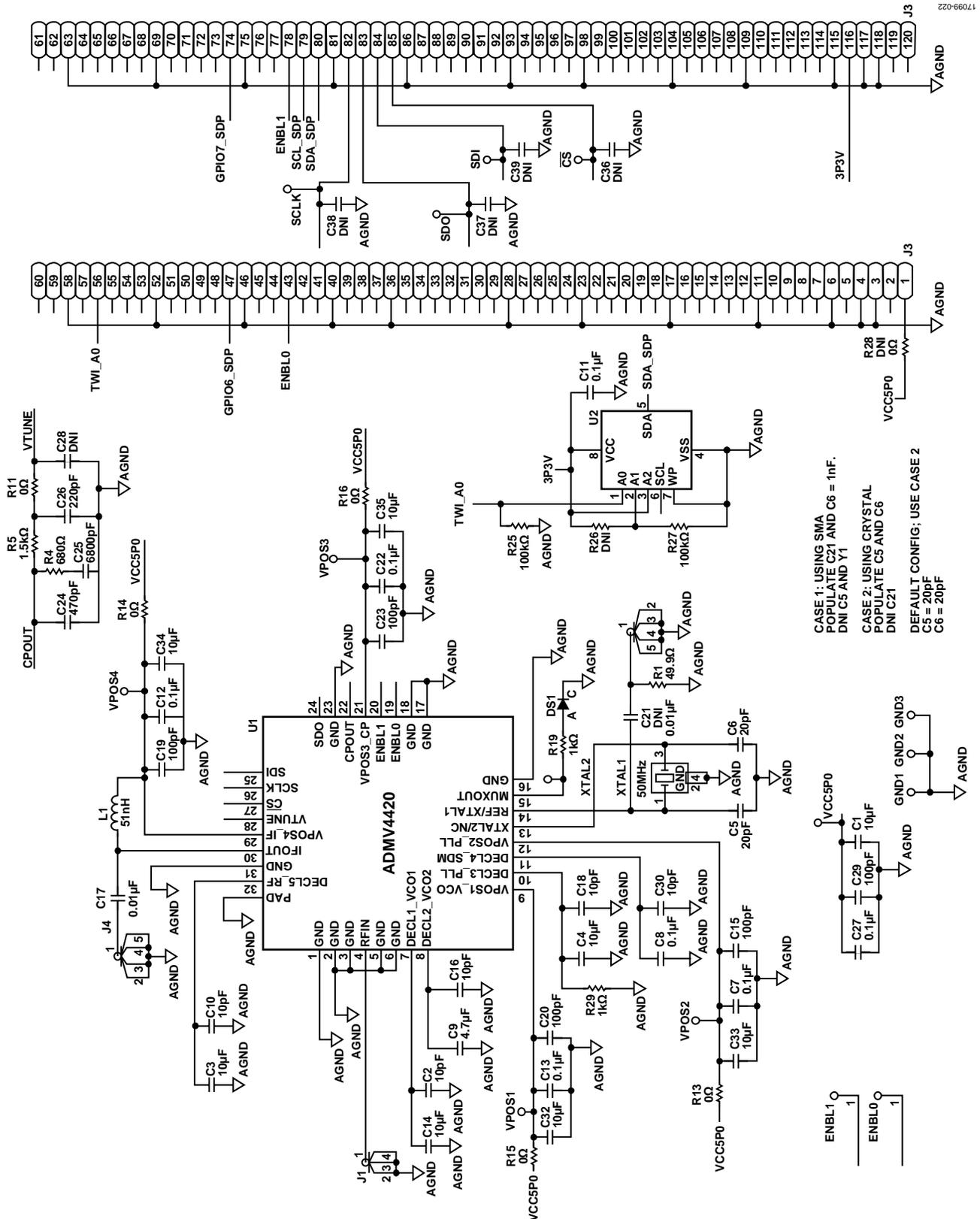


Figure 22. ADMV4420-EVALZ Schematic

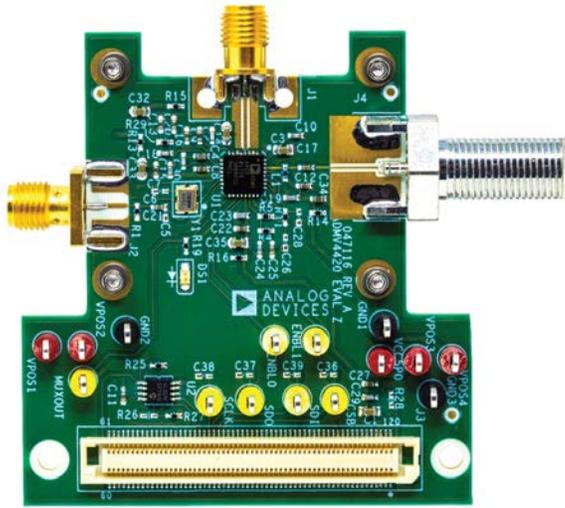


Figure 23. ADMV4420-EVALZ Top

17099-023

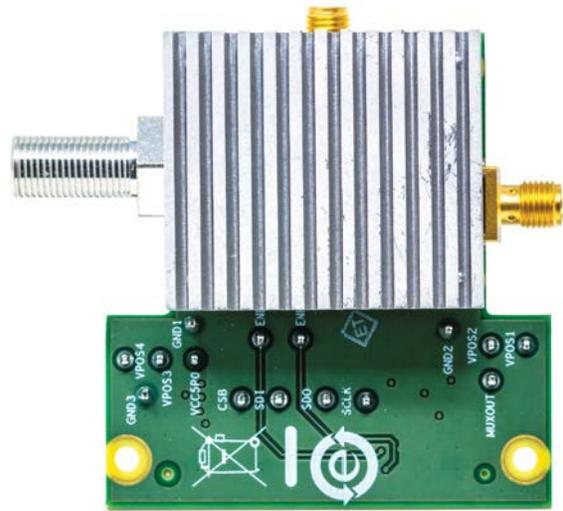


Figure 24. ADMV4420-EVALZ Bottom

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ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Configuration Options

Components	Description	Default Conditions
C1 to C4, C7 to C16, C18 to C20, C22, C23, C27, C29, C30, C32, C34, C35, R29	Power supply decoupling and low dropout (LDO) decoupling capacitors. R29 resistor is needed to aid in discharging the decoupling capacitor, C4, and Capacitor C18.	C1, C3, C14, C32, C35 = 10 μ F (Size 0603), C34, C4 = 10 μ F (Size 0402), C7, C8, C11 to C13, C22, C27 = 0.1 μ F (Size 0402), C15, C19, C20, C23, C29 = 100 pF (Size 0402), C2, C10, C16, C18, C30 = 10 pF (Size 0402), C9 = 4.7 μ F (Size 0402), R29 = 1 k Ω (Size 0402)
\overline{CS} , SDI, SDO, SCLK, ENBL0, ENBL1, MUXOUT	Test loops for SPI, enable pins, and MUXOUT.	CNLOOPTP
C17, L1, J4	IF output interface. The open collector IF output interface is biased through pull-up Choke Inductor L1. The C17 capacitor is an ac-coupling capacitor.	C17 = 0.01 μ F (Size 0402), L1 = 51 nH (Size 0402), J4 = 75 Ω connector (531-40039, AMPHENOL531-40039)
DS1	LED indicator for lock detect.	SML-210MTT86
C24, R4, R5, C25, C26, R11	Loop filter components.	C24 = 470 pF (Size 0402), R4 = 680 Ω (Size 0402), C25 = 6800 pF (Size 0402), R5 = 1.5 k Ω (Size 0402), R11 = 0 Ω (Size 0402), C26 = 220 pF (Size 0402)
VPOS1 to VPOS4, VCC5P0	VPOS test loops.	CNLOOPTP
GND1 to GND3	Test loops for ground.	CNLOOPTP
J1	RFIN connector.	Southwest Microwave 2.92 mm connector, 1092-04A-5/SRI K connector 25-146-1000-92
J2, R1, C21, C5, C6, Y1	Reference Circuits. Case 1 using SMA: populate C21, R1, and C6. Do not install (DNI) C5 and Y1. Case 2 using crystal: populate C5 and C6. DNI C21. Use Case 2 for default condition.	R1 = 49.9 Ω (Size 0402), J2 = JOHNSON142-0701-851 Case 1: C5 = DNI, C6 = 1 nF (Size 0402), Y1 = DNI, C21 = 0.01 μ F (Size 0402) Case 2: C5 = 20 pF (Size 0402), C6 = 20 pF (Size 0402), Y1 = 50 MHz crystal (NX3225SA 12 pF, YSML126W98H28), C21 = DNI
R13 to R16	Shorts.	0 Ω (Size 0402)
U2, R25, R27, C11	32-bit electronically erasable programmable read-only memory (EEPROM) circuits.	R25, R27 = 100 k Ω (Size 0402), U2 = 24LC32A-I/MS, C11 = 0.1 μ F
MTG1 to MTG4	Mounting holes for heatsinks.	Keystone Electronics CORP-5002
ADMV4420	Device under test (DUT).	Not applicable
J3	SDP-S connector.	FX8-120S-SV(21), HRSFX8-120S-SV

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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