PI6C485352

2.5V/3.3V, 500 MHz Twelve 2-to-1 Differential LVPECL Clock Multiplexer

Features

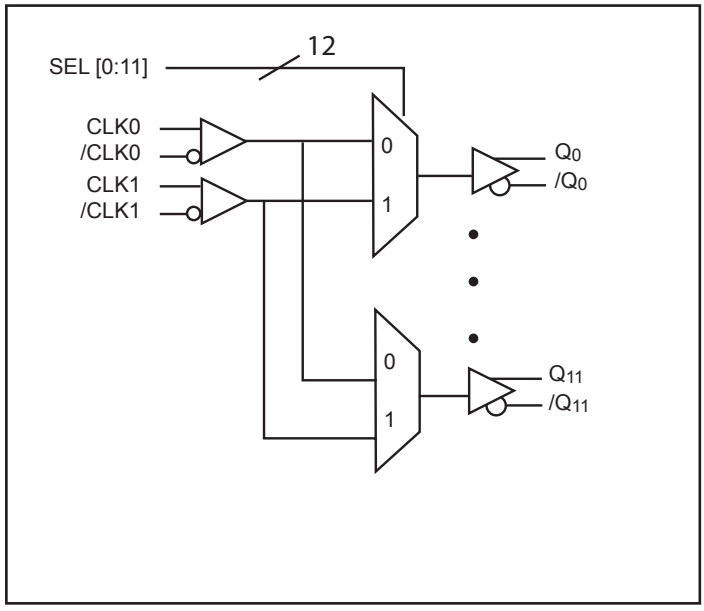
- Pin-to-pin compatible to ICS85352I
- $F_{MAX} \leq 500$ MHz
- Propagation Delay < 4ns
- Output-to-output skew < 100ps
- 12 pairs of differential LVPECL outputs
- Selectable differential CLK and /CLK inputs
- CLK, /CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- Select input accept CMOS/LVTTL levels
- 2.5V/3.3V power supply
- Operating Temperature: -40°C to +85°C
- Packaging (Pb-free & Green):
  — 48-pin TQFP (FA)

Description

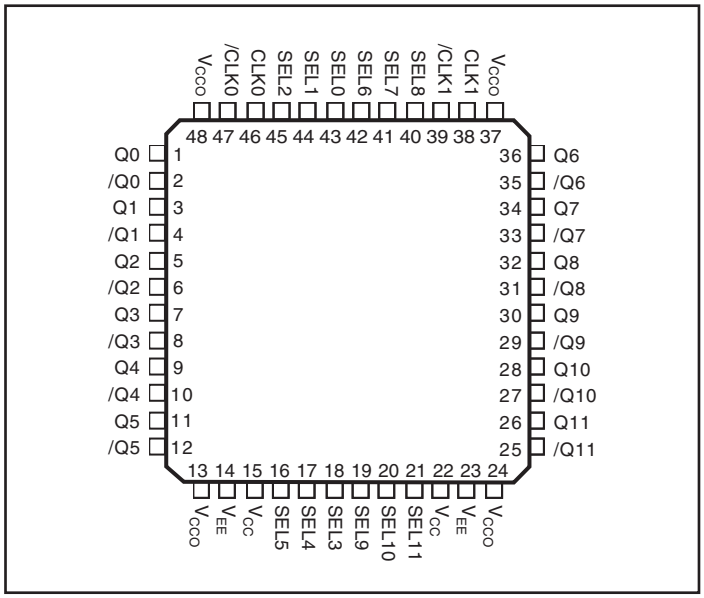
The PI6C485352 is a high-performance low-skew LVPECL fanout buffer. PI6C485352 features two selectable differential inputs and translates to twelve LVPECL output pairs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LVPECL, LVDS, LVHSTL, SSTL or HCSL signals. The PI6C485352 is ideal for differential to LVPECL translations and/or LVPECL clock distribution.

Typical clock translation and distribution applications are data-communications and telecommunications.

Block Diagram



Pin Configuration



Pin Description

Pin #	Name	Pullup/ Pulldown	Description
1, 2 3, 4 5, 6 7, 8 9, 10 11, 12 25, 26 27, 28 29, 30 31, 32 33, 34 35, 36	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 /Q11, Q11 /Q10, Q10 /Q9,Q9 /Q8,Q8 /Q7,Q7 /Q6,Q6		Differential LVPECL Output pairs. LVPECL interface levels
13, 24 37, 48	V_{CCO}		Output supply pins
14, 23	V_{EE}		Ground pins
15, 22	V_{CC}		Core supply pins
16, 17 18, 19 20, 21 40, 41 42, 43 44, 45	SEL5, SEL4, SEL3, SEL9, SEL10, SEL11, SEL8, SEL7, SEL6, SEL0, SEL1, SEL2	Pulldown	Clock select inputs. LVCMOS/LVTTL interface levels
38	CLK1	Pulldown	Non-inverting differential clock input
39	/CLK1	Pullup/ Pulldown	Inverting differential clock input.
46	CLK0	Pulldown	Non-inverting differential clock input
47	/CLK0	Pullup/ Pulldown	Inverting differential clock input.

Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{CC}+0.5V	
Outputs, I_O	Surge current				100	mA
T_{STG}	Storage temperature		-65		150	°C
θ_{jA}	Package thermal impedence				73	°C/W

Note:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance				4	pF
Rpullup	Input Pullup Resistance			50		kΩ
Rpulldown	Input Pulldown Resistance			50		kΩ

Control Input Function Table

SELx	Selected Clock Inputs
0	CLK0, /CLK0
1	CLK1, /CLK1

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
V_{CCO}	Output Power Supply Voltage		2.375		3.6	V
T_A	Ambient Temperature		-40		85	°C
I_{EE}	Power Supply Current				200	mA

LVCMOS/LVTTL DC Characteristics (T_A = -40°C to +85°C, V_{CC} = 3.3V ±10%, V_{CCO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage	SEL0:SEL11		2		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	SEL0:SEL11		-0.3		0.8	
I_{IH}	Input High Current	SEL0:SEL11	$V_{IN} = V_{CC}$ = 3.6V			150	µA
I_{IL}	Input Low Current	SEL0:SEL11	V_{IN} = 0V, V_{CC} = 3.6V	-5			µA

Differential DC Characteristics (T_A = -40°C to +85°C, V_{CC} = 3.3V ±10%, V_{CCO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{CC}$ = 3.6V			150	µA
		/CLK0, /CLK1	$V_{IN} = V_{CC}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{CC} = 3.6V, V_{IN} = 0V	-5			µA
		/CLK0, /CLK1	V_{CC} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage(1)			V_{EE}+0.5		V_{CC}-0.85V	V

Note:

1. For single ended applications, the maximum input voltage for CLK and /CLK is V_{CC}+0.3V

LVPECL DC Characteristics(1) (T_A = -40°C to +85°C, V_{CC} = 3.3V ±10%, V_{CCO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{CC}$ = 3.6V			150	µA
		/CLK0, /CLK1	$V_{IN} = V_{CC}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{CC} = 3.6V, V_{IN} = 0V	-5			µA
		/CLK0, /CLK1	V_{CC} = 3.6V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage(2)		V_{CCO} = 3.3V or 2.5V	V_{CCO}-1.4		V_{CCO}-0.9	V
V_{OL}	Output Low Voltage(2)		V_{CCO} = 3.3V or 2.5V	V_{CCO}-2.0		V_{CCO}-1.7	V

Notes:
1. For single-ended applications, the maximum input voltage for CLK and /CLK is V_{CC}+0.3V.
2. Outputs terminated with 50Ω to V_{CCO} -2.0V

AC Characteristics (T_A = -40°C to +85°C, V_{CC} = 3.3V ±10%, V_{CCO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency				500	MHz
t_{pd}	Propagation Delay(1)				4	ns
Tsk	Output-to-output Skew(2)				100	ps
Tskpp	Part-to-part Skew(3)				500	ps
t_r/t_f	Output Rise/Fall time	20% - 80%	150		700	ps
odc	Output duty cycle		45		55	%

Notes:
1. Measured from the differential input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal loads. Measured at the outputs differential crossing point.

Applications Information

Wiring the differenctial input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be placed as close as possible to the input pin. The ratio of R1 and R2 should be adjusted to postion the V_REF at the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

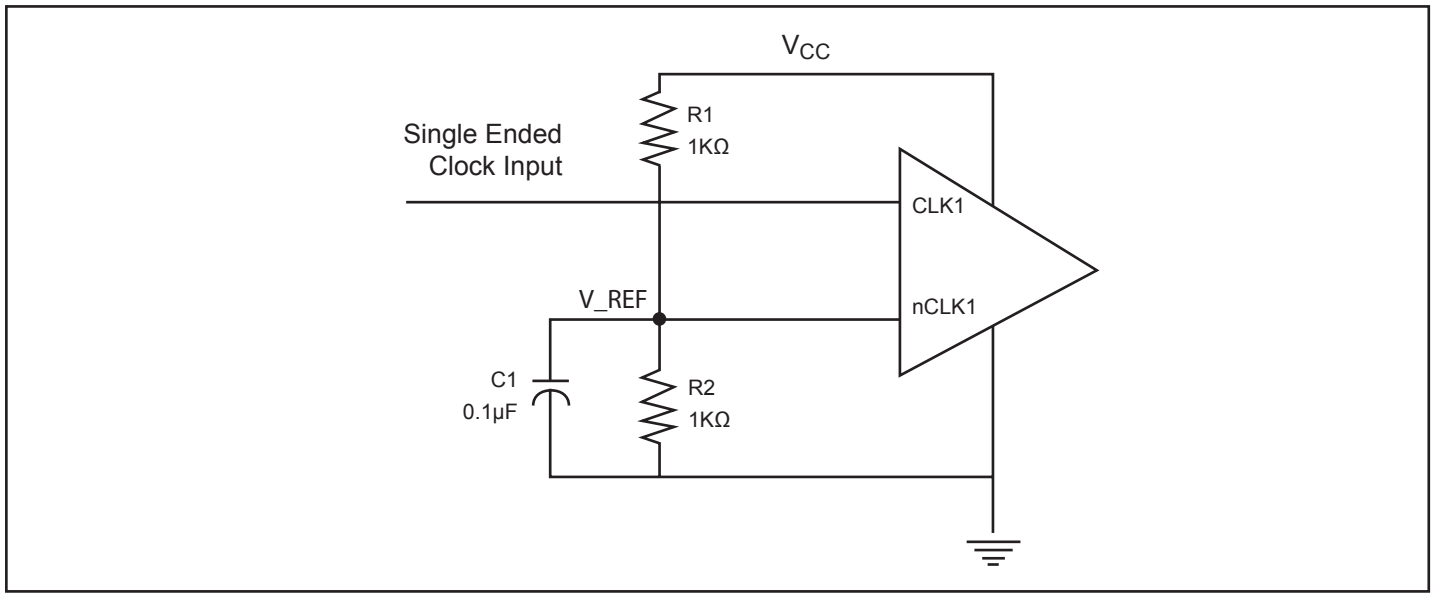
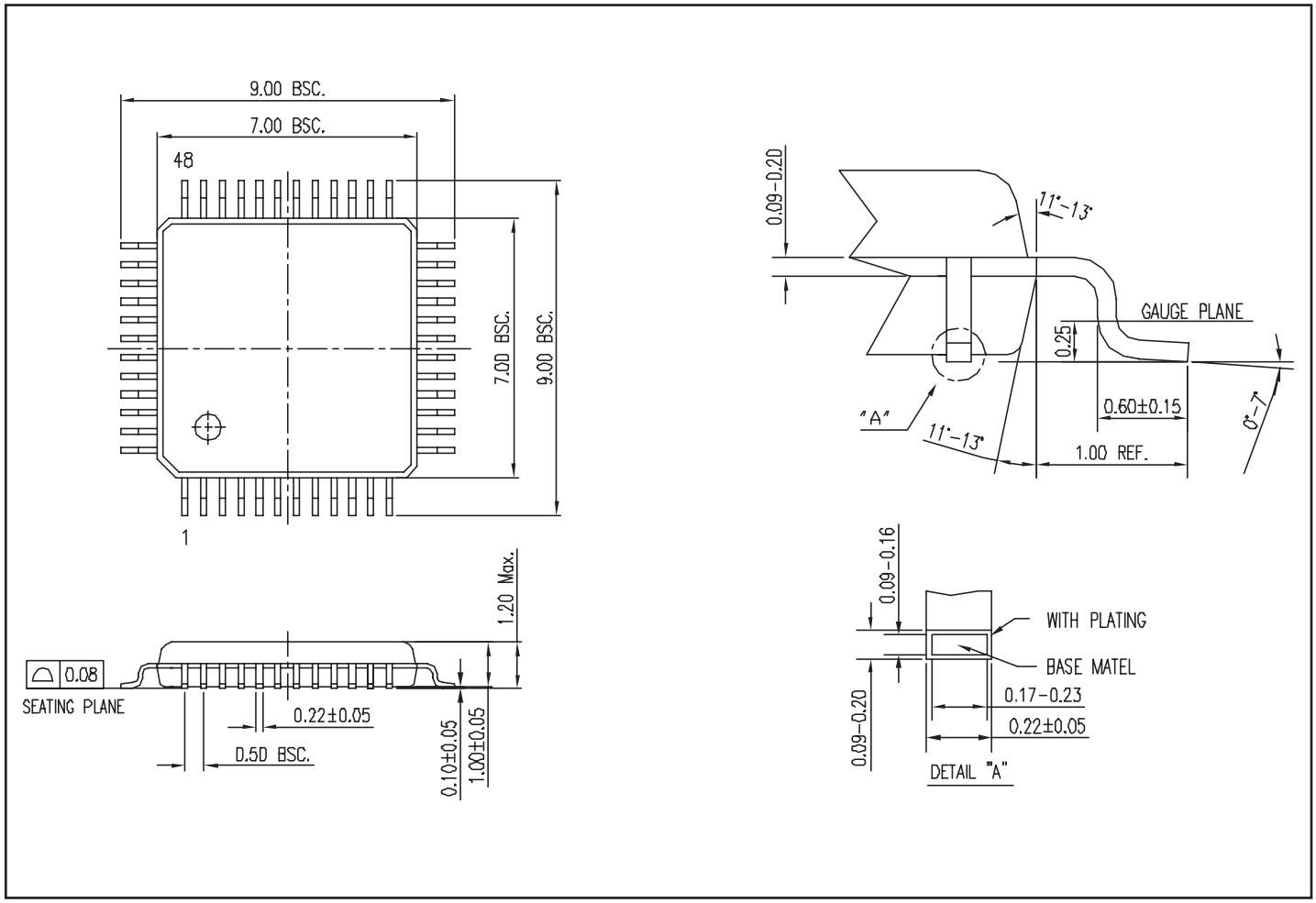


Figure 1: Single-ended Signal Driving Differential Input

Packaging Mechanical: 48-Pin TQFP (FA)



Ordering Information[1,2,3]

Ordering Code	Package Code	Package Description
PI6C485352FAE	FA	Pb-free & Green, 48-pin, 276-mil wide TQFP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X suffix = Tape/Reel