

GENERAL DESCRIPTION

The XRT83VSH28 is a fully integrated 8-channel short-haul line interface unit (LIU) that operates from a 1.8V and a 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in E1 75Ω or 120Ω mode with minimum external components. The LIU features are programmed through a standard parallel or serial microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

The on-chip clock synthesizer generates an E1 clock reference.

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, TAOS, DMO, and diagnostic loopback modes.

APPLICATIONS

- ISDN Primary Rate Interface
- CSU/DSU E1 Interface
- E1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- E1 Multiplexer and Channel Banks

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VSH28 E1 LIU (HOST MODE)

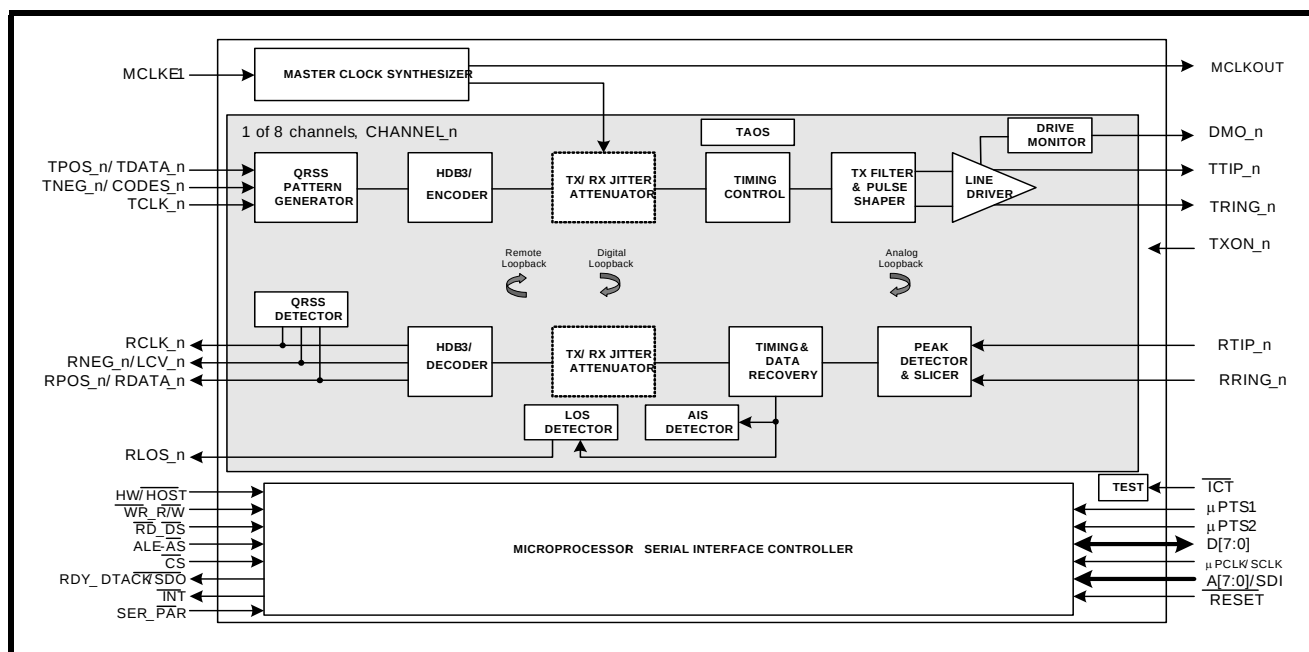
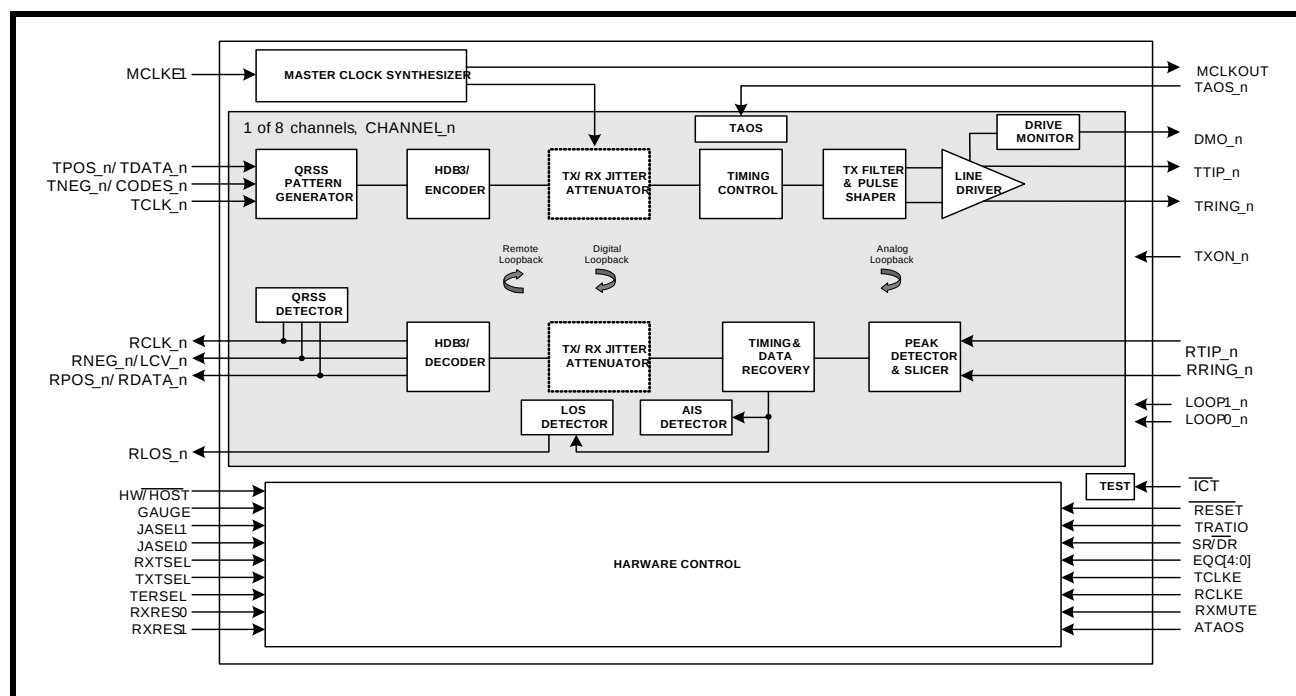


FIGURE 2. BLOCK DIAGRAM OF THE XRT83VSH28 E1 LIU (HARDWARE MODE)



**FEATURES**

- Fully integrated eight channel short-haul transceivers for E1 (2.048MHz) applications
- Internal Impedance matching on both receive and transmit for 75Ω (E1) and 120Ω (E1) applications are per port selectable through software without changing components
- Power down on a per channel basis with independent receive and transmit selection
- User programmable Arbitrary Pulse mode
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis
- Selectable Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive or transmit path
- Driver failure monitor output (DMO) alerts of possible system or external component problems
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis
- Support for automatic protection switching
- 1:1 and 1+1 protection without relays
- Receive monitor mode handles 0 to 6dB resistive attenuation (flat loss) along with 0 to 6dB cable loss
- Loss of signal (RLOS) according to ITU-T G.775/ETS300233 (E1)
- Programmable data stream muting upon RLOS detection
- On-Chip HDB3 encoder/decoder with an internal 16-bit LCV counter for each channel
- On-Chip digital clock recovery circuit for high input jitter tolerance
- QRSS/PRBS pattern generator and detection for testing and monitoring
- Error and bipolar violation insertion and detection
- Transmit all ones (TAOS) Generators and Detectors
- Supports local analog, remote, digital, and dual loopback modes
- Supports gapped clocks for mapper/multiplexer applications
- 1.8V Inner Core
- 3.3V I/O Supply Operation
- 225 ball BGA package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VSH28IB	225 Ball BGA	-40°C to +85°C

A	DGND	RNEG_0	TCLK_1	TPOS_1	TAOS_2	RDY	ALE	Reserved	DVDD3v3	A[1]	A[3]	A[7]	TXON_0	JASEL0	TCLK_2	RLOS_3	RCLK_3	DVDD3v3
B	TDO	RPOS_0	RCLK_0	TCLK_0	TNEG_1	TAOS_1	CS	Reserved	DGND	A[2]	A[6]	TXON_3	JASEL1	TPOS_2	TNEG_3	RNEG_3	RPOS_3	JTAGRing
C	RTIP_0	RVDD	RLOS_0	TNEG_0	TPOS_0	TAOS_3	RD_DS	Reserved	DGND	A[0]	A[5]	TXON_2	DMO_3	TCLK_3	DMO_2	TTIP_3	TGND	RTIP_3
D	RRING_0	RGND	TGND	DMO_1	DMO_0	TAOS_0	WR_RW	DGND	DVDD3v3	DVDD1v8	A[4]	TXON_1	TNEG_2	TPOS_3	RPOS_2	RVDD	RGND	RRING_3
E	TMS	TRING_0	TTIP_0	TVDD	RVDD										TGND	TRING_3	TVDD	JTAGTip
F	RRING_1	TGND	TRING_1	TVDD											TRING_2	TVDD	TTIP_2	RRING_2
G	RTIP_1	RPOS_1	RGND	TTIP_1											DGND	RVDD	RGND	RTIP_2
H	MCLKOUT	RNEG_1	RCLK_1	RLOS_1											RLOS_2	RCLK_2	DGND	RNEG_2
J	MCLK1	AVDD	AVDD	DVDD3v3											RLOS_6	μPTS1	AGND	GAUGE
K	Reserved	DGND	AGND	SR/DR											DVDD3v3	RXON	AVDDS	DVDD1v8
L	RTIP_5	RLOS_5	RCLK_5	AGND											μPTS2	INT	RPOS_6	RTIP_6
M	RRING_5	RGND	RPOS_5	RNEG_5											RCLK_6	RNEG_6	RGND	RRING_6
N	TCK	TTIP_5	RVDD	TRING_5											TVDD	TTIP_6	RVDD	NC
P	TVDD	TRING_4	TGND	DMO_5											TVDD	TTIP_7	TRING_7	SER_PAR
R	TDI	TTIP_4	TGND	TVDD	DMO_4	TAOS_7	D[0]	DGND	DVDD3v3	RXRES1	TERSEL	TXON_6	TXON_7	TNEG_7	TRING_6	TGND	RGND	RRING_7
T	RRING_4	RGND	TCLK_4	RNEG_4	TCLK_5	TAOS_4	D[7]	RESET	DGND	HW_HOST	Reserved	RXMUTE	μPCLK	TPOS_7	RLOS_7	TGND	RPOS_7	RTIP_7
U	RTIP_4	RPOS_4	RCLK_4	TNEG_4	TPOS_5	TAOS_5	D[6]	D[2]	D[1]	DVDD1v8	RXTSEL	TEST	TXON_5	TNEG_6	TCLK_7	RCLK_7	DMO_6	RVDD
V	DVDD1v8	RVDD	RLOS_4	TPOS_4	TNEG_5	TAOS_6	D[5]	D[4]	D[3]	RXRES0	TXTSEL	ICT	TXON_4	DMO_7	TPOS_6	TCLK_6	RNEG_7	DGND

XRT83VSH28
(Top View)

225 Ball BGA

GENERAL DESCRIPTION	1
APPLICATIONS	1
FIGURE 1. BLOCK DIAGRAM OF THE XRT83VSH28 E1 LIU (HOST MODE)	1
FIGURE 2. BLOCK DIAGRAM OF THE XRT83VSH28 E1 LIU (HARDWARE MODE)	2
FEATURES	3
ORDERING INFORMATION	3
PIN DESCRIPTION BY FUNCTION	5
RECEIVE SECTION	5
TRANSMIT SECTION	8
PARALLEL MICROPROCESSOR INTERFACE	10
JITTER ATTENUATOR	12
CLOCK SYNTHESIZER	13
ALARM FUNCTIONS/REDUNDANCY SUPPORT	14
SERIAL MICROPROCESSOR INTERFACE	16
POWER AND GROUND	16
FUNCTIONAL DESCRIPTION	19
1.0 HARDWARE MODE VS HOST MODE	19
1.1 FEATURE DIFFERENCES IN HARDWARE MODE	19
TABLE 1: DIFFERENCES BETWEEN HARDWARE MODE AND HOST MODE	19
2.0 RECEIVE PATH LINE INTERFACE	20
FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH	20
2.1 LINE TERMINATION (RTIP/RRING)	20
2.1.1 CASE 1: INTERNAL TERMINATION	20
TABLE 2: SELECTING THE INTERNAL IMPEDANCE	20
FIGURE 4. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION	20
2.1.2 CASE 2: INTERNAL TERMINATION WITH ONE EXTERNAL FIXED RESISTOR FOR ALL MODES	21
TABLE 3: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR	21
FIGURE 5. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR	21
2.2 CLOCK AND DATA RECOVERY	22
FIGURE 6. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK	22
FIGURE 7. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK	22
TABLE 4: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG	22
2.2.1 RECEIVE SENSITIVITY	23
FIGURE 8. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY	23
2.2.2 INTERFERENCE MARGIN	23
FIGURE 9. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN	23
2.2.3 GENERAL ALARM DETECTION AND INTERRUPT GENERATION	23
2.3 RECEIVE JITTER ATTENUATOR	24
2.4 HDB3 DECODER	25
2.5 RPOS/RNEG/RCLK	25
FIGURE 10. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN	25
FIGURE 11. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN	25
2.6 RXMUTE (RECEIVER LOS WITH DATA MUTING)	26
FIGURE 12. SIMPLIFIED BLOCK DIAGRAM OF THE RXMUTE FUNCTION	26
3.0 TRANSMIT PATH LINE INTERFACE	27
FIGURE 13. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH	27
3.1 TCLK/TPOS/TNEG DIGITAL INPUTS	27
FIGURE 14. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK	27
FIGURE 15. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK	27
TABLE 5: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG	28
3.2 HDB3 ENCODER	28
TABLE 6: EXAMPLES OF HDB3 ENCODING	28
3.3 TRANSMIT JITTER ATTENUATOR	29
TABLE 7: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS	29
3.4 TAOS (TRANSMIT ALL ONES)	29
FIGURE 16. TAOS (TRANSMIT ALL ONES)	29
3.5 TRANSMIT DIAGNOSTIC FEATURES	29
3.5.1 ATAOS (AUTOMATIC TRANSMIT ALL ONES)	29
FIGURE 17. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION	30
3.5.2 QRSS GENERATION	30

TABLE 8: RANDOM BIT SEQUENCE POLYNOMIALS	30
3.6 DMO (DIGITAL MONITOR OUTPUT)	31
3.7 LINE TERMINATION (TTIP/TRING)	31
FIGURE 18. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION	31
4.0 E1 APPLICATIONS	32
4.1 LOOPBACK DIAGNOSTICS	32
4.1.1 LOCAL ANALOG LOOPBACK	32
FIGURE 19. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK	32
4.1.2 REMOTE LOOPBACK	32
FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK	32
4.1.3 DIGITAL LOOPBACK	33
FIGURE 21. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK	33
4.1.4 DUAL LOOPBACK	33
FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK	33
4.2 LINE CARD REDUNDANCY	34
4.2.1 1:1 AND 1+1 REDUNDANCY WITHOUT RELAYS	34
4.2.2 TRANSMIT INTERFACE WITH 1:1 AND 1+1 REDUNDANCY	34
FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY	34
4.2.3 RECEIVE INTERFACE WITH 1:1 AND 1+1 REDUNDANCY	35
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY	35
4.2.4 N+1 REDUNDANCY USING EXTERNAL RELAYS	36
4.2.5 TRANSMIT INTERFACE WITH N+1 REDUNDANCY	36
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY	36
4.2.6 RECEIVE INTERFACE WITH N+1 REDUNDANCY	37
FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY	37
4.3 POWER FAILURE PROTECTION	38
4.4 OVERVOLTAGE AND OVERCURRENT PROTECTION	38
4.5 NON-INTRUSIVE MONITORING	38
FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION	38
5.0 MICROPROCESSOR INTERFACE	39
5.1 SERIAL MICROPROCESSOR INTERFACE BLOCK (BGA PACKAGE ONLY)	39
FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE	39
5.1.1 SERIAL TIMING INFORMATION	39
FIGURE 29. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE	39
5.1.2 24-BIT SERIAL DATA INPUT DESCRIPTION	40
5.1.3 ADDR[7:0] (SCLK1 - SCLK8)	40
5.1.4 R/W (SCLK9)	40
5.1.5 DUMMY BITS (SCLK10 - SCLK16)	40
5.1.6 DATA[7:0] (SCLK17 - SCLK24)	40
5.1.7 8-BIT SERIAL DATA OUTPUT DESCRIPTION	40
FIGURE 30. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE	41
TABLE 9: MICROPROCESSOR SERIAL INTERFACE TIMINGS (TA = 250C, VDD=3.3V± 5% AND LOAD = 10pF)	41
5.2 PARALLEL MICROPROCESSOR INTERFACE BLOCK	42
TABLE 10: SELECTING THE MICROPROCESSOR INTERFACE MODE	42
FIGURE 31. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK	42
5.3 THE MICROPROCESSOR INTERFACE BLOCK SIGNALS	43
TABLE 11: XRT83VSH28 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES	43
TABLE 12: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS	43
TABLE 13: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS	44
5.4 INTEL MODE PROGRAMMED I/O ACCESS (ASYNCHRONOUS)	45
FIGURE 32. INTEL μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS	46
TABLE 14: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS	46
5.5 MOTOROLA MODE PROGRAMMED I/O ACCESS (ASYNCHRONOUS)	47
FIGURE 33. MOTOROLA 68K μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS	48
TABLE 15: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS	48
5.6 POWERPC 403 SYNCHRONOUS MODE:	49
FIGURE 34. POWERPC 403 MODE TIMING - WRITE OPERATION	49
TABLE 16. POWER PC403 MODE TIMING - WRITE OPERATION	49
FIGURE 35. POWERPC 403 MODE TIMING - READ OPERATION	50
TABLE 17. POWER PC403 MODE TIMING - READ OPERATION	50
5.7 MICROPROCESSOR INTERFACE TIMING - MCP860 SYNCHRONOUS MODE	51
FIGURE 36. MPC86X MODE TIMING - WRITE OPERATION	51
TABLE 18. MPC86X MODE TIMING - WRITE OPERATION	51
TABLE 19. MPC86X TIMING INFORMATION - READ OPERATION	52



FIGURE 37: MPC86X MODE TIMING - READ OPERATION	52
TABLE 20: MICROPROCESSOR REGISTER ADDRESS (ADDR[7:0])	53
TABLE 21: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION	53
5.8 CHANNEL CONTROL REGISTERS	55
TABLE 22: MICROPROCESSOR REGISTER 0x00H BIT DESCRIPTION	55
TABLE 23: CABLE LENGTH SETTING.....	56
TABLE 24: MICROPROCESSOR REGISTER 0x01H BIT DESCRIPTION	56
TABLE 25: MICROPROCESSOR REGISTER 0x02H BIT DESCRIPTION	57
TABLE 26: MICROPROCESSOR REGISTER 0x03H BIT DESCRIPTION	58
TABLE 27: MICROPROCESSOR REGISTER 0x04H BIT DESCRIPTION	59
TABLE 28: MICROPROCESSOR REGISTER 0x05H BIT DESCRIPTION	60
TABLE 29: MICROPROCESSOR REGISTER 0x06H BIT DESCRIPTION	61
5.9 GLOBAL CONTROL REGISTERS	63
TABLE 30: MICROPROCESSOR REGISTER 0x80H, BIT DESCRIPTION	63
TABLE 31: MICROPROCESSOR REGISTER 0x81H, BIT DESCRIPTION	64
TABLE 32: MICROPROCESSOR REGISTER 0x82H BIT DESCRIPTION	64
TABLE 33: MICROPROCESSOR REGISTER 0x8CH BIT DESCRIPTION.....	65
TABLE 34: MICROPROCESSOR REGISTER 0x8DH BIT DESCRIPTION.....	65
TABLE 35: MICROPROCESSOR REGISTER 0x8EH BIT DESCRIPTION.....	66
TABLE 36: MICROPROCESSOR REGISTER 0xFEH BIT DESCRIPTION.....	67
TABLE 37: MICROPROCESSOR REGISTER 0xFFH BIT DESCRIPTION.....	67
6.0 ELECTRICAL CHARACTERISTICS	68
TABLE 38: ABSOLUTE MAXIMUM RATINGS.....	68
TABLE 39: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS	68
TABLE 40: AC ELECTRICAL CHARACTERISTICS	68
TABLE 41: POWER CONSUMPTION.....	69
TABLE 42: E1 RECEIVER ELECTRICAL CHARACTERISTICS.....	69
TABLE 43: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS	70
PACKAGE DIMENSIONS.....	71
225 BALL PLASTIC BALL GRID ARRAY (BOTTOM VIEW)	71
(19.0 x 19.0 x 1.0MM).....	71
ORDERING INFORMATION	72
REVISIONS	72

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTION

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
RXON	K16	I	Receiver On <u>Hardware Mode Only</u> This pin is used to enable the receivers for all channels. By default, the receivers are turned ON in hardware mode. To turn the receivers OFF, pull this pin "Low". <i>NOTE: Internally pulled "High" with a 50kΩ resistor.</i>
RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7	C3 H4 H15 A16 V3 L2 J15 T15	O	Receive Loss of Signal When a receive loss of signal occurs according to ITU-T G.775, the RLOS pin will go "High" for a minimum of one RCLK cycle. RLOS will remain "High" until the loss of signal condition clears. See the Receive Loss of Signal section of this datasheet for more details. <i>NOTE: This pin can be used for redundancy applications to initiate an automatic switch to a backup card.</i>
RCLK0 RCLK1 RCLK2 RCLK3 RCLK4 RCLK5 RCLK6 RCLK7	B3 H3 H16 A17 U3 L3 M15 U16	O	Receive Clock Output RCLK is the recovered clock from the incoming data stream. If the incoming signal is absent or RTIP/RRING are in "High-Z", RCLK maintains its timing by using an internal master clock as its reference. RPOS/RNEG data can be updated on either edge of RCLK selected by RCLKE. <i>NOTE: RCLKE is a global setting that applies to all 8 channels.</i>
RNEG/LCV0 RNEG/LCV1 RNEG/LCV2 RNEG/LCV3 RNEG/LCV4 RNEG/LCV5 RNEG/LCV6 RNEG/LCV7	A2 H2 H18 B16 T4 M4 M16 V17	O	RNEG/LCV_OF Output In dual rail mode, this pin is the receive negative data output. In single rail mode, this pin is a Line Code Violation / Counter Overflow indicator. If LCV is selected by programming the appropriate global register and if a line code violation, a bi-polar violation, or excessive zeros occur, the LCV pin will pull "High" for a minimum of one RCLK cycle. LCV will remain "High" until there are no more violations. However, if OF (Overflow) is selected the LCV pin will pull "High" if the internal LCV counter is saturated. The LCV pin will remain "High" until the LCV counter is reset.
RPOS0 RPOS1 RPOS2 RPOS3 RPOS4 RPOS5 RPOS6 RPOS7	B2 G2 D15 B17 U2 M3 L17 T17	O	RPOS/RDATA Output Receive digital output pin. In dual rail mode, this pin is the receive positive data output. In single rail mode, this pin is the receive non-return to zero (NRZ) data output.



SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7	C1 G1 G18 C18 U1 L1 L18 T18	I	Receive Differential Tip Input RTIP is the positive differential input from the line interface. Along with the RRING signal, these pins should be coupled to a 1:1 transformer for proper operation.
RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7	D1 F1 F18 D18 T1 M1 M18 R18	I	Receive Differential Ring Input RRING is the negative differential input from the line interface. Along with the RTIP-signal, these pins should be coupled to a 1:1 transformer for proper operation.
RXMUTE	T12	I	Receive Data Muting <u>Hardware Mode Only</u> This pin is AND-ed with each of the RLOS functions on a per channel basis. Therefore, if this pin is pulled "High" and a given channel experiences a loss of signal, then the RPOS/RNEG output pins are automatically pulled "Low" to prevent data chattering. To disable this feature, the RxMUTE pin must be pulled "Low". NOTE: This pin is internally pulled "High" with a 50kΩ resistor

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
RXRES1 RXRES0	R10 V10	I	Receive External Resistor Control Pins <u>Hardware mode Only</u> These pins are used in the Receive Internal Impedance mode for unique applications where an accurate resistor can be used to achieve optimal return loss. When RxRES[1:0] are used, the LIU automatically sets the internal impedance to match the line build out. For example: if 240Ω is selected, the LIU chooses an internal impedance such that the parallel combination equals the impedance chosen by TERSEL[1:0]. "00" = No External Fixed Resistor "01" = 320Ω "10" = 280Ω "11" = 190Ω NOTE: These pins are internally pulled "Low" with a 50kΩ resistor. This feature is available in Host mode by programming the appropriate channel register.
RCLKE/ μPTS1	J16	I	Receive Clock Edge <u>Hardware Mode</u> This pin is used to select which edge of the recovered clock is used to update data to the receiver on the RPOS/RNEG outputs. By default, data is updated on the rising edge. To update data on the falling edge, this pin must be pulled "High". <u>Host Mode</u> μPTS[2:1] pins are used to select the type of microprocessor to be used for Host communication. "00" = 8051 Intel Asynchronous "01" = 68K Motorola Asynchronous "10" = Power PC 403 "11" = MPC8xx Power PC Synchronous NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.

TRANSMIT SECTION

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TCLKE/ μ PTS2	L15	I	Transmit Clock Edge <u>Hardware Mode</u> This pin is used to select which edge of the transmit clock is used to sample data on the transmitter on the TPOS/TNEG inputs. By default, data is sampled on the falling edge. To sample data on the rising edge, this pin must be pulled "High". <u>Host Mode</u> μ PTS[2:1] pins are used to select the type of microprocessor to be used for Host communication. "00" = 8051 Intel Asynchronous "01" = 68K Motorola Asynchronous "10" = Power PC 403 "11" = MPC8xx Power PC Synchronous NOTE: This pin is internally pulled "Low" with a 50k Ω resistor.
TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7	E3 G4 F17 C16 R2 N2 N16 P16	O	Transmit Differential Tip Output TTIP is the positive differential output to the line interface. Along with the TRING signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7	E2 F3 F15 E16 P2 N4 R15 P17	O	Transmit Differential Ring Output TRING is the negative differential output to the line interface. Along with the TTIP signal, these pins should be coupled to a 1:2 step up transformer for proper operation.
TPOS0 TPOS1 TPOS2 TPOS3 TPOS4 TPOS5 TPOS6 TPOS7	C5 A4 B14 D14 V4 U5 V15 T14	I	TPOS/TDATA Input Transmit digital input pin. In dual rail mode, this pin is the transmit positive data input. In single rail mode, this pin is the transmit non-return to zero (NRZ) data input. NOTE: Internally pulled "Low" with a 50K Ω resistor.
TNEG0 TNEG1 TNEG2 TNEG3 TNEG4 TNEG5 TNEG6 TNEG7	C4 B5 D13 B15 U4 V5 U14 R14	I	Transmitter Negative NRZ Data Input In dual rail mode, this signal is the negative-rail input data for the transmitter. In single rail mode, this pin can be left unconnected while in Host mode. However, in Hardware mode, this pin is used to select the type of encoding/decoding for the E1 data format. Connecting this pin "Low" enables HDB3. Connecting this pin "High" selects AMI data format. NOTE: Internally pulled "Low" with a 50k Ω resistor.

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TCLK0 TCLK1 TCLK2 TCLK3 TCLK4 TCLK5 TCLK6 TCLK7	B4 A3 A15 C14 T3 T5 V16 U15	I	Transmit Clock Input TCLK is the input facility clock used to sample the incoming TPOS/TNEG data. If TCLK is absent, pulled "Low", or pulled "High", the transmitter outputs at TTIP/TRING sends an all zero signal to the line. TPOS/TNEG data can be sampled on either edge of TCLK selected by TCLKE. NOTE: TCLKE is a global setting that applies to all 8 channels. These pins are Internally pulled "Low" with 50k Ω resistors.
TAOS0 TAOS1 TAOS2 TAOS3 TAOS4 TAOS5 TAOS6 TAOS7	D6 B6 A5 C6 T6 U6 V6 R6	I	Transmit All Ones for Channel <u>Hardware Mode Only</u> Setting this pin "High" enables the transmission of an all ones pattern to the line from TTIP/TRING. If this pin is pulled "Low", the transmitters operate in normal throughput mode. NOTE: Internally pulled "Low" with a 50k Ω resistor for all channels. This feature is available in Host mode by programming the appropriate channel register.
TXON0 TXON1 TXON2 TXON3 TXON4 TXON5 TXON6 TXON7	A13 D12 C12 B12 V13 U13 R12 R13	I	Transmit On/Off Input Upon power up, the transmitters are powered off. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register while in Host mode. However, if TxONCNTL is set "High" in the appropriate global register or if in Hardware mode, the activity of the transmitter outputs is controlled by the TxON pins. NOTE: TxON is ideal for redundancy applications. See the Redundancy Applications Section of this datasheet for more details. Internally pulled "Low" with a 50K Ω resistor.

PARALLEL MICROPROCESSOR INTERFACE

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
HW/HOST	T10	I	Mode Control Input This pin is used to select Host mode or Hardware mode. By default, the LIU is set in Hardware mode. To use Host mode, this pin must be pulled "Low". NOTE: Internally pulled "High" with a 50kΩ resistor.
WR _{R/W} /EQC0	D7	I	Write Input(R/W)/Equalizer Control Signal 0 <u>Host Mode</u> This pin is used to communicate a Read or Write operation according to the which microprocessor is chosen. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 23 for more details. NOTE: Internally pulled "Low" with a 50kΩ resistor.
RD _{DS} /EQC1	C7	I	Read Input (Data Strobe)/Equalizer Control Signal 1 <u>Host Mode</u> This pin is used to communicate a Read or Write operation according to the which microprocessor is chosen. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 23 for more details. NOTE: Internally pulled "Low" with a 50kΩ resistor.
ALE/EQC2	A7	I	Address Latch Input (Address Strobe) <u>Host Mode</u> This pin is used to latch the address contents into the internal registers within the LIU device. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 23 for more details. NOTE: Internally pulled "Low" with a 50kΩ resistor.
CS/EQC3	B7	I	Chip Select Input - Host mode: <u>Host Mode</u> This pin is used to initiate communication with the microprocessor interface. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 23 for more details. NOTE: Internally pulled "Low" with a 50kΩ resistor.

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
$\overline{\text{RDY}}/\text{EQC4}$	A6	I/O	Ready Output (Data Transfer Acknowledge) <u>Host Mode (Parallel Microprocessor)</u> If Pin SER_PAR is pulled "Low", this output pin from the microprocessor block is used to inform the local μP that the Read or Write operation has been completed and is waiting for the next command. See the Microprocessor Section of this datasheet for details. <u>Host Mode (Serial Interface)</u> If Pin SER_PAR is pulled "High", this output pin from the serial interface is used to read back the register contents. See the Microprocessor Section of this datasheet for details. <u>Hardware Mode</u> EQC[4:0] are used to set the Receiver Gain, Receiver Impedance and the Transmit Line Build Out. See Table 23 for more details. NOTE: Internally pulled "Low" with a 50kΩ resistor.
D[7]/Loop14 D[6]/Loop04 D[5]/Loop15 D[4]/Loop05 D[3]/Loop16 D[2]/Loop06 D[1]/Loop17 D[0]/Loop07	T7 U7 V7 V8 V9 U8 U9 R7	I/O	Bi-Directional Data Bust/Loopback Mode Select <u>Host Mode</u> These pins are used for the 8-bit bi-directional data bus to allow data transfer to and from the microprocessor interface. <u>Hardware Mode (Channels 4 through 7)</u> These pins are used to select the loopback mode. Each channel has two loopback pins Loop[1:0]. "00" = No Loopback "01" = Analog Local Loopback "10" = Remote Loopback "11" = Digital Loopback NOTE: Internally pulled "Low" with a 50kΩ resistor.
A[7]/Loop13 A[6]/Loop03 A[5]/Loop12 A[4]/Loop02 A[3]/Loop11 A[2]/Loop01 A[1]/Loop10 A[0]/Loop00	A12 B11 C11 D11 A11 B10 A10 C10	I	Direct Address Bus/Loopback Mode Select <u>Host Mode</u> These pins are used for the 8-bit direct address bus to allow access to the internal registers within the microprocessor interface. <u>Hardware Mode (Channels 0 through 3)</u> These pins are used to select the loopback mode. Each channel has two loopback pins Loop[1:0]. "00" = No Loopback "01" = Analog Local Loopback "10" = Remote Loopback "11" = Digital Loopback NOTE: Internally pulled "Low" with a 50kΩ resistor.

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
μ PCLK/ATAOS	T13	I	Synchronous Microprocessor Clock/Automatic Transmit All Ones Host Mode This synchronous input clock is used as the internal master clock to the microprocessor interface when configured for in a synchronous mode. Hardware Mode This pin is used select an all ones signal to the line interface through TTIP/TRING any time that a loss of signal occurs. This feature is available in Host mode by programming the appropriate global register. NOTE: Internally pulled "Low" with a 50k Ω resistor.
$\overline{\text{INT}}$	L16	O	Interrupt Output Host Mode This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". GIE (Global Interrupt Enable) must be set "High" in the appropriate global register to enable interrupt generation. NOTE: This pin is an open-drain output that requires an external 10K Ω pull-up resistor.

JITTER ATTENUATOR

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION																										
JASEL0 JASEL1	A14 B13	I	Jitter Attenuator Select Pins Hardware Mode JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it. <table><tr><th rowspan="2">JASEL1</th><th rowspan="2">JASEL0</th><th rowspan="2">JA Path</th><th>JA BW Hz</th><th rowspan="2">FIFO Size</th></tr><tr><th>E1</th></tr><tr><td>0</td><td>0</td><td>Disabled</td><td>-----</td><td>-----</td></tr><tr><td>0</td><td>1</td><td>Transmit</td><td>10</td><td>32/32</td></tr><tr><td>1</td><td>0</td><td>Receive</td><td>10</td><td>32/32</td></tr><tr><td>1</td><td>1</td><td>Receive</td><td>1.5</td><td>64/64</td></tr></table> NOTE: These pins are internally pulled “Low” with 50kΩ resistors.	JASEL1	JASEL0	JA Path	JA BW Hz	FIFO Size	E1	0	0	Disabled	-----	-----	0	1	Transmit	10	32/32	1	0	Receive	10	32/32	1	1	Receive	1.5	64/64
JASEL1	JASEL0	JA Path	JA BW Hz				FIFO Size																						
			E1																										
0	0	Disabled	-----	-----																									
0	1	Transmit	10	32/32																									
1	0	Receive	10	32/32																									
1	1	Receive	1.5	64/64																									

CLOCK SYNTHESIZER

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
MCLKOUT	H1	O	Synthesized Master Clock Output This signal is the output of the Master Clock Synthesizer PLL which is at E1 rate.
MCLKE1	J1	I	E1 Master Clock Input A 2.048MHz clock for with an accuracy of better than ± 50 ppm and a duty cycle of 40% to 60% can be provided at this pin. NOTE: This pin is internally pulled "Low" with a 50k Ω resistor.

ALARM FUNCTIONS/REDUNDANCY SUPPORT

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
GAUGE	J18	I	Twisted Pair Cable Wire Gauge Select <u>Hardware Mode Only</u> This pin is used to match the frequency characteristics according to the gauge of wire used in Telecom circuits. By default, the LIU is matched to 22 gauge or 24 gauge wire. To select 26 gauge, this pin must be pulled "High". NOTE: Internally pulled "Low" with a 50k Ω resistor.
DMO0 DMO1 DMO2 DMO3 DMO4 DMO5 DMO6 DMO7	D5 D4 C15 C13 R5 P4 U17 V14	O	Digital Monitor Output When no transmit output pulse is detected for more than 128 TCLK cycles within the transmit output buffer, the DMO pin will go "High" for a minimum of one TCLK cycle. DMO will remain "High" until the transmitter sends a valid pulse. NOTE: This pin can be used for redundancy applications to initiate an automatic switch to a backup card.
$\overline{\text{RESET}}$	T8	I	Hardware Reset Input Active low signal. When this pin is pulled "Low" for more than 10 μ S, the internal registers are set to their default state. See the register description for the default values. NOTE: Internally pulled "High" with a 50K Ω resistor.
$\overline{\text{SR/DR}}$	K4	I	Single-Rail/Dual-Rail Data Format <u>Hardware Mode Only</u> This pin is used to control the data format on the facility side of the LIU to interface to a Framer or Mapper/ASIC device. By default, dual rail mode is selected which relies upon the Framer to handle the encoding/decoding functions. To select single rail mode, this pin must be pulled "High". If single rail mode is selected, the LIU can encode/decode AMI or HDB3 data formats. NOTE: Internally pulled "Low" with a 50k Ω resistor.
RXTSEL	U11	I	Receiver Termination Select <u>Hardware Mode</u> This pin is used to select between the internal and external impedance modes for the receive path. By default, the receivers are configured for external impedance mode, which is ideal for redundancy applications without relays. To select internal impedance, this pin must be pulled "High". <u>Host Mode</u> Internal/External impedance can be selected by programming the appropriate channel registers. However, to assist in redundancy applications, this pin can be used for a hard switch if the RxTCNTL bit is set "High" in the appropriate global register. If RxTCNTL is set "High", the individual RxTSEL register bits are ignored. NOTE: This pin is internally pulled "Low" with a 50k Ω resistor.
TXTSEL	V11	I	Transmitter Termination Select <u>Hardware Mode</u> This pin is used to select between the internal and external impedance modes for the transmit path. By default, the receivers are configured for external impedance mode, which is ideal for redundancy applications without relays. To select internal impedance, this pin must be pulled "High". NOTE: This pin is internally pulled "Low".

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TERSEL	R11	I	Termination Impedance Select <u>Hardware Mode Only</u> The TERSEL pin is used to select the transmitter and receiver impedance. By default, the impedance is set to 75Ω. "Low" = 75Ω "High" = 120Ω <i>NOTE: This pin is internally pulled "Low" with a 50kΩ resistor.</i>
TEST	U12	I	Factory Test Mode For normal operation, the TEST pin should be tied to ground. <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i>
$\overline{\text{ICT}}$	V12	I	In Circuit Testing When this pin is tied "Low", all output pins are forced to "High" impedance for in circuit testing. <i>NOTE: Internally pulled "High" with a 50KΩ resistor.</i>

SERIAL MICROPROCESSOR INTERFACE

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
SER_PAR	P18	I	Serial/Parallel Select Input (Host Mode Only) This pin is used in the Host mode to select between the parallel microprocessor or serial interface. By default, the Host mode operates in the parallel microprocessor mode. To configure the device for a serial interface, this pin must be pulled "High". <i>NOTE: Internally pulled "Low" with a 50kΩ resistor.</i>
SCLK	T13	I	Serial Clock Input (Host Mode Only) If Pin SER_PAR is pulled "High", this input pin is used as the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.
SDI	C10	I	Serial Data Input (Host Mode Only) If Pin SER_PAR is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.
SDO	R7	O	Serial Data Output (Host Mode Only) If Pin SER_PAR is pulled "High", this output pin from the serial interface is used to read back the register contents. See the Microprocessor Section of this datasheet for details.
JTAGtip JTAGring	E18 B18		Analog JTAG Positive Pin Analog JTAG Negative Pin
TDO	B1		Test Data Out This pin is used as the output data pin for the boundary scan chain.
TDI	R1		Test Data In This pin is used as the input data pin for the boundary scan chain.
TCK	N1		Test Clock Input This pin is used as the input clock source for the boundary scan chain.
TMS	E1		Test Mode Select This pin is used as the input mode select for the boundary scan chain.
SENSE	N18	****	Factory Test Pin

POWER AND GROUND

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TGND	D3 F2 E15 C17 R3 P3 T16 R16	****	Transmitter Analog Ground It's recommended that all ground pins of this device be tied together.

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
TVDD	E4 F4 F16 E17 R4 P1 N15 P15	****	Transmit Analog Power Supply (3.3V ±5%) TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RVDD	C2 E5 G16 D16 V2 N3 N17 U18	****	Receive Analog Power Supply (3.3V ±5%) RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.
RGND	D2 G3 G17 D17 T2 M2 M17 R17	****	Receiver Analog Ground It's recommended that all ground pins of this device be tied together.
AVDD-Bias	K17 J3 J2	****	Analog Power Supply (1.8V ±5%) AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.
AGND	J17 K3 L4	****	Analog Ground It's recommended that all ground pins of this device be tied together.
DVDD3v3	A18 R9 D9 K15 J4	****	Digital Power Supply (3.3V ±5%) DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.
DVDD1v8	V1 U10 K18 D10 A9	****	Digital Power Supply (1.8V ±5%) DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor. NOTE: For proper operation, the power-up sequence is: bring up 1.8V power before the 3.3V.



SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
DGND	A1 R8 T9 H17 B9 D8 C9 G15 K2 V18	****	Digital Ground It's recommended that all ground pins of this device be tied together.
NC	A8, B8, C8, K1, T11	I	No Connect Pins

FUNCTIONAL DESCRIPTION

The XRT83VSH28 is a fully integrated 8-channel short-haul line interface unit (LIU) that operates from a 1.8V and a 3.3V power supply. The LIU features are programmed through a standard microprocessor interface or controlled through Hardware mode. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays. Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, Network Loop Code generation/detection, TAOS, DMO, and diagnostic loopback modes.

1.0 HARDWARE MODE VS HOST MODE

The LIU supports a parallel or serial microprocessor interface (Host mode) for programming the internal features, or a Hardware mode that can be used to configure the device.

1.1 Feature Differences in Hardware Mode

Some features within the Hardware mode are not supported on a per channel basis. The differences between Hardware mode and Host mode are described below in [Table 1](#).

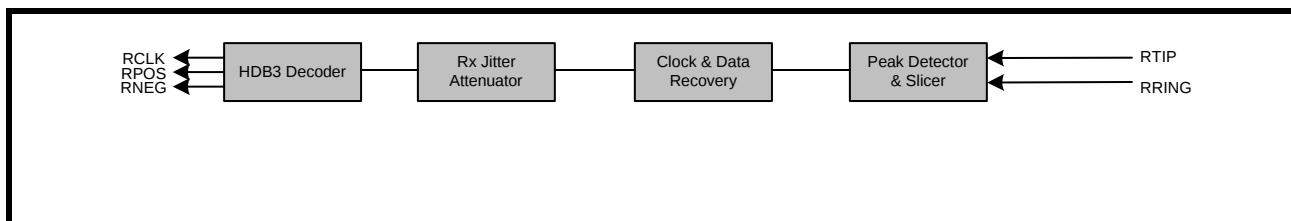
TABLE 1: DIFFERENCES BETWEEN HARDWARE MODE AND HOST MODE

FEATURE	HOST MODE	HARDWARE MODE
Tx Test Patterns	Fully Supported	QRSS diagnostic patterns are not available in Hardware mode. The TAOS feature is available.
RxRES[1:0]	Per Channel	In Hardware mode, RxRES[1:0] is a global setting that applies to all channels.
TERSEL	Per Channel	In Hardware mode, TERSEL is a global setting that applies to all channels.
EQC[4:0]	Per Channel	In Hardware mode, the EQC[4:0] is a global setting that applies to all channels.
Dual Loopback	Fully Supported	In Hardware mode, dual loopback mode is not supported. Remote, Analog local, and digital loopback modes are available.
JASEL[1:0]	Per Channel	In Hardware mode, the jitter attenuator selection is a global setting that applies to all channels.
RxTSEL	Per Channel	In Hardware mode, the receive termination select is a global setting that applies to all channels.
TxTSEL	Per Channel	In Hardware mode, the transmit termination select is a global setting that applies to all channels.

2.0 RECEIVE PATH LINE INTERFACE

The receive path of the XRT83VSH28 LIU consists of 8 independent E1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS/RNEG outputs. A simplified block diagram of the receive path is shown in [Figure 3](#).

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH



2.1 Line Termination (RTIP/RRING)

2.1.1 CASE 1: Internal Termination

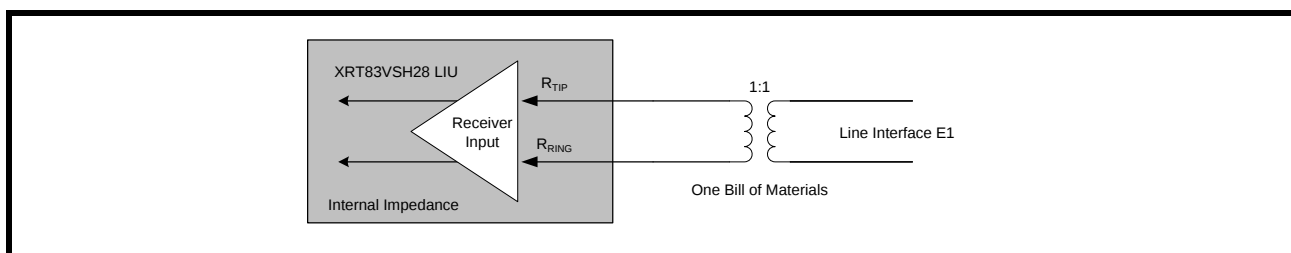
The input stage of the receive path accepts standard E1 twisted pair or E1 coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The receive termination impedance is selected by programming TERSEL to match the line impedance. Selecting the internal impedance is shown in [Table 2](#).

TABLE 2: SELECTING THE INTERNAL IMPEDANCE

TERSEL	RECEIVE TERMINATION
0h	75Ω
1h	120Ω

The XRT83VSH28 has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). For redundancy applications, a dedicated hardware pin (RxTSEL) is also available to control the receive termination for all channels simultaneously. This hardware pin takes priority over the register setting if RxTCNTL is set to "1" in the appropriate global register. If RxTCNTL is set to "0", the state of this pin is ignored. See [Figure 4](#) for a typical connection diagram using the internal termination.

FIGURE 4. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



2.1.2 CASE 2: Internal Termination With One External Fixed Resistor for All Modes

Along with the internal termination, a high precision external fixed resistor can be used to optimize the return loss. This external resistor can be used for all modes of operation ensuring one bill of materials. There are three resistor values that can be used by setting the RxRES[1:0] bits in the appropriate channel register. Selecting the value for the external fixed resistor is shown in [Table 3](#).

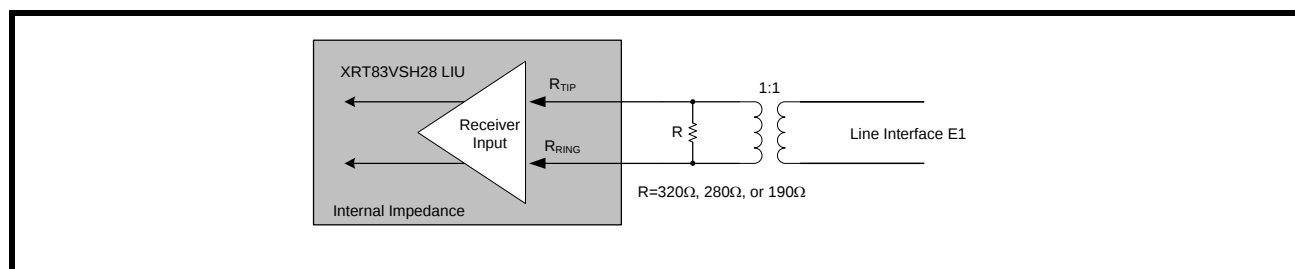
TABLE 3: SELECTING THE VALUE OF THE EXTERNAL FIXED RESISTOR

RxRES[1:0]	EXTERNAL FIXED RESISTOR
0h (00)	None
1h (01)	320Ω
2h (10)	280Ω
3h (11)	190Ω

By default, RxRES[1:0] is set to "None" for no external fixed resistor. If an external fixed resistor is used, the XRT83VSH28 uses the parallel combination of the external fixed resistor and the internal termination as the input impedance. See [Figure 5](#) for a typical connection diagram using the external fixed resistor.

NOTE: Without the external resistor, the XRT83VSH28 meets all return loss specifications. This mode was created to add flexibility for optimizing return loss by using a high precision external resistor.

FIGURE 5. TYPICAL CONNECTION DIAGRAM USING ONE EXTERNAL FIXED RESISTOR



2.2 Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channels to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock as its reference. The recovered data can be updated on either edge of RCLK. By default, data is updated on the rising edge of RCLK. To update data on the falling edge of RCLK, set RCLKE to "1" in the appropriate global register. **Figure 6** is a timing diagram of the receive data updated on the rising edge of RCLK. **Figure 7** is a timing diagram of the receive data updated on the falling edge of RCLK. The timing specifications are shown in **Table 4**.

FIGURE 6. RECEIVE DATA UPDATED ON THE RISING EDGE OF RCLK

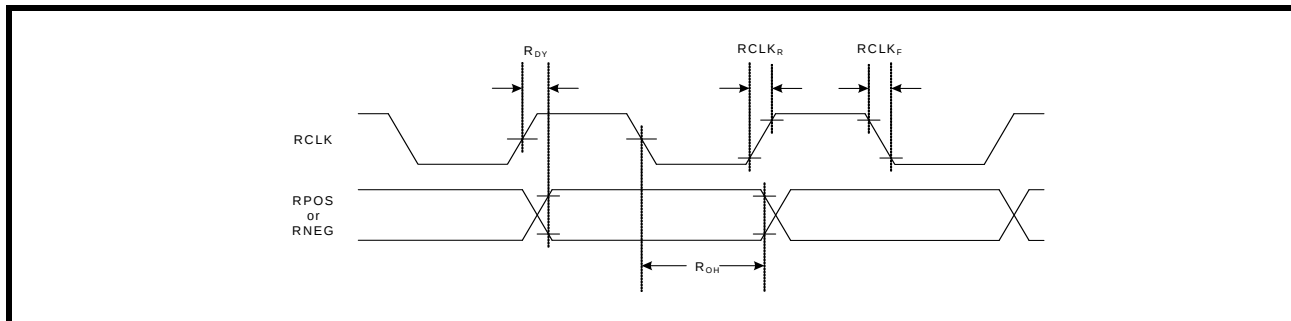


FIGURE 7. RECEIVE DATA UPDATED ON THE FALLING EDGE OF RCLK

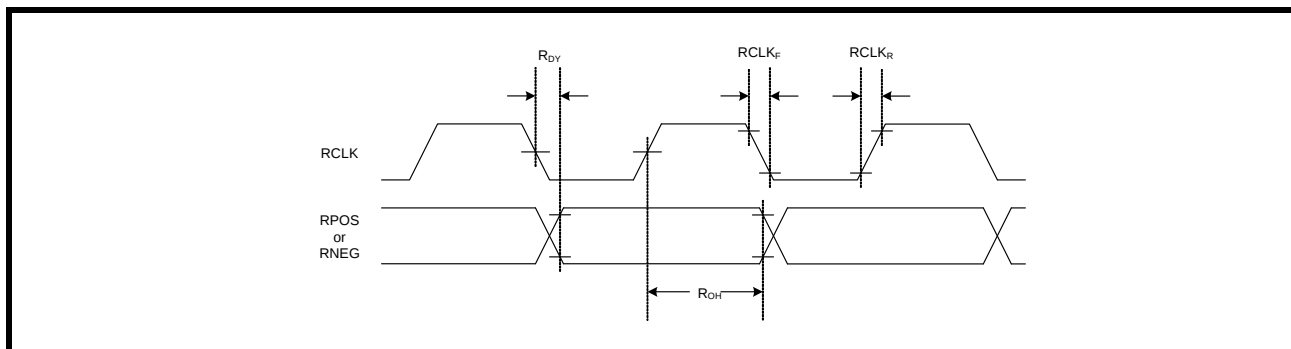


TABLE 4: TIMING SPECIFICATIONS FOR RCLK/RPOS/RNEG

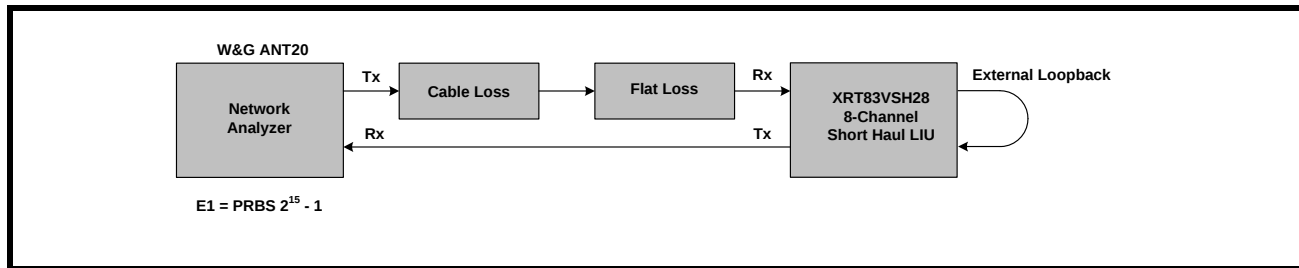
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Duty Cycle	R _{CDU}	45	50	55	%
Receive Data Setup Time	R _{SU}	150	-	-	ns
Receive Data Hold Time	R _{HO}	150	-	-	ns
RCLK to Data Delay	R _{DY}	-	-	40	ns
RCLK Rise Time (10% to 90%) with 25pF Loading	RCLK _R	-	-	40	ns
RCLK Fall Time (90% to 10%) with 25pF Loading	RCLK _F	-	-	40	ns

NOTE: VDD=3.3V ±5%, T_A=25°C, Unless Otherwise Specified

2.2.1 Receive Sensitivity

To meet short haul requirements, the XRT83VSH28 can accept E1 signals that have been attenuated by 12dB of flat loss. However, the XRT83VSH28 can tolerate cable loss and flat loss beyond the industry specifications. The receive sensitivity in the short haul mode is approximately 1,800 feet without experiencing bit errors, LOF, pattern synchronization, etc. Although data integrity is maintained, the RLOS function (if enabled) will report an RLOS condition according to the receiver loss of signal section in this datasheet. The test configuration for measuring the receive sensitivity is shown in **Figure 8**.

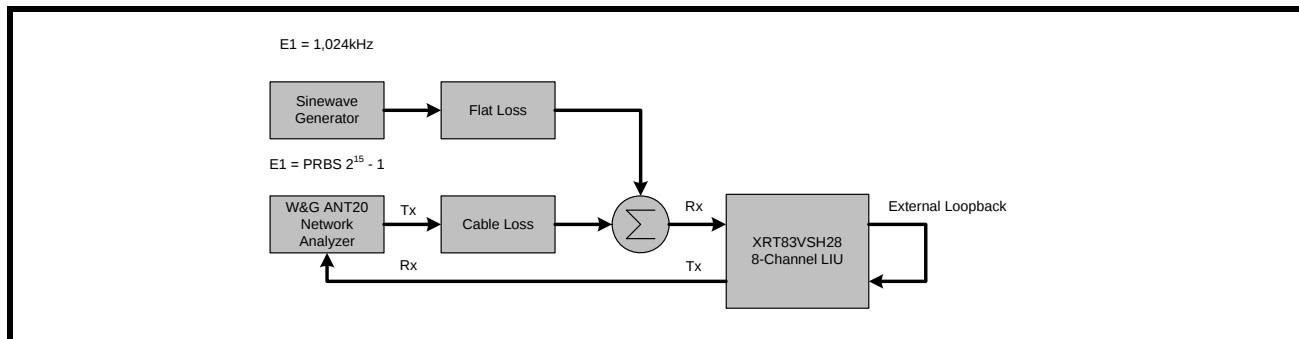
FIGURE 8. TEST CONFIGURATION FOR MEASURING RECEIVE SENSITIVITY



2.2.2 Interference Margin

The interference margin for the XRT83VSH28 is -15db. The test configuration for measuring the interference margin is shown in **Figure 9**.

FIGURE 9. TEST CONFIGURATION FOR MEASURING INTERFERENCE MARGIN



2.2.3 General Alarm Detection and Interrupt Generation

The receive path detects RLOS, AIS, QRPD and FLS. These alarms can be individually masked to prevent the alarm from triggering an interrupt. To enable interrupt generation, the Global Interrupt Enable (GIE) bit must be set "High" in the appropriate global register. Any time a change in status occurs (if the alarms are enabled), the interrupt pin will pull "Low" to indicate an alarm has occurred. Once the status registers have been read, the INT pin will return "High". The status registers are Reset Upon Read (RUR). The interrupts are categorized in a hierarchical process block. **Figure** is a simplified block diagram of the interrupt generation process.

NOTE: The interrupt pin is an open-drain output that requires a 10kΩ external pull-up resistor.

2.2.3.1 RLOS (Receiver Loss of Signal)

The XRT83VSH28 supports both G.775 or ETSI-300-233 RLOS detection scheme.

In G.775 mode, RLOS is declared when the received signal is less than 375mV for 32 consecutive pulse periods (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 425mV (typical).

In ETSI-300-233 mode the device declares RLOS when the input level drops below 375mV (typical) for more than 2048 pulse periods (1msec).

The device exits RLOS when the input signal exceeds 425mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window. ETSI-300-233 RLOS detection method is only available in Host mode.

2.2.3.2 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital RLOS is extended to count 4,096 consecutive zeros before declaring RLOS. By default, EXLOS is disabled and RLOS operates in normal mode.

2.2.3.3 AIS (Alarm Indication Signal)

The XRT83VSH28 adheres to the ITU-T G.775 specification for an all ones pattern. The AIS is set to "1" if the incoming signal has 2 or less zeros in a 512-bit window. AIS will clear when the incoming signal has 3 or more zeros in the 512-bit window.

2.2.3.4 FLSD (FIFO Limit Status Detection)

The purpose of the FIFO limit status is to indicate when the Read and Write FIFO pointers are within a pre-determined range (over-flow or under-flow indication). The FLSD is set to "1" if the FIFO Read and Write Pointers are within ± 3 -Bits.

2.2.3.5 LCVD (Line Code Violation Detection)

The LIU contains 8 independent, 16-bit LCV counters. When the counters reach full-scale, they remain saturated at FFFFh until they are reset globally or on a per channel basis. For performance monitoring, the counters can be updated globally or on a per channel basis to place the contents of the counters into holding registers. The LIU uses an indirect address bus to access a counter for a given channel. Once the contents of the counters have been placed in holding registers, they can be individually read out 8-bits at a time according to the BYTEsel bit in the appropriate global register. By default, the LSB is placed in the holding register until the BYTEsel is pulled "High" where upon the MSB will be placed in the holding register for read back. Once both bytes have been read, the next channel may be selected for read back.

By default, the LVC/OFD will be set to a "1" if the receiver is currently detecting line code violations or excessive zeros for HDB3. In AMI mode, the LCVD will be set to a "1" if the receiver is currently detecting bipolar violations or excessive zeros. However, if the LIU is configured to monitor the 16-bit LCV counter by programming the appropriate global register, the LCV/OFD will be set to a "1" if the counter saturates.

2.3 Receive Jitter Attenuator

The receive path has a dedicated jitter attenuator that reduces phase and frequency jitter in the recovered clock. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. The bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to $\frac{1}{2}$ of the FIFO bit depth.

NOTE: If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the transmit path has a dedicated jitter attenuator to smooth out the gapped clock. See the Transmit Section of this datasheet.

2.4 HDB3 Decoder

In single rail mode, RPOS can decode AMI or HDB3 signals. HDB3 is defined as any block of 4 successive zeros replaced with 000V or B00V, so that two successive V pulses are of opposite polarity to prevent a DC component. If the HDB3 decoder is selected, the receive path removes the V and B pulses so that the original data is output to RPOS.

2.5 RPOS/RNEG/RCLK

The digital output data can be programmed to either single rail or dual rail formats. **Figure 10** is a timing diagram of a repeating "0011" pattern in single-rail mode. **Figure 11** is a timing diagram of the same fixed pattern in dual rail mode.

FIGURE 10. SINGLE RAIL MODE WITH A FIXED REPEATING "0011" PATTERN

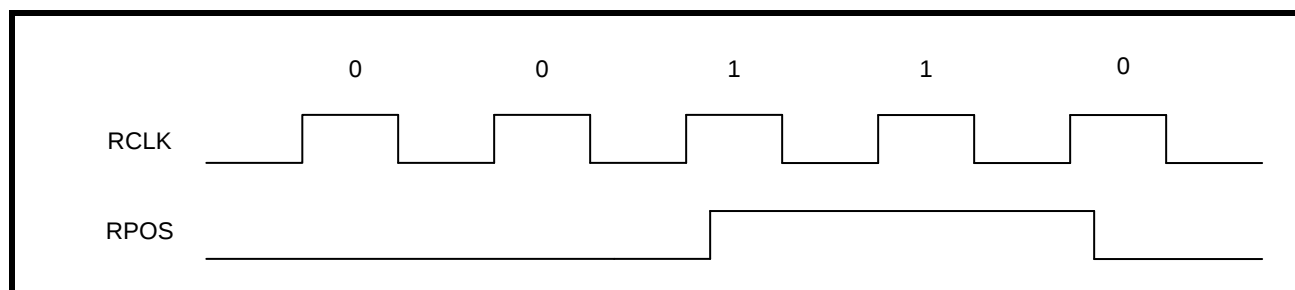
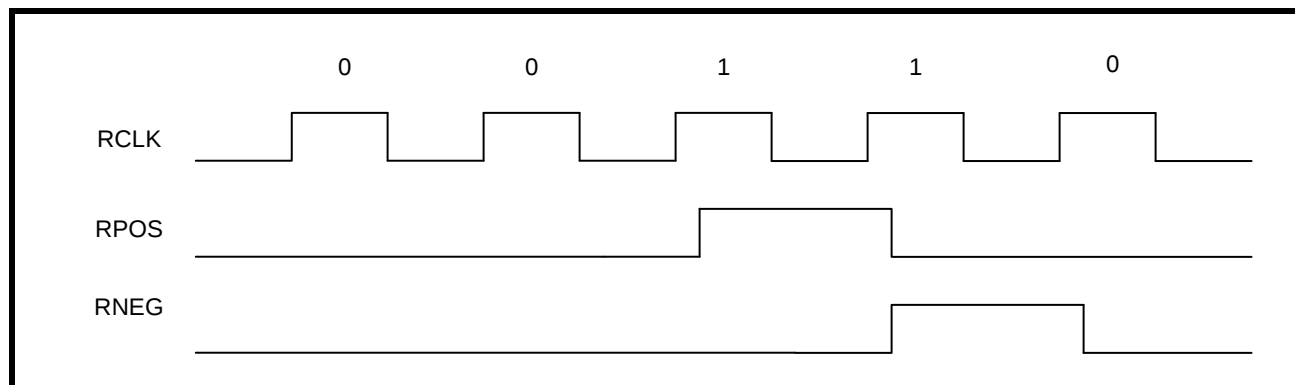


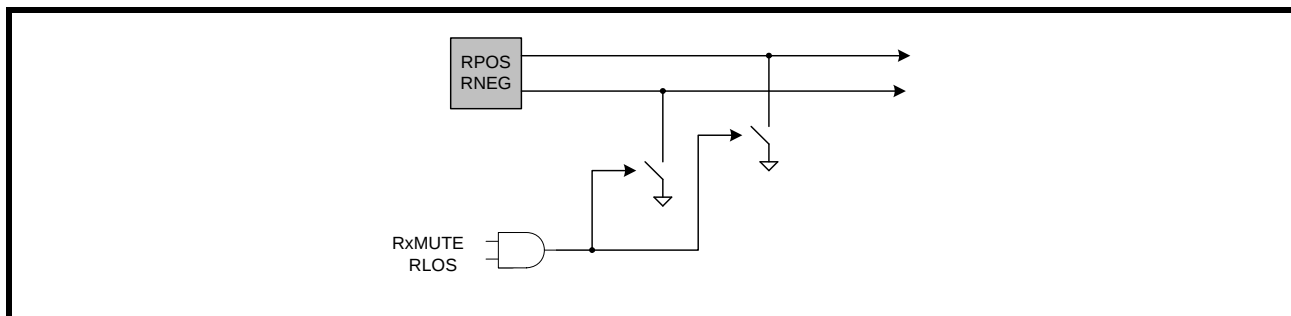
FIGURE 11. DUAL RAIL MODE WITH A FIXED REPEATING "0011" PATTERN



2.6 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull RPOS and RNEG "Low" to prevent data chattering. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in **Figure 12**.

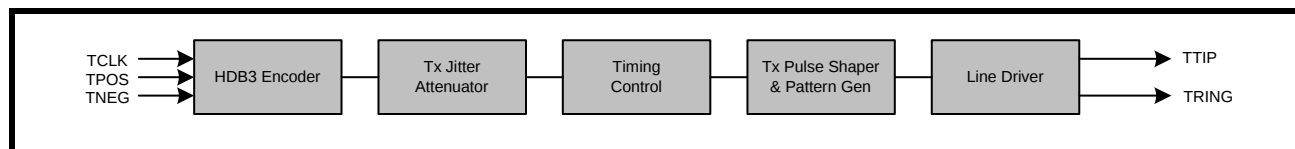
FIGURE 12. SIMPLIFIED BLOCK DIAGRAM OF THE RxMUTE FUNCTION



3.0 TRANSMIT PATH LINE INTERFACE

The transmit path of the XRT83VSH28 LIU consists of 8 independent E1 transmitters. The following section describes the complete transmit path from TCLK/TPOS/TNEG inputs to TTIP/TRING outputs. A simplified block diagram of the transmit path is shown in **Figure 13**.

FIGURE 13. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT PATH



3.1 TCLK/TPOS/TNEG Digital Inputs

In dual rail mode, TPOS and TNEG are the digital inputs for the transmit path. In single rail mode, TNEG has no function and can be left unconnected. The XRT83VSH28 can be programmed to sample the inputs on either edge of TCLK. By default, data is sampled on the falling edge of TCLK. To sample data on the rising edge of TCLK, set TCLK_E to "1" in the appropriate global register. **Figure 14** is a timing diagram of the transmit input data sampled on the falling edge of TCLK. **Figure 15** is a timing diagram of the transmit input data sampled on the rising edge of TCLK. The timing specifications are shown in **Table 5**.

FIGURE 14. TRANSMIT DATA SAMPLED ON FALLING EDGE OF TCLK

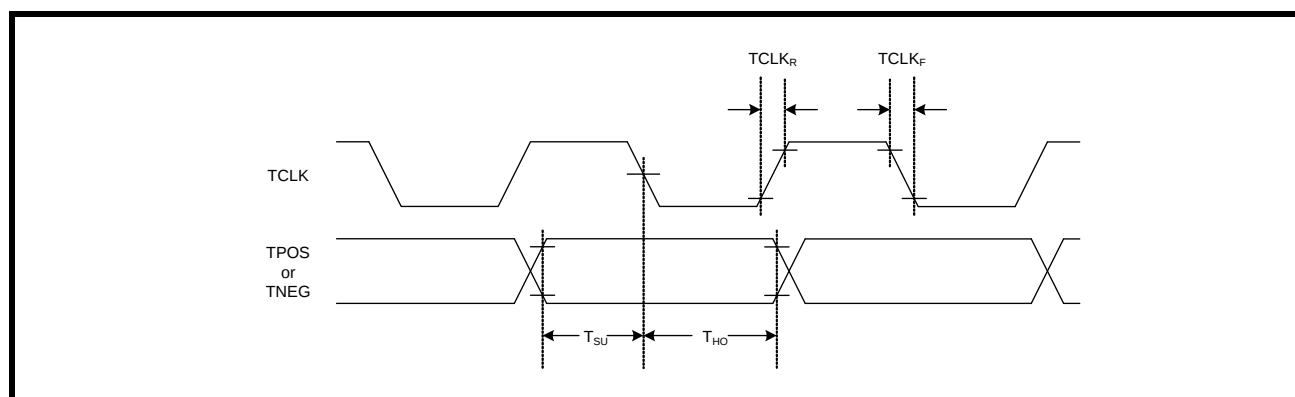


FIGURE 15. TRANSMIT DATA SAMPLED ON RISING EDGE OF TCLK

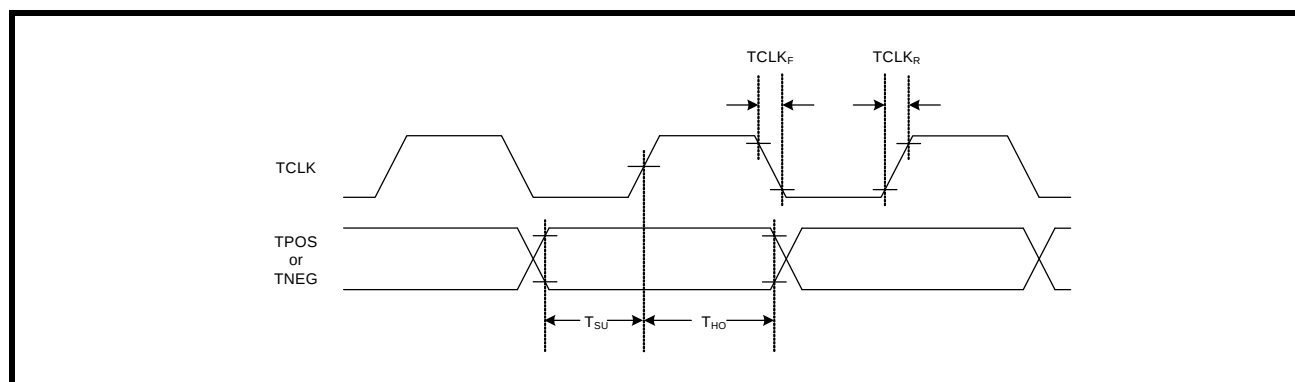


TABLE 5: TIMING SPECIFICATIONS FOR TCLK/TPOS/TNEG

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TCLK Rise Time (10% to 90%)	$TCLK_R$	-	-	40	ns
TCLK Fall Time (90% to 10%)	$TCLK_F$	-	-	40	ns

NOTE: $VDD=3.3V \pm 5\%$, $T_A=25^{\circ}C$, Unless Otherwise Specified

3.2 HDB3 Encoder

In single rail mode, the LIU can encode the TPOS input signal to AMI or HDB3 data. With HDB3 encoding selected, any sequence with four or more consecutive zeros in the input will be replaced with 000V or B00V, where "B" indicates a pulse conforming to the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 encoding is shown in [Table 6](#).

TABLE 6: EXAMPLES OF HDB3 ENCODING

	NUMBER OF PULSES BEFORE NEXT 4 ZEROS	
Input		0000
HDB3 (Case 1)	Odd	000V
HDB3 (Case 2)	Even	B00V

3.3 Transmit Jitter Attenuator

The XRT83VSH28 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The transmit path has a dedicated jitter attenuator with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady E1 output. The maximum gap width of the 8-channel LIU is shown in [Table 7](#).

TABLE 7: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

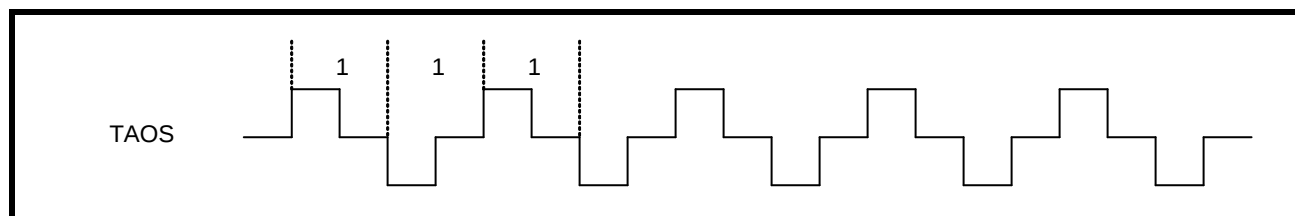
FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: If the LIU is used in a loop timing system, the receive path has a dedicated jitter attenuator. See the Receive Section of this datasheet.

3.4 TAOS (Transmit All Ones)

The XRT83VSH28 has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data present on the TPOS/TNEG inputs. For example: If a fixed "0011" pattern is present on TPOS in single rail mode and TAOS is enabled, the transmitter will output all ones. In addition, if digital or dual loopback is selected, the data on the RPOS output will be equal to the data on the TPOS input. [Figure 16](#) is a diagram showing the all ones signal at TTIP and TRING.

FIGURE 16. TAOS (TRANSMIT ALL ONES)



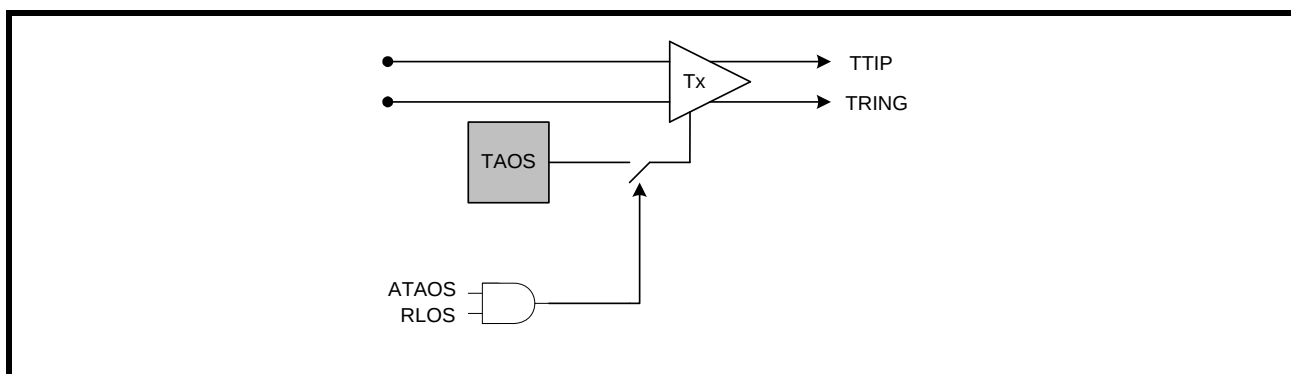
3.5 Transmit Diagnostic Features

In addition to TAOS, the XRT83VSH28 offers diagnostic features for analyzing network integrity such as ATAOS and QRSS on a per channel basis by programming the appropriate registers. These diagnostic features take priority over the digital data present on TPOS/TNEG inputs. The transmitters will send the diagnostic code to the line and will be maintained in the digital loopback if selected. When the LIU is responsible for sending diagnostic patterns, the LIU is automatically placed in the single rail mode.

3.5.1 ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in [Figure 17](#).

FIGURE 17. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION



3.5.2 QRSS Generation

The XRT83VSH28 can transmit a QRSS random sequence to a remote location from TTIP/TRING. The polynomial is shown in [Table 8](#).

TABLE 8: RANDOM BIT SEQUENCE POLYNOMIALS

RANDOM PATTERN	E1
QRSS	$2^{15} - 1$

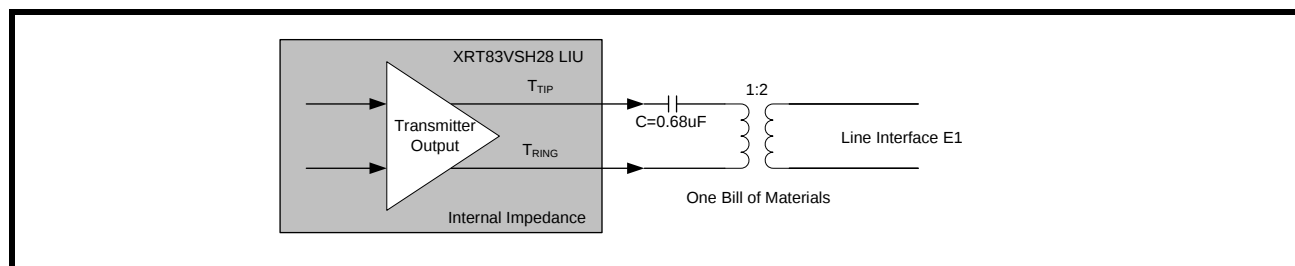
3.6 DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

3.7 Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for E1 twisted pair or E1 coaxial cable. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for all modes of operation reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of $0.68\mu\text{F}$. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "1" in the appropriate channel register. A typical transmit interface is shown in **Figure 18**.

FIGURE 18. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION



4.0 E1 APPLICATIONS

This applications section describes common E1 system considerations along with references to application notes available for reference where applicable.

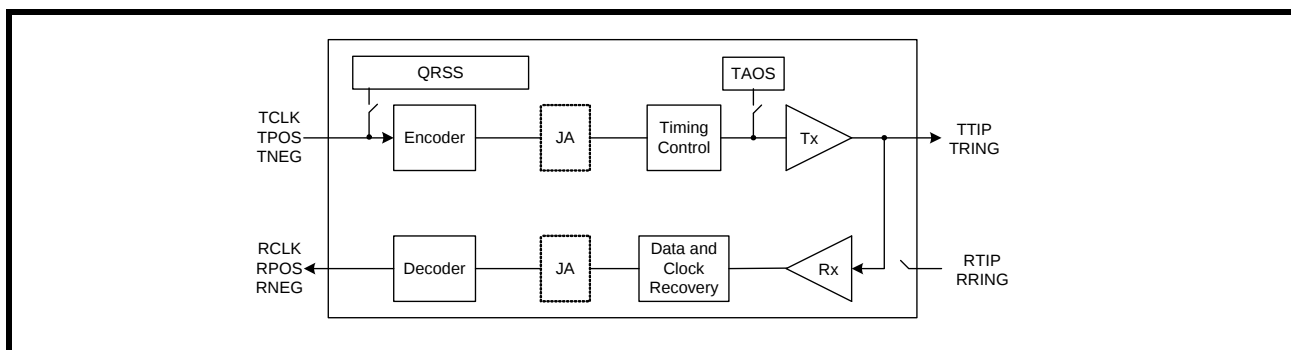
4.1 Loopback Diagnostics

The XRT83VSH28 supports several loopback modes for diagnostic testing. The following section describes the local analog loopback, remote loopback, digital loopback, and dual loopback modes.

4.1.1 Local Analog Loopback

With local analog loopback activated, the transmit output data at TTIP/TRING is internally looped back to the analog inputs at RTIP/RRING. External inputs at RTIP/RRING are ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of local analog loopback is shown in [Figure 19](#).

FIGURE 19. SIMPLIFIED BLOCK DIAGRAM OF LOCAL ANALOG LOOPBACK

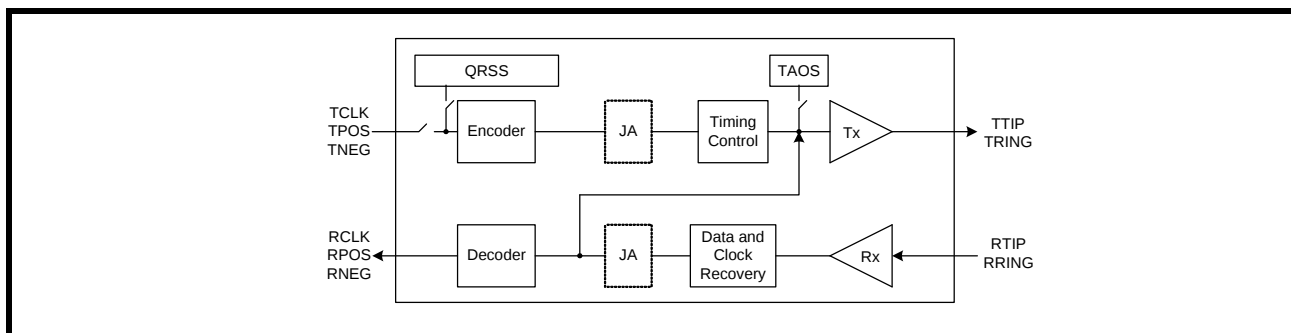


NOTE: The transmit diagnostic features such as TAOS and QRSS take priority over the transmit input data at TCLK/TPOS/TNEG.

4.1.2 Remote Loopback

With remote loopback activated, the receive input data at RTIP/RRING is internally looped back to the transmit output data at TTIP/TRING. The remote loopback includes the Receive JA (if enabled). The transmit input data at TCLK/TPOS/TNEG are ignored while valid receive output data continues to be sent to the system. A simplified block diagram of remote loopback is shown in [Figure 20](#).

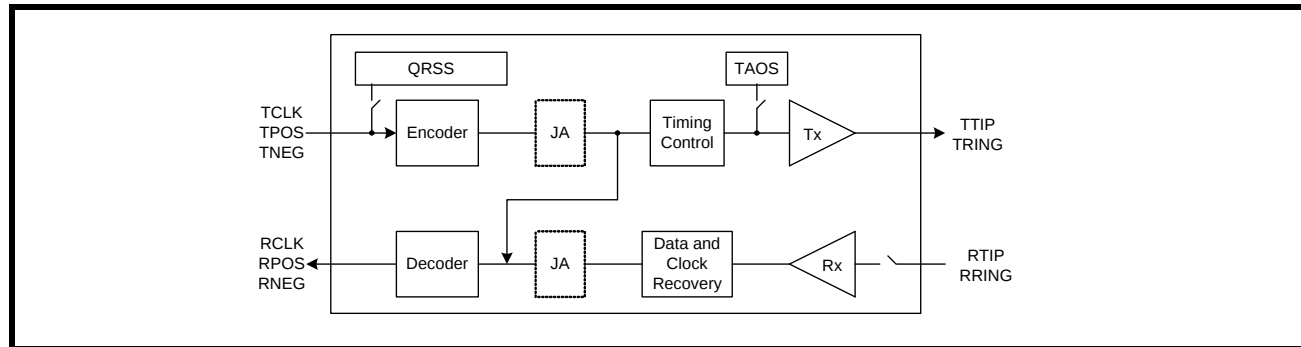
FIGURE 20. SIMPLIFIED BLOCK DIAGRAM OF REMOTE LOOPBACK



4.1.3 Digital Loopback

With digital loopback activated, the transmit input data at TCLK/TPOS/TNEG is looped back to the receive output data at RCLK/RPOS/RNEG. The digital loopback mode includes the Transmit JA (if enabled). The receive input data at RTIP/RRING is ignored while valid transmit output data continues to be sent to the line. A simplified block diagram of digital loopback is shown in [Figure 21](#).

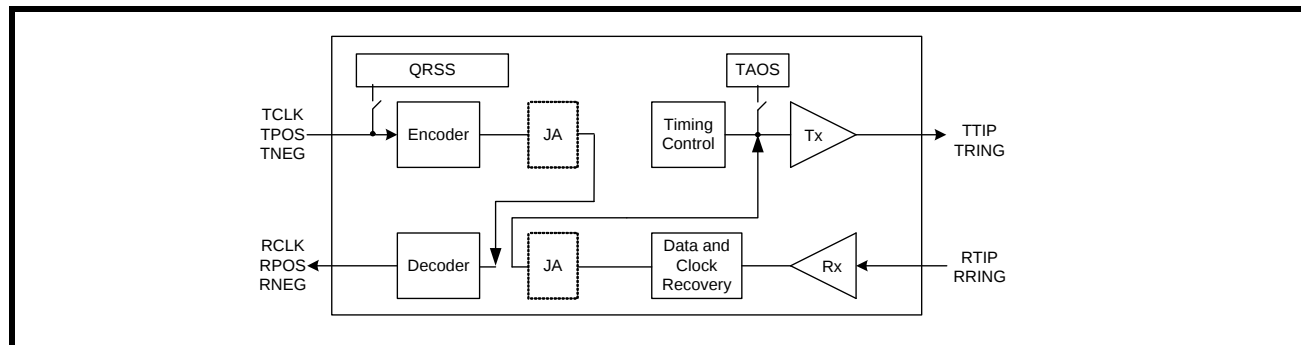
FIGURE 21. SIMPLIFIED BLOCK DIAGRAM OF DIGITAL LOOPBACK



4.1.4 Dual Loopback

With dual loopback activated, the remote loopback is combined with the digital loopback. A simplified block diagram of dual loopback is shown in [Figure 22](#).

FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF DUAL LOOPBACK



4.2 Line Card Redundancy

Telecommunication system design requires signal integrity and reliability. When an E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT83VSH28 LIU. EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

RLOS and DMO

If an RLOS or DMO condition occurs, the XRT83VSH28 reports the alarm to the individual status registers on a per channel basis. However, for redundancy applications, an RLOS or DMO alarm can be used to initiate an automatic switch to the back up card. For this application, two global pins RLOS and DMO are used to indicate that one of the 8-channels has an RLOS or DMO condition.

Typical Redundancy Schemes

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- ·N+1 One backup card for N primary cards

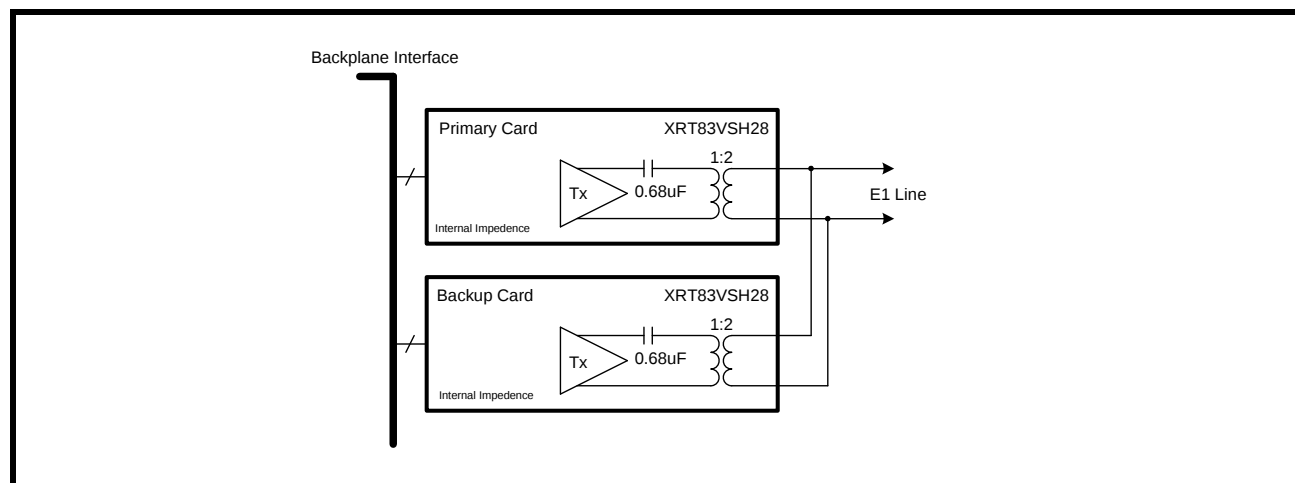
4.2.1 1:1 and 1+1 Redundancy Without Relays

The 1:1 facility protection and 1+1 line protection have one backup card for every primary card. When using 1:1 or 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. For 1+1 line protection, the receiver inputs on the backup card have the ability to monitor the line for bit errors while in high impedance. The transmit and receive sections of the LIU device are described separately.

4.2.2 Transmit Interface with 1:1 and 1+1 Redundancy

The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See [Figure 23](#). for a simplified block diagram of the transmit section for a 1:1 and 1+1 redundancy.

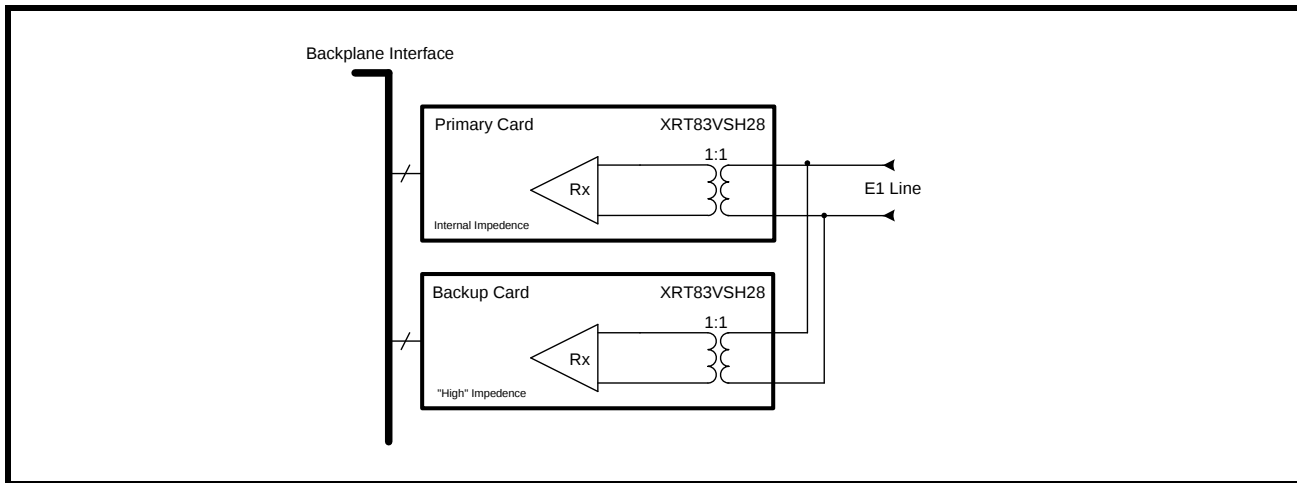
FIGURE 23. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



4.2.3 Receive Interface with 1:1 and 1+1 Redundancy

The receivers on the backup card should be programmed for "High" impedance. Since there is no external resistor in the circuit, the receivers on the backup card will not load down the line interface. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See [Figure 24](#) for a simplified block diagram of the receive section for a 1:1 redundancy scheme.

FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR 1:1 AND 1+1 REDUNDANCY



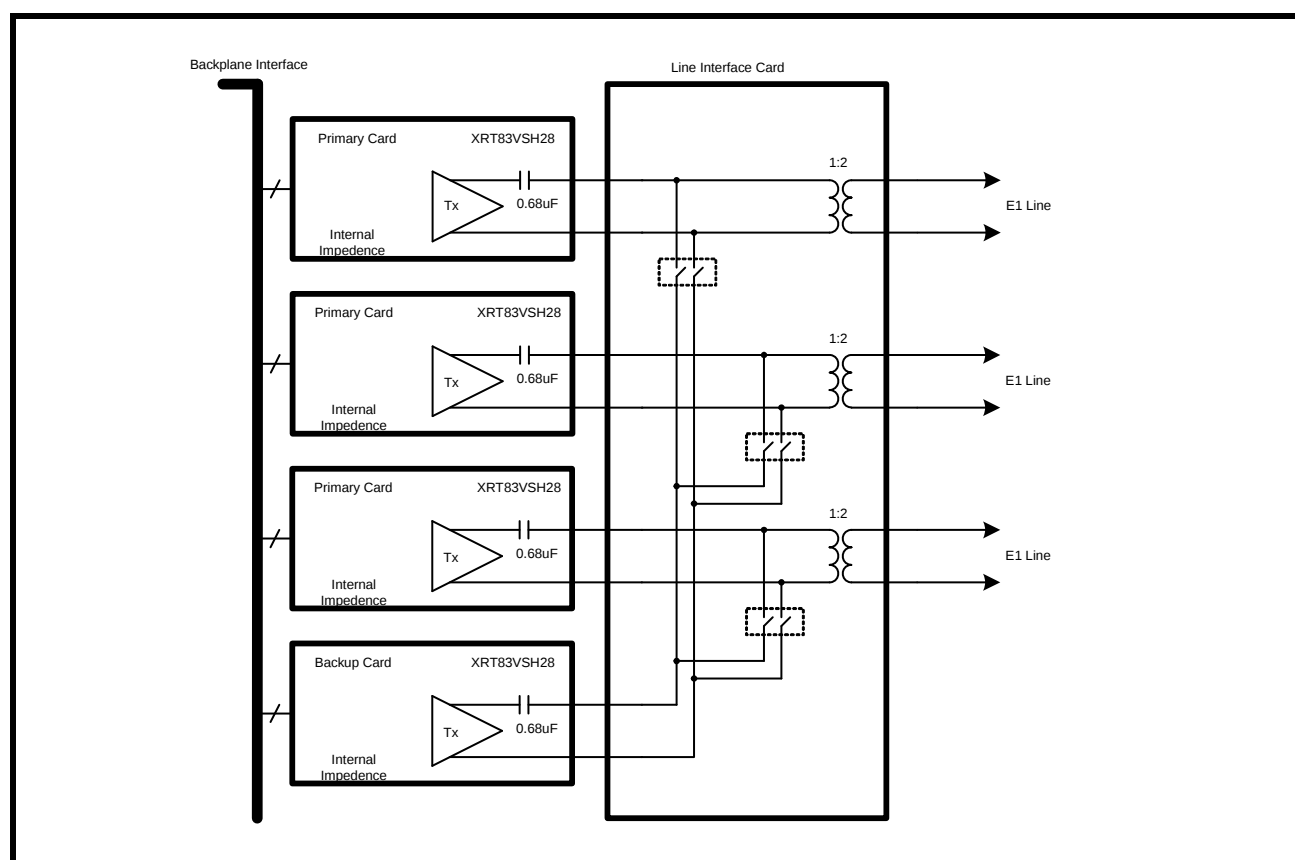
4.2.4 N+1 Redundancy Using External Relays

N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. The relays create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in internal impedance, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

4.2.5 Transmit Interface with N+1 Redundancy

For N+1 redundancy, the transmitters on all cards should be programmed for internal impedance. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays, and tri-state the transmitters on the failed primary card. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See **Figure 25** for a simplified block diagram of the transmit section for an N+1 redundancy scheme.

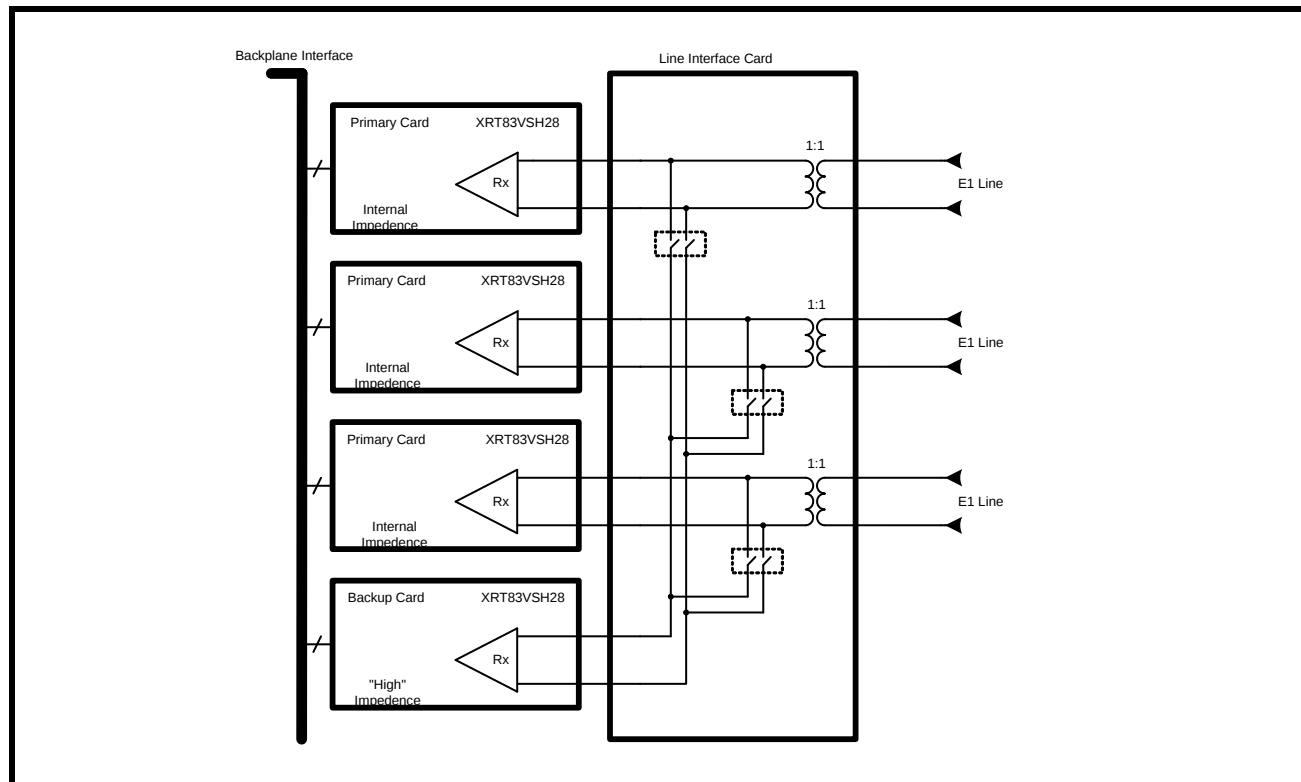
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT INTERFACE FOR N+1 REDUNDANCY



4.2.6 Receive Interface with N+1 Redundancy

For N+1 redundancy, the receivers on the primary cards should be programmed for internal impedance. The receivers on the backup card should be programmed for "High" impedance mode. To swap the primary card, set the backup card to internal impedance, then the primary card to "High" impedance. See [Figure 26](#) for a simplified block diagram of the receive section for a N+1 redundancy scheme.

FIGURE 26. SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE INTERFACE FOR N+1 REDUNDANCY



4.3 Power Failure Protection

For 1:1 or 1+1 line card redundancy in E1 applications, power failure could cause a line card to change the characteristics of the line impedance, causing a degradation in system performance. The XRT83VSH28 was designed to ensure reliability during power failures. The LIU has patented high impedance circuits that allow the receiver inputs and the transmitter outputs to be in "High" impedance when the LIU experiences a power failure or when the LIU is powered off.

NOTE: For power failure protection, a transformer must be used to couple to the line interface. See the TAN-56 application note for more details.

4.4 Overvoltage and Overcurrent Protection

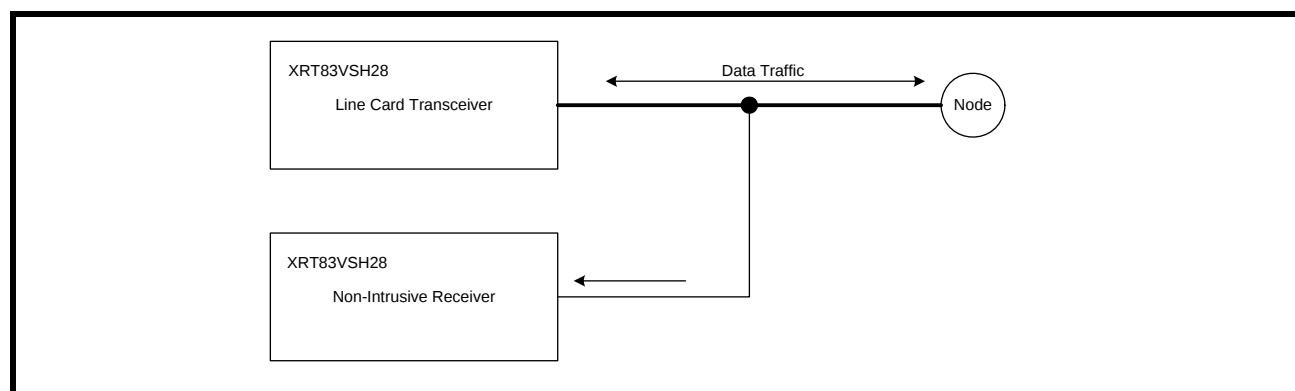
Physical layer devices such as LIUs that interface to telecommunications lines are exposed to overvoltage transients posed by environmental threats. An Overvoltage transient is a pulse of energy concentrated over a small period of time, usually under a few milliseconds. These pulses are random and exceed the operating conditions of CMOS transceiver ICs. Electronic equipment connecting to data lines are susceptible to many forms of overvoltage transients such as lightning, AC power faults and electrostatic discharge (ESD). There are three important standards when designing a telecommunications system to withstand overvoltage transients.

- UL1950 and FCC Part 68
- Telcordia (Bellcore) GR-1089
- ITU-T K.20, K.21 and K.41

4.5 Non-Intrusive Monitoring

In non-intrusive monitoring applications, the transmitters are shut off by setting TxON "Low". The receivers must be actively receiving data without interfering with the line impedance. The XRT83VSH28's internal termination ensures that the line termination meets E1 specifications for 75Ω or 120Ω while monitoring the data stream. System integrity is maintained by placing the non-intrusive receiver in "High" impedance, equivalent to that of a 1+1 redundancy application. A simplified block diagram of non-intrusive monitoring is shown in [Figure 27](#).

FIGURE 27. SIMPLIFIED BLOCK DIAGRAM OF A NON-INTRUSIVE MONITORING APPLICATION



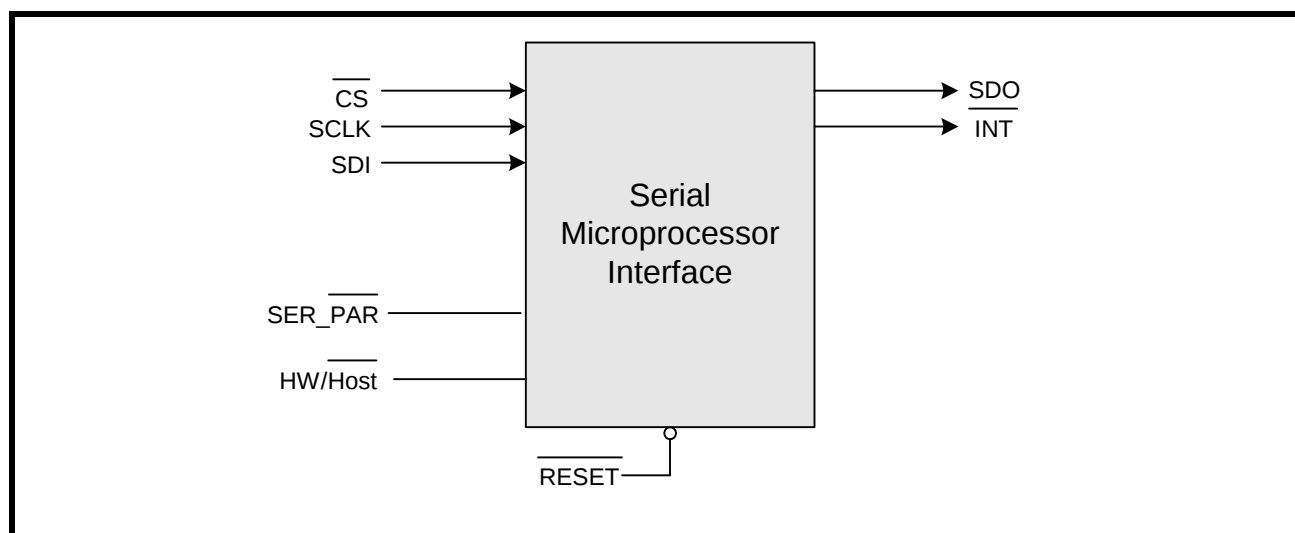
5.0 MICROPROCESSOR INTERFACE

The microprocessor interface can be accessed through a standard serial interface (BGA Package Only) or a standard parallel microprocessor interface. The SER_PAR pin is used to select between the two. By default, the chip is configured in the Parallel Microprocessor interface. For Serial communication, this pin must be pulled "High".

5.1 Serial Microprocessor Interface Block (BGA Package Only)

The serial microprocessor uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the LIU. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the LIU via an interrupt pin, and reset the LIU to its default configuration by pulling reset "Low" for more than 10 μ S. A simplified block diagram of the Serial Microprocessor is shown in **Figure 28**.

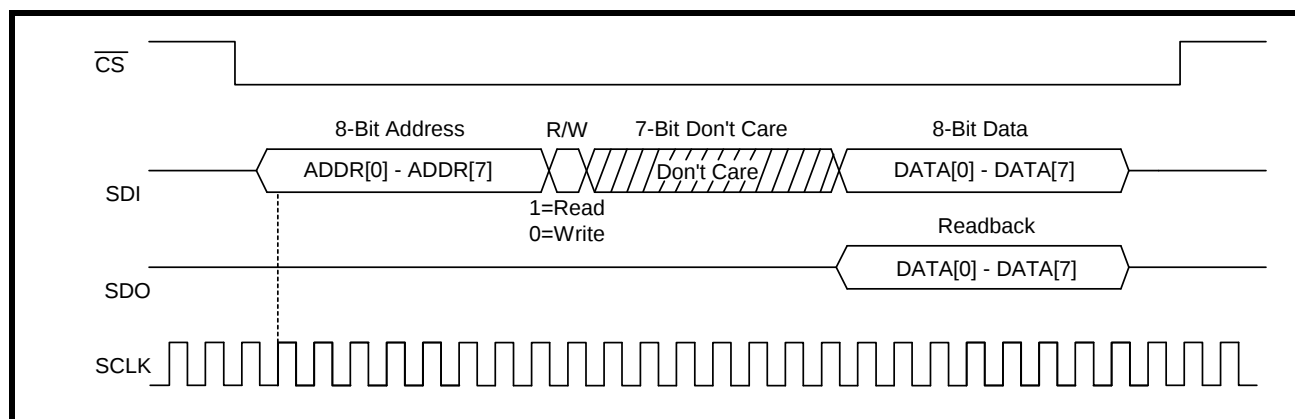
FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



5.1.1 Serial Timing Information

The serial port requires 24 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 24 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in **Figure 29**.

FIGURE 29. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: For applications without a free running SCLK, a minimum of 1 SCLK pulse must be applied when $\overline{CS}$ is "High", before pulling $\overline{CS}$ "Low".

5.1.2 24-Bit Serial Data Input Description

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the LIU LSB first. The 24 bits of serial data are described below.

5.1.3 ADDR[7:0] (SCLK1 - SCLK8)

The first 8 SCLK cycles are used to provide the address to which a Read or Write operation will occur. ADDR[0] (LSB) must be sent to the LIU first followed by ADDR[1] and so forth until all 8 address bits have been sampled by SCLK.

5.1.4 R/W (SCLK9)

The next serial bit applied to the LIU informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to "0", the microprocessor is configured for a Write operation. If the R/W bit is set to "1", the microprocessor is configured for a Read operation.

5.1.5 Dummy Bits (SCLK10 - SCLK16)

The next 7 SCLK cycles are used as dummy bits. Seven bits were chosen so that the serial interface can easily be divided into three 8-bit words to be compliant with standard serial interface devices. The state of these bits are ignored and can hold either "0" or "1" during both Read and Write operations.

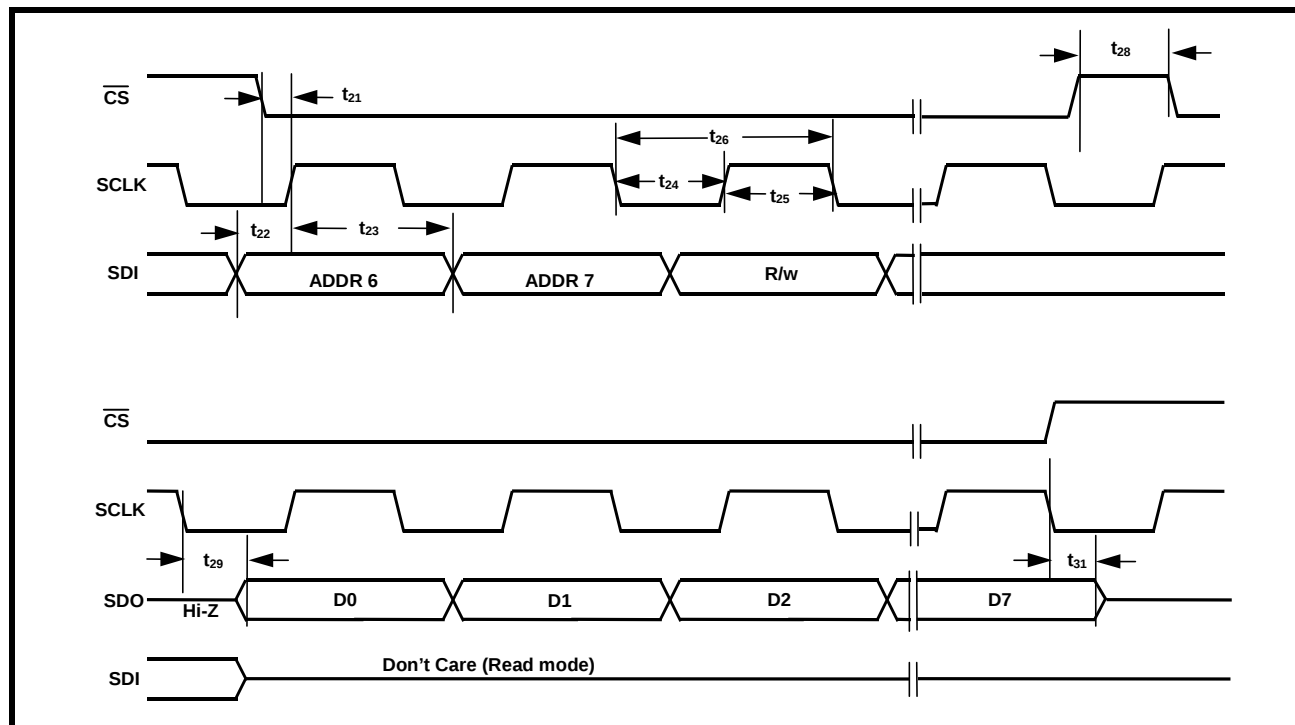
5.1.6 DATA[7:0] (SCLK17 - SCLK24)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. DATA[0] (LSB) must be sent to the LIU first followed by DATA[1] and so forth until all 8 data bits have been sampled by SCLK. Once 24 SCLK cycles have been completed, the LIU holds the data until $\overline{CS}$ is pulled "High" whereby, the serial microprocessor latches the data into the selected internal register.

5.1.7 8-Bit Serial Data Output Description

The serial data output is updated on the falling edge of SCLK17 - SCLK24 if R/W is set to "1". DATA[0] (LSB) is provided on SCLK17 to the SDO pin first followed by DATA[1] and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

FIGURE 30. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

TABLE 9: MICROPROCESSOR SERIAL INTERFACE TIMINGS ($T_A = 25^{\circ}\text{C}$, $V_{DD}=3.3\text{V}\pm 5\%$ AND LOAD = 10pF)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{\text{CS}}$ Low to Rising Edge of SCLK	5			ns
t_{22}	SDI to Rising Edge of SCLK	5			ns
t_{23}	SDI to Rising Edge of SCLK Hold Time	5			ns
t_{24}	SCLK "Low" Time	20			ns
t_{25}	SCLK "High" Time	20			ns
t_{26}	SCLK Period	40			ns
t_{28}	$\overline{\text{CS}}$ Inactive Time	40			ns
t_{29}	Falling Edge of SCLK to SDO Valid Time			5	ns
t_{31}	Rising edge of $\overline{\text{CS}}$ to High Z			5	ns

5.2 Parallel Microprocessor Interface Block

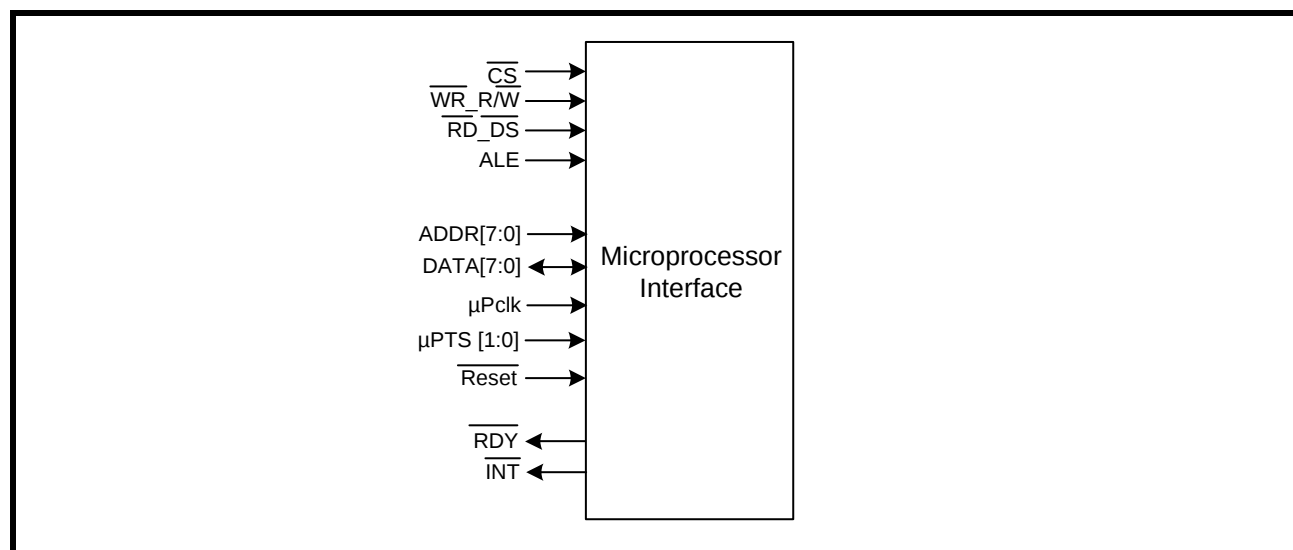
The Parallel Microprocessor Interface section supports communication between the local microprocessor (μ P) and the LIU. The XRT83VSH28 supports an Intel asynchronous interface, Motorola 68K asynchronous, and an Intel/Motorola interface. The microprocessor interface is selected by the state of the μ PTS[1:0] input pins. Selecting the microprocessor interface is shown in [Table 10](#).

TABLE 10: SELECTING THE MICROPROCESSOR INTERFACE MODE

μ PTS[1:0]	MICROPROCESSOR MODE
0h (00)	Intel 68HC11, 8051, 80C188 (Asynchronous)
1h (01)	Motorola 68K (Asynchronous)
2h (10)	Power PC 403 (Synchronous)
3h (11)	MPC8xx (Synchronous)

The XRT83VSH28 uses multipurpose pins to configure the device appropriately. The local μ P configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The microprocessor interface also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in [Figure 31](#).

FIGURE 31. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



5.3 The Microprocessor Interface Block Signals

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in [Table 11](#), [Table 12](#), and [Table 13](#). The microprocessor interface can be configured to operate in Intel mode or Motorola mode. When the microprocessor interface is operating in Intel mode, some of the control signals function in a manner required by the Intel 80xx family of microprocessors. Likewise, when the microprocessor interface is operating in Motorola mode, then these control signals function in a manner as required by the Motorola microprocessors. (For using a Motorola 68K asynchronous processor, see [Figure 33](#) and [Table 15](#)) [Table 11](#) lists and describes those microprocessor interface signals whose role is constant across the two modes. [Table 12](#) describes the role of some of these signals when the microprocessor interface is operating in the Intel mode. Likewise, [Table 13](#) describes the role of these signals when the microprocessor interface is operating in the Motorola Power PC mode.

TABLE 11: XRT83VSH28 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
μ PTS[1:0]	I	Microprocessor Interface Mode Select Input pins These three pins are used to specify the microprocessor interface mode. The relationship between the state of these three input pins, and the corresponding microprocessor mode is presented in Table 10 .
DATA[7:0]	I/O	Bi-Directional Data Bus for register "Read" or "Write" Operations.
ADDR[7:0]	I	Eight-Bit Address Bus Inputs The XRT83VSH28 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
$\overline{\text{CS}}$	I	Chip Select Input This active low signal selects the microprocessor interface of the XRT83VSH28 LIU and enables Read/Write operations with the on-chip register locations.

TABLE 12: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83VSH28 PIN NAME	INTEL EQUIVALENT PIN	TYPE	DESCRIPTION
ALE	ALE	I	Address-Latch Enable: This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of ALE.
$\overline{\text{RD}}_{\text{DS}}$	$\overline{\text{RD}}$	I	Read Signal: This active low input functions as the read signal from the local μ P. When this pin is pulled "Low" (if $\overline{\text{CS}}$ is "Low") the LIU is informed that a read operation has been requested and begins the process of the read cycle.
$\overline{\text{WR}}_{\text{R/W}}$	$\overline{\text{WR}}$	I	Write Signal: This active low input functions as the write signal from the local μ P. When this pin is pulled "Low" (if $\overline{\text{CS}}$ is "Low") the LIU is informed that a write operation has been requested and begins the process of the write cycle.
$\overline{\text{RDY}}$	$\overline{\text{RDY}}$	O	Ready Output: This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

TABLE 13: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83VSH28 PIN NAME	MOTOROLA EQUIVALENT PIN	TYPE	DESCRIPTION
ALE	AS	I	Address Strobe: This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of TS.
$\overline{\text{WR_R/W}}$	R/W	I	Read/Write: This input pin from the local μP is used to inform the LIU whether a Read or Write operation has been requested. When this pin is pulled "High", DS will initiate a read operation. When this pin is pulled "Low", DS will initiate a write operation.
$\overline{\text{RD_DS}}$	DS	I	Data Strobe: This active low input functions as the read or write signal from the local μP dependent on the state of R/W. When DS is pulled "Low" (If CS is "Low") the LIU begins the read or write operation.
$\overline{\text{RDY}}$	$\overline{\text{DTACK}}$	O	Data Transfer Acknowledge: This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

5.4 Intel Mode Programmed I/O Access (Asynchronous)

If the LIU is interfaced to an Intel type μ P, then it should be configured to operate in the Intel mode. Intel type Read and Write operations are described below.

Intel Mode Read Cycle

Whenever an Intel-type μ P wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The μ P should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. Next, the μ P should indicate that this current bus cycle is a Read operation by toggling the $\overline{RD}$ input pin "Low". This action also enables the bi-directional data bus output drivers of the LIU.
6. After the μ P toggles the Read signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this in order to inform the μ P that the data is available to be read by the μ P, and that it is ready for the next command.
7. After the μ P detects the $\overline{RDY}$ signal and has read the data, it can terminate the Read Cycle by toggling the $\overline{RD}$ input pin "High".

NOTE: $\overline{ALE}$ can be tied "High" if this signal is not available.

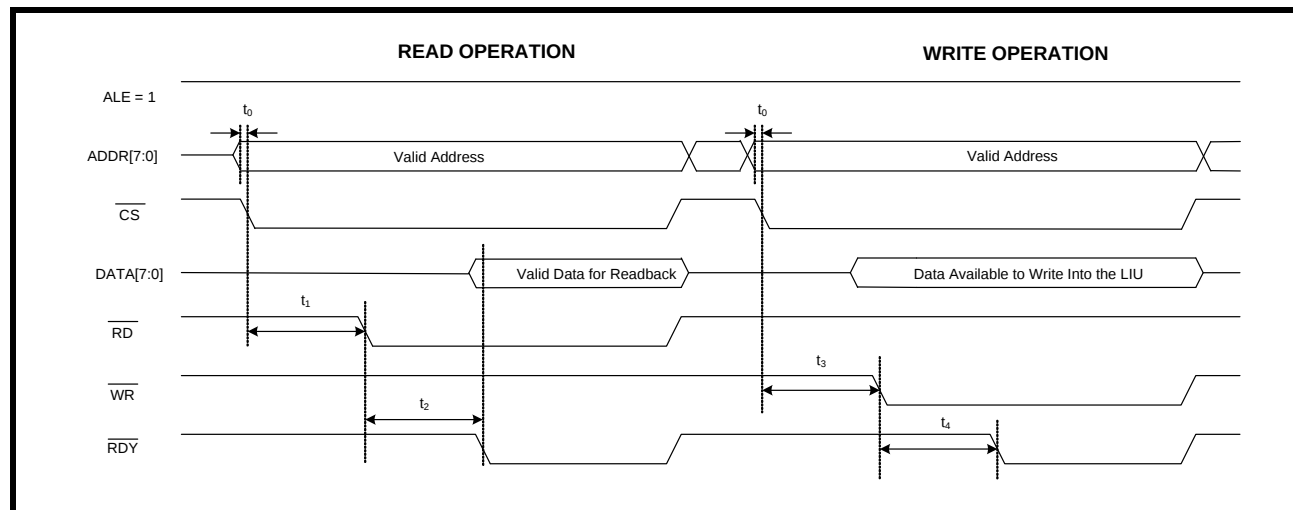
The Intel Mode Write Cycle

Whenever an Intel type μ P wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The μ P should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. The μ P should then place the byte or word that it intends to write into the target register, on the bi-directional data bus DATA[7:0].
6. Next, the μ P should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$ input pin "Low". This action also enables the bi-directional data bus input drivers of the LIU.
7. After the μ P toggles the Write signal "Low", the LIU will toggle the $\overline{RDY}$ output pin "Low". The LIU does this in order to inform the μ P that the data has been written into the internal register location, and that it is ready for the next command.

NOTE: $\overline{ALE}$ can be tied "High" if this signal is not available.

The Intel Read and Write timing diagram is shown in **Figure 32**. The timing specifications are shown in **Table 14**.

FIGURE 32. INTEL μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

TABLE 14: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	65	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{RD}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	65	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{WR}$ Pulse Width (t_4)	90	-	ns

5.5 Motorola Mode Programmed I/O Access (Asynchronous)

If the LIU is interfaced to a Motorola type μ P, it should be configured to operate in the Motorola mode. Motorola type programmed I/O Read and Write operations are described below.

Motorola Mode Read Cycle

Whenever a Motorola type μ P wishes to read the contents of a register, it should do the following.

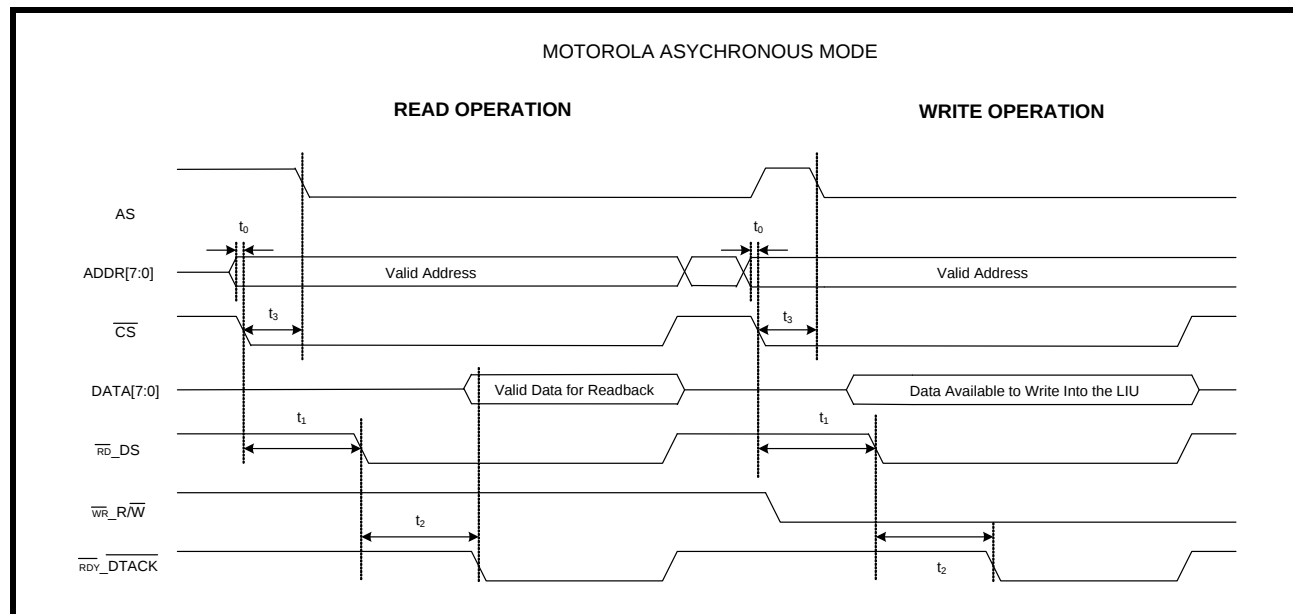
1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the CS pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. The μ P should then toggle the AS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the μ P should indicate that this current bus cycle is a Read operation by pulling the R/W input pin "High".
5. Toggle the DS input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the μ P toggles the DS signal "Low", the LIU will toggle the $\overline{\text{DTACK}}$ output pin "Low". The LIU does this in order to inform the μ P that the data is available to be read by the μ P, and that it is ready for the next command.
7. After the μ P detects the $\overline{\text{DTACK}}$ signal and has read the data, it can terminate the Read Cycle by toggling the DS input pin "High".

Motorola Mode Write Cycle

Whenever a motorola type μ P wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the μ P is placing this address value on the address bus, the address decoding circuitry should assert the CS pin of the LIU, by toggling it "Low". This action enables further communication between the μ P and the LIU microprocessor interface block.
3. The μ P should then toggle the AS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the μ P should indicate that this current bus cycle is a Write operation by pulling the R/W input pin "Low".
5. Toggle the DS input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the μ P toggles the DS signal "Low", the LIU will toggle the $\overline{\text{DTACK}}$ output pin "Low". The LIU does this in order to inform the μ P that the data has been written into the internal register location, and that it is ready for the next command.
7. After the μ P detects the $\overline{\text{DTACK}}$ signal and has read the data, it can terminate the Read Cycle by toggling the DS input pin "High".

The Motorola Read and Write timing diagram is shown in **Figure 33**. The timing specifications are shown in **Table 15**.

FIGURE 33. MOTOROLA 68K μ P INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

TABLE 15: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD_DS}$) Assert	65	-	ns
t_2	DS Assert to $\overline{DTACK}$ Assert	-	90	ns
NA	DS Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE) Falling Edge	0	-	ns

5.6 PowerPC 403 Synchronous Mode:

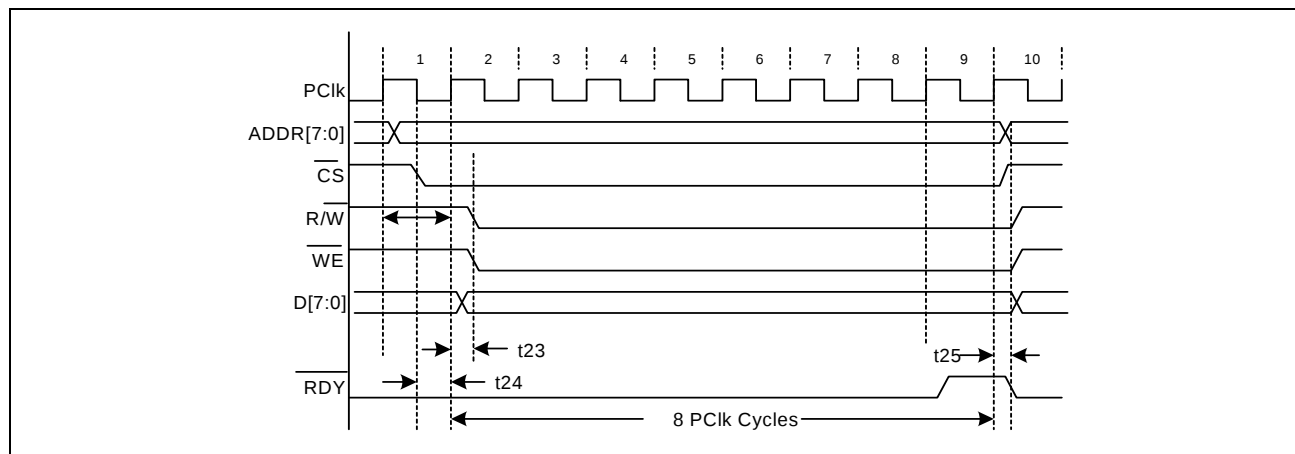
In PowerPC mode the active signals are ADDR[7:0], DATA[7:0], $\overline{CS}$, $\overline{R/W}$ (Intel WR), $\overline{WE}$ (Intel RD), RDY and PCLK. In this mode all input signals are sampled by the PCLK. For all inputs minimum setup time is 4ns and minimum hold time is 3ns. Maximum PCLK frequency is 50 MHz.

A READ cycle starts with $\overline{R/W}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

Operation with wait-states is possible, provided the wait is longer than the minimum cycle time. Use of RDY is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to the READ operation except that the cycle starts with $\overline{R/W}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{WE}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WE}$ is asserted. $\overline{WE}$ should remain asserted until RDY is asserted by the device. Following RDY assertion $\overline{WE}$ and $\overline{CS}$ may be de-asserted.

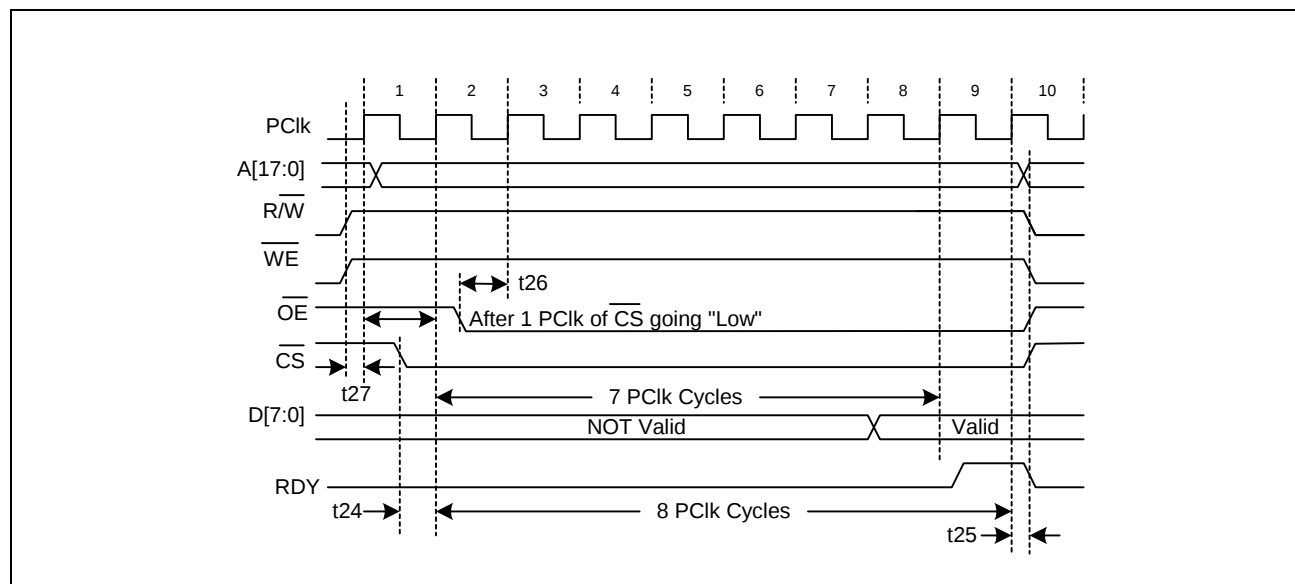
FIGURE 34. POWERPC 403 MODE TIMING - WRITE OPERATION



Note: The value for t25 through t38 can be found in [Table 16](#).

Table 16 Power PC403 Mode Timing - Write Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V±5%, unless otherwise specified					
Timing	Description	Min.	Typ.	Max.	Units
t23	$\overline{R/W}$ "Low" to rising edge of PCLK set-up time (Write Operation)	5	-	-	ns
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to $\overline{RDY}$ "Low" delay	4	-	-	ns

FIGURE 35. POWERPC 403 MODE TIMING - READ OPERATION


Note: The value for t25 through t38 can be found in [Table 17](#).

Table 17 Power PC403 Mode Timing - Read Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V±5%, unless otherwise specified					
Timing	Description	Min.	Typ.	Max.	Units
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "Low" delay	4	-	-	ns
t26	$\overline{OE}$ "Low" to rising edge of PCLK	5	-	-	ns
t27	$\overline{R/W}$ "High" to rising edge of PCLK set-up time	5	-	-	ns

5.7 MICROPROCESSOR INTERFACE TIMING - MCP860 SYNCHRONOUS MODE

In MPC86x mode the active signals are ADDR[17:0], DATA[7:0], $\overline{\text{CS}}$, $\overline{\text{RW}}$, $\overline{\text{WE}}$, $\overline{\text{DBEN}}$, $\overline{\text{TA}}$ and PCLK. In this mode all input signals are sampled by the PCLK. For all inputs minimum setup time is 4ns and minimum hold time is 3ns. Maximum PCLK frequency is 70 MHz.

A READ cycle starts with $\overline{\text{RW}}$ being 'HIGH' and assertion of $\overline{\text{CS}}$, address is assumed to be stable at this time since $\overline{\text{CS}}$ is usually derived from the decoding the address bus.

Following falling edge of $\overline{\text{CS}}$, $\overline{\text{DBEN}}$ is asserted for the READ operation. $\overline{\text{DBEN}}$ must remain asserted until $\overline{\text{TA}}$ is asserted by the XRT86SH221 device, which indicates DATA from the addressed location is available on the data bus. $\overline{\text{DBEN}}$ and $\overline{\text{CS}}$ can be de-asserted when the data has been read by the processor. $\overline{\text{WE}}$ should be high during the entire read cycle.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{\text{TA}}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{\text{RW}}$ being 'LOW', followed by $\overline{\text{CS}}$ assertion further followed by assertion of $\overline{\text{WE}}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{\text{WE}}$ is asserted. $\overline{\text{WE}}$ should remain asserted until $\overline{\text{TA}}$ is asserted by the XRT86SH221 device. Following assertion of $\overline{\text{TA}}$ $\overline{\text{WE}}$ and $\overline{\text{CS}}$ may be de-asserted. $\overline{\text{DBEN}}$ should be high during the entire write cycle.

FIGURE 36. MPC86X MODE TIMING - WRITE OPERATION

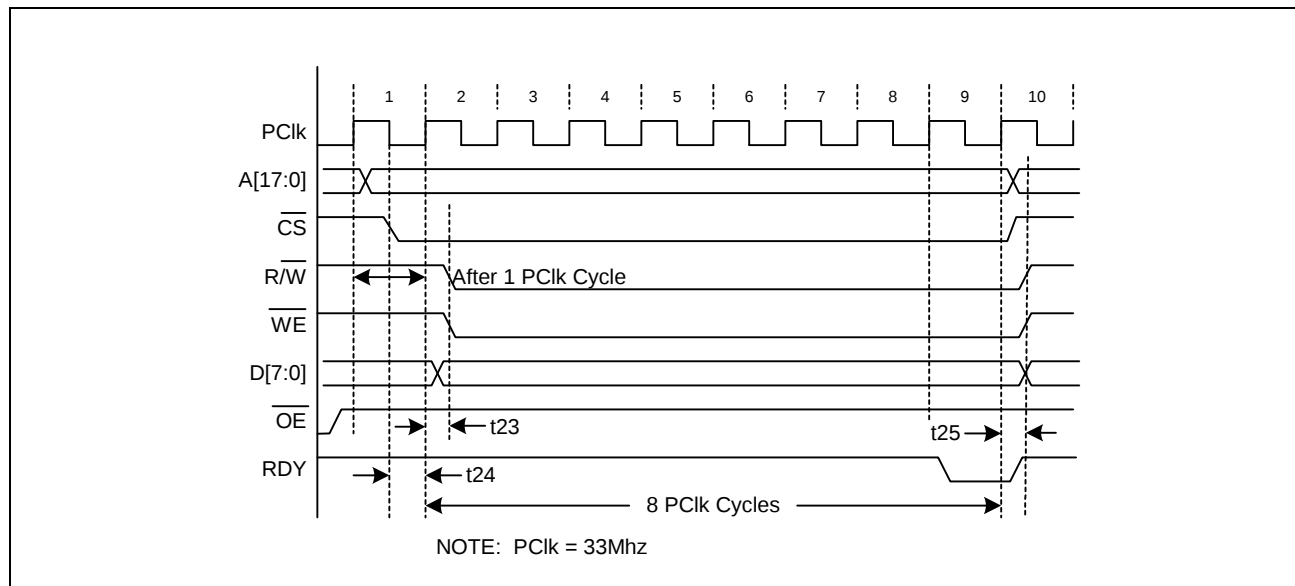


Table 18 MPC86X Mode Timing - Write Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V±5%, unless otherwise specified					
Timing	Description	Min.	Typ.	Max.	Units
t23	$\overline{\text{R/W}}$ "Low" to rising edge of PCLK set-up time (Write Operation)	5	-	-	ns
t24	$\overline{\text{CS}}$ "Low" to rising edge of PCLK set-up time	4	-	-	ns
t25	Rising edge of PCLK to RDY "High" delay	4	-	-	ns

FIGURE 37. MPC86X MODE TIMING - READ OPERATION

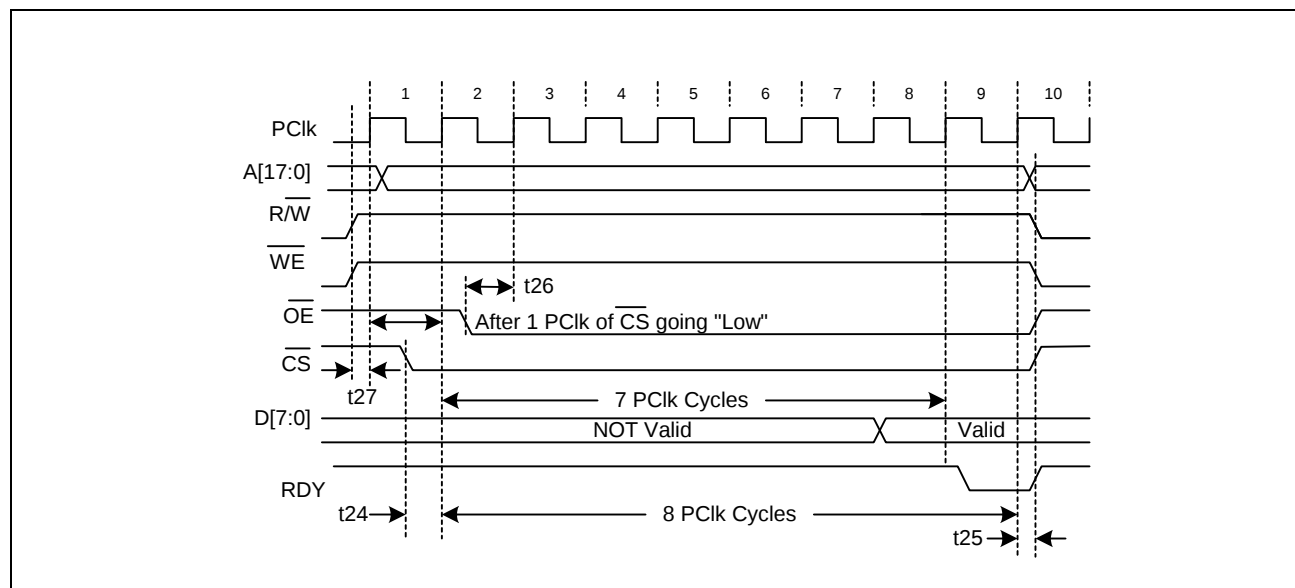


Table 19 MPC86X Timing Information - Read Operation

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V±5%, unless otherwise specified					
Timing	Description	Min.	Typ.	Max.	Units
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "High" delay	4	-	-	ns
t26	$\overline{OE}$ "Low" to rising edge of PCLK	5	-	-	ns
t27	$\overline{R/W}$ "High" to rising edge of PCLK set-up time	5	-	-	ns

TABLE 20: MICROPROCESSOR REGISTER ADDRESS (ADDR[7:0])

REGISTER NUMBER	ADDRESS (HEX)	FUNCTION
0 - 15	0x00 - 0x0F	Channel 0 Control Registers
16 - 31	0x10 - 0x1F	Channel 1 Control Registers
32 - 47	0x20 - 0x2F	Channel 2 Control Registers
48 - 63	0x30 - 0x3F	Channel 3 Control Registers
64 - 79	0x40 - 0x4F	Channel 4 Control Registers
80 - 95	0x50 - 0x5F	Channel 5 Control Registers
96 - 111	0x60 - 0x6F	Channel 6 Control Registers
112 - 127	0x70 - 0x7F	Channel 7 Control Registers
128 - 142	0x80 - 0x8E	Global Control Registers Applied to All 8 Channels
143 - 253	0x8F - 0xFD	R/W Registers Reserved for Testing (Except 0xC0h)
254	0xFE	Device "ID"
255	0xFF	Device "Revision ID"

TABLE 21: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Channel 0 Control Registers (0x00 - 0x0F)										
0	0x00	R/W	QRSS/PRBS	PRBS_Rx/Tx	RxON	EQC4	EQC3	EQC2	EQC1	EQC0
1	0x01	R/W	RxTSEL	TxTSEL	Reserved	TERSEL	JASEL1	JASEL0	JABW	FIFOS
2	0x02	R/W	INVQRSS	TxTEST2	TxTEST1	TxTEST0	TxON	LOOP2	LOOP1	LOOP0
3	0x03	R/W	Reserved	Reserved	CODES	RxRES1	RxRES0	INSBPV	INSBER	Reserved
4	0x04	R/W	Reserved	DMOIE	FLSIE	LCV/OFIE	Reserved	AISIE	RLOSIE	QRPDIE
5	0x05	RO	Reserved	DMO	FLS	LCV/OF	Reserved	AIS	RLOS	QRPD
6	0x06	RUR	Reserved	DMOIS	FLSIS	LCV/OFIS	Reserved	AISIS	RLOIS	QRPDIS
7	0x07	RO	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
8	0x08	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9	0x09	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10	0x0A	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	0x0B	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
12	0x0C	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
13	0x0D	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
14	0x0E	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
15	0x0F	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Channel (1 - 7) Control Registers (0x10 - 0x7F) See Channel 0										

TABLE 21: MICROPROCESSOR REGISTER CHANNEL DESCRIPTION

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Global Control Registers for All 8 Channels										
128	0x80	R/W	SR/DR	ATAOS	RCLKE	TCLKE	DATAP	Reserved	GIE	SRESET
129	0x81	R/W	OVFLO/LCV	Reserved	Reserved	Reserved	Reserved	RxMUTE	EXLOS	ICT
130	0x82	R/W	TxONCNTL	TERCNTL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
131	0x83	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
140	0x8C	R/W	Reserved	Reserved	Reserved	Reserved	LCVCH3	LCVCH2	LCVCH1	LCVCH0
141	0x8D	R/W	Reserved	Reserved	Reserved	allRST	allUPDATE	BYTEsel	chUPDATE	chRST
142	0x8E	RO	LCVCNT7	LCVCNT6	LCVCNT5	LCVCNT4	LCVCNT3	LCVCNT2	LCVCNT1	LCVCNT0
R/W Registers Reserved for Testing (0x8F - 0xFD)										
254	0xFE	RO	Device "ID"							
255	0xFF	RO	Device "Revision ID"							

5.8 Channel Control Registers

TABLE 22: MICROPROCESSOR REGISTER 0x00H BIT DESCRIPTION

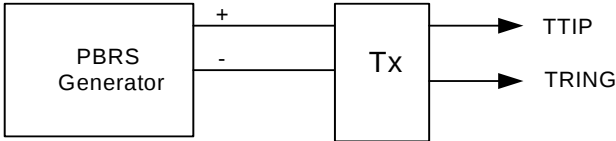
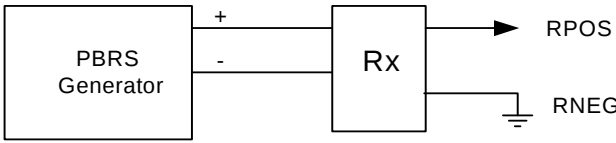
CHANNEL 0-7 (0x00H-0x70H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	QRSS/ PRBS	QRSS/PRBS Select Bits These bits are used to select between QRSS and PRBS. 1 = QRSS 0 = PRBS	R/W	0
D6	PRBS_Rx/ Tx	PRBS Receive/Transmit Select: This bit is used to select where the output of the PRBS Generator is directed if PRBS generation is enabled. 0 = Normal Operation - PRBS generator is output on TTIP and TRING if PRBS generation is enabled. 1 = PRBS Generator is output on RPOS (based on TCLK); RNEG is internally grounded, if PRBS generation is enabled. Bit 6 = "0"  Bit 6 = "1"  NOTE: If PRBS generation is disabled, user should set this bit to '0' for normal operation.	R/W	0
D5	RxON	Receiver ON/OFF Upon power up, the receiver is powered OFF. RxON is used to turn the receiver ON or OFF if the hardware pin RxON is pulled "High". If the hardware pin is pulled "Low", all receivers are turned off. 0 = Receiver is Powered Off 1 = Receiver is Powered On	R/W	0
D4	EQC4	Cable Length Setting The equalizer control bits are shown in Table 23 below.	R/W	0
D3	EQC3			0
D2	EQC2			0
D1	EQC1			0
D0	EQC0			0

TABLE 23: CABLE LENGTH SETTING

EQC[4:0]	E1 MODE/RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
0x1Ch	E1 Short Haul/15dB	ITU G.703	75Ω Coax	HDB3
0x1Dh	E1 Short Haul/15dB	ITU G.703	120Ω TP	HDB3

TABLE 24: MICROPROCESSOR REGISTER 0x01H BIT DESCRIPTION

CHANNEL 0-7 (0x01H-0x71H)																			
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)															
D7	RxTSEL	Receive Termination Select Upon power up, the receiver is in "High" impedance. RxTSEL is used to switch between the internal termination and "High" impedance. 0 = "High" Impedance 1 = Internal Termination	R/W	0															
D6	TxTSEL	Transmit Termination Select Upon power up, the transmitter is in "High" impedance. TxTSEL is used to switch between the internal termination and "High" impedance. 0 = "High" Impedance 1 = Internal Termination	R/W	0															
D5	Reserved	Reserved	R/W	0															
D4	TERSEL	Receive Line Impedance Select TERSEL is used to select the line impedance for E1. "0" = 75Ω "1" = 120Ω	R/W	0															
D3 D2	JASEL1 JASEL0	Jitter Attenuator Select JASEL[1:0] are used to select the jitter attenuator in the transmit or receive path. By default, the jitter attenuator is disabled. <table><tr><th>JASEL1</th><th>JASEL0</th><th>JA PATH</th></tr><tr><td>0</td><td>0</td><td>Disabled</td></tr><tr><td>0</td><td>1</td><td>Transmit Path</td></tr><tr><td>1</td><td>0</td><td>Receive Path</td></tr><tr><td>1</td><td>1</td><td>Receive Path</td></tr></table>	JASEL1	JASEL0	JA PATH	0	0	Disabled	0	1	Transmit Path	1	0	Receive Path	1	1	Receive Path	R/W	0
JASEL1	JASEL0	JA PATH																	
0	0	Disabled																	
0	1	Transmit Path																	
1	0	Receive Path																	
1	1	Receive Path																	

TABLE 24: MICROPROCESSOR REGISTER 0x01H BIT DESCRIPTION

CHANNEL 0-7 (0x01H-0x71H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D1	JABW	Jitter Bandwidth The jitter bandwidth is a global setting that is applied to both the receiver and transmitter jitter attenuator. 0 = 10Hz 1 = 1.5Hz	R/W	0
D0	FIFOS	FIFO Depth Select The FIFO depth select is used to configure the part for a 32-bit or 64-bit FIFO (within the jitter attenuator blocks). The delay of the FIFO is equal to ½ the FIFO depth. This is a global setting that is applied to both the receiver and transmitter FIFO. 0 = 32-Bit 1 = 64-Bit	R/W	0

TABLE 25: MICROPROCESSOR REGISTER 0x02H BIT DESCRIPTION

CHANNEL 0-7 (0x02H-0x72H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	INVQRSS	QRSS inversion INVQRSS is used to invert the transmit QRSS pattern set by the TxTEST[2:0] bits. By default, INVQRSS is disabled and the QRSS will be transmitted with normal polarity. 0 = Disabled 1 = Enabled	R/W	0
D6 D5 D4	TxTEST2 TxTEST1 TxTEST0	Test Code Pattern TxTEST[2:0] are used to select a diagnostic test pattern to the line (transmit outputs). 0XX = No Pattern 100 = Tx QRSS 101 = Tx TAOS 110 = Reserved 111 = Reserved	R/W	0 0 0

TABLE 25: MICROPROCESSOR REGISTER 0x02H BIT DESCRIPTION

CHANNEL 0-7 (0x02H-0x72H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D3	TxOn	Transmit ON/OFF Upon power up, the transmitters are powered off. This bit is used to turn the transmitter for this channel On or Off. 0 = Transmitter is Powered OFF 1 = Transmitter is Powered ON	R/W	0
D2 D1 D0	LOOP2 LOOP1 LOOP0	Loopback Diagnostic Select LOOP[2:0] are used to select the loopback mode. 0XX = No Loopback 100 = Dual Loopback 101 = Analog Loopback 110 = Remote Loopback 111 = Digital Loopback	R/W	0 0 0

TABLE 26: MICROPROCESSOR REGISTER 0x03H BIT DESCRIPTION

CHANNEL 0-7 (0x03H-0x73H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D[7:6]	Reserved	This Register Bit is Not Used.		
D5	CODES	Encoding/Decoding Select (Single Rail Mode Only) 0 = HDB3 1 = AMI Coding	R/W	0
D4 D3	RxRES1 RxRES0	Receive External Fixed Resistor RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss. 00 = None 01 = 320Ω 10 = 280Ω 11 = 190Ω	R/W	0 0
D2	INSBPV	Insert Bipolar Violation When this bit transitions from a "0" to a "1", a bipolar violation will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0

TABLE 26: MICROPROCESSOR REGISTER 0x03H BIT DESCRIPTION

CHANNEL 0-7 (0x03H-0x73H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D1	INSBER	Insert Bit Error When this bit transitions from a "0" to a "1", a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a "0" to this bit before writing a "1".	R/W	0
D0	Reserved			

TABLE 27: MICROPROCESSOR REGISTER 0x04H BIT DESCRIPTION

CHANNEL 0-7(0x04H-0x74H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used.		
D6	DMOIE	Digital Monitor Output Interrupt Enable 0 = Masks the DMO function 1 = Enables Interrupt Generation	R/W	0
D5	FLSIE	FIFO Limit Status Interrupt Enable 0 = Masks the FLS function 1 = Enables Interrupt Generation	R/W	0
D4	LCV/OFIE	Line Code Violation / Counter Overflow Interrupt Enable 0 = Masks the LCV/OF function 1 = Enables Interrupt Generation	R/W	0
D3	Reserved	This Register Bit is Not Used.		
D2	AISIE	Alarm Indication Signal Interrupt Enable 0 = Masks the AIS function 1 = Enables Interrupt Generation	R/W	0
D1	RLOSIE	Receiver Loss of Signal Interrupt Enable 0 = Masks the RLOS function 1 = Enables Interrupt Generation	R/W	0
D0	QRPDIE	Quasi Random Signal Source Interrupt Enable 0 = Masks the QRPD function 1 = Enables Interrupt Generation	R/W	0

NOTE: The GIE bit in the global register 0xE0h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 28: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

CHANNEL 0-7 (0X05H-0X75H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used.		
D6	DMO	Digital Monitor Output The digital monitor output is always active regardless if the interrupt generation is disabled. This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = Transmit output driver has failures	RO	0
D5	FLS	FIFO Limit Status The FIFO limit status is always active regardless if the interrupt generation is disabled. This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = RD/WR FIFO pointers are within ± 3 -Bits	RO	0
D4	LCV/OF	Line Code Violation / Counter Overflow This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0x81h is set to a "1", this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV/OFIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0x80h. 0 = No Alarm 1 = A line code violation, bipolar violation, or excessive zeros has occurred	RO	0
D3	Reserved	This Register Bit is Not Used.		
D2	AIS	Alarm Indication Signal The alarm indication signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = An all ones signal is detected	RO	0

NOTE: The GIE bit in the global register 0xE0h must be set to "1" in addition to the individual register bits to enable the interrupt pin.

TABLE 28: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

CHANNEL 0-7 (0X05H-0X75H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D1	RLOS	Receiver Loss of Signal The receiver loss of signal detection is always active regardless if the interrupt generation is disabled. This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = An RLOS condition is present	RO	0
D0	QRPD	Quasi Random Pattern Detection The quasi random pattern detection is always active regardless if the interrupt generation is disabled. This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set to "1" in the channel register 0x04h and GIE is set to "1" in the global register 0xE0h. 0 = No Alarm 1 = A QRP is detected	RO	0

TABLE 29: MICROPROCESSOR REGISTER 0X06H BIT DESCRIPTION

CHANNEL 0-7 (0X06H-0X76H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used.		
D6	DMOIS	Digital Monitor Output Status 0 = No change 1 = Change in status occurred	RUR	0
D5	FLSIS	FIFO Limit Status 0 = No change 1 = Change in status occurred	RUR	0
D4	LCV/OFIS	Line Code Violation / Overflow Status 0 = No change 1 = Change in status occurred	RUR	0
D3	Reserved	This Register Bit is Not Used.		
D2	AISIS	Alarm Indication Signal Status 0 = No change 1 = Change in status occurred	RUR	0

TABLE 29: MICROPROCESSOR REGISTER 0x06H BIT DESCRIPTION

CHANNEL 0-7 (0x06H-0x76H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D1	RLOSIS	Receiver Loss of Signal Status 0 = No change 1 = Change in status occurred	RUR	0
D0	QRPDIS	Quasi Random Pattern Detection Status 0 = No change 1 = Change in status occurred	RUR	0

NOTE: Any change in status will generate an interrupt (if enabled in channel register 0x04h and GIE is set to "1" in the global register 0x80h). The status registers are reset upon read (RUR).

5.9 Global Control Registers

TABLE 30: MICROPROCESSOR REGISTER 0x80H, BIT DESCRIPTION

REGISTER ADDRESS 0x80H	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #				
D7	SR/DR	Single-rail/Dual-rail Select: Writing a "1" to this bit configures all 4channels in the XRT83VSH28 to operate in the Single-rail mode. Writing a "0" configures the XRT83VSH28 to operate in Dual-rail mode.	R/W	0
D6	ATAOS	Automatic Transmit All Ones Upon RLOS: Writing a "1" to this bit enables the automatic transmission of All "Ones" data to the line for the channel that detects an RLOS condition. Writing a "0" disables this feature.	R/W	0
D5	RCLKE	Receive Clock Edge: Writing a "1" to this bit selects receive output data of all channels to be updated on the negative edge of RCLK. Writing a "0" selects data to be updated on the positive edge of RCLK.	R/W	0
D4	TCLKE	Transmit Clock Edge: Writing a "0" to this bit selects transmit data at TPOS_n/TDATA_n and TNEG_n/CODES_n of all channels to be sampled on the falling edge of TCLK_n. Writing a "1" selects the rising edge of the TCLK_n for sampling.	R/W	0
D3	DATAP	DATA Polarity: Writing a "0" to this bit selects transmit input and receive output data of all channels to be active "High". Writing a "1" selects an active "Low" state.	R/W	0
D2	Reserved			0
D1	GIE	Global Interrupt Enable: Writing a "1" to this bit globally enables interrupt generation for all channels. Writing a "0" disables interrupt generation.	R/W	0
D0	SRESET	Software Reset μP Registers: Writing a "1" to this bit longer than 10 μ s initiates a device reset through the microprocessor interface. All internal circuits are placed in the reset state with this bit set to a "1" except the microprocessor register bits.	R/W	0

TABLE 31: MICROPROCESSOR REGISTER 0x81H, BIT DESCRIPTION

REGISTER ADDRESS 0x81H	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #				
D7	Reserved		R/W	0
D6	Reserved		R/W	0
D5	Reserved		R/W	0
D4	Reserved		R/W	0
D3	Reserved		R/W	0
D2	RXMUTE	Receive Output Mute: Writing a “1” to this bit, mutes receive outputs at RPOS/RDATA and RNEG/LCV pins to a “0” state for any channel that detects an RLOS condition. <i>NOTE: RCLK is not muted.</i>	R/W	0
D1	EXLOS	Extended LOS: Writing a “1” to this bit extends the number of zeros at the receive input of each channel before RLOS is declared to 4096 bits. Writing a “0” reverts to the normal mode (32 bits for E1).	R/W	0
D0	ICT	In-Circuit-Testing: Writing a “1” to this bit configures all the output pins of the chip in high impedance mode for In-Circuit-Testing. Setting the ICT bit to “1” is equivalent to connecting the Hardware ICT pin 88 to ground.	R/W	0

TABLE 32: MICROPROCESSOR REGISTER 0x82H BIT DESCRIPTION

GLOBAL REGISTER (0x82H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	TxONCNTL	Transmit On Control This register bit grants access to controlling the state of the transmitter outputs. 0 = Control comes from the TxON Register Bits 1 = Control comes from the TxON Hardware Pins	R/W	0
D6	TERCNTL	Receive Termination Select Control This bit sets the LIU to control the RxTSEL function with either the individual channel register bit or the global hardware pin. 0 = Control of the receive termination is set to the register bits 1 = Control of the receive termination is set to the RxTSEL hardware pin	R/W	0
D[5:0]	Reserved	These Register Bits are Not Used	R/W	0

TABLE 33: MICROPROCESSOR REGISTER 0x8Ch BIT DESCRIPTION

GLOBAL REGISTER (0x8Ch)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0
D4	Reserved	This Register Bit is Not Used	R/W	0
D3	LCVCH3	Line Code Violation Counter Select These bits are used to select which channel is to be addressed for reading the contents in register 0x8Eh. It is also used to address the counter for a given channel when performing an update or reset on a per channel basis. By default, Channel 0 is selected. 0000 = None 0001 = Channel 0 0010 = Channel 1 0011 = Channel 2 0100 = Channel 3 0100 = Channel 4 0100 = Channel 5 0100 = Channel 6 0100 = Channel 7	R/W	0
D2	LCVCH2			0
D1	LCVCH1			0
D0	LCVCH0			0

TABLE 34: MICROPROCESSOR REGISTER 0x8Dh BIT DESCRIPTION

GLOBAL REGISTER (0x8Dh)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	R/W	0
D6	Reserved	This Register Bit is Not Used	R/W	0
D5	Reserved	This Register Bit is Not Used	R/W	0
D4	allRST	LCV Counter Reset for All Channels This bit is used to reset all internal LCV counters to their default state 0000h. This bit must be set to "1" for 1 μ S. 0 = Normal Operation 1 = Resets all Counters	R/W	0
D3	allUPDATE	LCV Counter Update for All Channels This bit is used to latch the contents of all counters into holding registers so that the value of each counter can be read. The channel is addressed by using bits D[3:0] in register 0x8Ch. 0 = Normal Operation 1 = Updates all Counters	R/W	0

TABLE 34: MICROPROCESSOR REGISTER 0x8Dh BIT DESCRIPTION

GLOBAL REGISTER (0x8Dh)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D2	BYTEsel	LCV Counter Byte Select This bit is used to select the MSB or LSB for Reading the contents of the LCV counter for a given channel. The channel is addressed by using bits D[3:0] in register 0x8Ch. By default, the LSB byte is selected. 0 = Low Byte 1 = High Byte	R/W	0
D1	chUPDATE	LCV Counter Update Per Channel This bit is used to latch the contents of the counter for a given channel into a holding register so that the value of the counter can be read. The channel is addressed by using bits D[3:0] in register 0x8Ch. 0 = Normal Operation 1 = Updates the Selected Channel	R/W	0
D0	chRESET	LCV Counter Reset Per Channel This bit is used to reset the LCV counter of a given channel to its default state 0000h. The channel is addressed by using bits D[3:0] in register 0x8Ch. This bit must be set to "1" for 1 μ S. 0 = Normal Operation 1 = Resets the Selected Channel	R/W	0

TABLE 35: MICROPROCESSOR REGISTER 0x8Eh BIT DESCRIPTION

GLOBAL REGISTER (0x8Eh)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	LCVCNT7	Line Code Violation Byte Contents These bits contain the LCV counter contents of the Byte selected by bit D2 in register 0x8Dh for a given channel. The channel is addressed by using bits D[3:0] in register 0x8Ch. By default, the contents contain the LSB, however no channel is selected..	R/W	0
D6	LCVCNT6			0
D5	LCVCNT5			0
D4	LCVCNT4			0
D3	LCVCNT3			0
D2	LCVCNT2			0
D1	LCVCNT1			0
D0	LCVCNT0			0

TABLE 36: MICROPROCESSOR REGISTER 0xFEh BIT DESCRIPTION

DEVICE "ID" REGISTER (0xFEh)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Device "ID"	The device "ID" of the XRT83VSH28 short haul LIU is 0xF1h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1
D6				1
D5				1
D4				1
D3				0
D2				0
D1				0
D0				1

TABLE 37: MICROPROCESSOR REGISTER 0xFFh BIT DESCRIPTION

REVISION "ID" REGISTER (0xFFh)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Revision "ID"	The revision "ID" of the XRT83VSH28 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon will be 0x01h.	RO	0
D6				0
D5				0
D4				0
D3				0
D2				0
D1				1
D0				1

6.0 ELECTRICAL CHARACTERISTICS
TABLE 38: ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5V to +3.8V
V _{in}	-0.5V to +5.5V
Maximum Junction Temperature	125°C
Theta JA	24°C/W
Theta JC	10°C/W

TABLE 39: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	3.13	3.3	3.46	V
Input High Voltage	V _{IH}	2.0	-	5.0	V
Input Low Voltage	V _{IL}	-0.5	-	0.8	V
Output High Voltage IOH=2.0mA	V _{OH}	2.4	-		V
Output Low Voltage IOL=2.0mA	V _{OL}	-	-	0.4	V
Input Leakage Current	I _L	-	-	±10	µA
Input Capacitance	C _I	-	5.0		pF
Output Lead Capacitance	C _L	-	-	25	pF

NOTE: Input leakage current excludes pins that are internally pulled "Low" or "High"

TABLE 40: AC ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
MCLKin Clock Duty Cycle		40	-	60	%
MCLKin Clock Tolerance		-	±50	-	ppm

TABLE 41: POWER CONSUMPTION

VDD=3.3V $\pm$ 5%, T _A =25°C, UNLESS OTHERWISE SPECIFIED								
MODE	SUPPLY VOLTAGE	IMPEDANCE	RECEIVER	TRANSMITTER	TYP	MAX	UNIT	TEST CONDITION
E1	3.3V	75 Ω	1:1	1:2	1.401 1.037	-	W	100% ones 50% ones
E1	3.3V	120 Ω	1:1	1:2	1.293 0.977	-	W	100% ones 50% ones

NOTE: The typical power consumption of the 1.8V supply represents ~ 36mW of the above listed.

TABLE 42: E1 RECEIVER ELECTRICAL CHARACTERISTICS

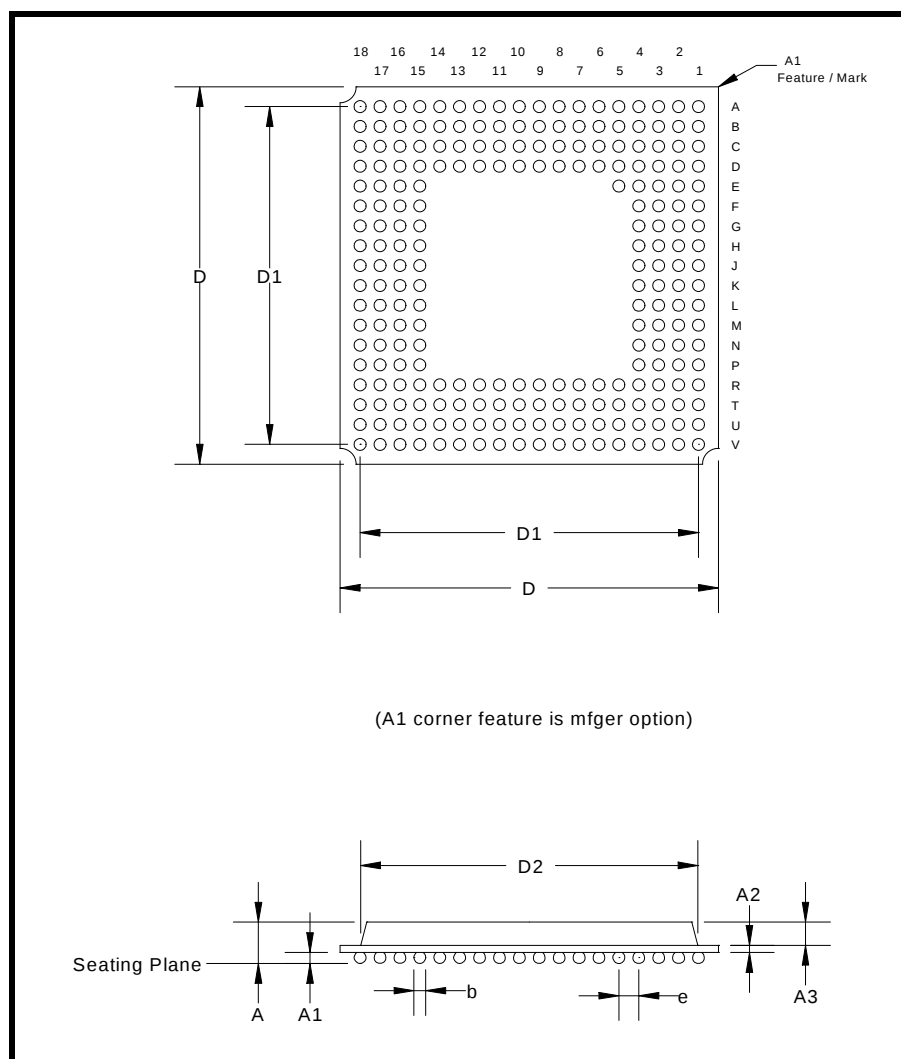
(VDD=3.3V $\pm$ 5%, T _A =25°C UNLESS OTHERWISE SPECIFIED)					
PARAMETER	MIN	TYP.	MAX	UNIT	TEST CONDITIONS
Receiver loss of signal:					
Number of consecutive zeros before LOS is set	-	32	-	bit	Cable attenuation @1024KHz ITU-G.775, ETS1 300 233
Input signal level at LOS	13	16	-	dB	
RLOS Clear	12.5	-	-	% ones	
Receiver Sensitivity	9	-	-	dB	With nominal pulse amplitude of 3.0V for 120 Ω and 2.37V for 75 Ω application.
Interference Margin	-18	-14	-	dB	With 6dB cable loss
Input Impedance	15		-	K Ω	
Jitter Tolerance: 1 Hz 10KHz---100KHz	37 0.3	- -	- -	U _{lpp} U _{lpp}	ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	-	20	36 0.5	KHz dB	
Jitter Attenuator Corner Frequency(-3dB curve) JABW=0 JSBW=1	- -	10 1.5	- -	Hz Hz	ITU G.736
Return Loss: 51KHz --- 102KHz 102KHz --- 2048KHz 2048KHz --- 3072KHz	12 8 8	- - -	- - -	dB dB dB	

TABLE 43: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V ±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
AMI Output Pulse Amplitude					
75Ω	2.13	2.37	2.60	V	1:2 Transformer
120Ω	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05		ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05		ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	U _{I p-p}	Broad Band with jitter free TCLK applied to the input.
Output Return Loss					
51kHz - 102kHz	15	-	-	dB	ETSI 300 166
102kHz - 2048kHz	9	-	-	dB	
2048kHz - 3072kHz	8	-	-	dB	

PACKAGE DIMENSIONS

225 BALL PLASTIC BALL GRID ARRAY (BOTTOM VIEW)
(19.0 X 19.0 X 1.0mm)



Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.049	0.096	1.24	2.45
A1	0.016	0.024	0.40	0.60
A2	0.013	0.024	0.32	0.60
A3	0.020	0.048	0.52	1.22
D	0.740	0.756	18.80	19.20
D1	0.669 BSC		17.00 BSC	
D2	0.665	0.669	16.90	17.00
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VSH28IB	225 Ball BGA	-40°C to +85°C

REVISIONS

REVISION #	DATE	DESCRIPTION
1.0.0	09/17/07	First release of the 8-channel E1 LIU Final Datasheet
2.0.0	03/01/10	Changed Device and Revision ID's

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2010 EXAR Corporation

Datasheet March 2010.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.