Freescale Semiconductor
Technical Data

MPC8260 PowerQUICC™ II Integrated Communications Processor Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the .29 µm (HiP3) devices of the PowerQUICC II™ family of communications processors: the MPC8260 and the MPC8255. Throughout this document, the MPC8260 and the MPC8255 are collectively referred to as the MPC8260.

Contents

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NOTE: Document Revision History

Changes to this document are summarized in Table 17.

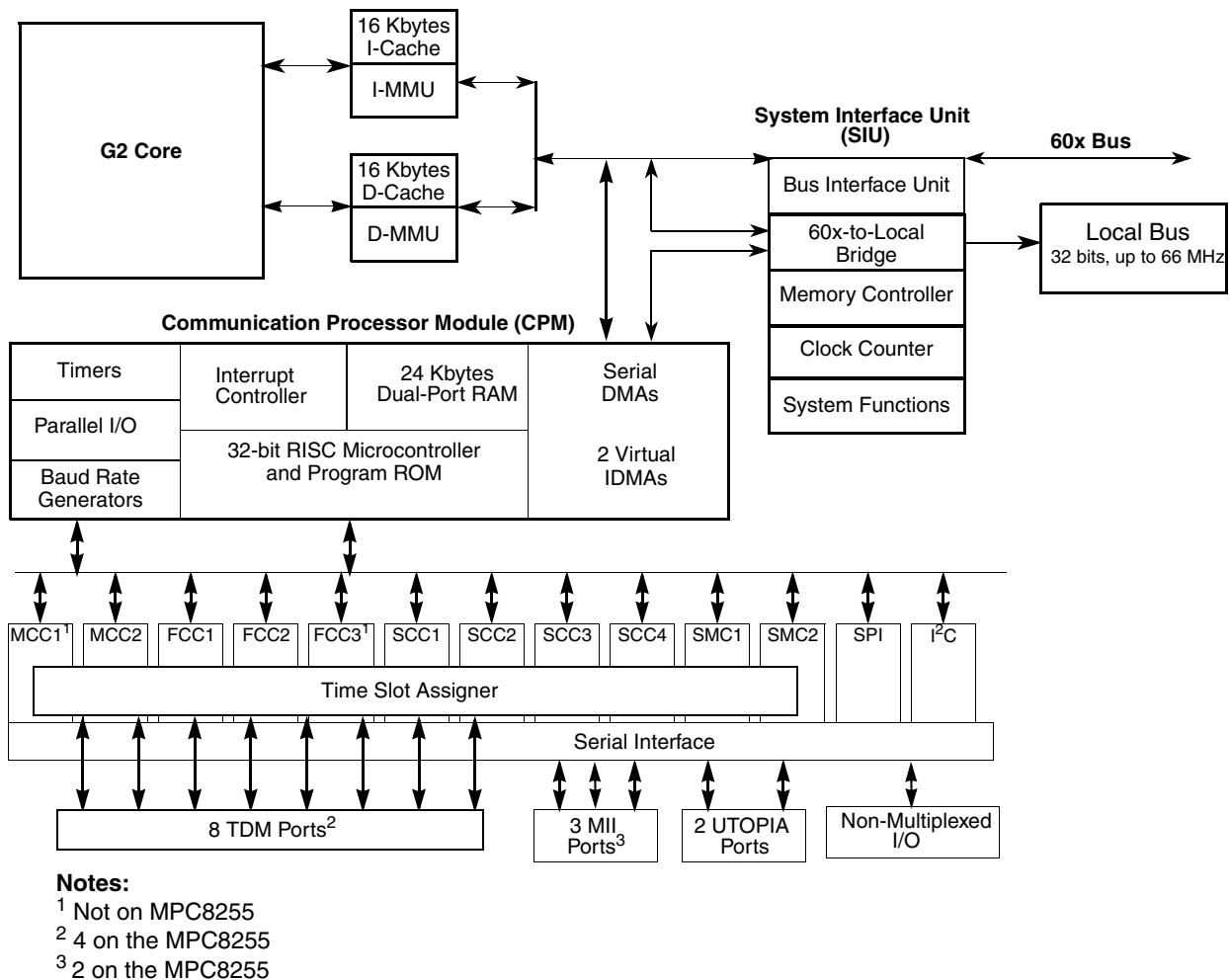Figure 1 shows the block diagram for the MPC8260.

Figure 1. MPC8260 Block Diagram

1   Features

The major features of the MPC8260 are as follows:

- Dual-issue integer core
  - — A core version of the EC603e microprocessor
  - — System core microprocessor supporting frequencies of 133–200 MHz (150–200 MHz for the MPC8255)
  - — Separate 16-Kbyte data and instruction caches:
    - – Four-way set associative
    - – Physically addressed

- – LRU replacement algorithm
  - — PowerPC architecture-compliant memory management unit (MMU)
  - — Common on-chip processor (COP) test interface
  - — High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)
  - — Supports bus snooping for data cache coherency
  - — Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
  - — G2 core and CPM can run at different frequencies for power/performance optimization
  - — Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - — Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - — Bus supports multiple master designs
  - — Supports single- and four-beat burst transfers
  - — 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - — Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - — Single-master bus, supports external slaves
  - — Eight-beat burst transfers
  - — 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- System interface unit (SIU)
  - — Clock synthesizer
  - — Reset controller
  - — Real-time clock (RTC) register
  - — Periodic interrupt timer
  - — Hardware bus monitor and software watchdog timer
  - — IEEE 1149.1 JTAG test access port
- Twelve-bank memory controller
  - — Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - — Byte write enables and selectable parity generation
  - — 32-bit address decodes with programmable bank size
  - — Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - — Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - — Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core

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- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 24-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers (two on the MPC8255) supporting the following protocols:
    – 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
    – ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    – Transparent
    – HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    – Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
    – Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    – Ethernet/IEEE 802.3 CDMA/CS
    – HDLC/SDLC and HDLC bus
    – Universal asynchronous receiver transmitter (UART)
    – Synchronous UART
    – Binary synchronous (BISYNC) communications
    – Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    – Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
    – Transparent
    – UART (low-speed operation)
  - One serial peripheral interface identical to the MPC860 SPI
  - One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
    – Microwire compatible
    – Multiple-master, single-master, and slave modes

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— Up to eight TDM interfaces (4 on the MPC8255)

    – Supports two groups of four TDM channels for a total of eight TDMs

    – 2,048 bytes of SI RAM

    – Bit or byte resolution

    – Independent transmit and receive routing, frame synchronization

    – Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces

— Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels

— Four independent 16-bit timers that can be interconnected as two 32-bit timers

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8260.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8260. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings [1]

Rating	Symbol	Value	Unit
Core supply voltage [2]	VDD	-0.3 – 2.75	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.75	V
I/O supply voltage [3]	VDDH	-0.3 – 4.0	V
Input voltage [4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(-55) – (+150)	°C

[1]   Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

[2]   **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

[3]   **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.0 V during normal operation.

[4]   **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions [1]

Rating	Symbol	2.5-V Device [2]	Unit
Core supply voltage	VDD	2.4–2.7	V
PLL supply voltage	VCCSYN	2.4–2.7	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T_j	105	°C

[1] **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

[2] Parts labeled with an "-HVA" suffix are 2.6-V devices.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.
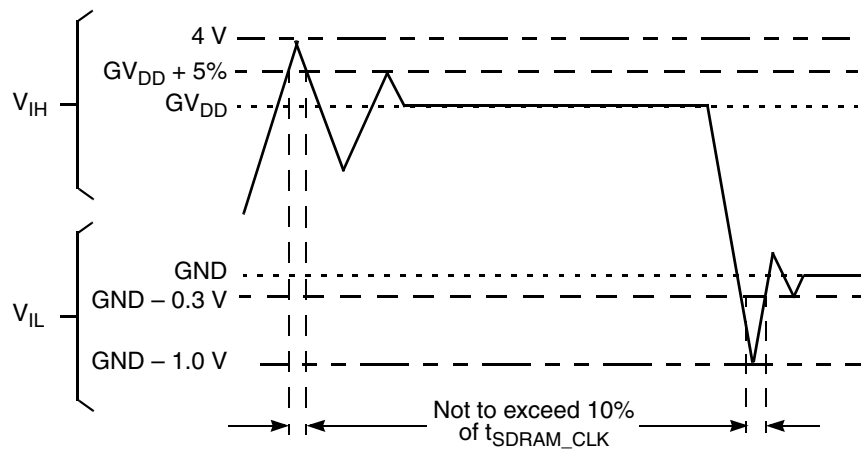

Figure 2. Overshoot/Undershoot Voltage

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics [1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH [2]	I_{IN}	—	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.8 V	I_L	—	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	µA

Output high voltage, I_{OH} = –2 mA
except XFC, UTOPIA mode, and open drain pins
 	
In UTOPIA mode: I_{OH} = -8.0mA
    PA[0-31]
    PB[4-31]
    PC[0-31]
    PD[4-31]
	V_{OH}	2.4	—	V

In UTOPIA mode: I_{OL} = 8.0mA
    PA[0-31]
    PB[4-31]
    PC[0-31]
    PD[4-31]
	V_{OL}	—	0.5	V

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA $\overline{BR}$ $\overline{BG}$ $\overline{ABB}/\overline{IRQ2}$ $\overline{TS}$ A[0-31] TT[0-4] $\overline{TBST}$ TSIZE[0–3] $\overline{AACK}$ $\overline{ARTRY}$ $\overline{DBG}$ $\overline{DBB}/\overline{IRQ3}$ D[0-63] DP(0)/$\overline{RSRV}/\overline{EXT\_BR2}$ DP(1)/$\overline{IRQ1}/\overline{EXT\_BG2}$ DP(2)/$\overline{TLBISYNC}/\overline{IRQ2}/\overline{EXT\_DBG2}$ DP(3)/$\overline{IRQ3}/\overline{EXT\_BR3}/\overline{CKSTP\_OUT}$ DP(4)/$\overline{IRQ4}/\overline{EXT\_BG3}/\overline{CORE\_SREST}$ DP(5)/TBEN/$\overline{IRQ5}/\overline{EXT\_DBG3}$ DP(6)/CSE(0)/$\overline{IRQ6}$ DP(7)/CSE(1)/$\overline{IRQ7}$ $\overline{PSDVAL}$ $\overline{TA}$ $\overline{TEA}$ $\overline{GBL}/\overline{IRQ1}$ $\overline{CI}/BADDR29/\overline{IRQ2}$ $\overline{WT}/BADDR30/\overline{IRQ3}$ $\overline{L2\_HIT}/\overline{IRQ4}$ $\overline{CPU\_BG}/BADDR31/\overline{IRQ5}$ $\overline{CPU\_DBG}$ $\overline{CPU\_BR}$ $\overline{IRQ0}/\overline{NMI\_OUT}$ $\overline{IRQ7}/\overline{INT\_OUT}/APE$ $\overline{PORESET}$ $\overline{HRESET}$ $\overline{SRESET}$ $\overline{RSTCONF}$ $\overline{QREQ}$	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0:3]/LBS[0–3] LSDA10/LGPL0 LSDWE/LGPL1 LOE/LSDRAS/LGPL2 LSDCAS/LGPL3 LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX [3]/LGPL5 LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2) I_{OL} = 3.2mA L_A14 L_A15/SMI L_A16 L_A17/CKSTP_OUT L_A18 L_A19 L_A20 L_A21 L_A22 L_A23 L_A24 L_A25 L_A26 L_A27 L_A28/CORE_SRESET L_A29 L_A30 L_A31 LCL_D(0-31) LCL_DP(0-3) PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO	V_{OL}	—	0.4	V

[1] The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

[2] The leakage current is measured for nominal VDD, VCCSYN, and VDD.

[3] Rev C.2 silicon only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics

Characteristics	Symbol	Value	Unit	Air Flow
Thermal resistance for TBGA	θ_{JA}	13.07 [1]	°C/W	NC [2]
	θ_{JA}	9.55 [1]	°C/W	1 m/s
	θ_{JA}	10.48 [3]	°C/W	NC
	θ_{JA}	7.78 [3]	°C/W	1 m/s

[1] Assumes a single layer board with no thermal vias

[2] Natural convection

[3] Assumes a four layer board

2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \tag{1}$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° \text{ C}) \tag{2}$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° \text{ C}) + \theta_{JA} \times P_D^2 \tag{3}$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8260 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3W$ (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations [1]

Bus (MHz)	CPM Multiplier	CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT} (W) [2]				
					Vddl				
					2.4	2.5	2.6	2.7	2.8 [3]
33.3	4	4	133.3	133.3	2.04	2.14	2.26	2.38	2.50
50.0	2	3	100	150.0	2.21	2.30	2.45	2.59	2.69
66.7	2	2.5	133.3	166.7	2.47	2.62	2.74	2.88	3.02
66.7	2.5	2.5	166.7	166.7	2.57	2.69	2.83	2.98	3.12
66.7	2	3	133.3	200.0	2.81	2.95	3.12	3.29	3.43
66.7	2.5	3	166.7	200.0	2.88	3.05	3.22	3.38	3.55
50.0	3	4	150	200.0	2.83	3.00	3.14	3.31	3.48

[1] Test temperature = room temperature (25° C)

[2] $P_{INT} = I_{DD} \times V_{DD}$ Watts

[3] 2.8 Vddl does not apply to HiP3 Rev C silicon.

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8260 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

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Table 6. Output Buffer Impedances [1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46

[1] These are typical values at 65° C. The impedance may vary by
±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs [1]

Spec Number		Characteristic	Max Delay (ns)	Min Delay (ns)
Max	Min		66 MHz	66 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	2
sp40	sp41	TDM outputs/SI	25	5
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	1
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	2
sp42	sp43	PIO/TIMER/IDMA outputs	14	1

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the
signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	3
sp20	sp21	TDM inputs/SI	15	12
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	5
sp22	sp23	PIO/TIMER/IDMA inputs	10	3

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of
CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC
timing diagrams also apply when the falling edge is the active edge.

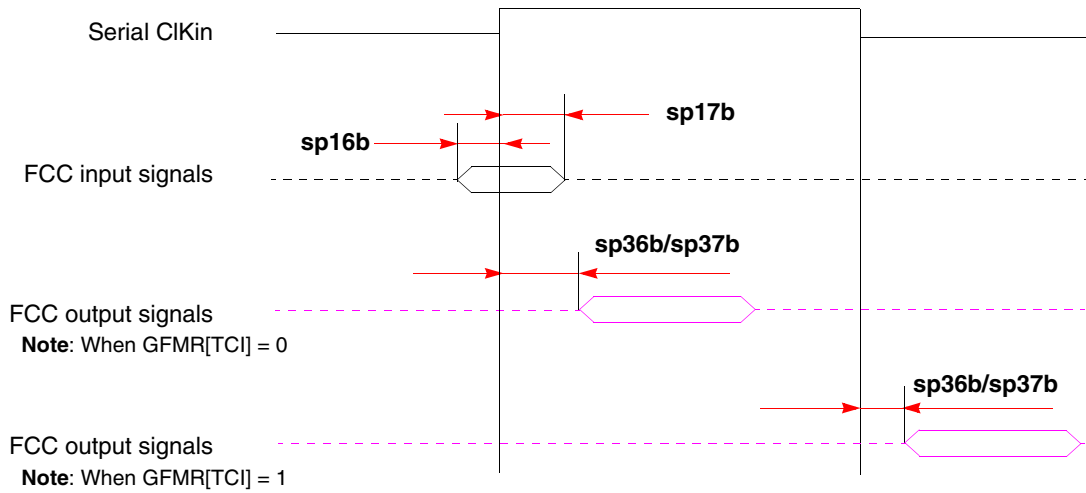Figure 3 shows the FCC external clock.

Serial ClKin

sp17b

sp16b

FCC input signals

sp36b/sp37b

FCC output signals
Note: When GFMR[TCI] = 0

sp36b/sp37b

FCC output signals
Note: When GFMR[TCI] = 1

Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

BRG_OUT

sp17a

sp16a

FCC input signals

sp36a/sp37a

FCC output signals
Note: When GFMR[TCI] = 0

sp36a/sp37a

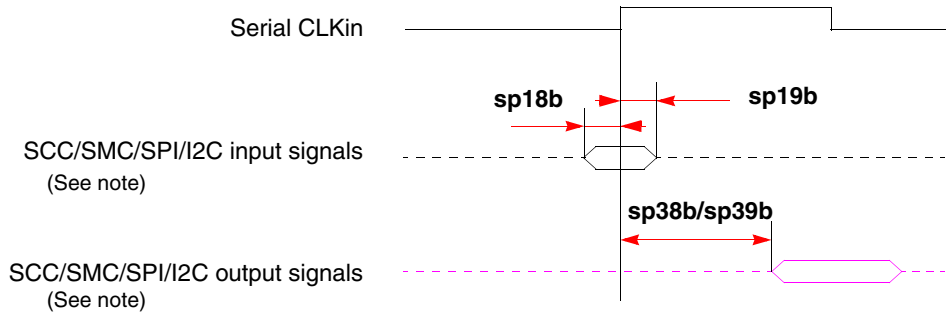FCC output signals
Note: When GFMR.[TCI] = 1
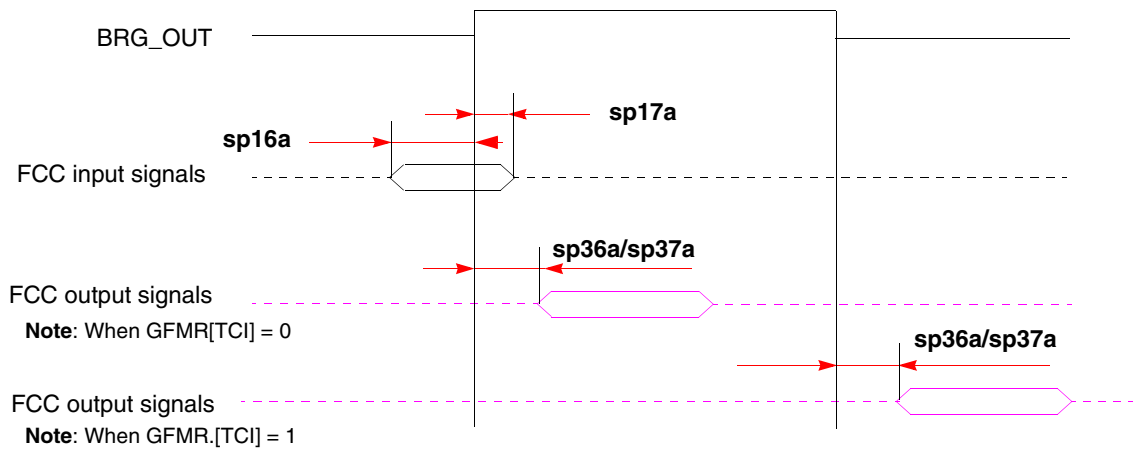
Figure 4. FCC Internal Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I^{2}C external clock.
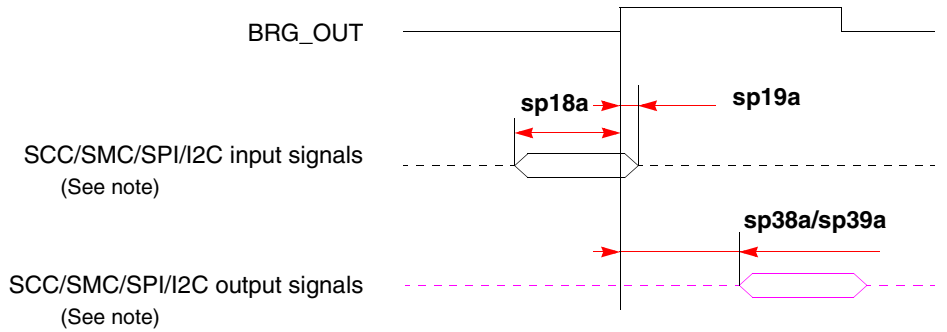

Note: There are four possible timing conditions for SCC and SPI:
  1. Input sampled on the rising edge and output driven on the rising edge (shown).
  2. Input sampled on the rising edge and output driven on the falling edge.
  3. Input sampled on the falling edge and output driven on the falling edge.
  4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^{2}C External Clock Diagram

Figure 6 shows the SCC/SMC/SPI/I^{2}C internal clock.
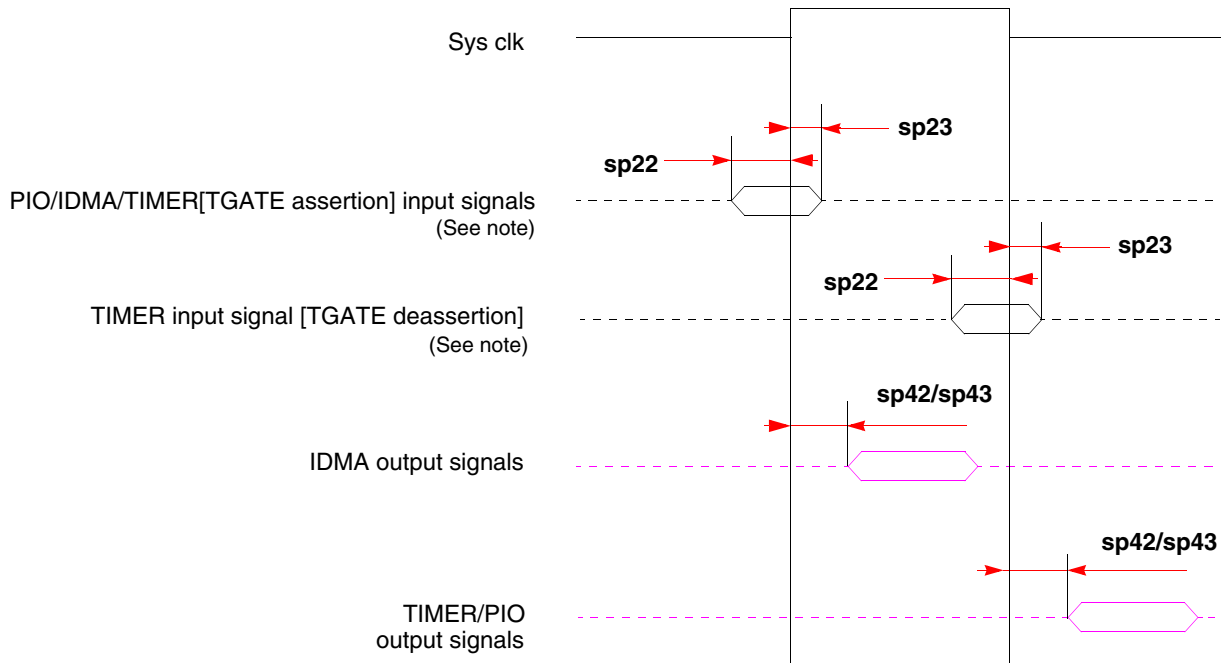

Note: There are four possible timing conditions for SCC and SPI:
  1. Input sampled on the rising edge and output driven on the rising edge (shown).
  2. Input sampled on the rising edge and output driven on the falling edge.
  3. Input sampled on the falling edge and output driven on the falling edge.
  4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

Figure 7 shows PIO, timer, and DMA signals.

Sys clk

sp23

sp22

PIO/IDMA/TIMER[TGATE assertion] input signals
(See note)

sp23

sp22

TIMER input signal [TGATE deassertion]
(See note)

sp42/sp43

IDMA output signals

sp42/sp43

TIMER/PIO
output signals

Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 7. PIO, Timer, and DMA Signal Diagram

Table 9 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs [1]

Spec Number		Characteristic	Setup (ns)	Hold (ns)
Setup	Hold		66 MHz	66 MHz
sp11	sp10	AACK/ARTRY/TA/TS/TEA/DBG/BG/BR	6	1
sp12	sp10	Data bus in normal mode	5	1
sp13	sp10	Data bus in ECC and PARITY modes	8	1
sp14	sp10	DP pins	8	1
sp14	sp10	All other pins	5	1

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

**Table 10. AC Characteristics for SIU Outputs** [1]

Spec Number		Characteristic	Max Delay (ns)	Min Delay (ns)
Max	Min		66 MHz	66 MHz
sp31	sp30	PSDVAL/TEA/TA	10	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	0.5
sp33a	sp30	Data bus	8	0.5
sp33b	sp30	DP	12	0.5
sp34	sp30	memc signals/ALE	6	0.5
sp35	sp30	all other signals	7.5	0.5

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 8 shows TDM input and output signals.
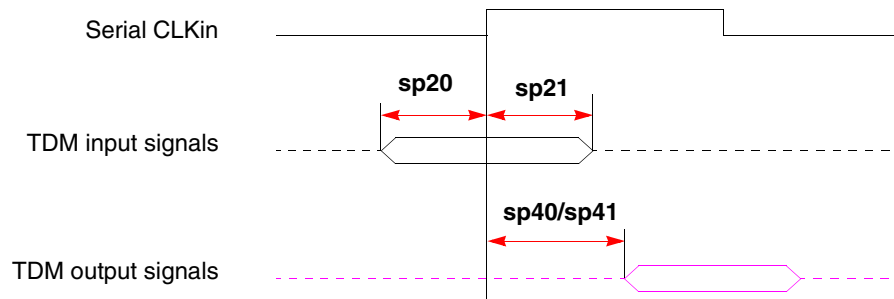
Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 8. TDM Signal Diagram

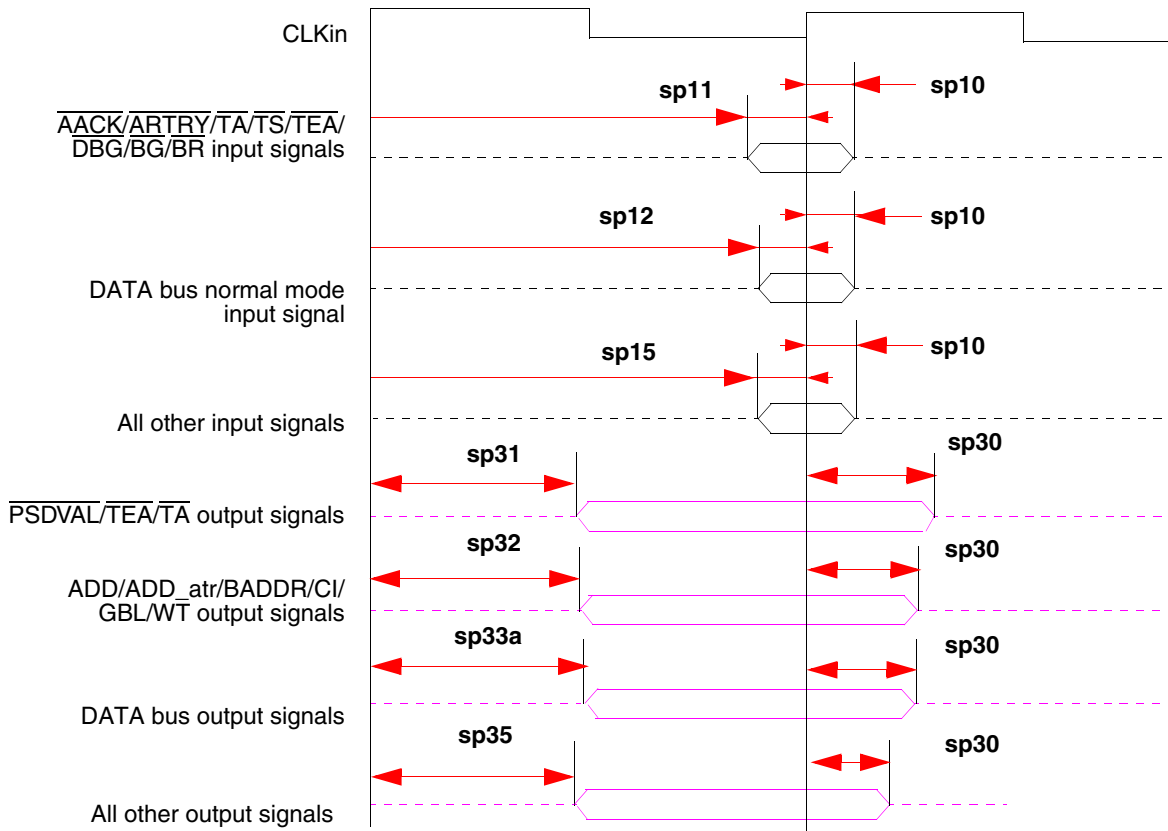Figure 9 shows the interaction of several bus signals.

Figure 9. Bus Signals

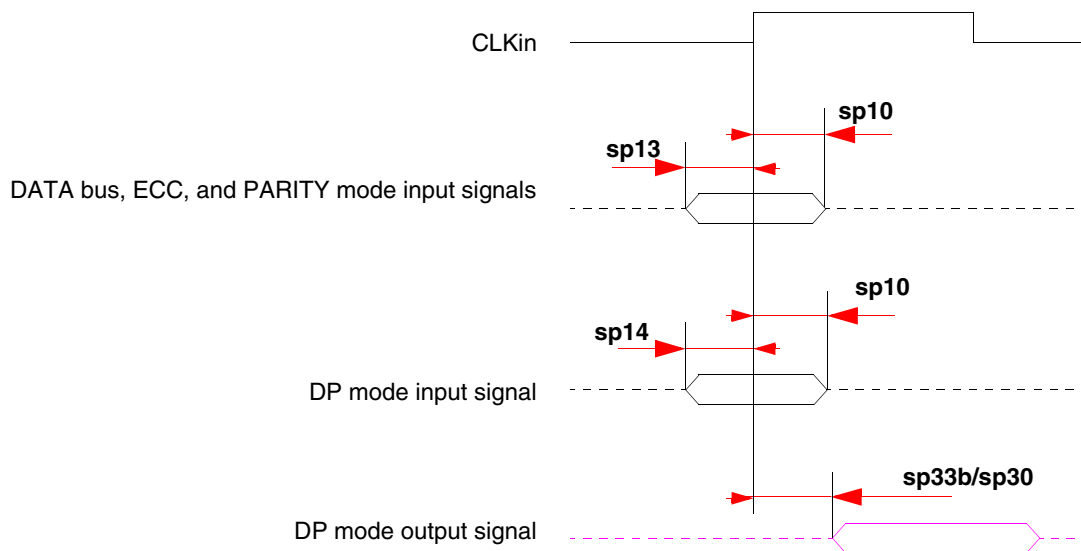Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

Figure 10. Parity Mode Diagram
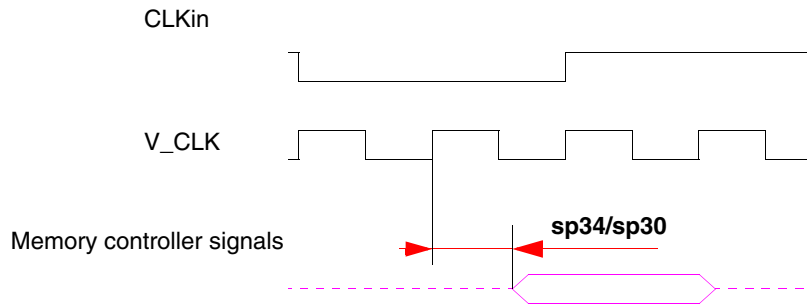
Figure 11 shows signal behavior in MEMC mode.

Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC8260 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	**T3**	**T4**
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

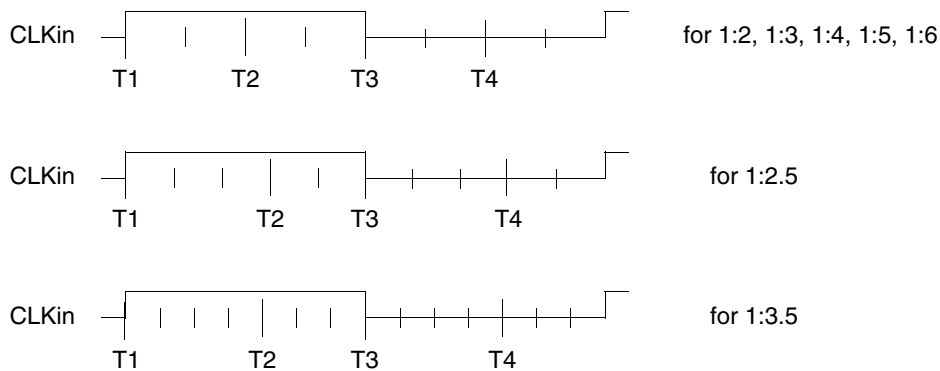Figure 12 is a graphical representation of Table 11.

Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the
memory controller programming; the AC specifications are relative to the
internal tick. Note that SDRAM and GPCM machine outputs change on
CLKin's rising edge.

3   Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the
MODCK[1–3] pins are sampled while HRESET is asserted. Table 12 shows the eight basic configuration
modes. Another 49 modes are available by using the configuration pin (RSTCONF) and driving four pins
on the data bus.

NOTE

Clock configurations change only after POR is asserted.

3.1   Local Bus Mode

Table 12 describes default clock modes for the MPC8260.

Table 12. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 13 describes all possible clock configurations when using the hard reset configuration sequence.
Note also that basic modes are shown in boldface type.

Table 13. Clock Configuration Modes [1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3,4]	CPM Multiplication Factor[2,5]	CPM Frequency[2]	Core Multiplication Factor[2,6]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 13. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3,4]	CPM Multiplication Factor[2, 5]	CPM Frequency[2]	Core Multiplication Factor[2, 6]	Core Frequency[2]
0001_101	**33 MHz**	**3**	**100 MHz**	4	**133 MHz**
0001_110	**33 MHz**	**3**	**100 MHz**	5	**166 MHz**
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	**33 MHz**	**4**	**133 MHz**	**4**	**133 MHz**
0010_011	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

Table 13. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3,4]	CPM Multiplication Factor[2, 5]	CPM Frequency[2]	Core Multiplication Factor[2, 6]	Core Frequency[2]
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

[1] Because of speed dependencies, not all of the possible configurations in Table 13 are applicable.

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2   The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU ranges between 133–200 and the CPM ranges between 50–166 MHz.

3   Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

4   60x and local bus frequency. Identical to CLKIN.

5   CPM multiplication factor = CPM clock/bus clock

6   CPU multiplication factor = Core PLL multiplication factor

4   Pinout

This section provides the pin assignments and pinout list for the MPC8260.

4.1   Pin Assignments

Figure 13 shows the pinout of the MPC8260 480 TBGA package as viewed from the top surface.
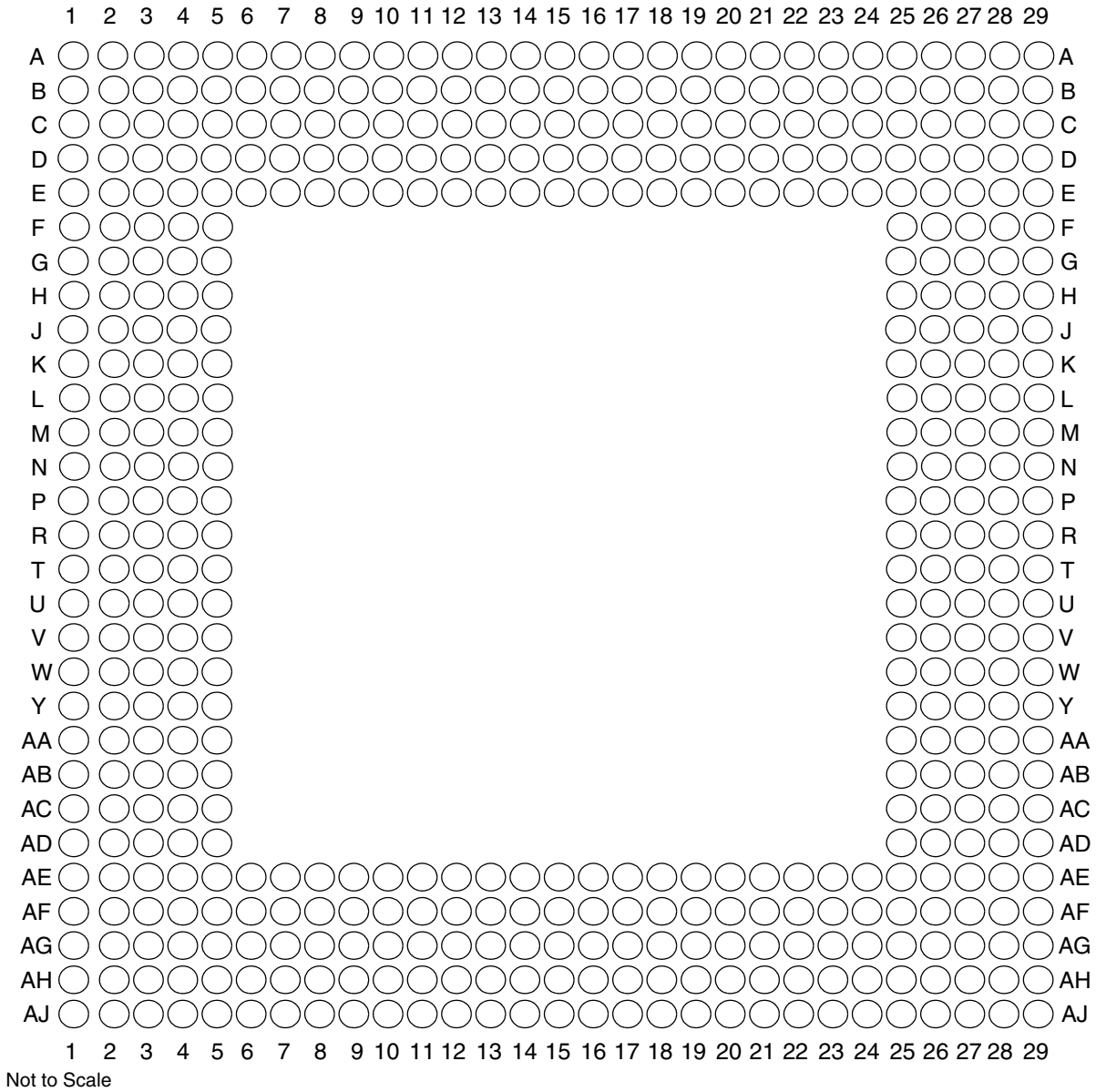

Not to Scale

Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.
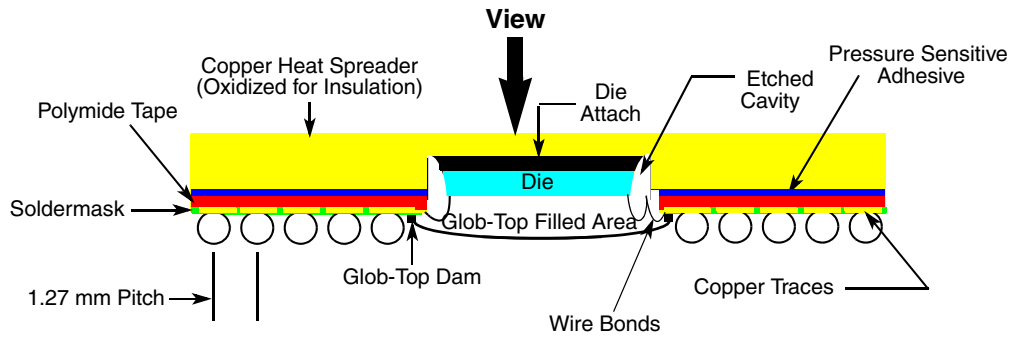

Figure 14. Side View of the TBGA Package

Table 14 shows the pinout list of the MPC8260. Table 15 defines conventions and acronyms used in Table 14.

Table 14. Pinout List

Pin Name	Ball
$\overline{BR}$	W5
$\overline{BG}$	F4
$\overline{ABB}/\overline{IRQ2}$	E2
$\overline{TS}$	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1

Table 14. Pinout List (continued)

Pin Name	Ball
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
$\overline{\text{DBB}}/\overline{\text{IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6

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Table 14. Pinout List (continued)

Pin Name	Ball
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17

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Table 14. Pinout List (continued)

Pin Name	Ball
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/EXT_BR2	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/EXT_DBG2	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/EXT_BR3	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/EXT_BG3	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/EXT_DBG3	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20
$\overline{\text{PSDVAL}}$	V3
$\overline{\text{TA}}$	C22
$\overline{\text{TEA}}$	V5
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2

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Table 14. Pinout List (continued)

Pin Name	Ball
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	U3
L2_HIT/$\overline{\text{IRQ4}}$	Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	U4
$\overline{\text{CPU\_DBG}}$	R2
$\overline{\text{CPU\_BR}}$	Y3
$\overline{\text{CS0}}$	F25
$\overline{\text{CS1}}$	C29
$\overline{\text{CS2}}$	E27
$\overline{\text{CS3}}$	E28
$\overline{\text{CS4}}$	F26
$\overline{\text{CS5}}$	F27
$\overline{\text{CS6}}$	F28
$\overline{\text{CS7}}$	G25
$\overline{\text{CS8}}$	D29
$\overline{\text{CS9}}$	E29
$\overline{\text{CS10}}$/$\overline{\text{BCTL1}}$	F29
$\overline{\text{CS11}}$/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
$\overline{\text{BCTL0}}$	A27
PWE0/PSDDQM0/$\overline{\text{PBS0}}$	C25
$\overline{\text{PWE1}}$/PSDDQM1/$\overline{\text{PBS1}}$	E24
$\overline{\text{PWE2}}$/PSDDQM2/$\overline{\text{PBS2}}$	D24
$\overline{\text{PWE3}}$/PSDDQM3/$\overline{\text{PBS3}}$	C24
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
$\overline{\text{PWE6}}$/PSDDQM6/$\overline{\text{PBS6}}$	B25
$\overline{\text{PWE7}}$/PSDDQM7/$\overline{\text{PBS7}}$	A25
PSDA10/PGPL0	E23
$\overline{\text{PSDWE}}$/PGPL1	B24
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	A24
$\overline{\text{PSDCAS}}$/PGPL3	B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22

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Freescale Semiconductor

Table 14. Pinout List (continued)

Pin Name	Ball
$\overline{\text{LWE0}}$/$\overline{\text{LSDDQM0}}$/$\overline{\text{LBS0}}$	H28
$\overline{\text{LWE1}}$/$\overline{\text{LSDDQM1}}$/$\overline{\text{LBS1}}$	H27
$\overline{\text{LWE2}}$/$\overline{\text{LSDDQM2}}$/$\overline{\text{LBS2}}$	H26
$\overline{\text{LWE3}}$/$\overline{\text{LSDDQM3}}$/$\overline{\text{LBS3}}$	G29
LSDA10/LGPL0	D27
$\overline{\text{LSDWE}}$/LGPL1	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2	E26
$\overline{\text{LSDCAS}}$/LGPL3	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX [1]	B27
$\overline{\text{LWR}}$	D28
L_A14	N27
L_A15/$\overline{\text{SMI}}$	T29
L_A16	R27
L_A17/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18	R29
L_A19	R28
L_A20	W29
L_A21	P28
L_A22	N26
L_A23	AA27
L_A24	P29
L_A25	AA26
L_A26	N25
L_A27	AA25
L_A28/$\overline{\text{CORE\_SRESET}}$	AB29
L_A29	AB28
L_A30	P25
L_A31	AB27
LCL_D0	H29
LCL_D1	J29
LCL_D2	J28
LCL_D3	J27
LCL_D4	J26
LCL_D5	J25

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Table 14. Pinout List (continued)

Pin Name	Ball
LCL_D6	K25
LCL_D7	L29
LCL_D8	L27
LCL_D9	L26
LCL_D10	L25
LCL_D11	M29
LCL_D12	M28
LCL_D13	M27
LCL_D14	M26
LCL_D15	N29
LCL_D16	T25
LCL_D17	U27
LCL_D18	U26
LCL_D19	U25
LCL_D20	V29
LCL_D21	V28
LCL_D22	V27
LCL_D23	V26
LCL_D24	W27
LCL_D25	W26
LCL_D26	W25
LCL_D27	Y29
LCL_D28	Y28
LCL_D29	Y25
LCL_D30	AA29
LCL_D31	AA28
LCL_DP0	L28
LCL_DP1	N28
LCL_DP2	T28
LCL_DP3	W28
$\overline{\text{IRQ0}}$/NMI_OUT	T1
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$/$\overline{\text{APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3

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Table 14. Pinout List (continued)

Pin Name	Ball
TDI	AE6
TDO	AF5
$\overline{\text{TRIS}}$	AB4
$\overline{\text{PORESET}}$	AG6
$\overline{\text{HRESET}}$	AH5
$\overline{\text{SRESET}}$	AF6
$\overline{\text{QREQ}}$	AA3
$\overline{\text{RSTCONF}}$	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29 [2]
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25 [2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28 [2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29 [2]
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28 [2]
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26 [2]
PA6/L1RSYNCA1	AE24 [2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25 [2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23 [2]
PA9/SMTXD2/L1TXD0A1	AH23 [2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22 [2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22 [2]
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21 [2]
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20 [2]
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19 [2]
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18 [2]
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17 [2]
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16 [2]
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16 [2]
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15 [2]
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13 [2]
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13 [2]

Table 14. Pinout List (continued)

Pin Name	Ball
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12[2]
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11[2]
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9[2]
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8[2]
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7[2]
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7[2]
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5[2]
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1[2]
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/FCC1_RTS	AD3[2]
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5[2]
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28[2]
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26[2]
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25[2]
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26[2]
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27[2]
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24[2]
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24[2]
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22[2]
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21[2]
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19[2]
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18[2]
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17[2]
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14[2]
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13[2]
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12[2]
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11[2]
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16[2]
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15[2]
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9[2]
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7[2]
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6[2]

Table 14. Pinout List (continued)

Pin Name	Ball
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[2]
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/ FCC2_MII_TX_EN	AE2[2]
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5[2]
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4[2]
PC0/$\overline{\text{DREQ1}}$/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[2]
PC1/$\overline{\text{DREQ2}}$/BRGO6/$\overline{\text{L1RQA2}}$	AD29[2]
PC2/$\overline{\text{FCC3\_CD}}$/FCC2_UT8_TXD3/$\overline{\text{DONE2}}$	AE29[2]
PC3/$\overline{\text{FCC3\_CTS}}$/FCC2_UT8_TXD2/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[2]
PC4/$\overline{\text{FCC2\_UTM\_RXENB}}$/$\overline{\text{FCC2\_UTS\_RXENB}}$/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27[2]
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24[2]
PC6/$\overline{\text{FCC1\_CD}}$/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26[2]
PC7/$\overline{\text{FCC1\_CTS}}$/$\overline{\text{L1RQC1}}$/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25[2]
PC8/$\overline{\text{CD4}}$/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[2]
PC9/$\overline{\text{CTS4}}$/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[2]
PC10/$\overline{\text{CD3}}$/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20[2]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19[2]
PC12/$\overline{\text{CD2}}$/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18[2]
PC13/$\overline{\text{CTS2}}$/CLSN2/$\overline{\text{L1RQD1}}$/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18[2]
PC14/$\overline{\text{CD1}}$/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17[2]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16[2]
PC16/CLK16/TIN4	AF15[2]
PC17/CLK15/TIN3/BRGO8	AJ15[2]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[2]
PC19/CLK13/BRGO7/SPICLK	AG13[2]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[2]
PC21/CLK11/BRGO6	AJ11[2]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[2]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[2]
PC24/FCC2_UT8_TXD3/CLK8/$\overline{\text{TOUT4}}$	AF9[2]
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8[2]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[2]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[2]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[2]

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Table 14. Pinout List (continued)

Pin Name	Ball
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27[2]
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC1_UTM_TXADDR4/FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/FCC1_UTM_RXCLAV3/ SPICLK/FCC2_UTM_RXADDR3/FCC2_UTS_RXADDR0	AF16[2]
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/FCC1_UTM_TXCLAV3/ SPISEL/BRGO1/FCC2_UTM_TXADDR3/FCC2_UTS_TXADDR0	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4/FCC2_UTS_RXADDR1	AG1[2]
PD30/$\overline{\text{FCC2\_UTM\_TXENB}}$/$\overline{\text{FCC2\_UTS\_TXENB}}$/TXD1	AD4[2]
PD31/RXD1	AD2[2]
VCCSYN	AB3

Table 14. Pinout List (continued)

Pin Name	Ball
VCCSYN1	B9
GNDSYN	AB1
SPARE1 [3]	AE11
SPARE4[3]	U5
SPARE5 [4]	AF25
SPARE6[3]	V4
THERMAL0 [5]	AA1
THERMAL1[5]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

[1] Only on Rev C.2 silicon.

[2] The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

[3] Must be pulled down or left floating.

[4] Must be pulled down or left floating. However, if compatibility with HiP4 silicon is required, this pin must be pulled up or left floating.

[5] For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

Symbols used in Table 14 are described in Table 15.

Table 15. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.

Table 15. Symbol Legend (continued)

UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

5   Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC8260.

5.1   Package Parameters

Package parameters are provided in Table 16. The package type is a 37.5 x 37.5 mm, 480-lead TBGA.

Table 16. Package Parameters

Parameter	Value
Package Outline	37.5 x 37.5 mm
Interconnects	480 (29 x 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

5.2   Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.

2. Dimensions in millimeters.

3. Dimension b is measured at the

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	
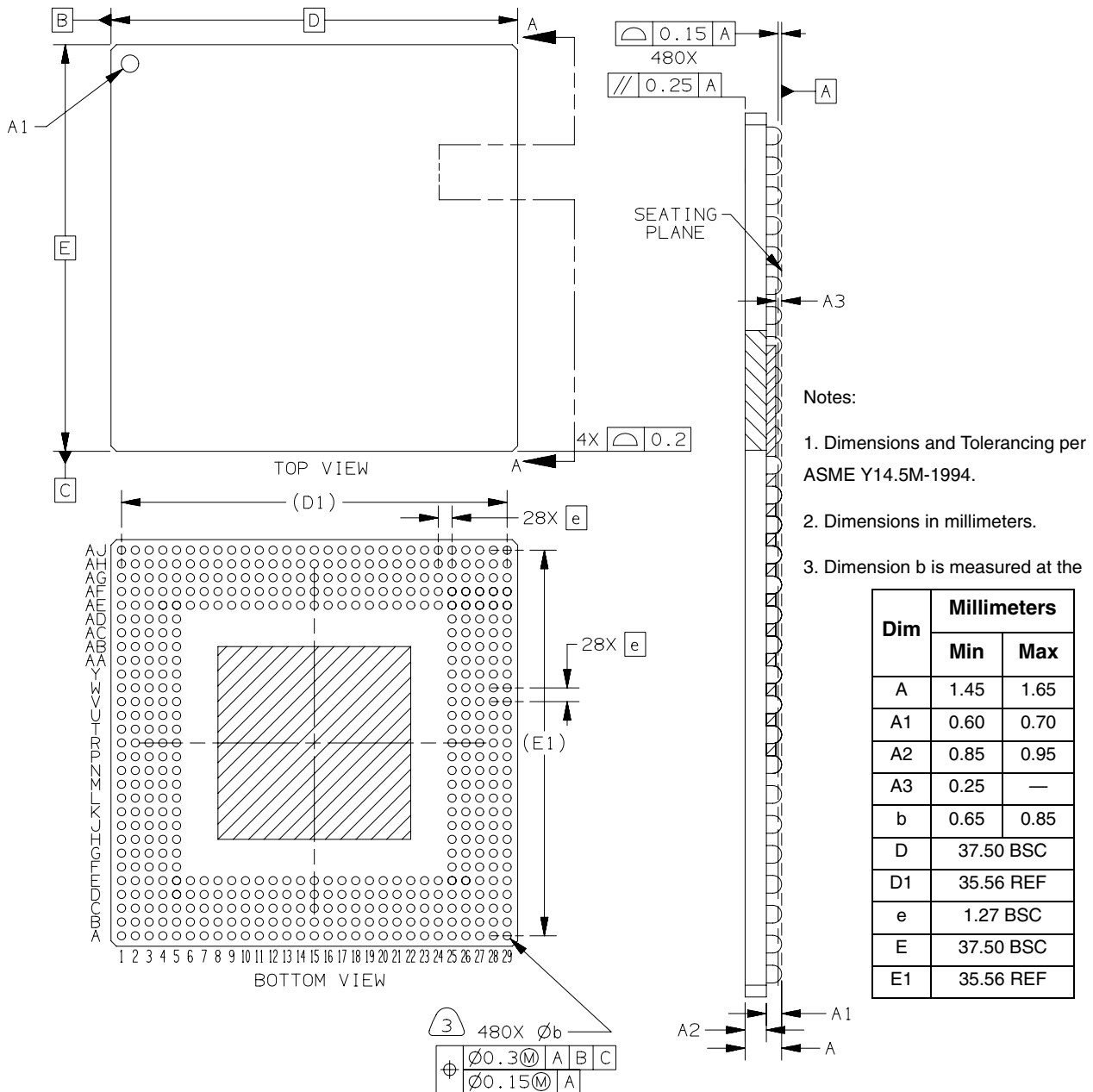
Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

6   Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC8260. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that

indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

MPC 82XX C ZU XXX X XX

Product Code

Die Revision Level
(Nn = Major.minor)

Core Voltage

Device Number

Processor Frequency
(CPU/CPM/Bus)

Temperature Range
Blank = 0 to 105 °C
C = -40 to 105 °C

Package
(ZU = 480 TBGA)
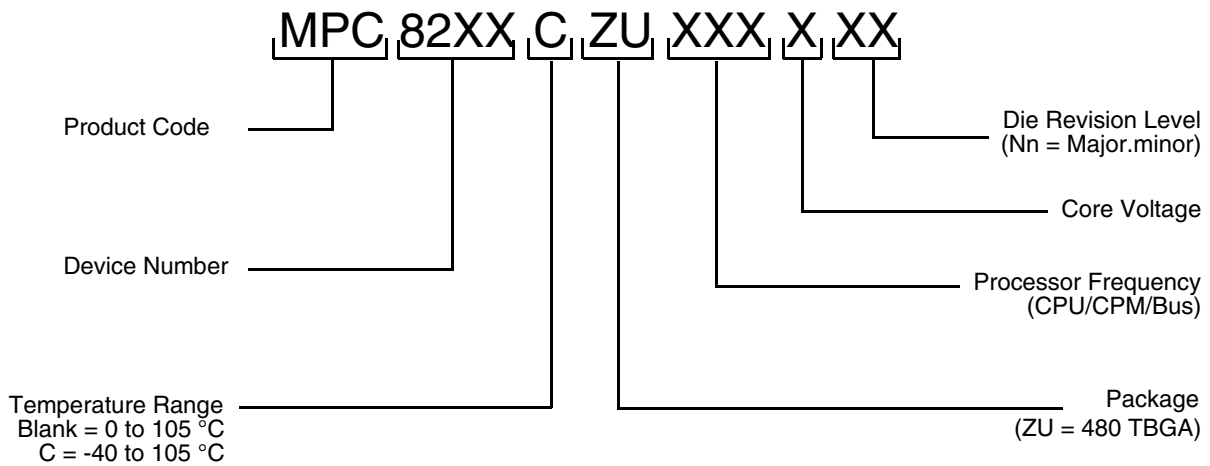
Figure 16. Freescale Part Number Key

7   Document Revision History

Table 17 lists significant changes in each revision of this document.

Table 17. Document Revision History

Revision	Date	Substantive Changes
0	—	Initial version
0.1	1/2000	—
0.2–0.5	—	Temporary revisions
0.6	5/2001	Corrected the thermal values in Table 3, "Thermal Characteristics."
0.7	11/2001	• Revision of Table 5, "Power Dissipation" • Modifications to Figure 9, Table 2,Table 10, Table 11 • Additional revisions to text and figures throughout
0.8	2/2002	• Table 7, Table 8, Table 9, and Table 10: revision 0.7 of this document incorrectly included values for 83 MHz. 83 MHz is not supported on the MPC8260. • Table 14: notes added to pins at AE11, AF25, U5, and V4.
0.9	2/2002	• Table 14: additional note added to AE11
1.0	3/2002	• Table 14: modified notes to pins AE11 and AF25. • Table 14: added note to pins AA1 and AG4 (Therm0 and Therm1).
1.1	5/2002	• Section 1, "Features": updated minimum supported core frequency to 133 MHz • Addition of "Note" at bottom of page 5. • Table 13: Note 3.

Table 17. Document Revision History (continued)

Revision	Date	Substantive Changes
1.2	8/2003	• Note: In revision 0.7, sp30 (Table 10) was changed. This change was not previously recorded in this "Document Revision History" Table. • Addition of MPC8255 description to Section 1, "Features" • Addition of Figure 2 • Addition of VCCSYN to "Note: Core, PLL, and I/O Supply Voltages" following Table 2 • Addition of note 1 to Table 3 • Addition of notes or modifications to Figure 3 through Figure 8 • Addition of reference notes 4, 5, and 6 to Table 13 • Addition of note 2 to Table 14 • Addition of SPICLK to PC19 in Table 14. It is documented correctly in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 14.
1.3	9/2005	• Document template update.

Document Number: MPC8260EC
Rev. 1.3
10/2005

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