HEXFET® Power MOSFET

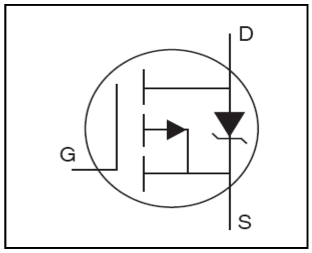
Applications

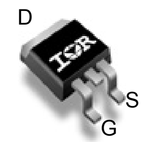
- Reset Switch for Active Clamp Reset DC-DC converters

V_{DSS}	$R_{DS(on)}$ (max)	I_D
- 150V	150mΩ @ V_{GS} = -10V	-27A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current
- Lead-Free





D2 Pak
IRF6218SPbF

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF6218SPbF	D2-Pak	Tube	50	IRF6218SPbF
		Tape and Reel Left	800	IRF6218STRLPbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-150	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	- 27	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	-19	
I_{DM}	Pulsed Drain Current ①	- 110	
P_D @T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	1.6	W/°C
dv/dt	Peak Diode Recovery dv/dt③	8.2	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	——	0.61	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑥	——	40	

Notes ① through ⑥ are on page 2

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-150	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.17	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	120	150	mΩ	V_{GS} = -10V, I_D = -16A ④
$V_{GS(th)}$	Gate Threshold Voltage	-3.0	—	- 5.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V_{DS} = -120V, V_{GS} = 0V
		—	—	-250		V_{DS} = -120V,V_{GS} = 0V,T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 20V

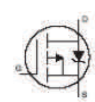
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Trans conductance	11	—	—	S	V_{DS} = -50V, I_D = -16A
Q_g	Total Gate Charge	—	71	110	nC	I_D = -16A
Q_{gs}	Gate-to-Source Charge	—	21	—		V_{DS} = -120V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	32	—		V_{GS} = -10V ④
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	V_{DD} = -75V
t_r	Rise Time	—	70	—		I_D = -16A
$t_{d(off)}$	Turn-Off Delay Time	—	35	—		R_G = 3.9Ω
t_f	Fall Time	—	30	—		V_{GS} = -10V ④
C_{iss}	Input Capacitance	—	2210	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	370	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	89	—		f = 1.0MHz
C_{oss}	Output Capacitance	—	2220	—		V_{GS} = 0V, V_{DS} = -1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	170	—		V_{GS} = 0V, V_{DS} = -120V, f = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance	—	340	—		V_{GS} = 0V, V_{DS} = 0V to -120V

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	210	mJ
I_{AR}	Avalanche Current ①	—	-16	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-27	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-110		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	T_J = 25°C,I_S = -16A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	150	—	ns	T_J = 25°C ,I_F = -16A, V_{DD} = -25V
Q_{rr}	Reverse Recovery Charge	—	860	—	nC	di/dt = 100A/μs ④

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② starting T_J = 25°C, L = 1.6mH, R_G = 25Ω, I_{AS} = -17A
③ $I_{SD} \leq$ -17A, di/dt $\leq$ -520A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.
④ Pulse width $\leq$ 300μs; duty cycle $\leq$ 2%.
⑤ R_θ is measured at T_J of approximately 90°C.
⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

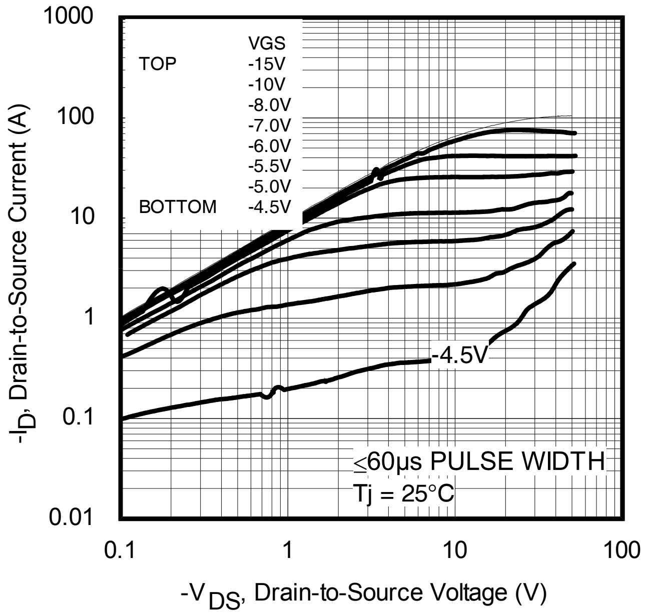


Fig. 1 Typical Output Characteristics

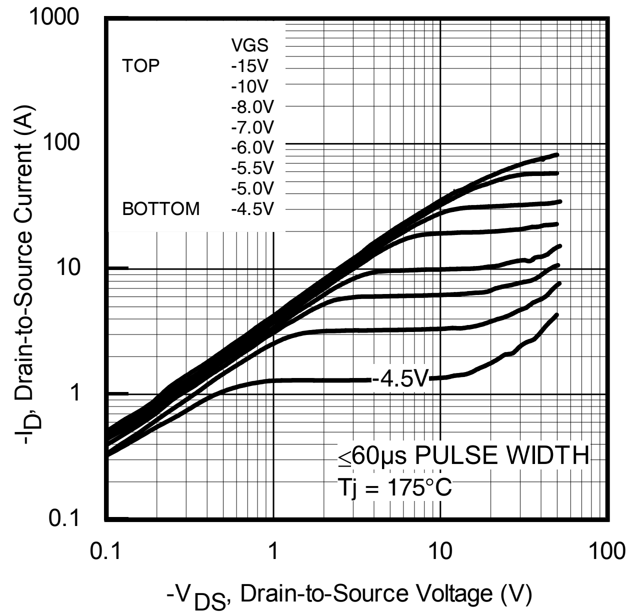


Fig. 2 Typical Output Characteristics

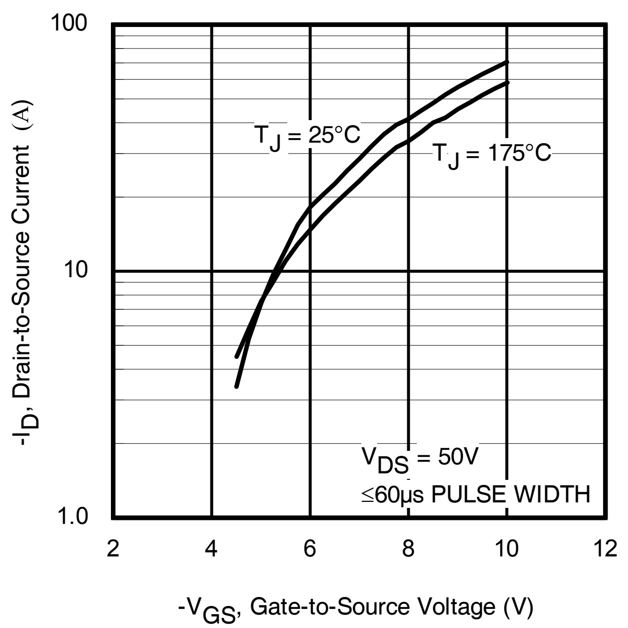


Fig. 3 Typical Transfer Characteristics

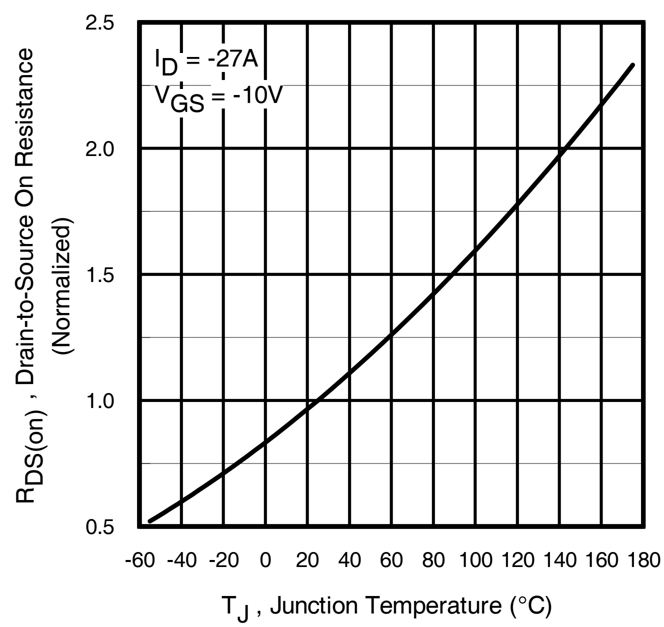


Fig. 4 Normalized On-Resistance vs. Temperature

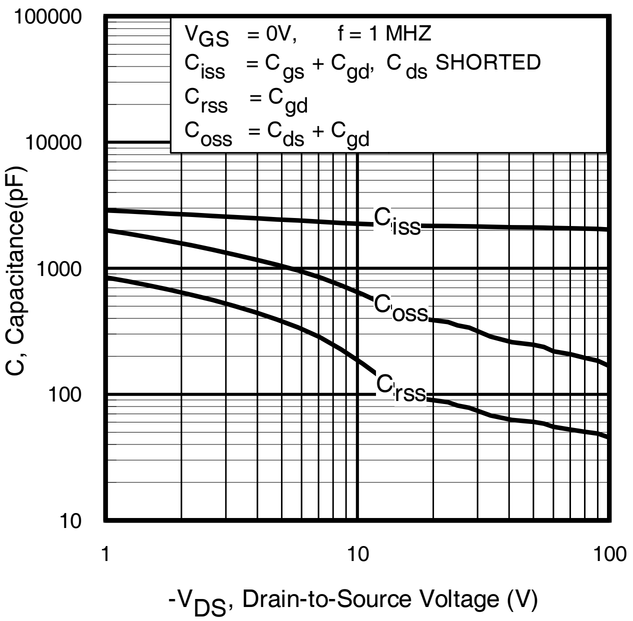


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

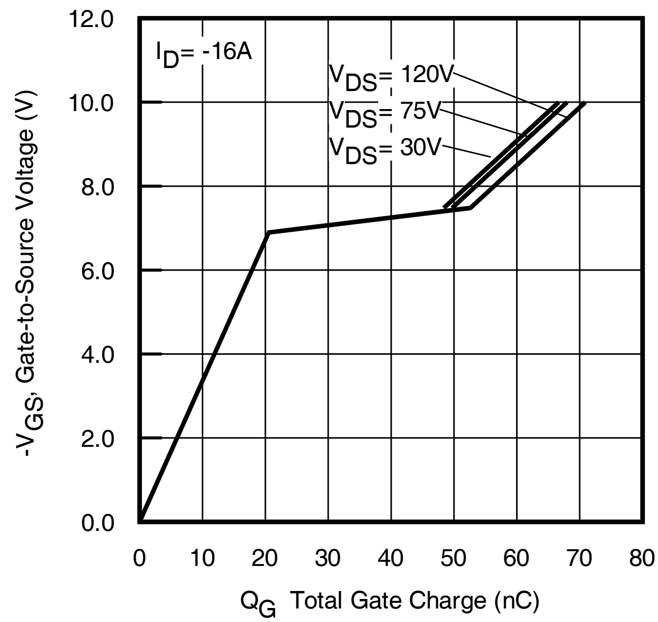


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

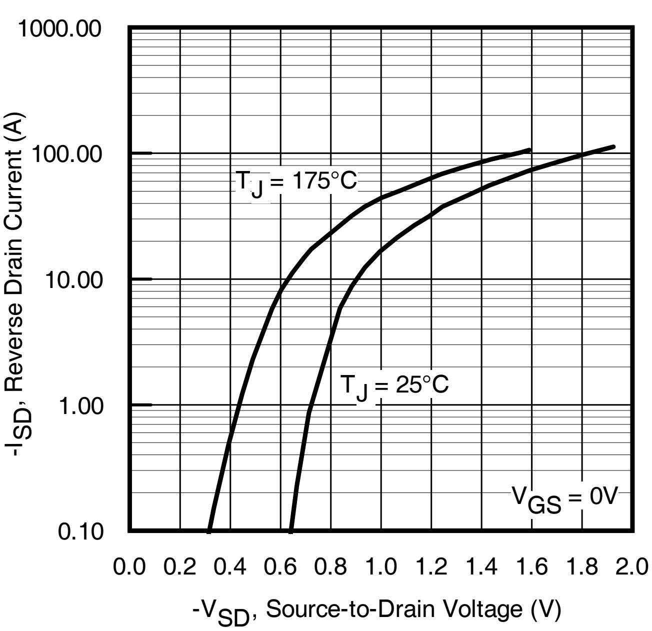


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

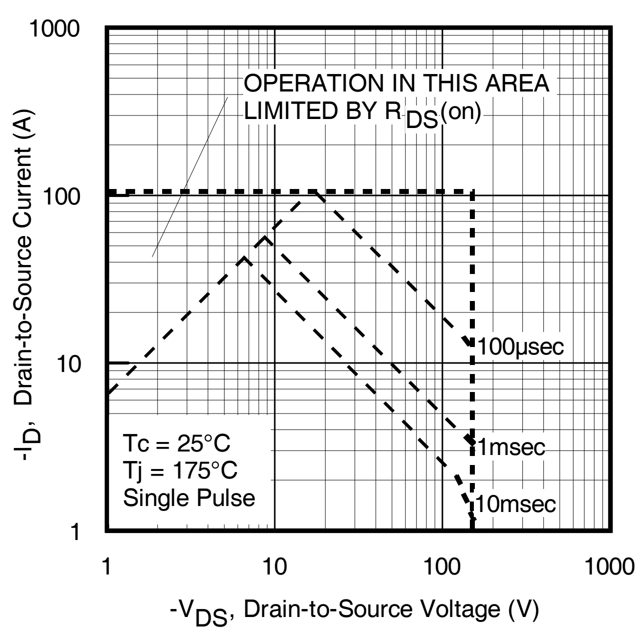


Fig 8. Maximum Safe Operating Area

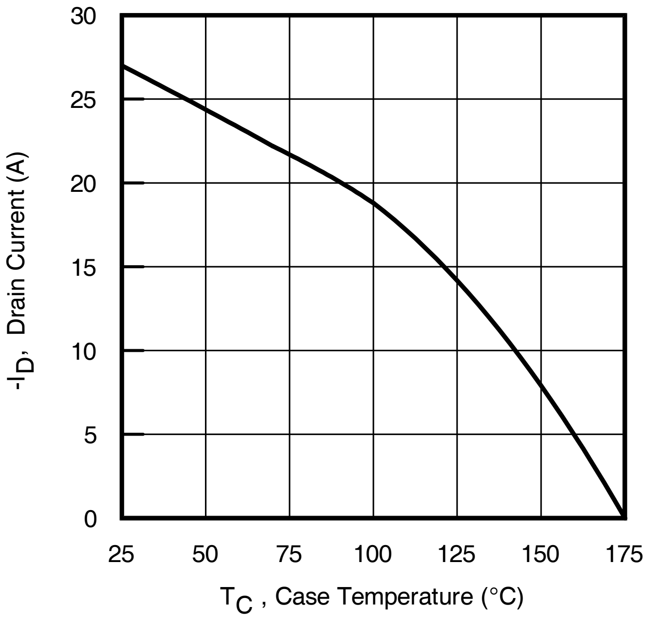


Fig 9. Maximum Drain Current vs. Case Temperature

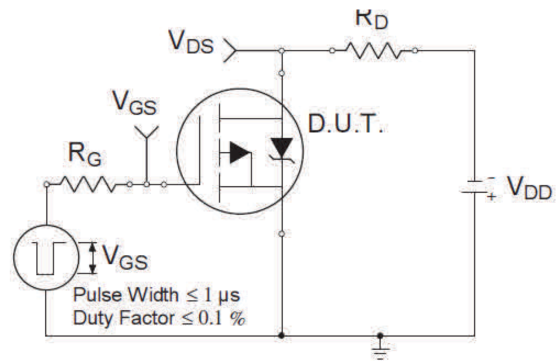


Fig 10a. Switching Time Test Circuit

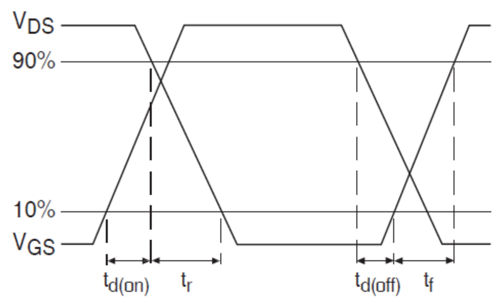
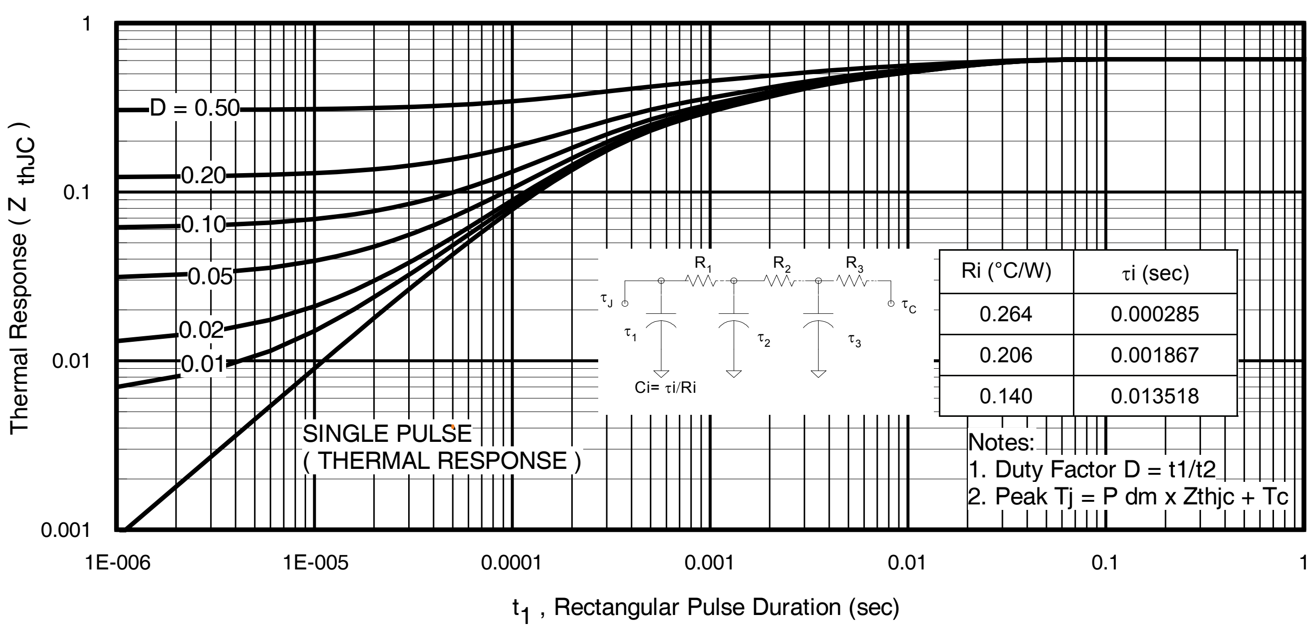


Fig 10b. Switching Time Waveforms



Ri (°C/W)	τi (sec)
0.264	0.000285
0.206	0.001867
0.140	0.013518

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

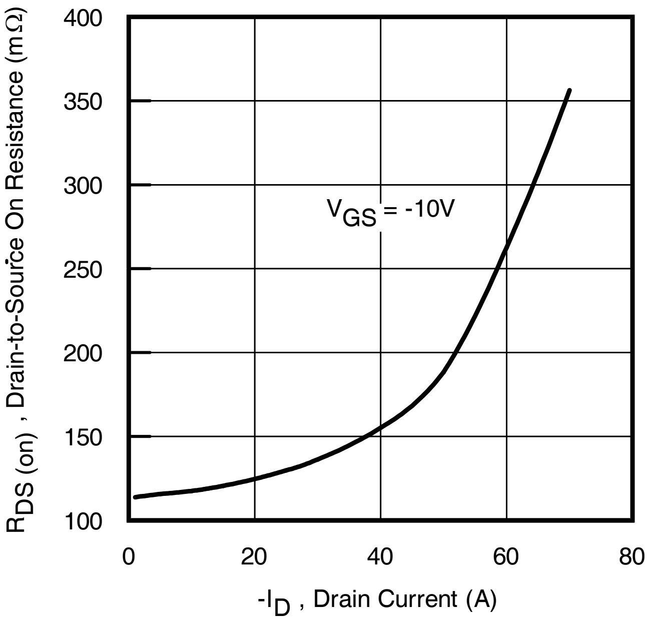


Fig 12. On-Resistance vs. Drain Current

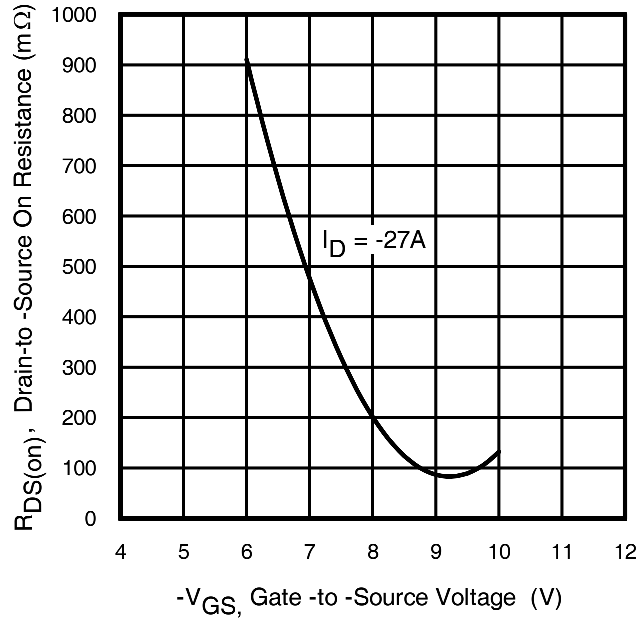


Fig 13. On-Resistance vs. Gate Voltage

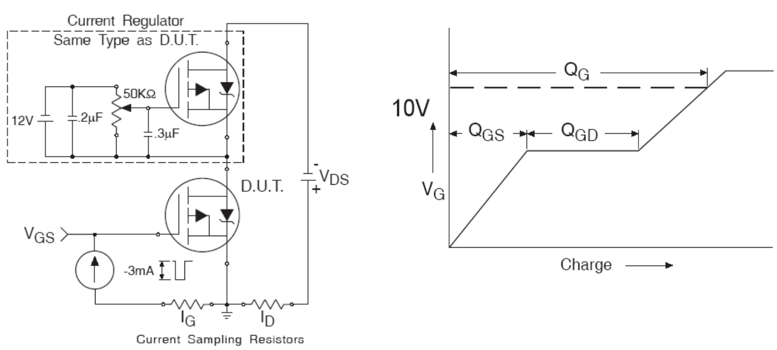


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

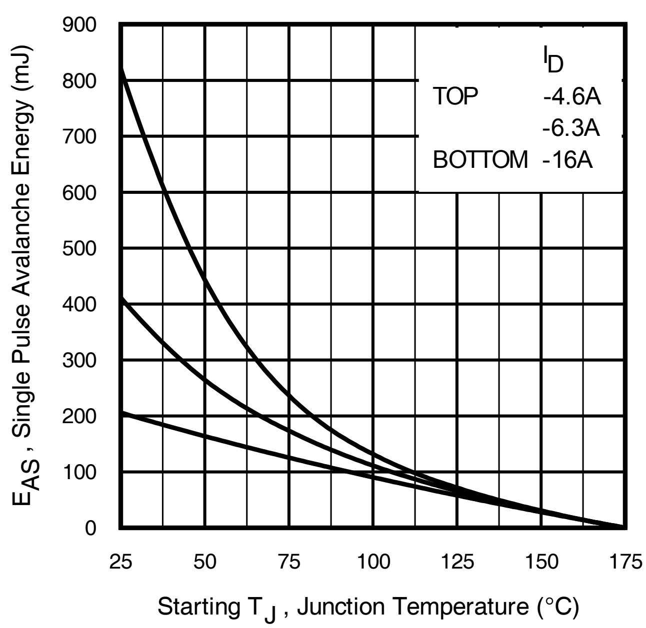


Fig 15c. Maximum Avalanche Energy vs. Drain Current

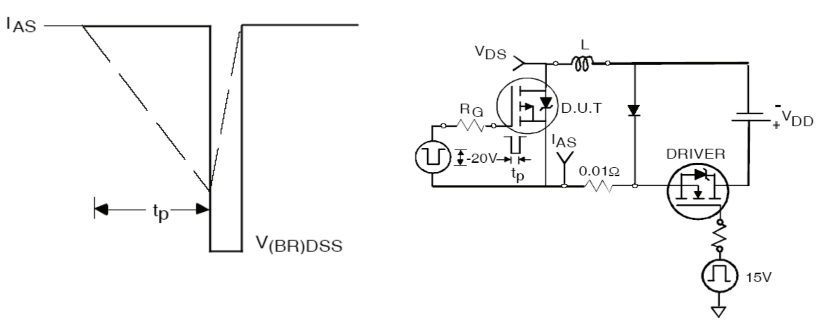
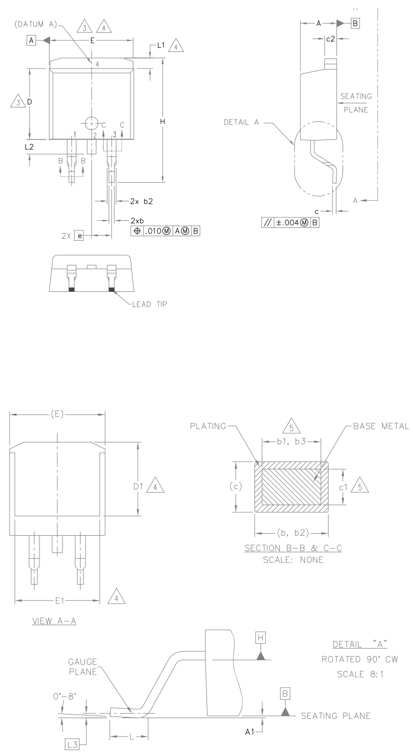


Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

D2-Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. △ THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. △ DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES
1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

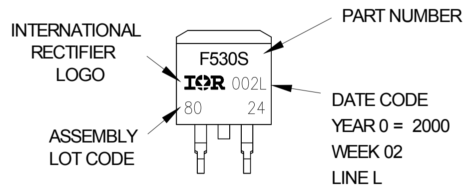
HEXFET
1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

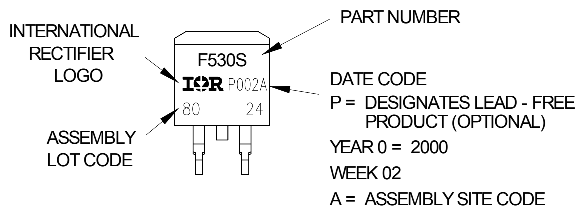
D2-Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead – Free"

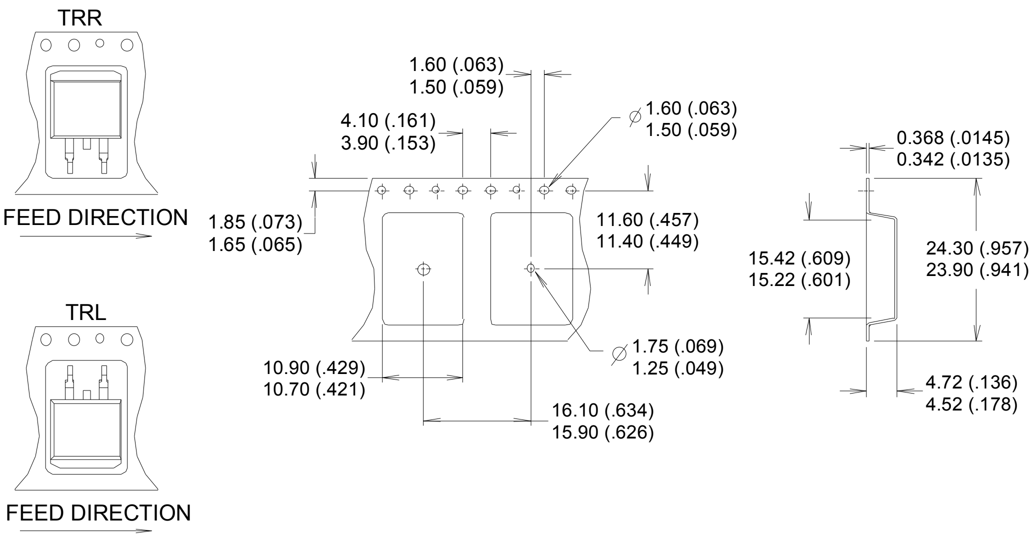


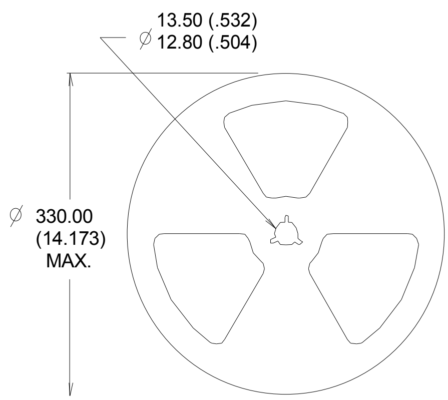
OR

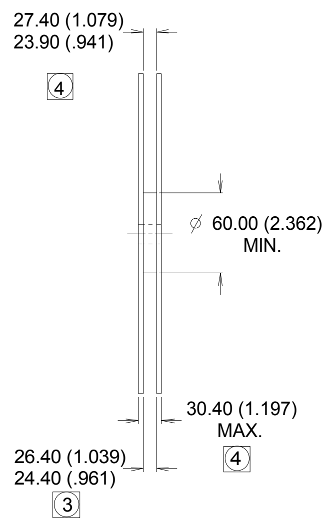


Note: For the most current drawing please refer to Infineon's web site www.infineon.com

D2-Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D2-Pak	MSL1 (per JEDEC J-STD-020D) ††
RoHS Compliant	Yes	

† Qualification standards can be found at Infineon's web site www.infineon.com

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
3/25/2015	• Updated datasheet based on IR corporate template. • Updated package outline and part marking on page 7. • Removed TO-262 Pak (IRF6218LPbF) from datasheet-all pages
5/26/2016	• Updated datasheet with corporate template. • Added disclaimer on last page.

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