

## Automotive Grade AUIRS2016S(TR)

High Side Driver with Internal Vs Recharge

### Features

- Leadfree, RoHS compliant
- Automotive qualified\*
- One high side output and internal low side Vs recharge.
- CMOS Schmitt trigger inverted input with pull up resistor
- CMOS Schmitt trigger inverted reset with pull down resistor
- 5V compatible logic level inputs
- Immune to  $-V_s$  spike and tolerant to  $dV_s/dt$

### Typical Applications

- Common-rail magnetic valve application

### Product Summary

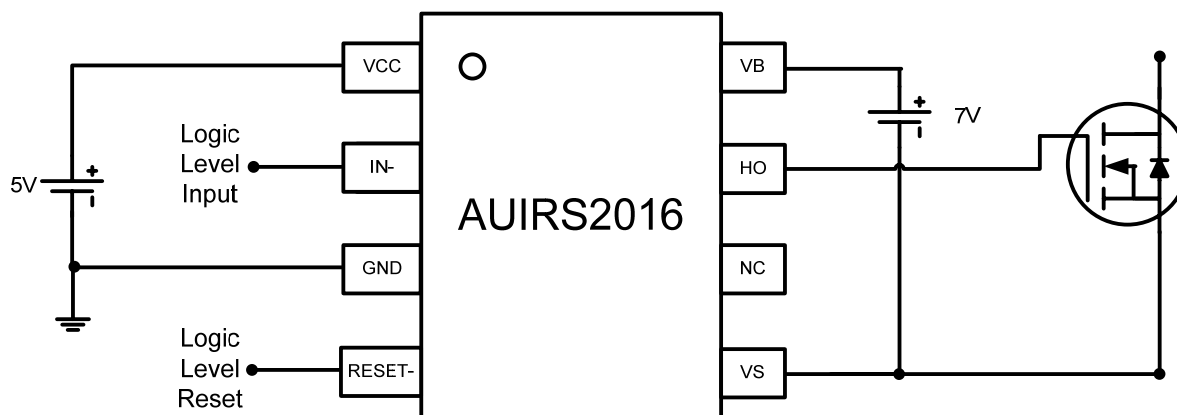
Topology	Low side input, high side driver with Vs recharge
$V_{\text{OFFSET}}$	150 V
$V_{\text{OUT}}$	4.4 V – 20 V
$I_{\text{O+}} \& I_{\text{O-}}$ (typical)	0.25 A
$t_{\text{ON}} \& t_{\text{OFF}}$ (typical)	150 ns
Deadtime $DT_{\text{ON}} / DT_{\text{OFF}}$ (typical)	70ns / 6 us

### Package Options



8 - Lead SOIC  
AUIRS2016S

### Typical Connection Diagram



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## Description

The AUIRS2016 is a high voltage power MOSFET and IGBT high side driver with internal VS-to-GND recharge NMOS. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard 5V CMOS or LSTTL logic. The output driver features a 250mA high pulse current buffer stage. The channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 150 volts above GND ground.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Automotive (per AEC-Q100 <sup>††</sup> )	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SOIC8	MSL3 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M1 (per AEC-Q100-003)	
	Human Body Model	Class H2 (per AEC-Q100-002)	
	Charged Device Model	Class C5 (per AEC-Q100-011)	
<b>IC Latch-Up Test</b>		Class II, Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND, all currents are defined positive into any lead. An operation above the absolute maximum limit is not implied and could damage the part.

Symbol	Definition	Min.	Max.	Units
V <sub>BS</sub>	High Side Floating Supply Voltage	-0.3	20	V
V <sub>B</sub>	High Side Driver Output Stage Voltage, Neg. transient: 0.5 ms, external MOSFET off	-5.0	166	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage Neg. transient 0.4 $\mu$ s	-8.0	150	V
V <sub>H<sub>o</sub></sub>	Output Voltage Gate Connection	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	V
V <sub>CC</sub>	Supply Voltage	-0.3	20	V
V <sub>IN</sub>	Input Voltage	-0.3	V <sub>CC</sub> + 0.3	V
I <sub>IN</sub>	Input Injection Current. Full function, no latch-up; (guaranteed by design). Test at 5V and 7V on Eng. Samples.	---	+1	mA
V <sub>RES</sub>	Reset Input Voltage	-0.3	V <sub>CC</sub> + 0.3	V
V <sub>ESD</sub>	Electrostatic Discharge Voltage(Human body model)	2k		V
V <sub>CDM</sub>	Charge Device Model CDM, EOS/ESD Ass. Std 5.3. Number of discharges per pin: 6	2K		V
dV/dt	Allowable Offset Voltage Slew Rate	-50	50	V/nsec
T <sub>J</sub>	Junction Temperature	-55	150	
T <sub>S</sub>	Storage Temperature	-55	150	°C

### Recommended Operating Conditions

For proper operations the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$ 1)	High Side Driver Output Stage Voltage	$V_S+4.4$	$V_S+20$	V
$V_S$	High Side Floating Supply Offset Voltage	-3	150	V
$V_{HO}$	Output Voltage Gate	$V_S$	$V_B$	V
$V_{CC}$	Supply Voltage	4.4	6.5	V
$V_{IN}$	Input Voltage	0	$V_{CC}$	V
$V_{RES}$	Reset Input Voltage	0	$V_{CC}$	V
$T_a$	Ambient Temperature ( $V_{BS}=14V$ , load: 50 Ohm 2.5nF into $V_S$ )	-40	125	°C
$f_s$	Switching frequency 2)	---	200	kHz
$t_{inlowmin}$	Minimum low input width 3)	1000	---	ns
$t_{inhighin}$	Minimum high input width 3)	60	---	ns

1) Reset-logic functional for  $V_{BS} > 2V$

2) Duty cycle = 0.5,  $V_{BS} = 7V$

3) Guaranteed by design. Pulse width below the specified values may be ignored. Output will either follow the input or will ignore it. No false output state is guaranteed when minimum input width is smaller than  $t_{in}$ .

### Electrical Characteristics

Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ .

Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}C \leq T_j \leq 125^{\circ}C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>VCC Supply Characteristics</b>						
VCCUV+	VCC Supply Undervoltage Positive Going Threshold			4.3	V	VCC rising from 0V
VCCUV-	VCC Supply Undervoltage Negative Going Threshold	2.8				Vcc dropping from 5V
VCCUVH YS	VCC Supply Undervoltage Lockout Hysteresis	0.02	0.3	0.60		
tdUVCC	Undervoltage Lockout Response Time	0.5		20	$\mu sec$	VCC steps either from 6.5V to 2.7V or from 2.7V to 6.5V
IQCC	VCC Supply Current			400	$\mu A$	VCC = 3.6V & 6.5V
<b>VBS Supply Characteristics</b>						
VBSUV+	VBS Supply Undervoltage Positive Going Threshold			4.3	V	VBS rising from 0V
VBSUV-	VBS Supply Undervoltage Negative Going Threshold	2.8				VBS dropping from 5V
VBSUVH YS	VBS Supply Undervoltage Lockout Hysteresis	0.02	0.3	0.60		
tdUVBS	Undervoltage Lockout Response Time	0.5		20	$\mu sec$	VBS steps either from 6.5V to 2.7V or from 2.7V to 6.5V
IQBS1	VBS Supply Current			130	$\mu A$	static mode, VBS = 7V, $I_N = 0V$ or 5V
IQBS2	VBS Supply Current			200	$\mu A$	static mode, VBS = 16V, $I_N = 0V$ or 5V
$\Delta V_{BS}$	VBS Drop Due to Output Turn-On			210	mV	VBS = 7V, CBS = $1\mu F$ , $t_{dIG-IN} = 3\mu sec$ , $t_{TEST} = 100\mu sec$

### Electrical Characteristics

Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ .  
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^\circ C \leq T_j \leq 125^\circ C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver Characteristics						
IPKSo1	Peak Output Source Current	120	250		mA	$T_j = 25^\circ C$ , (Note 2)
IPKSo2	Peak Output Source Current	70	150		mA	(Note 2)
IPKSo3	Peak Output Source Current	250	500		mA	$V_{BS} = 16V$ , $T_j = 25^\circ C^{\dagger\dagger}$
IPKSo4	Peak Output Source Current	150	300		mA	$V_{BS} = 16V^{\dagger\dagger}$
IHO,off	HO off-state leakage current (guaranteed by design)			1	$\mu A$	
tr1	Output Rise Time		0.2	0.4	$\mu sec$	$T_j = 25^\circ C$
tr2	Output Rise Time		0.3	0.5	$\mu sec$	
tr3	Output Rise Time		0.1	0.2	$\mu sec$	$V_{BS} = 16V$ , $T_j = 25^\circ C$
tr4	Output Rise Time		0.15	0.3	$\mu sec$	$V_{BS} = 16V$
IPKSi1	Peak Output Sink Current	120	250		mA	$I_N = 5V$ , $T_j = 25^\circ C^{\dagger\dagger}$
IPKSi2	Peak Output Sink Current	70	150		mA	$I_N = 5V$ , (Note 2)
IPKSi3	Peak Output Sink Current	250	500		mA	$V_{BS} = 16V$ , $I_N = 5V$ , $T_j = 25^\circ C$ , (Note 2)
IPKSi4	Peak Output Sink Current	150	300		mA	$V_{BS} = 16V$ , $I_N = 5V^{\dagger\dagger}$
tf1	Output Fall Time		0.2	0.4	$\mu sec$	$I_N = 5V$ , $T_j = 25^\circ C$
tf2	Output Fall Time		0.3	0.5	$\mu sec$	$I_N = 5V$
tf3	Output Fall Time		0.1	0.2	$\mu sec$	$V_{BS} = 16V$ , $I_N = 5V$ , $T_j = 25^\circ C$
tf4	Output Fall Time		0.15	0.3	$\mu sec$	$V_{BS} = 16V$ , $I_N = 5V$

$\dagger\dagger PW < 10\mu s$



### Electrical Characteristics

Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ .  
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}C \leq T_j \leq 125^{\circ}C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{plh}$	Input-to-Output Turn-On Propagation Delay (50% input level to 10% output level)		0.15	0.35	$\mu sec$	
$t_{phl}$	Input-to-Output Turn-Off Propagation Delay (50% input level to 90% output level)		0.15	0.35	$\mu sec$	
$t_{phl\_res}$	RES-to-Output Turn-Off Propagation Delay (50% input level to 90% $[t_{phl}]$ output levels)		0.15	0.35	$\mu sec$	
$t_{plh\_res}$	RES-to-Output Turn-On Propagation Delay (50% input level to 10% $[t_{plh}]$ output levels)		0.15	0.35	$\mu sec$	

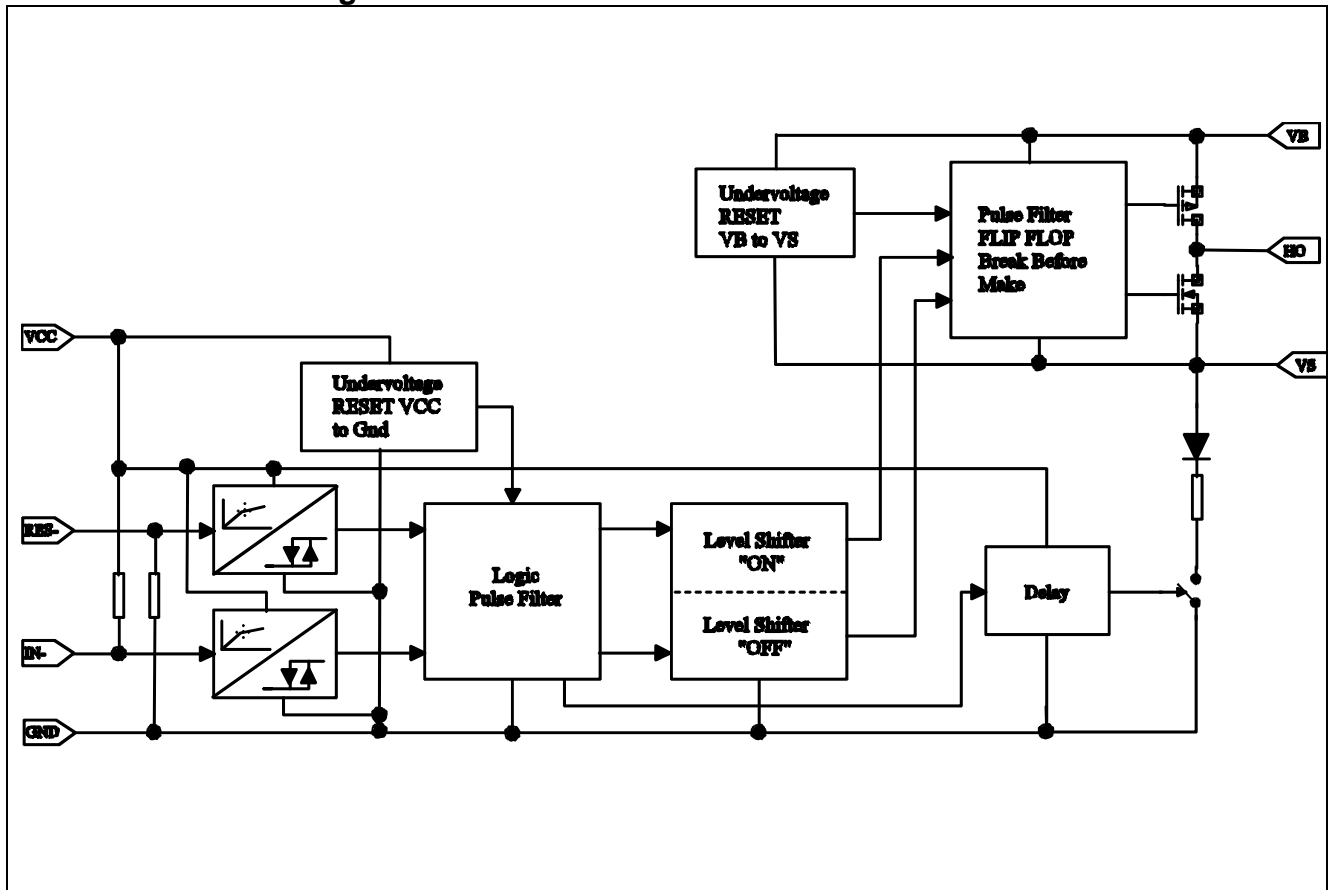
### Electrical Characteristics

Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ .

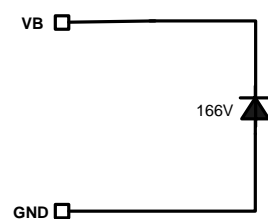
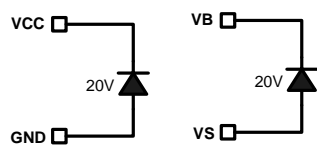
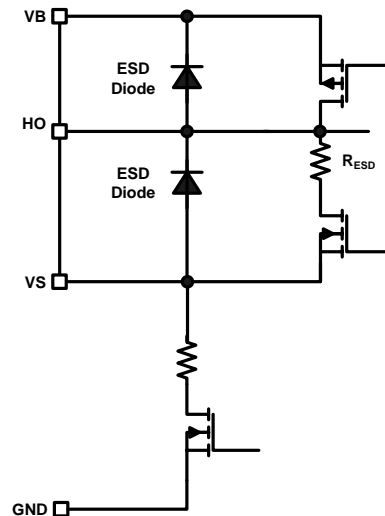
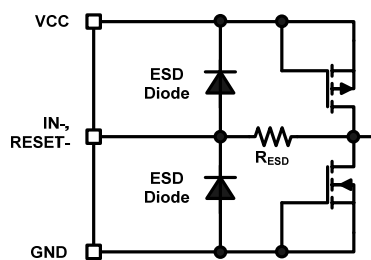
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}C \leq T_j \leq 125^{\circ}C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Input Characteristics</b>						
VINH	High Logic Level Input Threshold	0.6* V <sub>cc</sub>			V	V <sub>CC</sub> =5V
VINL	Low Logic Level Input Threshold			0.28* V <sub>cc</sub>	V	V <sub>CC</sub> =5V
RIN	High Logic Level Input Resistance	60	100	220	k $\Omega$	
IIN	High Logic Level Input Current			5	$\mu A$	V <sub>IN</sub> =V <sub>CC</sub>
VH_RES	High Logic Level RES Input Threshold	3			V	V <sub>CC</sub> =5V
VL_RES	Low Logic Level RES Input Threshold			1.4	V	V <sub>CC</sub> =5V
RRES	High Logic Level RES Input Resistance	60	100	220	k $\Omega$	
IRES	Low Logic Level Input Current			5	$\mu A$	V <sub>RES</sub> =0
<b>Recharge Characteristics</b>						
ton_rech	Recharge Transistor Turn-On Propagation Delay	3	6	9	$\mu sec$	V <sub>S</sub> = 5V
toff_rech	Recharge Transistor Turn-Off Propagation Delay		0.08	0.2	$\mu sec$	
VRECH	Recharge Output Transistor On-State Voltage Drop			1.2	V	I <sub>S</sub> = 1mA, I <sub>N</sub> = 5V.
<b>Deadtime Characteristics</b>						
DTHOFF	High Side Turn-Off to Recharge gate Turn-On	3	6	9	$\mu sec$	V <sub>CC</sub> = 5V, V <sub>BS</sub> = 7V
DTHON	Recharge gate Turn-Off to High Side Turn-On	0.01	0.07	0.4	$\mu sec$	V <sub>CC</sub> = 5V, V <sub>BS</sub> = 7V

# Functional Block Diagram



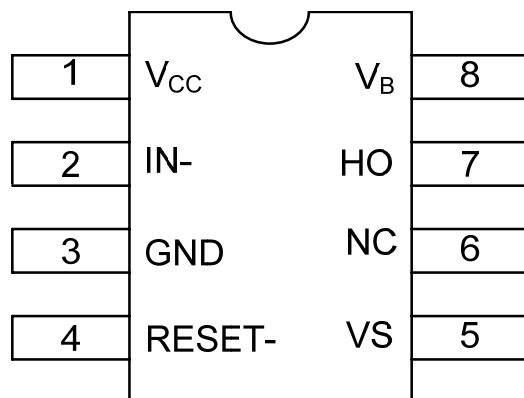
# Input/Output Pin Equivalent Circuit Diagrams



## Lead Definitions

Pin Number	Symbol	Pin description
1	VCC	Driver Supply, typically 5.0V
2	IN-	Driver Control Signal Input (negative logic)
3	GND	Ground
4	RESET-	Driver Enable Signal Input (negative logic)
5	VS	MOSFET Source Connection
6	NC	No Connection (no Bondwire)
7	HO	MOSFET Gate Connection
8	VB	Driver Output Stage Supply

## Lead Assignments



8 Lead SOIC

### Application Information and Additional Details

A Truth table for  $V_{CC}$ ,  $V_{BS}$ , RESET, IN,  $H_O$  and RechFET is shown as follows. This truth table is for ACTIVE LOW IN.

supply voltages and thresholds		Signals		Output $H_O$	Recharge Path
$V_{CC}$	$V_{BS}$	RESET-	IN-		
$< V_{CCUV-}$	X	X	X	OFF	ON
X	X	LOW	X	OFF	ON
X	X	X	HIGH	OFF	ON
$> V_{CCUV+}$	$> V_{BSUV+}$	HIGH	LOW	ON	OFF
$> V_{CCUV+}$	$< V_{BSUV-}$	HIGH	LOW	OFF	OFF

X means independent from signal

RESET = HIGH indicates that high side NMOS is allowed to be turned on.

RESET = LOW indicates that high side NMOS is OFF.

IN = LOW indicates that high side NMOS is on.

IN = HIGH indicates that high side NMOS is off.

RechFET = ON indicates that the recharge MOSFET is on.

RechFET = OFF indicates that the recharge MOSFET is off.

## Timing Diagrams

### Input / Output

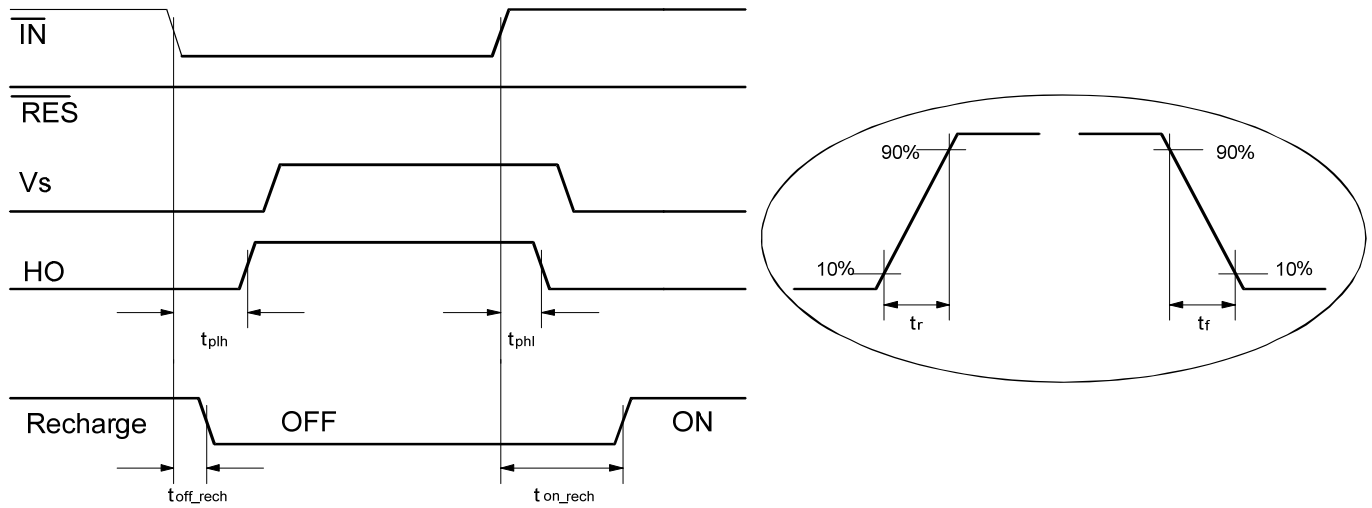


Figure 3: Input/Output Timing Diagram

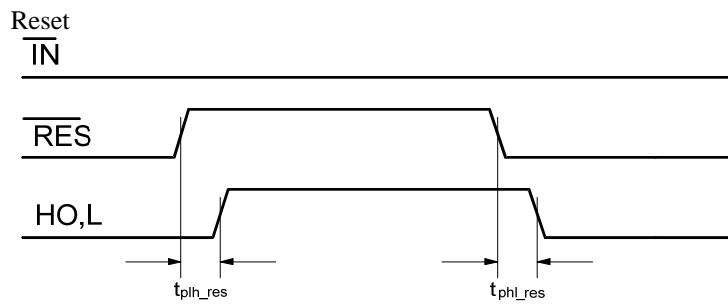
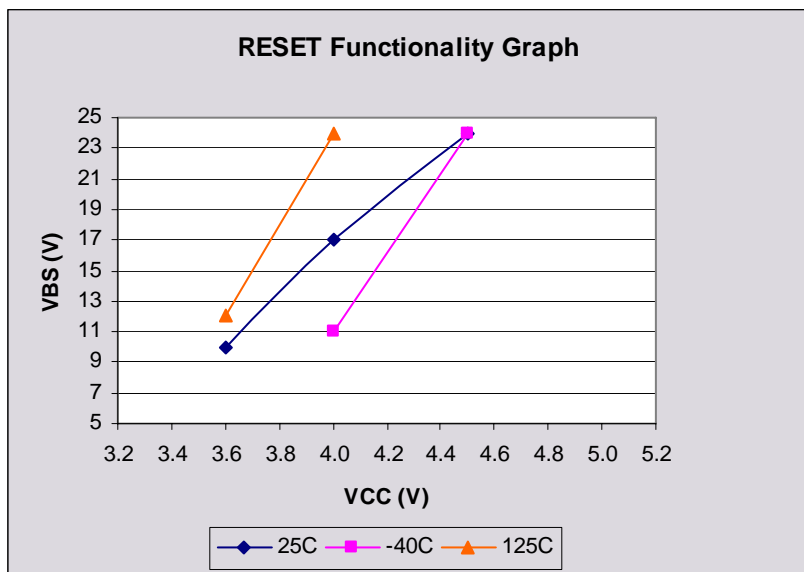


Figure 4: Reset Timing Diagram

## Performance Graphs

### RESET Functionality Graph:



**Figure 6. RESET Functionality:**

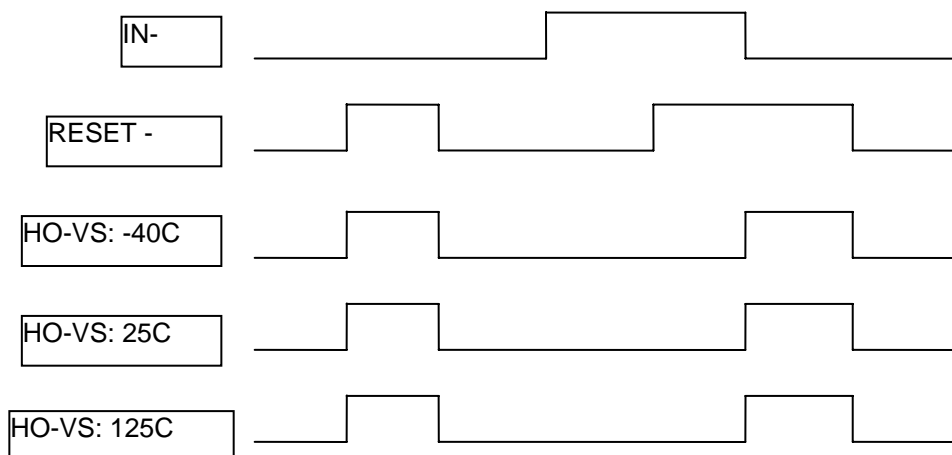
This graph explains the functionality limitation as a function of VCC, VBS and temperature.

For each particular temperature and VCC, the output is non-functional for any value of VBS above the drawn curve. But for any value of VBS below the curve the functionality is fine.

### RESET Functional Diagram:

The diagram is guaranteed for the following condition:

VCC=4.28V to 20V; VBS= 2V to 20V @ Tj= -40°C to +125°C (TBD)





Input and Reset Thresholds:

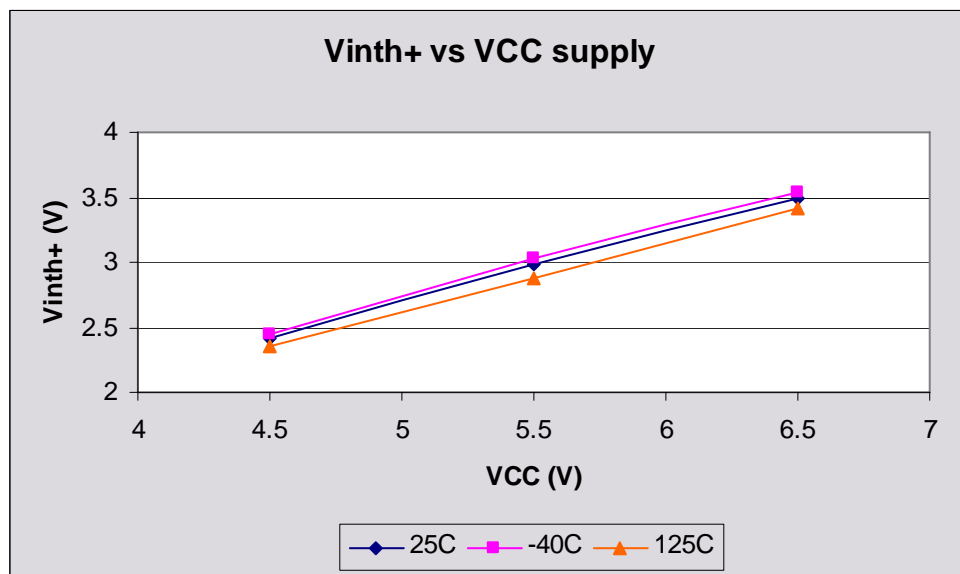


Figure 7-1: Positive Input and Reset Threshold Voltage Distribution Curves

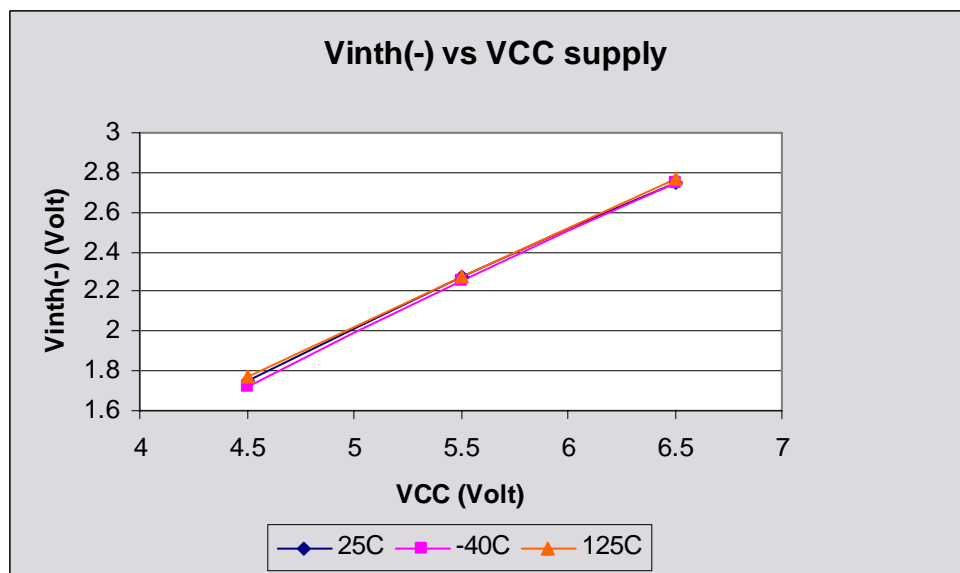


Figure 7-2: Negative Input and Reset Threshold Voltage Distribution Curves

$V_{B_{UV}}$  Undervoltage Shutdown Threshold  $V_B$ : TBD

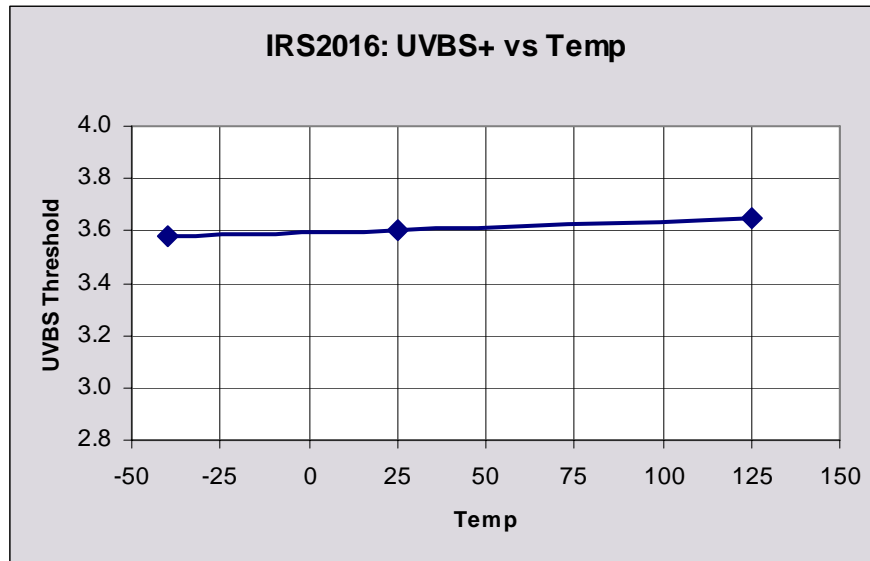


Figure 8-1: Positive going  $V_{B_{UV}}$  value vs. Temperature: TBD

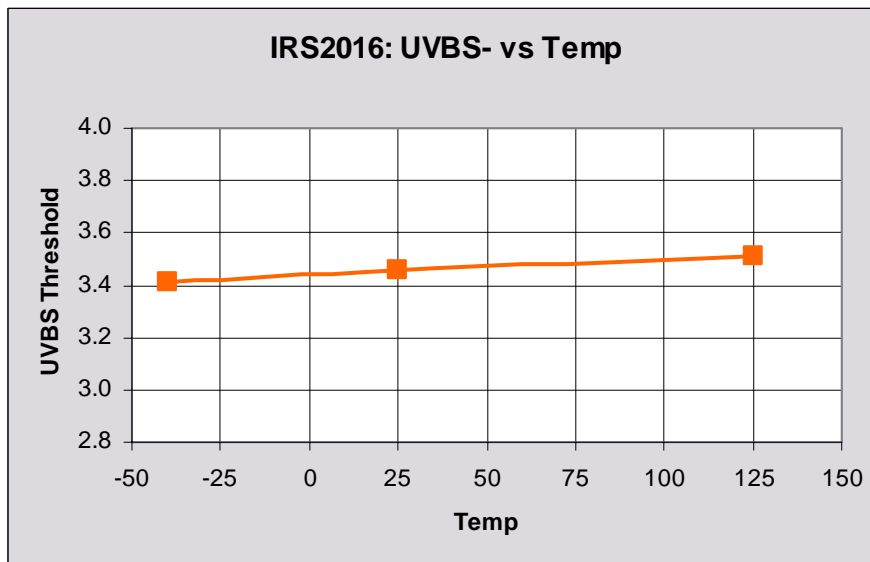


Figure 8-2: Negative going  $V_{B_{UV}}$  Value vs. Temperature

Input and Reset Impedance

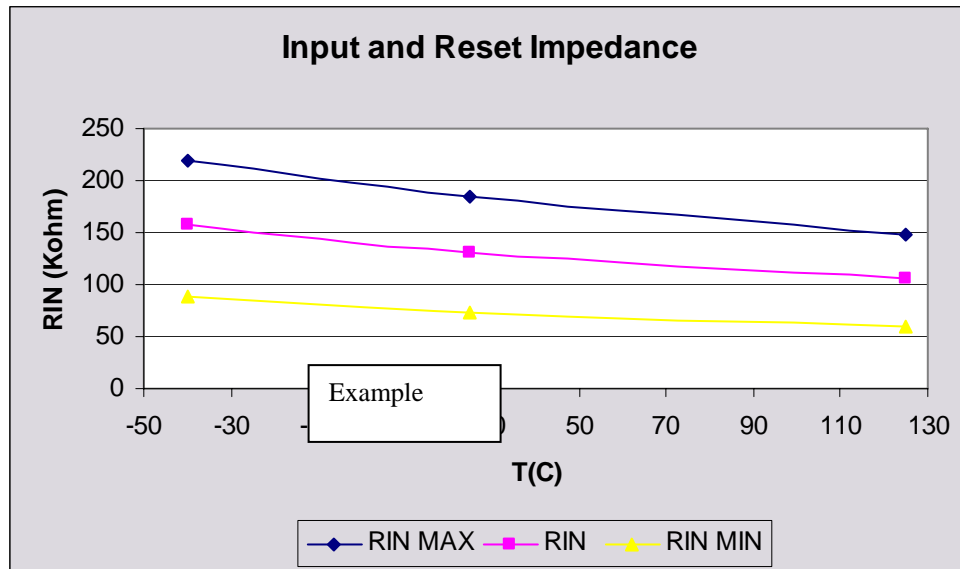


Figure 9: Input and Reset Impedance Distribution Curves

Recharge FET I-V Curve at -40C, 25C and 125C

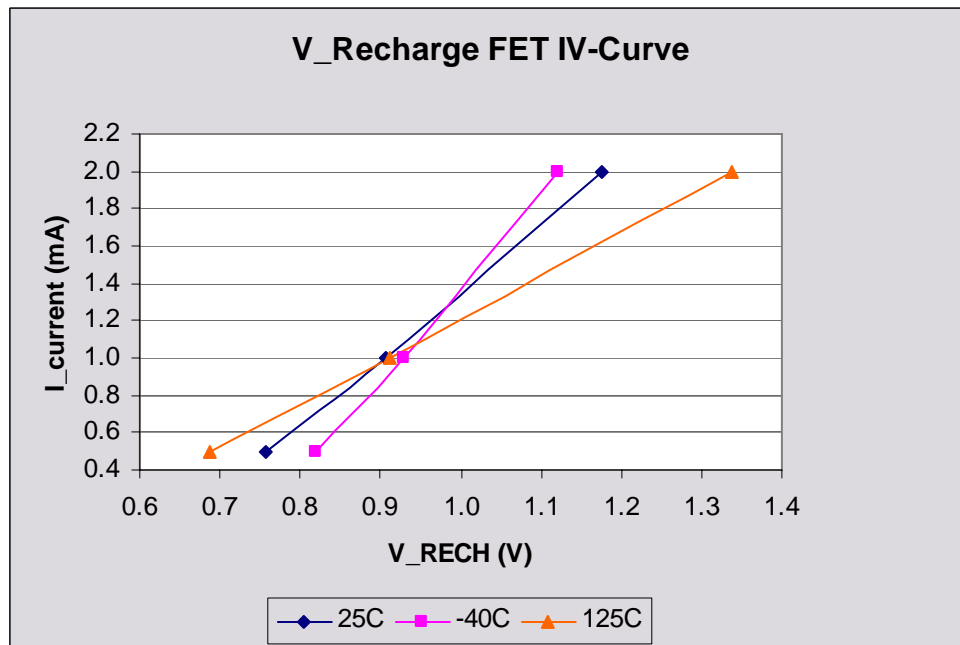
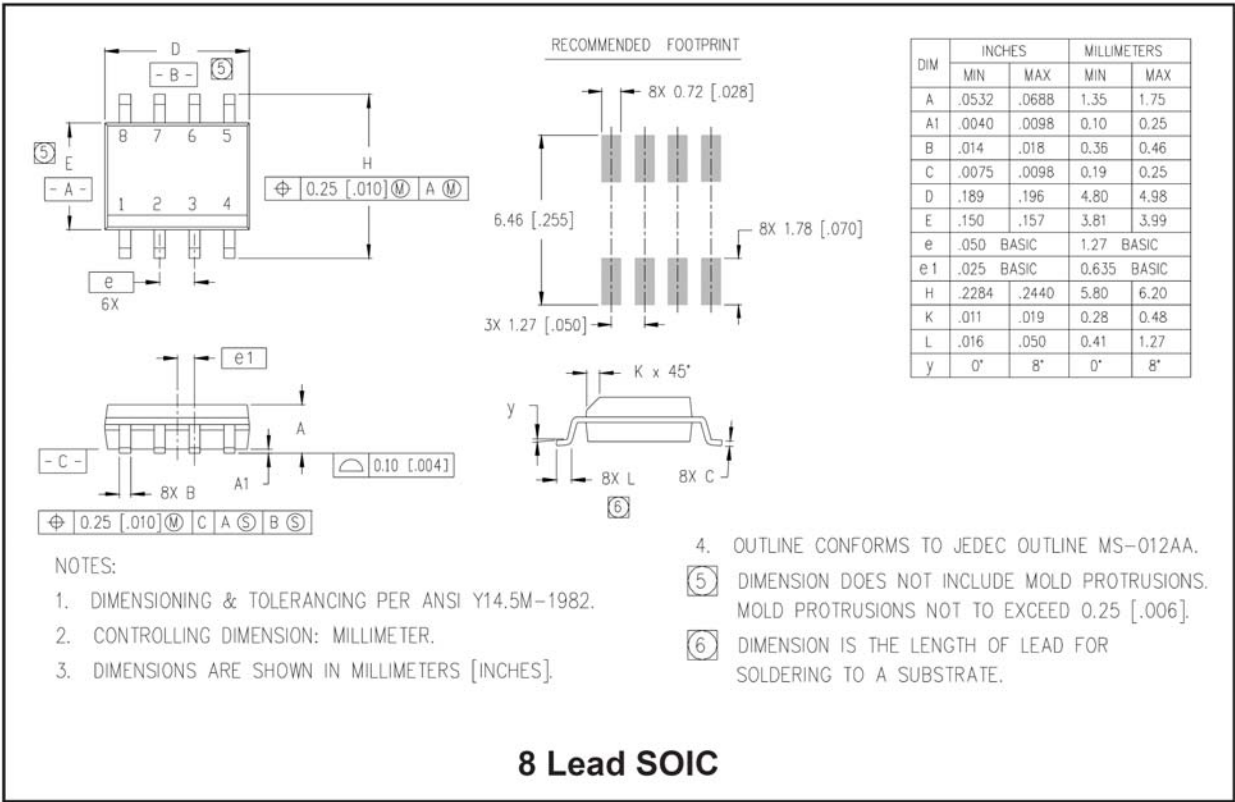
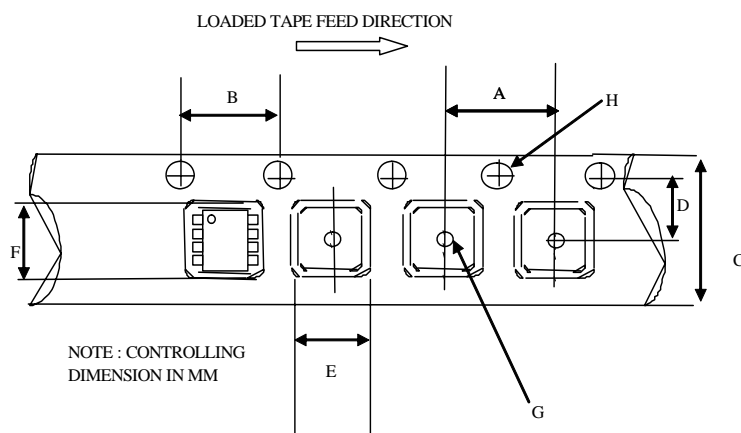


Figure 10: Recharge FET IV-Curve

**Package Details: SOIC8**

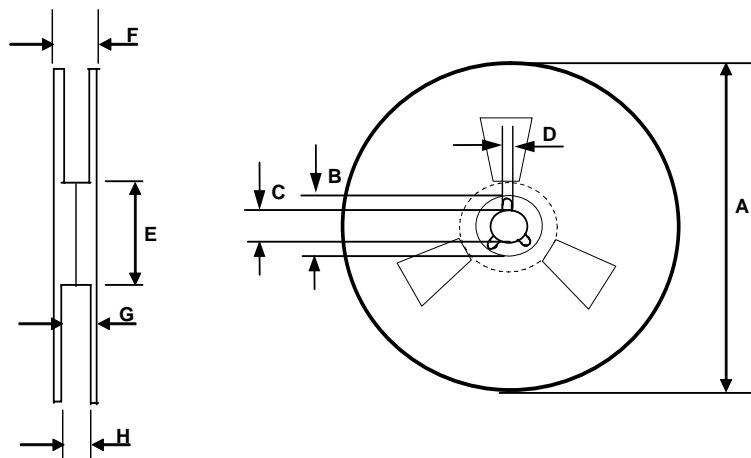


**Tape and Reel Details: SOIC8**



CARRIER TAPE DIMENSION FOR 8SOICN

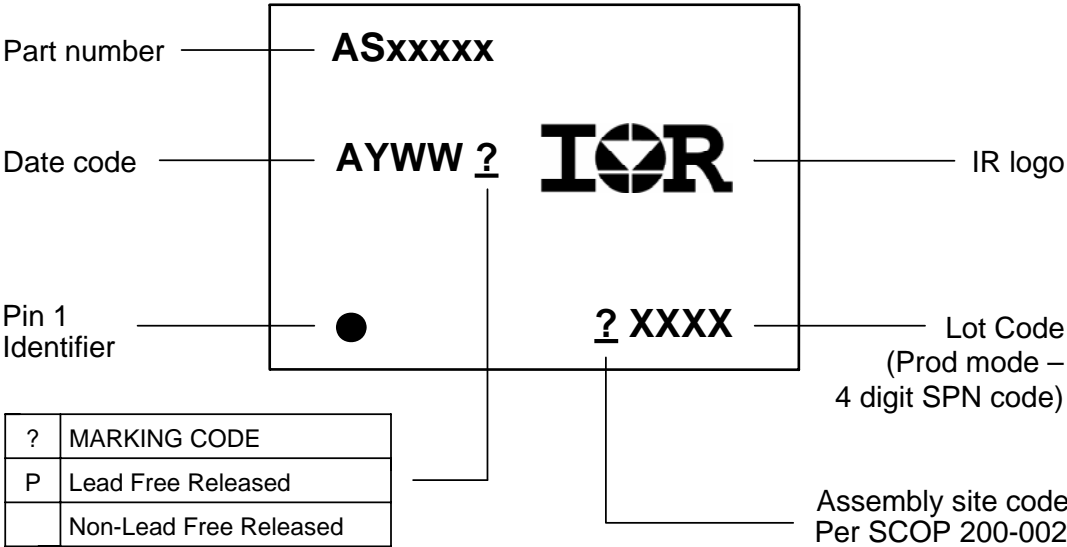
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2016S(TR)	SOIC8	Tube/Bulk	95	AUIRS2016S
		Tape and Reel	2500	AUIRS2016STR

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