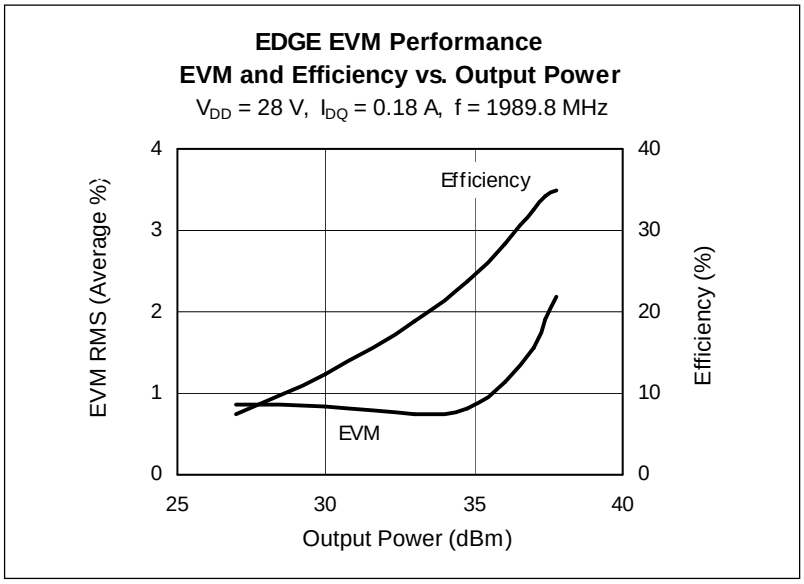
green Product

LDMOS RF Power Field Effect Transistor
10 W, 1805 – 1880 MHz, 1930 – 1990 MHz
10 W, 2110 – 2170 MHz

Description

The PTF180101S is a 10-watt, internally-matched *GOLDMOS*® FET device intended for EDGE applications in the DCS/PCS band. Full gold metallization ensures excellent device lifetime and reliability.

PTF180101S
Package H-32259-2



Features

- RoHS-compliant, Pb-free package
- Typical EDGE performance
  - Average output power = 4.0 W
  - Gain = 19.0 dB
  - Efficiency = 28%
  - EVM = 1.1 %
- Typical WCDMA performance
  - Average output power = 1.8 W
  - Gain = 18.0 dB
  - Efficiency = 20%
  - ACPR = –45 dBc
- Typical CW performance
  - Output power at P–1dB = 15 W
  - Efficiency = 50%
- Integrated ESD protection: Human Body Model Class 1 (minimum)
- Low HCI drift, excellent thermal stability
- Capable of handling 10:1 VSWR @ 28 V, 10 W (CW) output power

RF Characteristics, EDGE Operation

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 180 mA, P_{OUT} = 4 W, f = 1989.8 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Error Vector Magnitude	EVM (RMS)	—	1.1	—	%
Modulation Spectrum @ 400 kHz	ACPR	—	–60	—	dBc
Modulation Spectrum @ 600 kHz	ACPR	—	–70	—	dBc
Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	28	—	%

table continued on next page

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics, EDGE Operation (cont.)

Two-tone Measurements (tested in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 180 mA, P_{OUT} = 10 W PEP, f = 1990 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18	19	—	dB
Drain Efficiency	η_D	30	33	—	%
Intermodulation Distortion	IMD	—	–30	–28	dBc

RF Characteristics, WCDMA Operation

WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 135 mA, P_{OUT} = 1.8 W,
f = 2170 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8.7 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Adjacent Channel Power Ratio	ACPR	—	–45	—	dBc
Gain	G_{ps}	—	18	—	dB
Drain Efficiency	η_D	—	20	—	%

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 135 mA, P_{OUT} = 10 W PEP, f = 2170 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	18	—	dB
Drain Efficiency @ –30 dBc IM3	η_D	—	37	—	%
Intermodulation Distortion	IMD	—	–30	—	dBc

DC Characteristincs

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 A	$R_{DS(on)}$	—	0.83	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 180 mA	V_{GS}	2.5	3.2	4.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

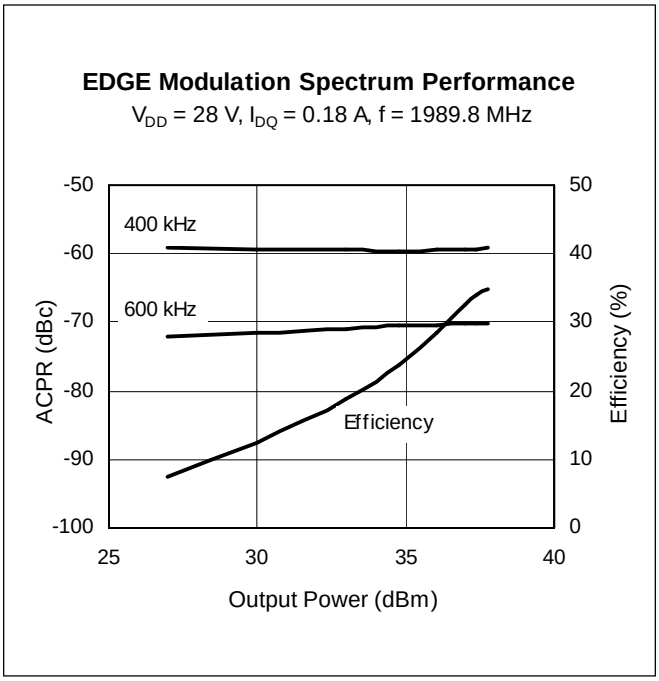
Maximum Ratings

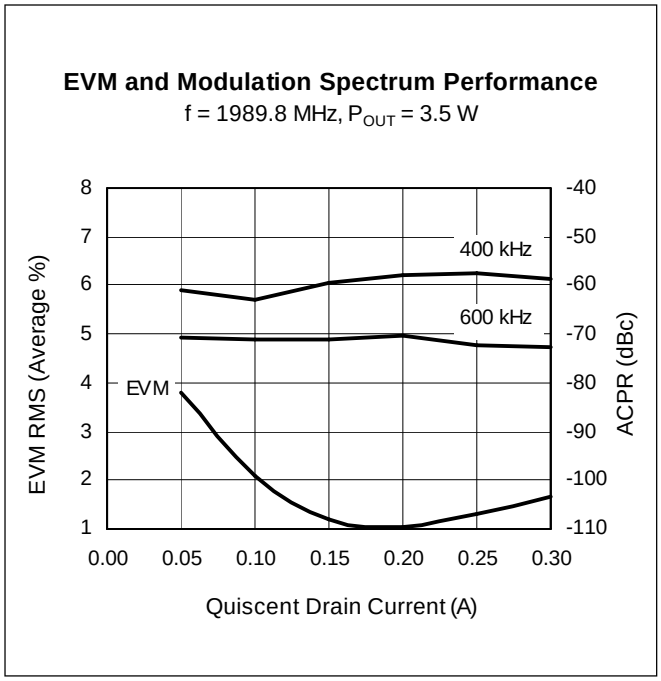
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	58	W
Above 25°C derate by		0.333	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 10 W CW)	$R_{\theta JC}$	3.0	°C/W

Ordering Information

Type	Package Outline	Package Description	Marking
PTF180101S	H-32259-2	Thermally enhanced, surface mount	PTF180101S

Typical Performance measurements taken in broadband test fixture

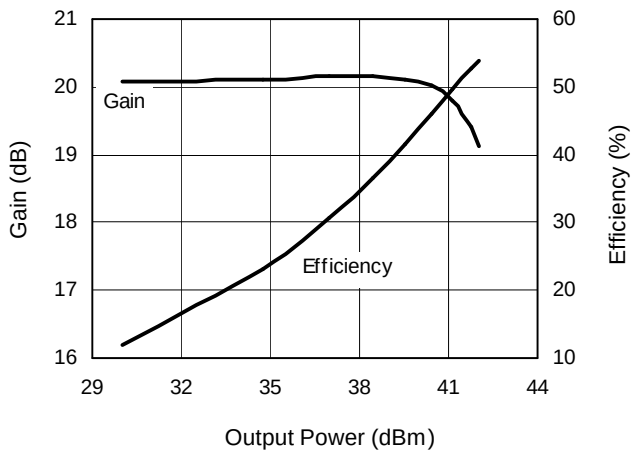




Typical Performance (cont.)

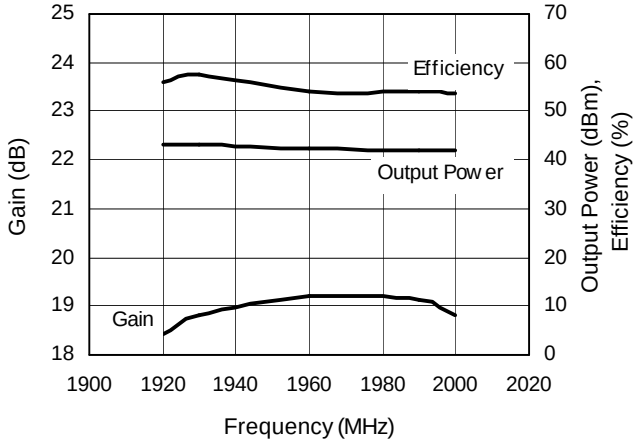
Gain & Efficiency vs. Output Power

V_{DD} = 28 V, I_{DQ} = 0.18 A, f = 1990 MHz



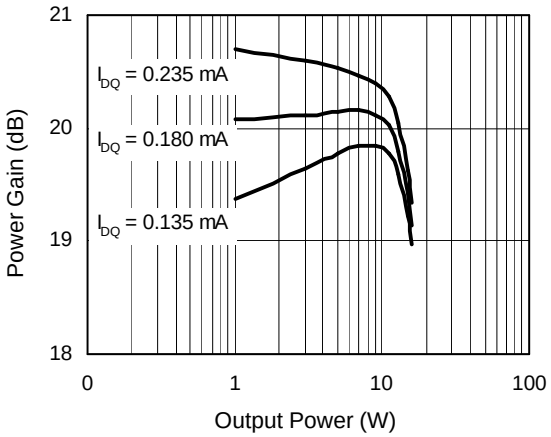
Output Power, Gain & Efficiency (at P-1dB) vs. Frequency

V_{DD} = 28 V, I_{DQ} = 0.18 A



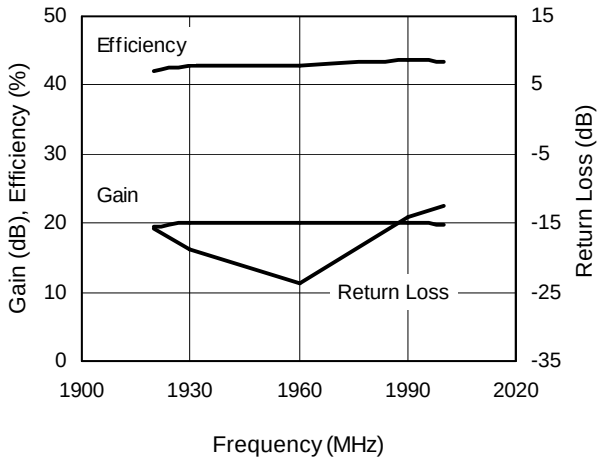
Power Gain vs. Output Power

V_{DD} = 28 V, f = 1990 MHz



Broadband Test Fixture Performance

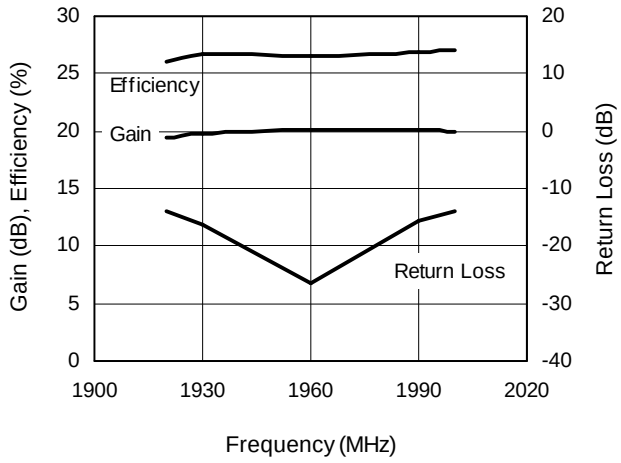
V_{DD} = 28 V, I_{DQ} = 0.18 A, P_{OUT} = 10 W



Typical Performance (cont.)

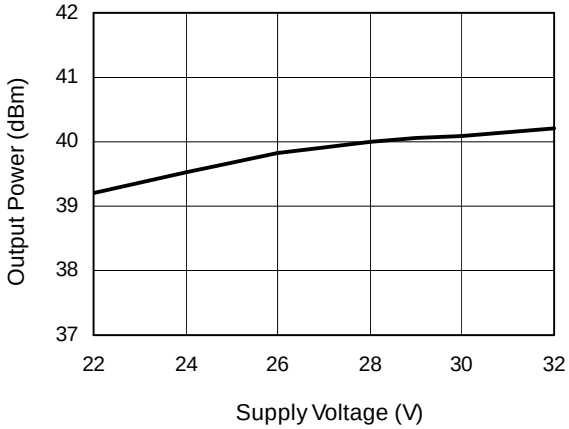
Broadband Test Fixture Performance

V_{DD} = 28 V, I_{DQ} = 0.18 A, P_{OUT} = 4 W



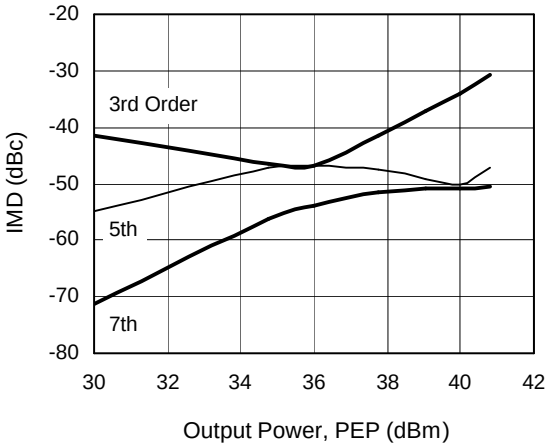
Output Power vs. Supply Voltage

I_{DQ} = 0.18 A, f = 1990 MHz



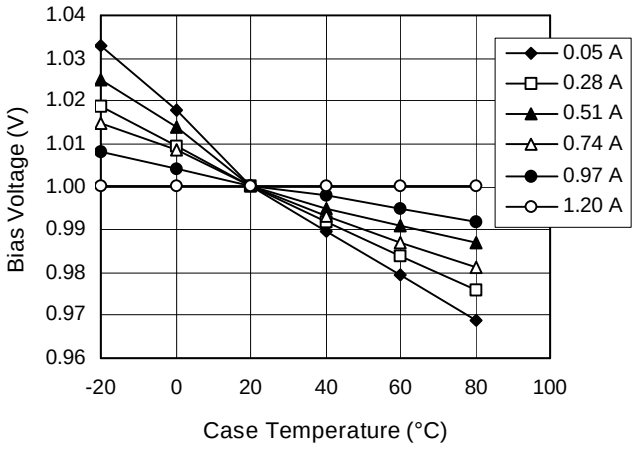
Intermodulation Distortion vs. Output Power

V_{DD} = 28 V, I_{DQ} = 0.18 A, f_1 = 1990 MHz, f_2 = 1991 MHz

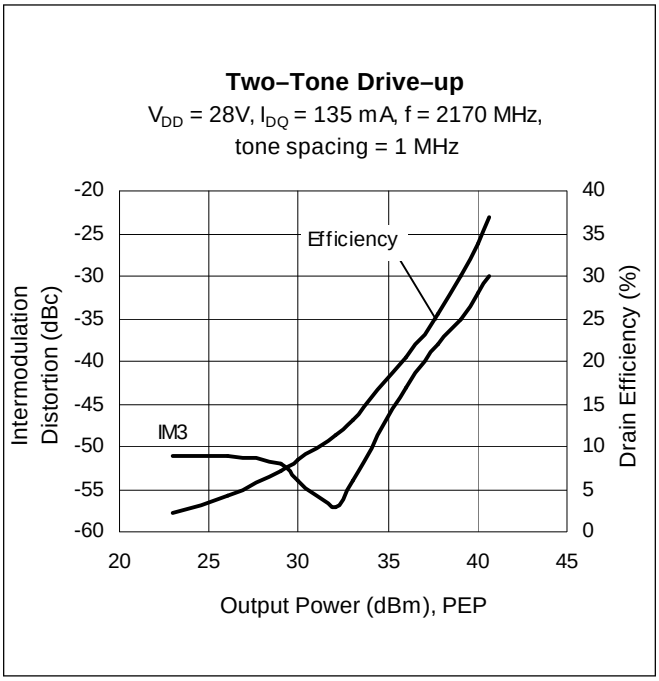


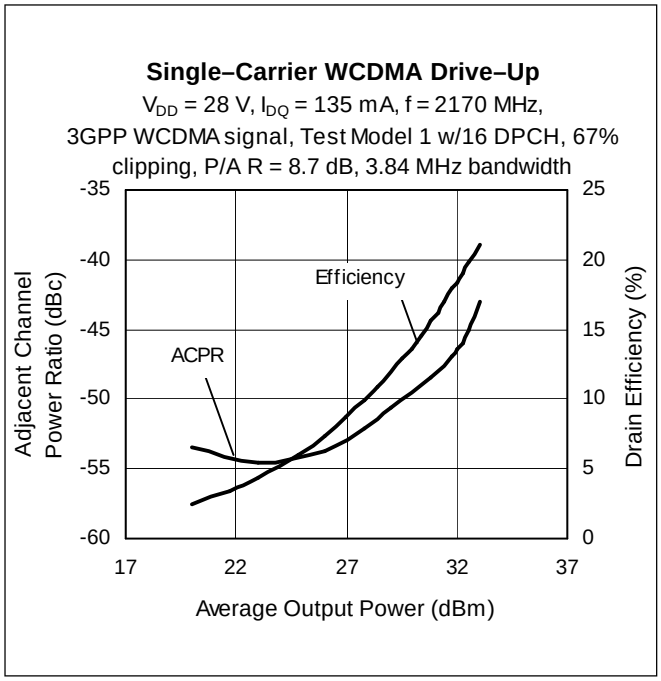
Gate-Source Voltage vs. Case Temperature

Voltage normalized to 1.0 V, series show current

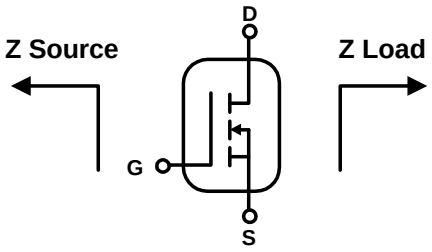


Typical Performance, WCDMA Operation

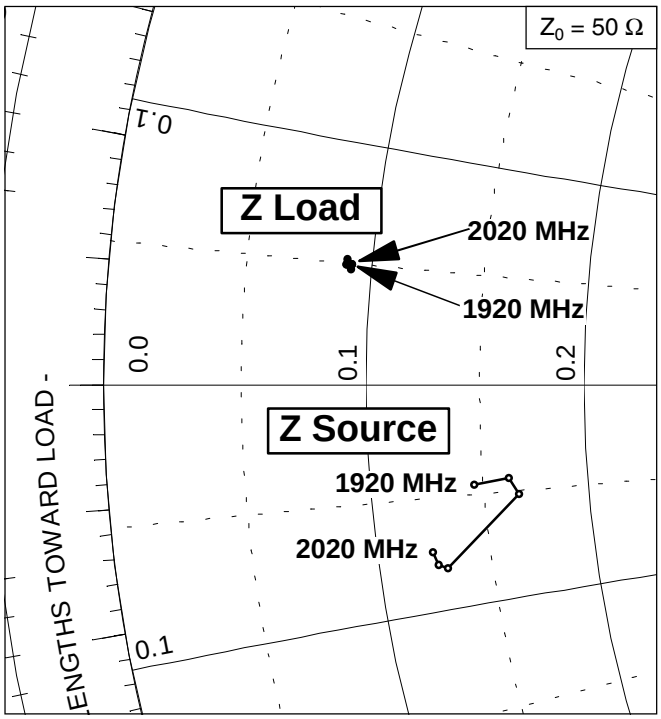




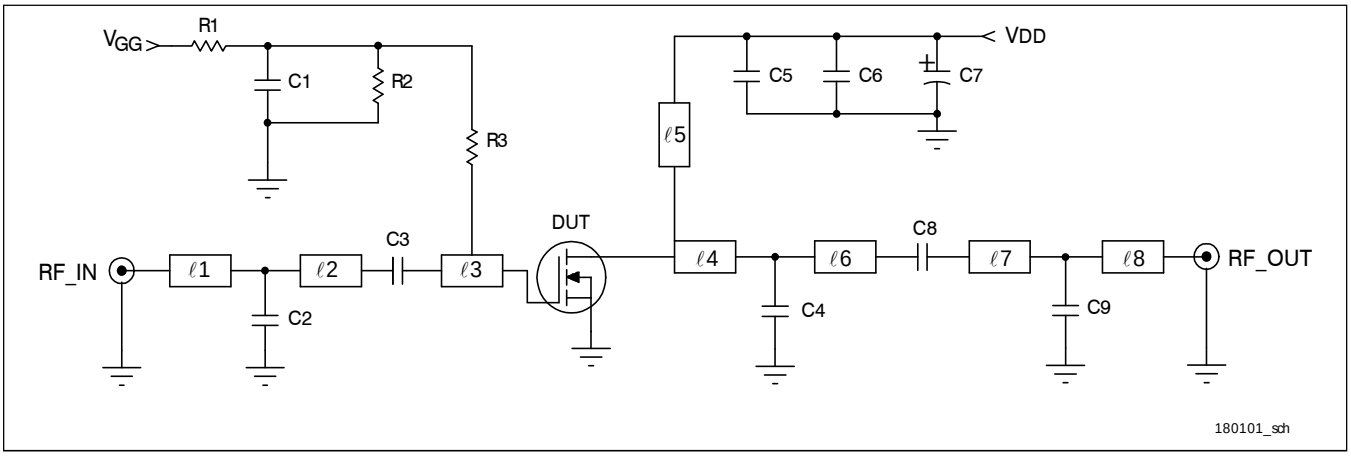
Broadband Circuit Impedance Data



Frequency	Z Source W		Z Load W	
MHz	R	jX	R	jX
1920	7.3	-2.3	4.6	2.4
1930	8.1	-2.2	4.6	2.5
1960	8.3	-2.6	4.5	2.6
1990	6.5	-4.1	4.5	2.5
2000	6.3	-4.0	4.5	2.5
2020	6.2	-3.7	4.6	2.5



Reference Circuits



Reference circuit schematic for 1990 MHz

Circuit Assembly Information

DUT	PTF180101S	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	Rogers TMM4, 2 oz. Copper	

Microstrip	Electrical Characteristics at 1990 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.133 λ, 50 Ω	10.92 x 1.37	0.430 x 0.054
ℓ2	0.096 λ, 50 Ω	7.87 x 1.37	0.310 x 0.054
ℓ3	0.155 λ, 9.5 Ω	11.30 x 12.45	0.445 x 0.490
ℓ4	0.008 λ, 12.8 Ω	0.64 x 8.86	0.025 x 0.349
ℓ5	0.286 λ, 70 Ω	23.88 x 0.71	0.940 x 0.028
ℓ6	0.247 λ, 12.8 Ω	18.29 x 8.86	0.720 x 0.349
ℓ7	0.145 λ, 50 Ω	11.81 x 1.37	0.465 x 0.054
ℓ8	0.008 λ, 50 Ω	0.64 x 1.37	0.025 x 0.054

[1]Electrical characteristics are rounded.

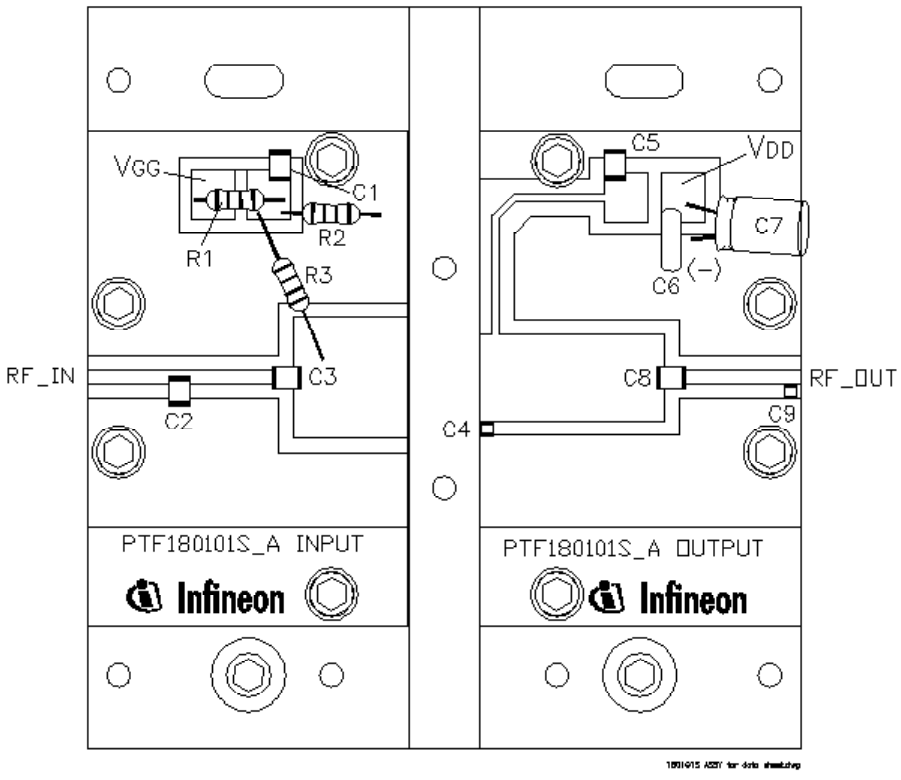
Reference Circuits (cont.)

1930 – 1990 MHz Operation

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C3, C5, C8	Capacitor, 10 pF	ATC	100B 100
C2	Capacitor, 1.7 pF	ATC	100B 1R7
C4	Capacitor, 2.0 pF	ATC	100A 2R0
C6	Capacitor, 0.1 µF, 50 V	Digi-Key	P4525-ND
C7	Capacitor, 100 µF, 50 V	Digi-Key	P5182-ND
C9	Capacitor, 0.6 pF	ATC	100A 0R6
R1, R2, R3	Resistor, 220 ohm, 1/4 W	Digi-Key	220QBK

2.11 – 2.17 GHz Operation

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C3, C5, C8	Capacitor, 10 pF	ATC	100B 100
C2	Capacitor, 0.8 pF	ATC	100B 0R8
C4	Capacitor, 2.2 pF	ATC	100A 2R2
C6	Capacitor, 0.1 µF, 50 V	Digi-Key	P4525-ND
C7	Capacitor, 100 µF, 50 V	Digi-Key	P5182-ND
C9	Capacitor, 1.0 pF	ATC	100A 1R0
R1, R2, R3	Resistor, 220 ohm, 1/4 W	Digi-Key	220QBK



Reference circuit assembly diagram (not to scale)*

**Gerber files for this circuit are available upon request.*

Package Outline Specifications

Package H-32259-2

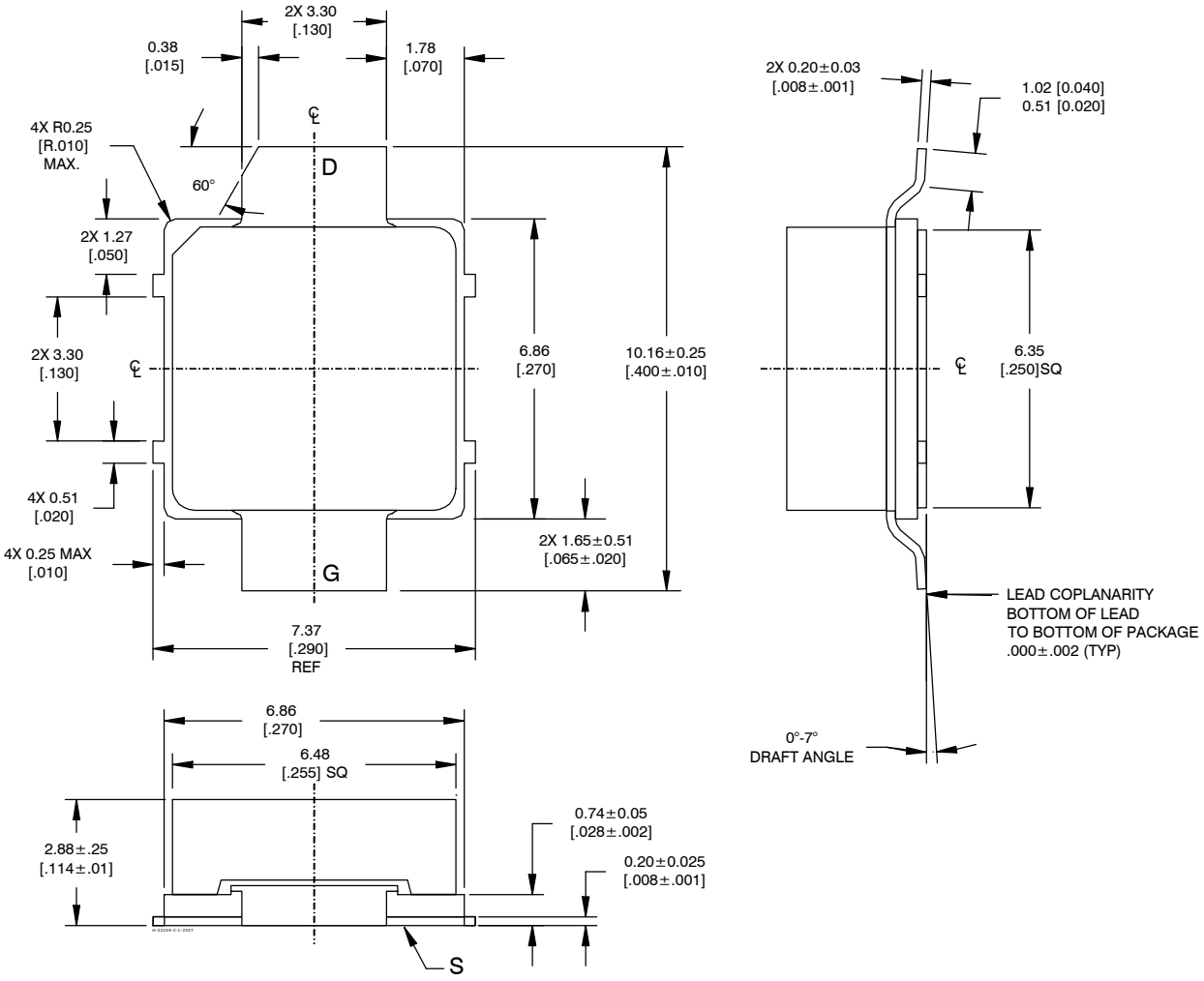


Diagram Notes—unless otherwise specified:

1. Lead thickness: 0.21 ± 0.03 [.008 ± .001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.

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PTF180101S
Confidential, Limited Internal Distribution
Revision History: 2007-03-01 Data Sheet
Previous Version: 2004-02-03

Page	Subjects (major changes since last revision)
all	Update document format
1	Add RoHS-compliant information.
9	Correct package diagram and dimensions.

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