

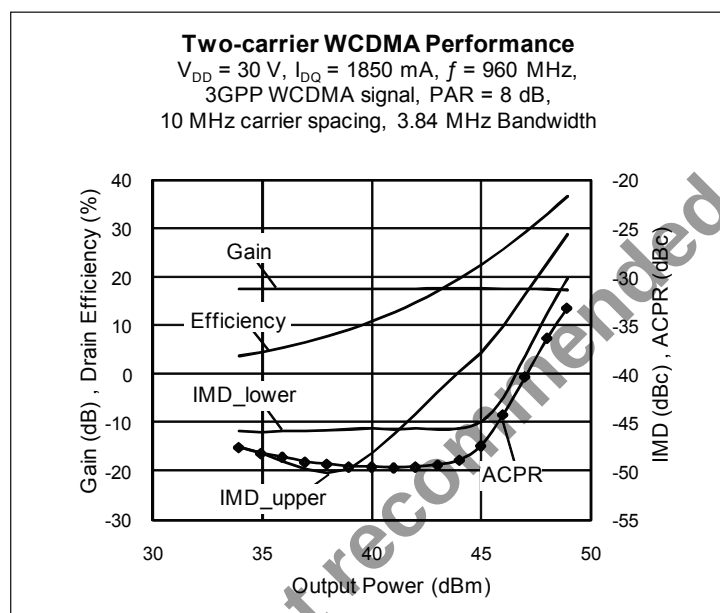
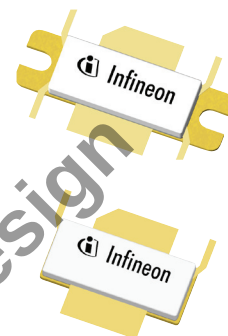
Thermally-Enhanced High Power RF LDMOS FETs 220 W, 920 – 960 MHz

Description

The PTFA092213EL and PTFA092213FL are 220-watt, internally-matched LDMOS FETs designed for use in cellular power amplifier applications in the 920 to 960 MHz band. These devices feature internal I/O matching and thermally-enhanced open-cavity ceramic packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA092213EL
Package H-33288-6

PTFA092213FL
Package H-34288-4/2



Features

- Broadband internal matching
- Typical two-carrier WCDMA performance at 960 MHz, 30 V
 - Average output power = 50 W
 - Linear Gain = 17.5 dB
 - Efficiency = 29%
 - Intermodulation distortion = -32 dBc
 - Adjacent channel power = -42.5 dBc
- Typical CW performance, 960 MHz, 30 V
 - Output power at $P_{1dB} = 250\text{ W}$
 - Linear Gain = 17.5 dB
 - Efficiency = 52%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 30 V, 220 W (CW) output power
- Pb-free, RoHS-compliant

RF Characteristics

Two-carrier WCDMA Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
 $V_{DD} = 30\text{ V}$, $I_{DQ} = 1850\text{ mA}$, $P_{OUT} = 50\text{ W}$ average, $f_1 = 950\text{ MHz}$, $f_2 = 960\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	17.5	—	dB
Drain Efficiency	η_D	—	29	—	%
Intermodulation Distortion	IMD	—	-32	—	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 30\text{ V}$, $I_{DQ} = 1850\text{ mA}$, $P_{OUT} = 200\text{ W PEP}$, $f = 960\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	17	17.5	—	dB
Drain Efficiency	η_D	40	42	—	%
Intermodulation Distortion	IMD	—	−30	−28	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.04	—	Ω
Operating Gate Voltage	$V_{DS} = 30\text{ V}$, $I_{DQ} = 1850\text{ mA}$	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

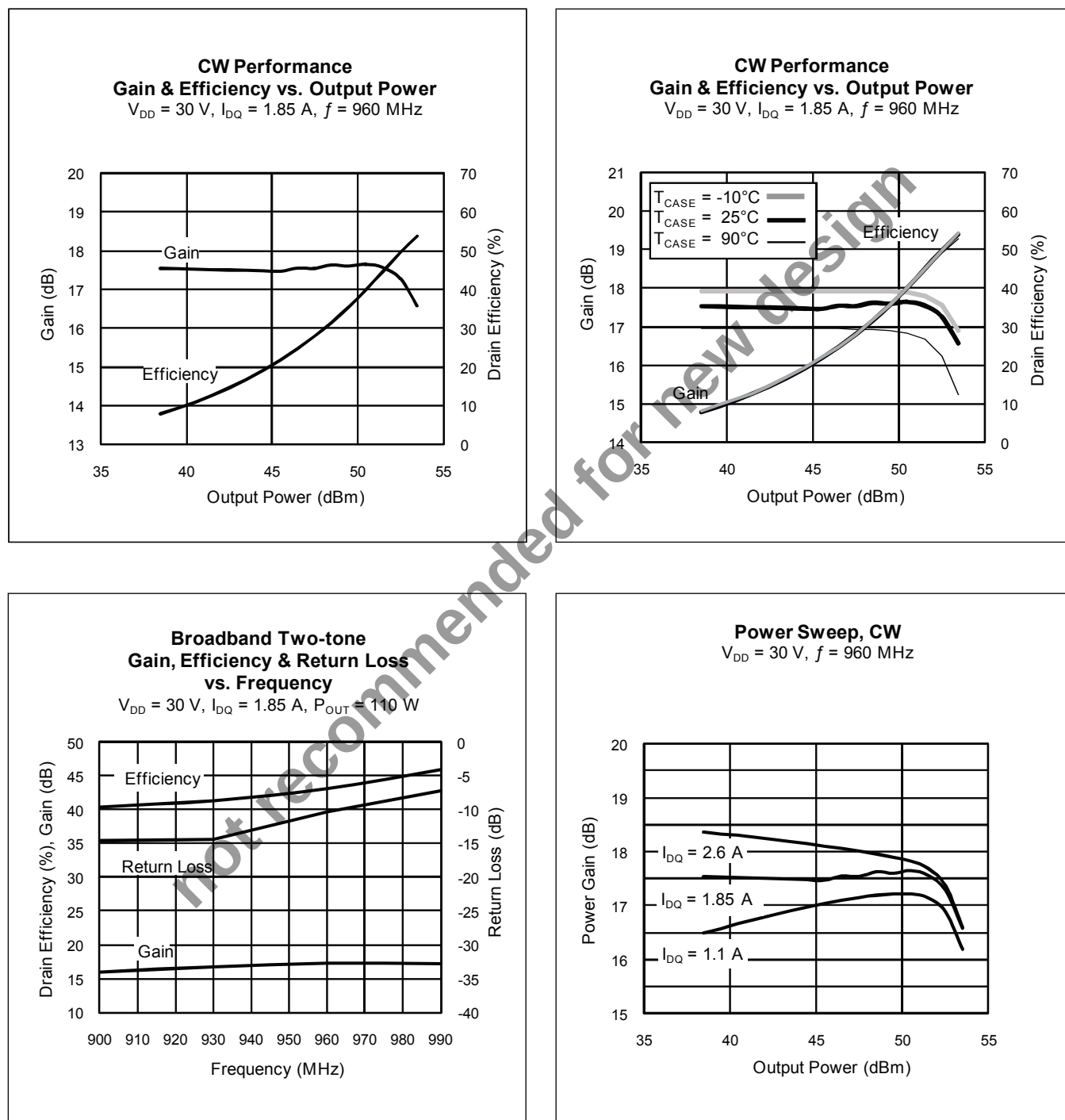
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	−0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70\text{ }^{\circ}\text{C}$, 220 W CW)	$R_{\theta JC}$	0.23	$^{\circ}\text{C/W}$

Ordering Information

Type and Version	Package Outline	Package Description	Shipping
PTFA092213EL V4	H-33288-6	Thermally-enhanced, slotted flange, single-ended	Tray
PTFA092213EL V4 R250	H-33288-6	Thermally-enhanced, slotted flange, single-ended	Tape & Reel, 250 pcs
PTFA092213FL V5	H-34288-4/2	Thermally-enhanced, earless flange, single-ended	Tray
PTFA092213FL V5 R250	H-34288-4/2	Thermally-enhanced, earless flange, single-ended	Tape & Reel, 250 pcs

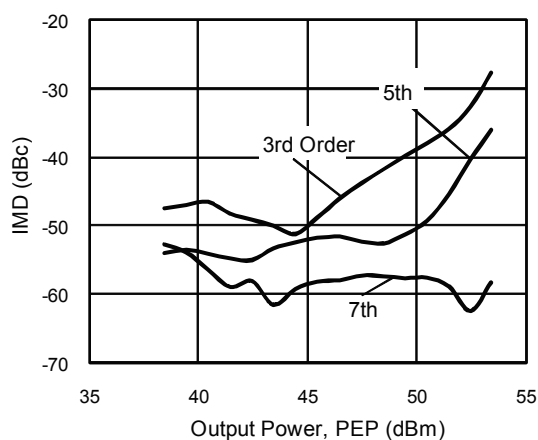
Typical Performance



Typical Performance (cont.)

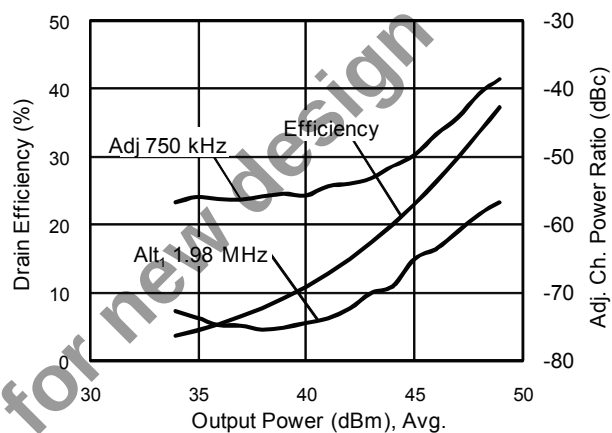
Intermodulation Distortion vs. Output Power

$V_{DD} = 30\text{ V}$, $I_{DQ} = 1.85\text{ A}$,
 $f_1 = 960\text{ MHz}$, $f_2 = 959\text{ MHz}$



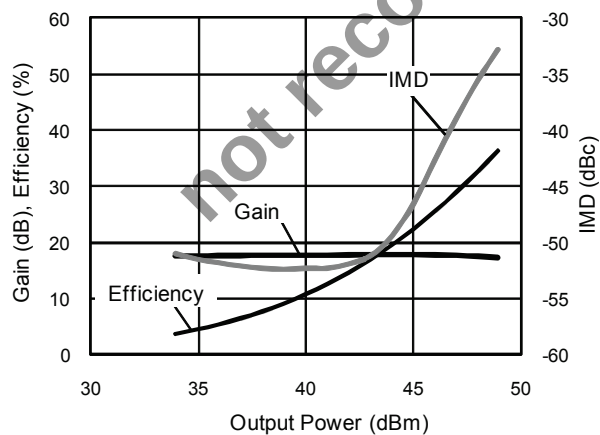
IS-95 CDMA Performance

$V_{DD} = 30\text{ V}$, $I_{DQ} = 1.85\text{ A}$, $f = 960\text{ MHz}$

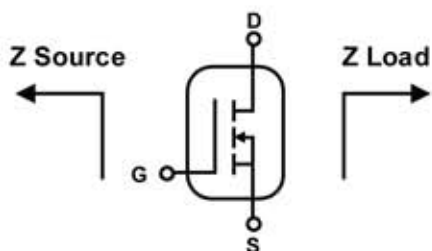


Single-carrier WCDMA Performance

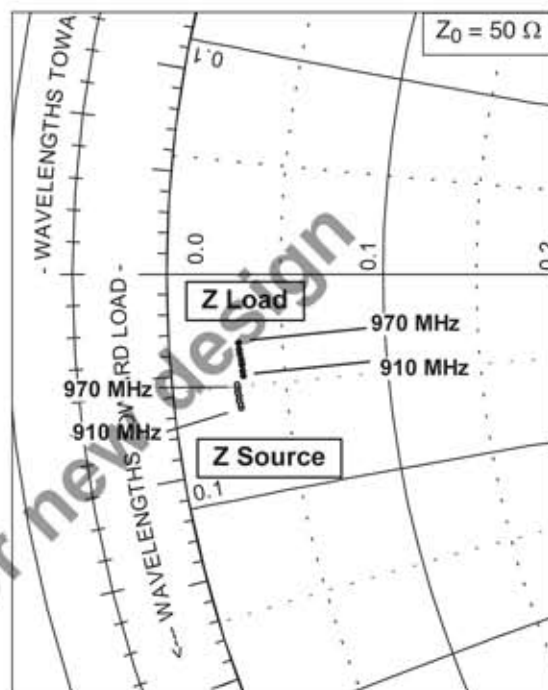
$V_{DD} = 30\text{ V}$, $I_{DQ} = 1850\text{ mA}$, $f = 960\text{ MHz}$,
3GPP WCDMA signal, PAR = 8.5 dB,
3.84 MHz Bandwidth



Broadband Circuit Impedance

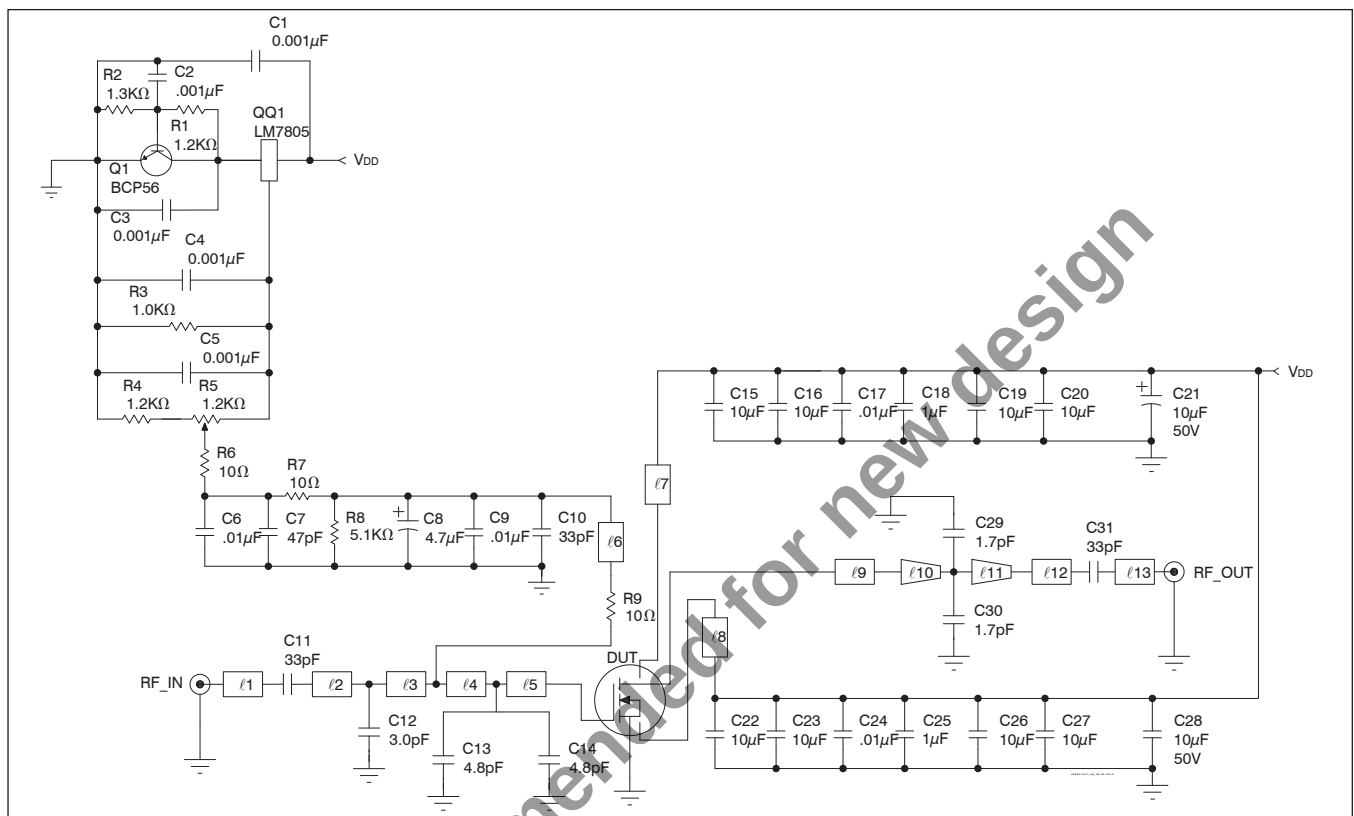


Frequency MHz	Z Source Ω		Z Load Ω	
	R	jX	R	jX
910	1.44	-3.01	1.57	-2.30
920	1.43	-2.92	1.56	-2.18
930	1.42	-2.83	1.55	-2.05
940	1.42	-2.74	1.54	-1.93
950	1.41	-2.66	1.53	-1.81
960	1.41	-2.57	1.52	-1.69
970	1.41	-2.48	1.51	-1.56



See next page for reference circuit information

Reference Circuit



Reference circuit block diagram for $f = 960 \text{ MHz}$

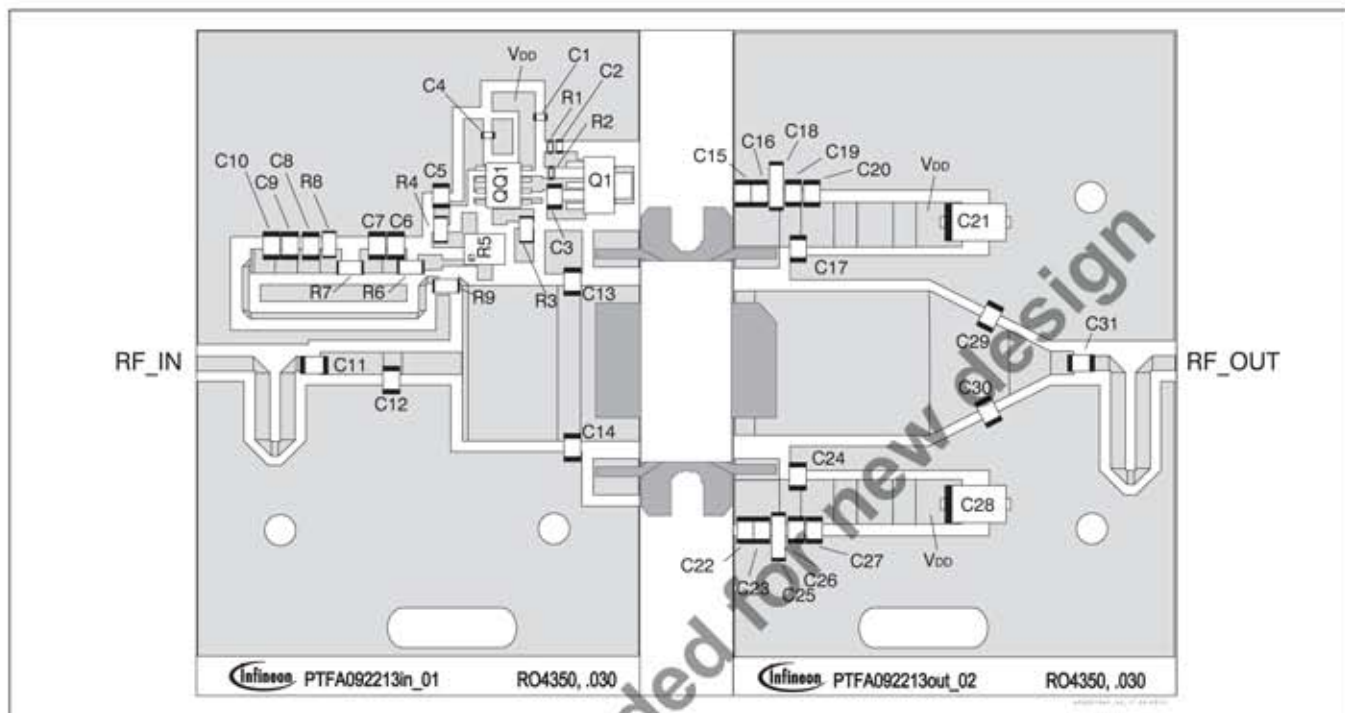
Circuit Assembly Information

DUT	PTFA092213EL or PTFA092213FL	
PCB	LTN/PTFA092213EF	0.76 mm [.030"] thick, $\epsilon_r = 3.48$, Rogers RO4350, 1 oz. copper

Electrical Characteristics at 960 MHz

Transmission Line	Electrical Characteristics	Dimensions: L x W (mm)	Dimensions: L x W (in.)
$\ell1$	0.167λ , 50.1Ω	31.75 x 1.65	1.250 x 0.065
$\ell2$	0.047λ , 38.0Ω	8.38 x 2.54	0.330 x 0.100
$\ell3$	0.039λ , 38.0Ω	7.37 x 2.54	0.290 x 0.100
$\ell4$	0.072λ , 7.8Ω	12.45 x 17.78	0.490 x 0.700
$\ell5$	0.046λ , 7.8Ω	7.87 x 17.78	0.310 x 0.700
$\ell6$	0.163λ , 78.3Ω	31.75 x 0.74	1.250 x 0.029
$\ell7, \ell8$	0.043λ , 23.5Ω	7.75 x 4.95	0.305 x 0.195
$\ell9$	0.130λ , 8.3Ω	22.61 x 16.51	0.890 x 0.650
$\ell10$ (taper)	0.032λ , $8.3 \Omega / 11.7 \Omega$	5.72 x 16.51 / 11.30	0.225 x 0.650 / 0.445
$\ell11$ (taper)	0.053λ , $11.7 \Omega / 37.0 \Omega$	9.78 x 11.30 / 2.64	0.385 x 0.445 / 0.104
$\ell12$	0.009λ , 37.0Ω	16.51 x 2.64	0.650 x 0.104
$\ell13$	0.167λ , 50.1Ω	31.75 x 1.65	1.250 x 0.065

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N
C1, C2, C3, C4, C5	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C18, C25	Capacitor, 1 μ F	ATC	920C105
C8	Capacitor, 4.7 μ F, 16 V	Digi-Key	PCS3475CT-ND
C6, C9, C17, C24	Capacitor, 0.01 μ F	ATC	200B 103
C15, C16, C19, C20, C22, C23, C26, C27	Tantalum Capacitor, 10 μ F, 50 V	Garrett Electronics	TPSE106K050R0400
C21, C28	Tantalum Capacitor, 10 μ F, 50 V	Digi-Key	P5571-ND
C29, C30	Ceramic Capacitor, 1.7 pF	ATC	100B 1R7
C13, C14	Ceramic Capacitor, 4.8 pF	ATC	100B 4R8
C12	Ceramic Capacitor, 3.0 pF	ATC	100B 3R0
C10, C11, C31	Ceramic Capacitor, 33 pF	ATC	100B 330
C7	Ceramic Capacitor, 47 pF	ATC	100B 470
Q1	Transistor	Infineon Technologies	BCP56
Q2	Voltage Regulator	National Semiconductor	LM7805
R1, R4	Chip Resistor, 1.2 k Ω	Digi-Key	P1.2KGCT-ND
R2	Chip Resistor, 1.3 k Ω	Digi-Key	P1.3KGCT-ND
R3	Chip Resistor, 2 k Ω	Digi-Key	P2KECT-ND
R5	Potentiometer, 2 k Ω	Digi-Key	3224W-202ETR-ND
R8	Chip Resistor, 5.1 k Ω	Digi-Key	P5.1KECT-ND
R6, R7, R9	Chip Resistor, 10 Ω	Digi-Key	P10ECT-ND

* Gerber Files for this circuit available on request

Package Outline Specifications

Package H-33288-6

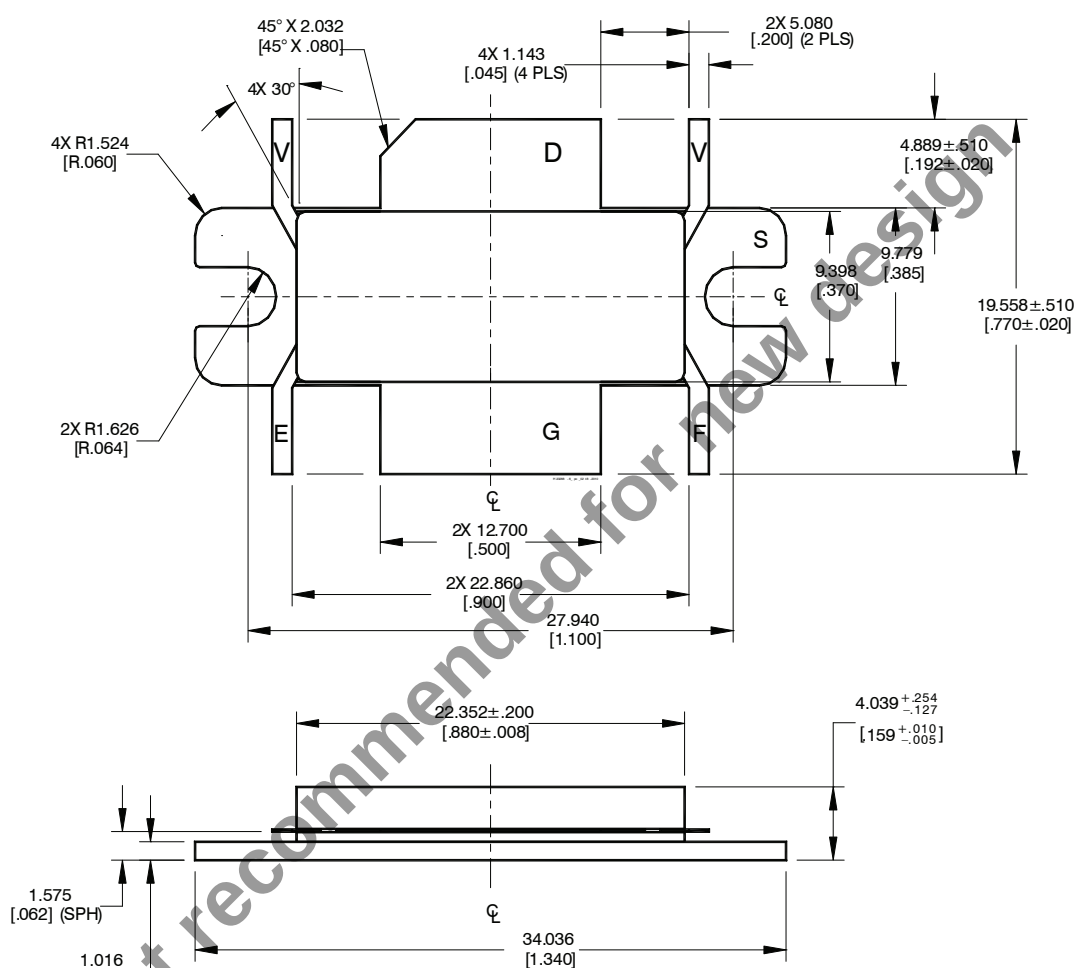


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: A = gate, B = source, C = drain, D = V_{DD} , E, F = N.C.
5. Lead thickness: $0.10 + 0.051/-0.025$ mm [$0.004 + 0.002/-0.001$ inch].
6. Gold plating thickness: 0.25 micron [10 microinch] max.

Package Outline Specifications (cont.)

Package H-34288-4/2

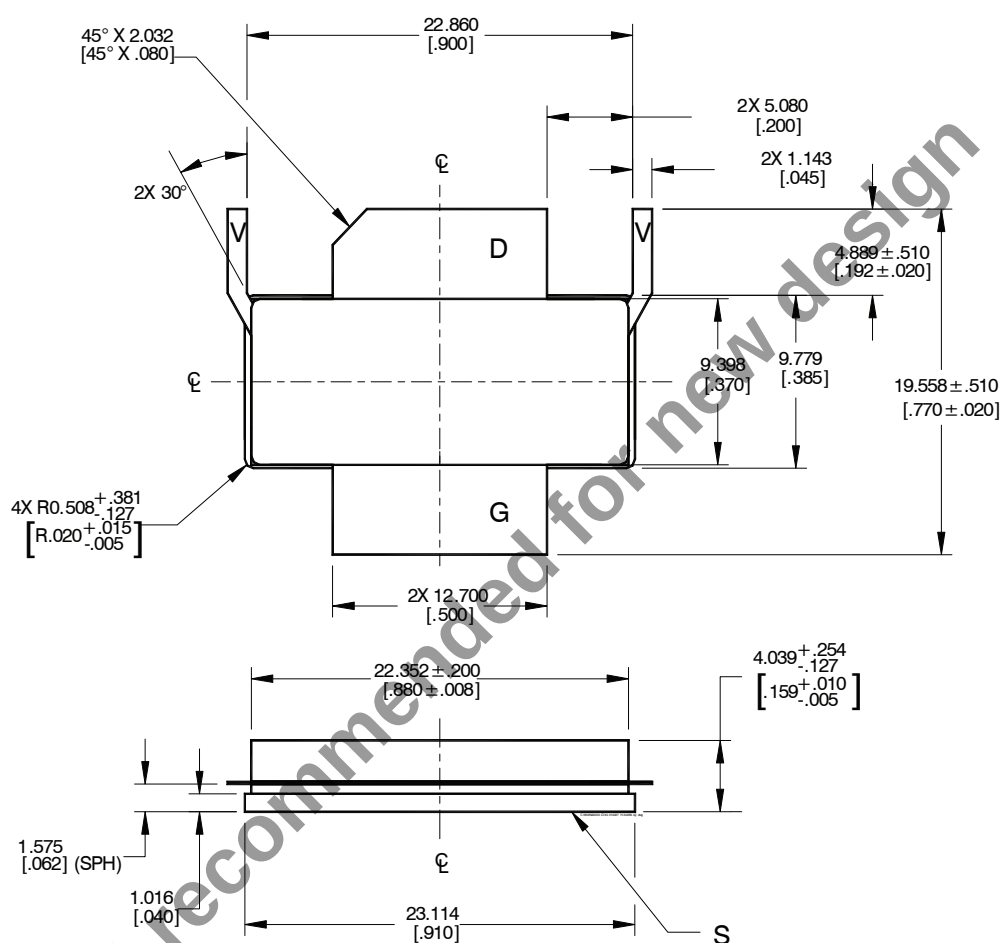


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [$.005$] unless specified otherwise.
4. Pins: D = drain; S = source; G = gate; V = V_{DD} .
5. Lead thickness: $0.10 + 0.051/-0.025$ mm [$.004 + 0.002/-0.001$ inch].
6. Gold plating thickness: 0.25 micron [10 microinch] max.

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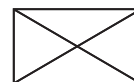
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Page	Subjects (major changes since last revision)	
All	Not recommended for new design	

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