

Description

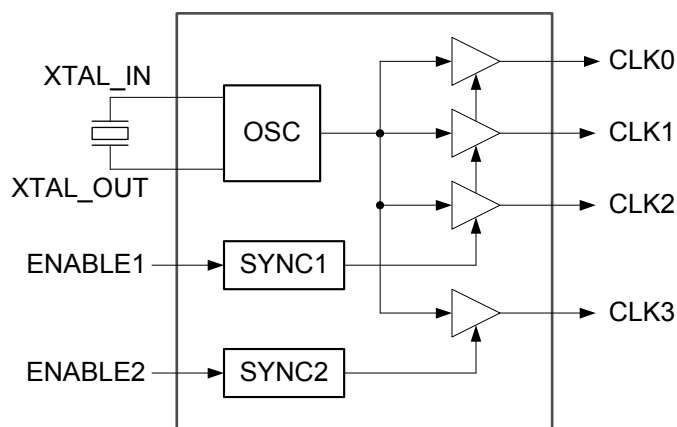
The 5P8390x is a high performance, 1-to-4/6/8 crystal input to LVCMOS fanout buffer with output enable pins. This device accepts a fundamental mode crystal from 10MHz to 40MHz and outputs LVCMOS clocks with best-in-class phase noise performance.

The 5P8390x family (5P83904, 5P83905, and 5P83908) features a synchronous glitch-free Output Enable function to eliminate any intermediate incorrect output clock cycles when enabling or disabling outputs. It comes in standard TSSOP packages or small QFN packages and can operate from 1.8V to 3.3V supplies.

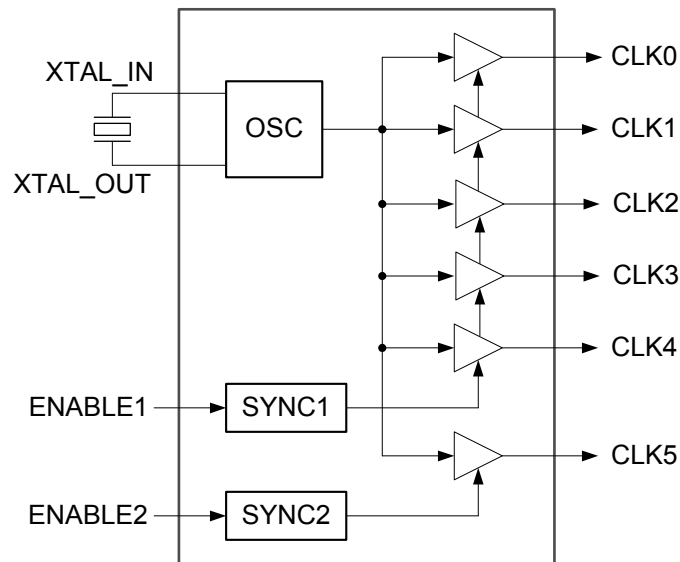
Features

- 4/6/8 copies of LVCMOS output clocks with best-in-class phase noise performance
- Phase Noise:
 - Offset Noise Power (3.3V)
 - 100Hz: -131 dBc/Hz
 - 1KHz: -145 dBc/Hz
 - 10KHz: -154 dBc/Hz
 - 100KHz: -161 dBc/Hz
- Operating power supply modes:
 - Full 3.3V, 2.5V, 1.8V
 - Mixed 3.3V core/2.5V output operating supply
 - Mixed 3.3V core/1.8V output operating supply
 - Mixed 2.5V core/1.8V output operating supply
- Crystal Oscillator Interface
- Synchronous Output Enable
- Packaged in 16-, 20-pin TSSOP and QFN packages (Pb free, fully RoHS compliant)
- Extended (-40°C to +105°C) temperature range

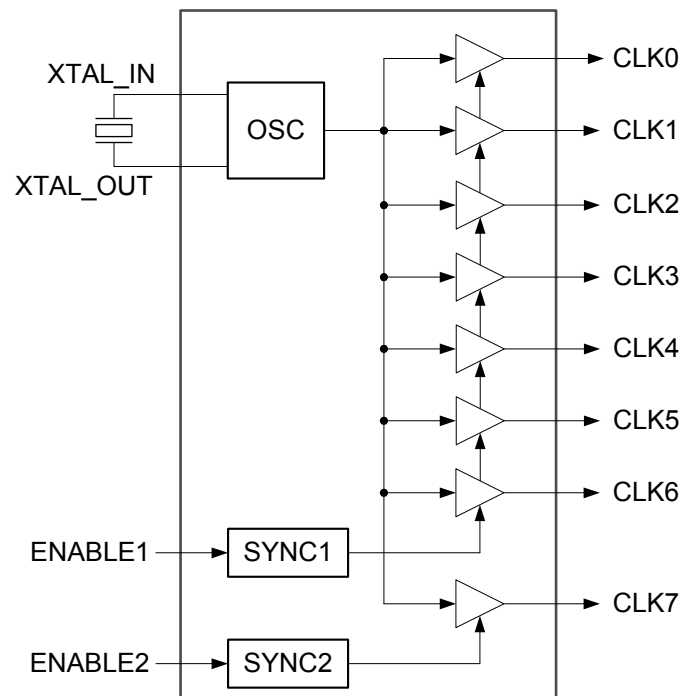
5P83904 Block Diagram



5P83905 Block Diagram



5P83908 Block Diagram



Pin Assignments for QFN Packages

Pin	Signal	Pin	Signal
1	XTAL_OUT	16	XTAL_IN
2	ENABLE2	15	ENABLE1
3	GND	14	CLK3
4	CLK0	13	VDDO
5	VDDO	12	CLK2
6	NC	11	GND
7	GND	10	NC
8	CLK1	9	VDD

Pin	Signal	Pin	Signal
1	XTAL_OUT	20	XTAL_IN
2	VDD	19	GND
3	ENABLE2	18	ENABLE1
4	CLK0	17	CLK7
5	GND	16	VDDO
6	CLK1	15	CLK6
7	VDDO	14	CLK5
8	CLK2	13	GND
9	GND	12	CLK4
10	CLK3	11	VDD

The diagram shows a square package with 16 pins. The pin numbers 1 through 16 are arranged in a circle around the central device label '5P83904CMG1'. The pin functions are as follows:

- Pin 1: XTAL_OUT
- Pin 2: ENABLE2
- Pin 3: GND
- Pin 4: CLK0
- Pin 5: VDDO
- Pin 6: NC
- Pin 7: GND
- Pin 8: CLK1
- Pin 9: VDD
- Pin 10: NC
- Pin 11: GND
- Pin 12: CLK2
- Pin 13: VDDO
- Pin 14: CLK3
- Pin 15: ENABLE1
- Pin 16: XTAL_IN

Pin configuration diagram for the 5P83908NDGI chip. The chip is shown as a square with pins numbered 1 to 15. The pin names are listed around the square:

- XTAL_OUT (pin 1)
- VDD (pin 2)
- ENABLE2 (pin 3)
- CLK0 (pin 4)
- GND (pin 5)
- XTAL_IN (pin 16)
- GND (pin 17)
- ENABLE1 (pin 18)
- CLK7 (pin 19)
- VDDO (pin 20)
- CLK1 (pin 6)
- VDDO (pin 7)
- CLK2 (pin 8)
- GND (pin 9)
- CLK3 (pin 10)
- CLK6 (pin 15)
- CLK5 (pin 14)
- GND (pin 13)
- CLK4 (pin 12)
- VDD (pin 11)

Pin diagram of the 5P83905CMG1 package. The package is a square with pins numbered 1 through 16. The pin functions are as follows:

Pin Number	Pin Function
1	XTAL_OUT
2	ENABLE2
3	GND
4	CLK0
5	VDDO
6	CLK1
7	GND
8	CLK2
9	VDD
10	CLK3
11	GND
12	CLK4
13	VDDO
14	CLK5
15	ENABLE1
16	XTAL_IN

Pin Descriptions

Pin Name	Pin Number			Pin Type	Pin Description
	5P83904	5P83905	5P83908		
XTAL_IN	16	16	20	Input	Oscillator Input from Crystal.
XTAL_OUT	1	1	1	Input	Oscillator Output to drive Crystal.
VDD	9	9	2, 11	Power	Positive power supply for core.
VDDO	5, 13	5, 13	7, 16	Power	Positive power supply for outputs.
GND	3, 7, 11	3, 7, 11	5, 9, 13, 19	Power	Power supply ground.
ENABLE1	15	15	18	Input	Output Enable pin. Please see below Output Enable Function Table. Active High. Internal pull-up.
ENABLE2	2	2	3	Input	Output Enable pin. Please see below Output Enable Function Table. Active High. Internal pull-up.
CLK0	4	4	4	Output	LVC MOS Clock Output 0. Voltage set by VDDO.
CLK1	8	6	6	Output	LVC MOS Clock Output 1. Voltage set by VDDO.
CLK2	12	8	8	Output	LVC MOS Clock Output 2. Voltage set by VDDO.
CLK3	14	10	10	Output	LVC MOS Clock Output 3. Voltage set by VDDO.
CLK4	—	12	12	Output	LVC MOS Clock Output 4. Voltage set by VDDO.
CLK5	—	14	14	Output	LVC MOS Clock Output 5. Voltage set by VDDO.
CLK6	—	—	15	Output	LVC MOS Clock Output 6. Voltage set by VDDO.
CLK7	—	—	17	Output	LVC MOS Clock Output 7. Voltage set by VDDO.
NC	6, 10	—	—	NC	No connect.

Output Enable Function Table

ENABLE1	ENABLE2	5P83904 CLK0-2	5P83905 CLK0-4	5P83908 CLK0-6	5P83904 CLK3	5P83905 CLK5	5P83908 CLK7
0	0	Low	Low	Low	Low	Low	Low
0	1	Low	Low	Low	Active	Active	Active
1	0	Active	Active	Active	Low	Low	Low
1(default)	1(default)	Active	Active	Active	Active	Active	Active

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P8390x. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Output Enable and All Outputs	-0.4 V to VDD+0.5 V
CLKIN	-0.4 V to 3.465V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V _{IH}	XTAL_IN, ENABLE1/2 pins	0.7xVDD			V
Input Low Voltage	V _{IL}	XTAL_IN, ENABLE1/2 pins			0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -4 mA	1.65		1.85	V
Output Low Voltage	V _{OL}	I _{OL} = 4 mA	0.03		0.05	V
Nominal Output Impedance	Z _O			14		Ω
Operating Supply Current						
5P83904	IDD	Outputs On, 25MHz with No Load		8.9		mA
5P83905		Outputs On, 25MHz with No Load		9.0		
5P83908		Outputs On, 25MHz with No Load		9.2		

VDD=2.5 V $\pm$ 5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V _{IH}	XTAL_IN, ENABLE1/2 pins	0.7xVDD			V
Input Low Voltage	V _{IL}	XTAL_IN, ENABLE1/2 pins			0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -4 mA	2.31		2.58	V
Output Low Voltage	V _{OL}	I _{OL} = 4 mA	0.03		0.05	V
Nominal Output Impedance	Z _O			14		Ω
Operating Supply Current						
5P83904	IDD	Outputs On, 25MHz with No Load		10.6		mA
5P83905		Outputs On, 25MHz with No Load		10.7		
5P83908		Outputs On, 25MHz with No Load		10.8		

VDD=3.3 V $\pm$ 5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage, CLKIN	V _{IH}	XTAL_IN, ENABLE1/2 pins	0.7xVDD			V
Input Low Voltage, CLKIN	V _{IL}	XTAL_IN, ENABLE1/2 pins			0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -4 mA	3.09		3.43	V
Output Low Voltage	V _{OL}	I _{OL} = 4 mA	0.03		0.04	V
Nominal Output Impedance	Z _O			14		Ω
Operating Supply Current						
5P83904	IDD	Outputs On, 25MHz with No Load		12.1		mA
5P83905		Outputs On, 25MHz with No Load		12.2		
5P83908		Outputs On, 25MHz with No Load		12.3		

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{MAX}	Input Frequency Crystal	8		40	MHz
		Input Frequency Clock	DC		200	
Delay for Output Enable / Disable Time ENABLEx to BCLKn	t_{EN} / t_{DIS}				3	cycles
Duty Cycle	t_{DC}		45		55	ns
Output to Output Skew	$t_{SKEWO-O}$			25	65	ps
Phase Noise	Φ_{noise}	$f_{OUT} = 25 \text{ MHz } 100 \text{ Hz off Carrier}$		-121.1974		dBc/Hz
		$f_{OUT} = 25 \text{ MHz } 1 \text{ kHz off Carrier}$		-132.1742		
		$f_{OUT} = 25 \text{ MHz } 10 \text{ kHz off Carrier}$		-143.8058		
		$f_{OUT} = 25 \text{ MHz } 100 \text{ kHz off Carrier}$		-155.2978		
RMS Phase Jitter	$t_{JIT}(\Phi)$	25MHz carrier, Integration Range: 12kHz-20MHz		0.279		ps
Output Rise/Fall Time	t_R / t_F	20% to 80%			0.8	ns
Device to Device Skew					200	ps
Propagation Delay		freq, LVCMOS INPUT	2.5	3.3	6	ns

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

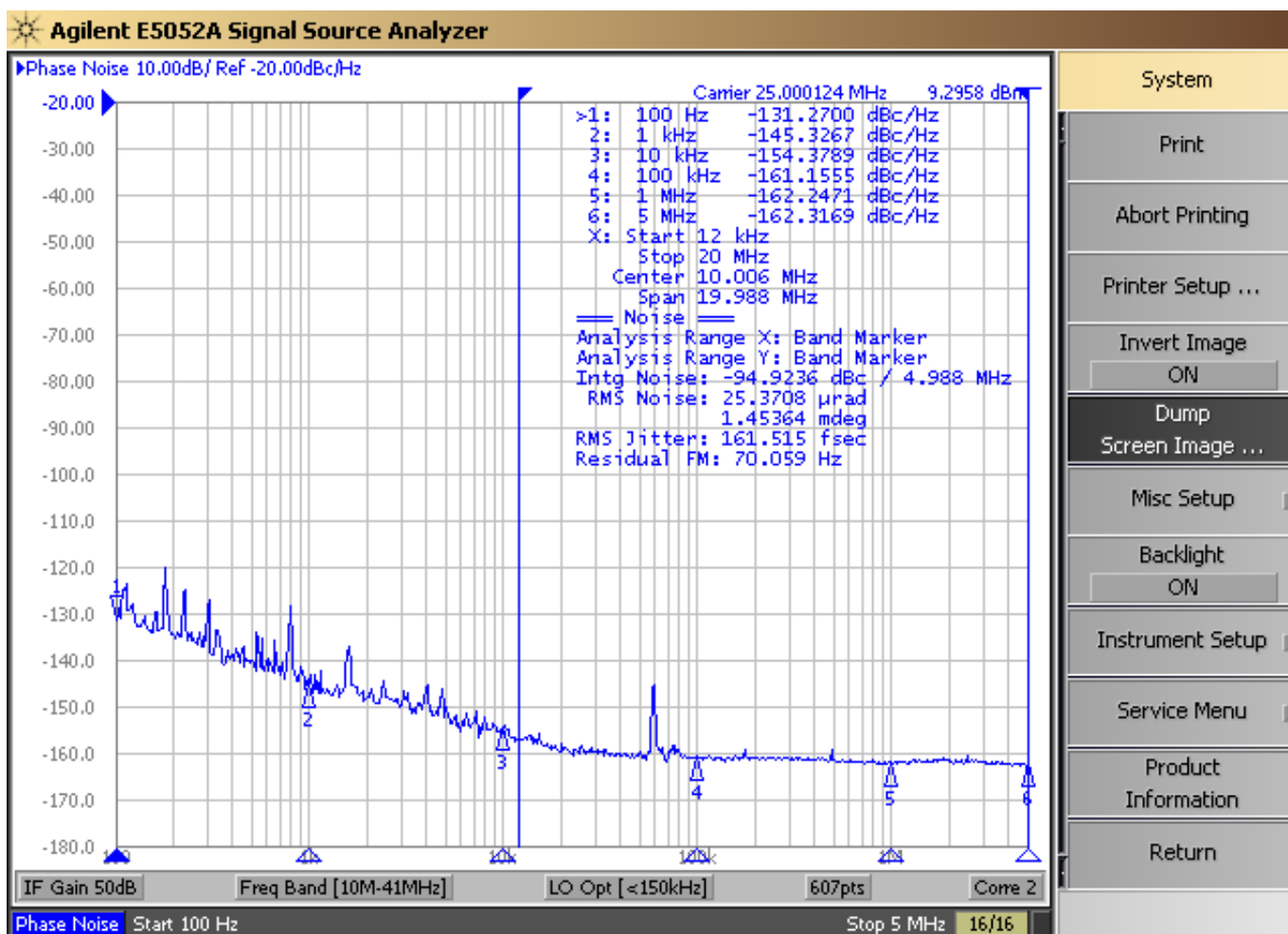
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{MAX}	Input Frequency Crystal	8		40	MHz
		Input Frequency Clock	DC		200	
Delay for Output Enable / Disable Time ENABLEx to BCLKn	t_{EN} / t_{DIS}				3	cycles
Duty Cycle	t_{DC}		45		55	ns
Output to Output Skew	$t_{SKEWO-O}$			25	65	ps
Phase Noise	Φ_{noise}	$f_{OUT} = 25 \text{ MHz } 100 \text{ Hz off Carrier}$		-131.26		dBc/Hz
		$f_{OUT} = 25 \text{ MHz } 1 \text{ kHz off Carrier}$		-139.2177		
		$f_{OUT} = 25 \text{ MHz } 10 \text{ kHz off Carrier}$		-149.5185		
		$f_{OUT} = 25 \text{ MHz } 100 \text{ kHz off Carrier}$		-158.7531		
RMS Phase Jitter	$t_{JIT}(\Phi)$	25MHz carrier, Integration Range: 12kHz-20MHz		0.2		ps
Output Rise/Fall Time	t_R / t_F	20% to 80%			0.8	ns
Device to Device Skew					200	ps
Propagation Delay		freq, LVCMOS INPUT	2.5	3.3	6	ns

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{MAX}	Input Frequency Crystal	8		40	MHz
		Input Frequency Clock	DC		200	
Delay for Output Enable / Disable Time ENABLEx to BCLKn	t_{EN} / t_{DIS}				3	cycles
Duty Cycle	t_{DC}		45		55	ns
Output to Output Skew	$t_{SKEWO-O}$			25	65	ps

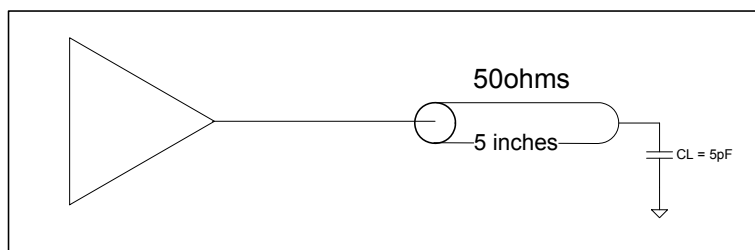
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Phase Noise	Φ_{noise}	$f_{\text{OUT}} = 25 \text{ MHz}$ 100 Hz off Carrier		-131.27		dBc/Hz
		$f_{\text{OUT}} = 25 \text{ MHz}$ 1 kHz off Carrier		-145.3267		
		$f_{\text{OUT}} = 25 \text{ MHz}$ 10 kHz off Carrier		-154.3789		
		$f_{\text{OUT}} = 25 \text{ MHz}$ 100 kHz off Carrier		-161.1555		
RMS Phase Jitter	$t_{\text{JIT}}(\Phi)$	25MHz carrier, Integration Range: 12kHz-20MHz		0.16		ps
Output Rise/Fall Time	$t_{\text{R}}/t_{\text{F}}$	20% to 80%			0.8	ns
Device to Device Skew					200	ps
Propagation Delay		freq, LVCMOS INPUT	2.5	3.3	6	ns

Phase Noise Plots

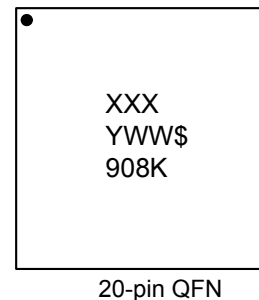
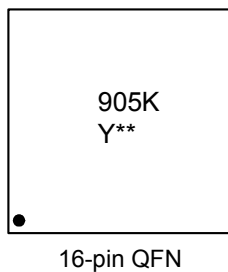
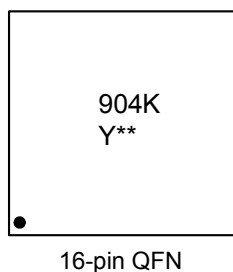
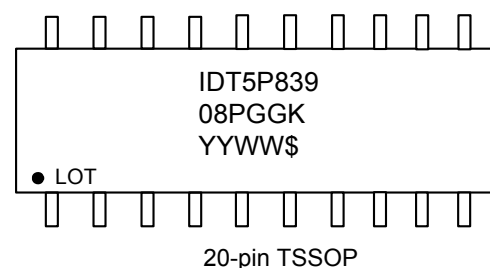
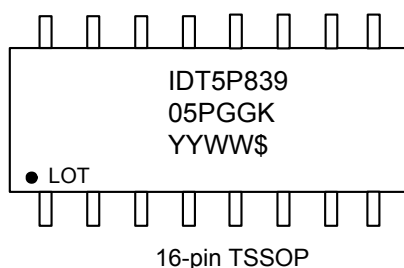
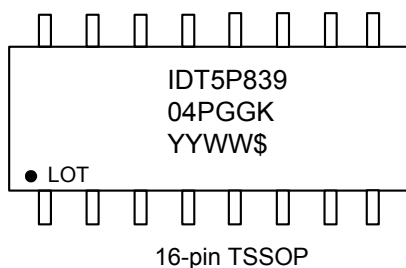


The phase noise plots above show the low Additive Jitter of the 5P8390x high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5P8390x has about 70.9fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 39fs.

Test Load and Circuit



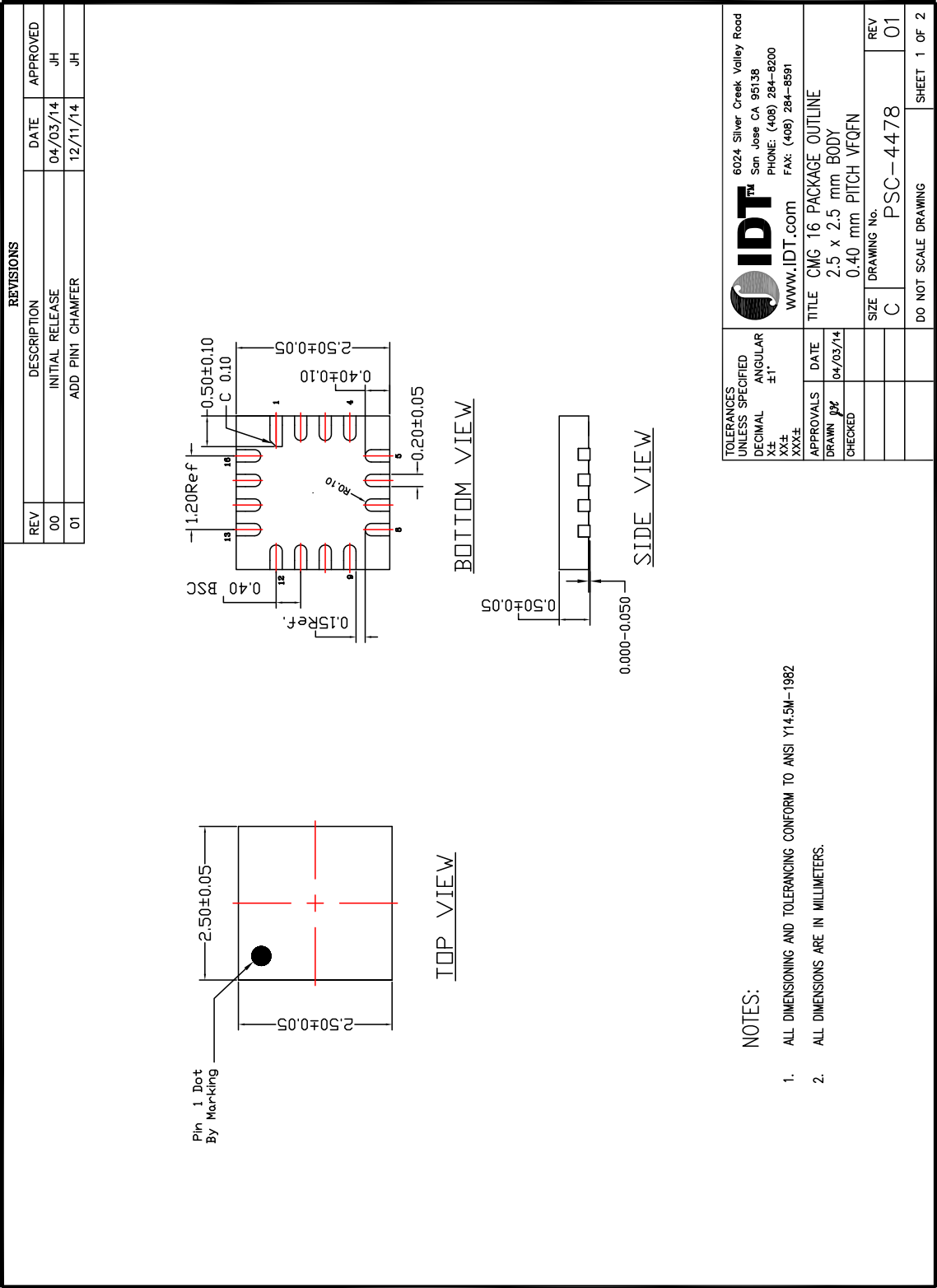
Marking Diagrams



Notes:

1. “**” is the lot sequence.
2. “XXX” denotes the last three characters of the Asm lot (20-pin QFN only).
3. “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and week that the part was assembled.
4. “\$” denotes the mark code.
5. “LOT” denotes lot number.
6. “G” after the two-letter package code denotes RoHS compliant package.
7. “I” denotes extended temperature range device.
8. Bottom marking: country of origin (TSSOP only).

Package Outline and Package Dimensions (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



Package Outline and Package Dimensions, cont. (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)

RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/03/14	JH
01	ADD PIN1 CHAMFER	12/11/14	JH

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX±	ANGULAR ±1°	IDT™ 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com	TITLE CMG 16 PACKAGE OUTLINE 2.5 x 2.5 mm BODY 0.40 mm PITCH VFQFN	SIZE C	DRAWING No. PSC-4478	REV 01	
	APPROVALS DRAWN BY CHECKED						DATE 04/03/14
DO NOT SCALE DRAWING						SHEET 2 OF 2	

Package Outline and Package Dimensions (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)

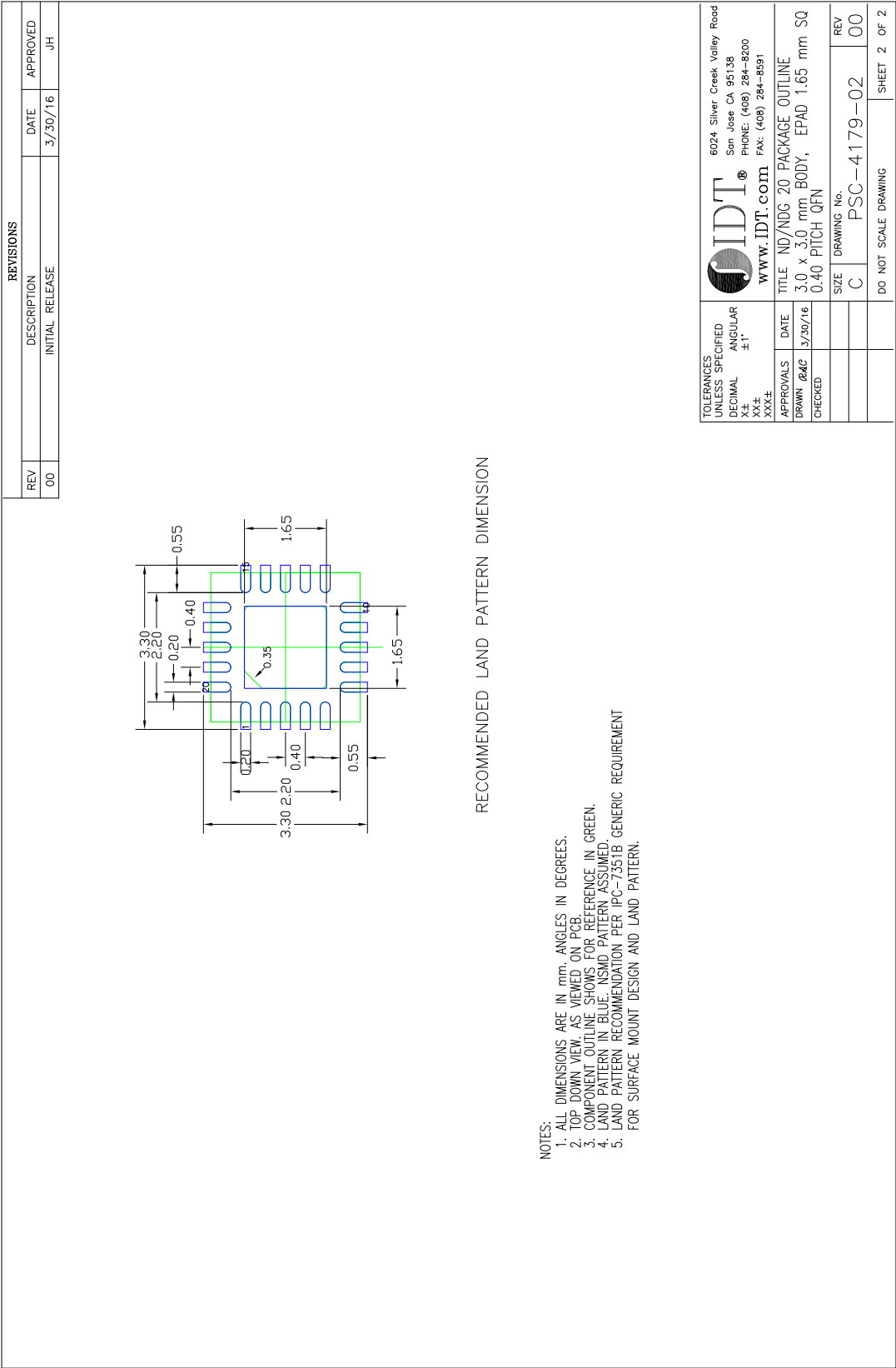
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	3/30/16	JH

NOTE :

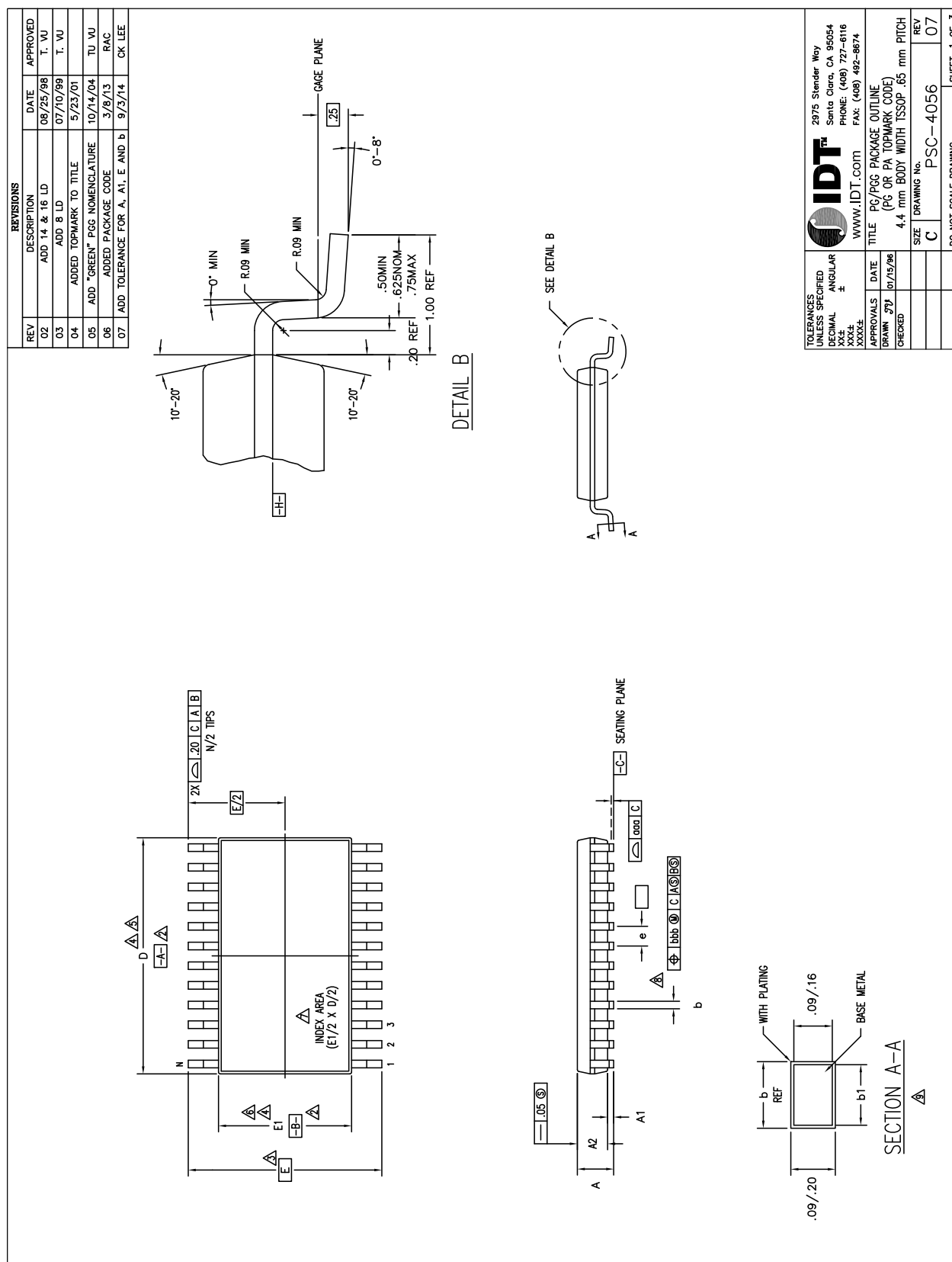
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. COPLANARITY SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.

DIMENSION			
Symbol	Min	Norm	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 Ref	
b	0.17	0.20	0.25
e		0.40 BASIC	
N		20	
ND		5	
NE		5	
D		3.00 BASIC	
E		3.00 BASIC	
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
L	0.30	0.40	0.50

Package Outline and Package Dimensions, cont. (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)



Package Outline and Package Dimensions (8-, 14-, 16-, 20-pin TSSOP)



Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

REVISIONS									
REV	DESCRIPTION	DATE	APPROVED						
02	ADD 14 & 16 LD	08/25/98	T. VU						
03	ADD 8 LD	07/10/99	T. VU						
04	ADDED TOPMARK TO TITLE	5/23/01							
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU						
06	ADDED PACKAGE CODE	3/8/13	RAC						
07	ADD TOLERANCE FOR A, A1, E AND b	9/3/14	CK LEE						

SYMBOL	PGC/PGG8			PGC/PGG14			PGC/PGG16			PGC/PGG20			PGC/PGG24			PGC/PGG28		
	JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION			JEDEC VARIATION		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	.85	1.10	1.20	.85	1.10	1.20	.85	1.10	1.20	.85	1.10	1.20	.85	1.10	1.20	.85	1.10	1.20
A1	.05	.10	.15	.05	.10	.15	.05	.10	.15	.05	.10	.15	.05	.10	.15	.05	.10	.15
A2	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05
D	2.90	3.00	3.10	4.5	4.90	5.00	4.5	4.90	5.00	4.5	4.90	5.00	4.5	4.90	5.00	4.5	4.90	5.00
E	6.20	6.40	6.60	3	6.20	6.40	3	6.20	6.40	3	6.20	6.40	3	6.20	6.40	3	6.20	6.40
E1	4.30	4.40	4.50	4.6	4.30	4.40	4.6	4.30	4.40	4.6	4.30	4.40	4.6	4.30	4.40	4.6	4.30	4.40
e	.65	BSC		.65	BSC		.65	BSC		.65	BSC		.65	BSC		.65	BSC	
b	.19	.25	.30	.19	.25	.30	.19	.25	.30	.19	.25	.30	.19	.25	.30	.19	.25	.30
b1	.19	.22	.25	.19	.22	.25	.19	.22	.25	.19	.22	.25	.19	.22	.25	.19	.22	.25
aaa	-	-	.10	-	-	.10	-	-	.10	-	-	.10	-	-	.10	-	-	.10
bbb	-	-	.10	-	-	.10	-	-	.10	-	-	.10	-	-	.10	-	-	.10
N	8			14			16			20			24			28		

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

1 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

2 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

3 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

5 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

8 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

9 ALL DIMENSIONS ARE IN MILLIMETERS

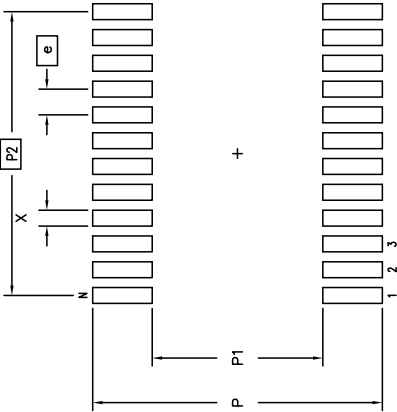
10 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED		IDT		2975 Stender Way	
DECIMAL	ANGULAR	±		Santa Clara, CA 95054	
XXX±				PHONE: (408) 727-8116	
XXXX±				FAX: (408) 492-8674	
APPROVALS	DATE	TITLE PGC/PGG PACKAGE OUTLINE			
DRAWN JTY	07/15/06	(PG OR PA TOPMARK CODE)			
CHECKED		4.4 mm BODY WIDTH TSSOP .65 mm PITCH			
		SIZE	DRAWING No.	REV	
		C	PSC-4056	07	
		DO NOT SCALE DRAWING			SHEET 2 OF 3

Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC
07	ADD TOLERANCE FOR A, A1, E AND b	9/3/14	OK LEE

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95	BSC	3.90	BSC	4.55	BSC	5.85	BSC	7.15	BSC	8.45	BSC
X	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50
e	.65	BSC	.65	BSC	.65	BSC	.65	BSC	.65	BSC	.65	BSC
N	8		14		16		20		24		28	

TOLERANCES UNLESS SPECIFIED		IDT		2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674	
DECIMAL	±	ANGULAR	±	www.IDT.com	
XX.X		XX.X°			
XX.XX		XX.XX°			
XX.XXX		XX.XXX°			
APPROVALS	DATE	TITLE PG/PGG PACKAGE OUTLINE			
DRWEN JYJ	07/15/98	(PG OR PA TOPMARK CODE)			
CHECKED		4.4 mm BODY WIDTH TSSOP .65 mm PITCH			
		SIZE	DRAWING No.	REV	
		C	PSC-4056	07	
		DO NOT SCALE DRAWING			
		SHEET 3 OF 3			

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P83904PGGK	see page 9	Tubes	16-pin TSSOP	-40° to +105°C
5P83904PGGK8		Tape and Reel	16-pin TSSOP	-40° to +105°C
5P83904CMGK		Cut Tape	16-pin QFN	-40° to +105°C
5P83904CMGK8		Tape and Reel	16-pin QFN	-40° to +105°C
5P83905PGGK		Tubes	16-pin TSSOP	-40° to +105°C
5P83905PGGK8		Tape and Reel	16-pin TSSOP	-40° to +105°C
5P83905CMGK		Cut Tape	16-pin QFN	-40° to +105°C
5P83905CMGK8		Tape and Reel	16-pin QFN	-40° to +105°C
5P83908PGGK		Tubes	20-pin TSSOP	-40° to +105°C
5P83908PGGK8		Tape and Reel	20-pin TSSOP	-40° to +105°C
5P83908NDGK		Tubes	20-pin QFN	-40° to +105°C
5P83908NDGK8		Tape and Reel	20-pin QFN	-40° to +105°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

“K” denotes extended temperature range.

Revision History

Rev.	Date	Originator	Description of Change
A	07/11/16	H.G.	Release to final.



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