2.5V Differential 1:5 Clock Buffer Terabuffer™

5T915

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES NOVEMBER 2, 2016 **DATA SHEET**

FEATURES:

- Guaranteed Low Skew < 60ps (max)
- Very low duty cycle distortion < 300ps (max)
- High speed propagation delay < 2ns (max)
- Up to 250MHz operation
- Very low CMOS power levels
- Hot insertable and over-voltage tolerant inputs
- 3-level inputs for selectable interface
- Selectable HSTL, eHSTL, 1.8V / 2.5V LVTTL, or LVEPECL input interface
- Selectable differential or single-ended inputs and five differential outputs
- 2.5V V_{DD}
- Available in TSSOP package

APPLICATIONS:

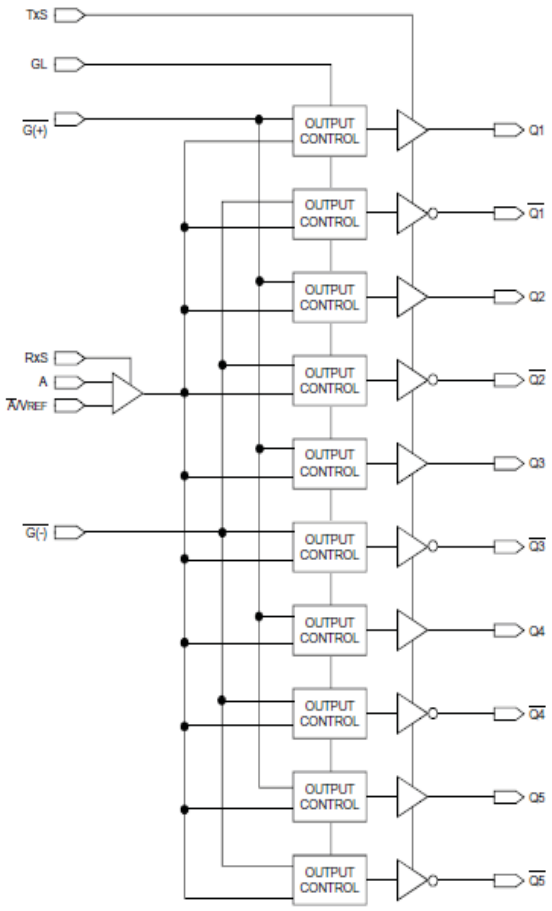
- Clock and signal distribution

DESCRIPTION:

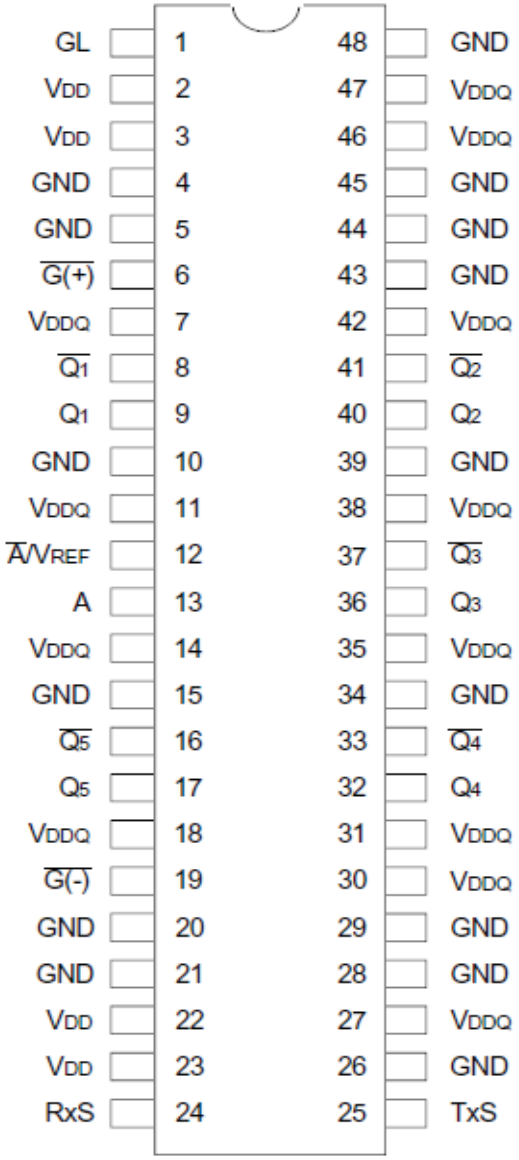
The 5T915 2.5V differential (DDR) clock buffer is a user-selectable single-ended or differential input to five differential outputs built on advanced metal CMOS technology. The differential clock buffer fanout from a single or differential input to five differential or single-ended outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The 5T915 can act as a translator from a differential HSTL, eHSTL, 1.8V/2.5V LVTTL, LVEPECL, or single-ended 1.8V/2.5V LVTTL input to HSTL, eHSTL, 1.8V/2.5V LVTTL outputs. Selectable interface is controlled by 3-level input signals that may be hard-wired to appropriate high-mid-low levels.

The 5T915 true or complementary outputs can be asynchronously enabled/disabled. Multiple power and grounds reduce noise.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage(2)	–0.5 to +3.6	V
V_{DDQ}	Output Power Supply(2)	–0.5 to +3.6	V
V_I	Input Voltage	–0.5 to +3.6	V
V_O	Output Voltage(3)	–0.5 to V_{DDQ} +0.5	V
V_{REF}	Reference Voltage(3)	–0.5 to +3.6	V
T_{STG}	Storage Temperature	–65 to +165	°C
T_J	Junction Temperature	150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DDQ} and V_{DD} internally operate independently. No power sequencing requirements need to be met.
3. Not to exceed 3.6V.

CAPACITANCE(1,2) (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	3.5	—	pF

NOTES:
1. This parameter is measured at characterization but not tested.
2. Capacitance applies to all inputs except RxS and TxS.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–40	+25	+85	°C
V_{DD}(1)	Internal Power Supply Voltage	2.4	2.5	2.6	V
V_{DDQ}(1)	HSTL Output Power Supply Voltage	1.4	1.5	1.6	V
	Extended HSTL and 1.8V LVTTL Output Power Supply Voltage	1.65	1.8	1.95	V
	2.5V LVTTL Output Power Supply Voltage		V_{DD}		V
V_T	Termination Voltage		V_{DDQ} / 2		V

NOTE:
1. All power supplies should operate in tandem. If V_{DD} or V_{DDQ} is at maximum, then V_{DDQ} or V_{DD} (respectively) should be at maximum, and vice-versa.

PIN DESCRIPTION

Symbol	I/O	Type	Description
A	I	Adjustable[1]	Clock input. A is the "true" side of the differential clock input. If operating in single-ended mode, A is the clock input.
$\overline{A}$/V_{REF}	I	Adjustable[1]	Complementary clock input. $\overline{A}$/V_{REF} is the "complementary" side of A if the input is in differential mode. If operating in single-ended mode, $\overline{A}$/V_{REF} is connected to GND. For single-ended operation in differential mode, $\overline{A}$/V_{REF} should be set to the desired toggle voltage for A: 2.5V LVTTL V_{REF} = 1250mV 1.8V LVTTL, eHSTL V_{REF} = 900mV HSTL V_{REF} = 750mV LVEPECL V_{REF} = 1082mV
$\overline{G(+)}$	I	LVTTL[5]	Gate control for "true", Qn, outputs. When $\overline{G(+)}$ is LOW, the "true" outputs are enabled. When $\overline{G(+)}$ is HIGH, the "true" outputs are asynchronously disabled to the level designated by GL[4].
$\overline{G(-)}$	I	LVTTL[5]	Gate control for "complementary", $\overline{Qn}$, outputs. When $\overline{G(-)}$ is LOW, the "complementary" outputs are enabled. When $\overline{G(-)}$ is HIGH, the "complementary" outputs are asynchronously disabled to the opposite level as GL[4].
GL	I	LVTTL[5]	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
Qn	O	Adjustable[2]	Clock outputs
$\overline{Qn}$	O	Adjustable[2]	Complementary clock outputs
RxS	I	3 Level[3]	Selects single-ended 2.5V LVTTL (HIGH), 1.8V LVTTL (MID) clock input or differential (LOW) clock input
TxS	I	3 Level[3]	Sets the drive strength of the output drivers to be 2.5V LVTTL (HIGH), 1.8V LVTTL (MID) or HSTL (LOW) compatible. Used in conjuction with V_{DDO} to set the interface levels.
V_{DD}		PWR	Power supply for the device core and inputs
V_{DDO}		PWR	Power supply for the device outputs. When utilizing 2.5V LVTTL outputs, V_{DDO} should be connected to V_{DD}.
GND		PWR	Power supply return for all power

NOTES:

1. Inputs are capable of translating the following interface standards. User can select between:
   Single-ended 2.5V LVTTL levels
   Single-ended 1.8V LVTTL levels
   or
   Differential 2.5V/1.8V LVTTL levels
   Differential HSTL and eHSTL levels
   Differential LVEPECL levels
2. Outputs are user selectable to drive 2.5V, 1.8V LVTTL, eHSTL, or HSTL interface levels when used with the appropriate V_{DDQ} voltage.
3. 3-level inputs are static inputs and must be tied to V_{DD} or GND or left floating. These inputs are not hot-insertable or over voltage tolerant.
4. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
5. Pins listed as LVTTL inputs will accept 2.5V signals when RxS = HIGH or 1.8V signals when RxS = LOW or MID.

INPUT/OUTPUT SELECTION(1)

Input	Output
2.5V LVTTL SE	2.5V LVTTL
1.8V LVTTL SE	
2.5V LVTTL DSE	
1.8V LVTTL DSE	
LVEPECL DSE	
eHSTL DSE	
HSTL DSE	
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	
eHSTL DIF	
HSTL DIF	
2.5V LVTTL SE	1.8V LVTTL
1.8V LVTTL SE	
2.5V LVTTL DSE	
1.8V LVTTL DSE	
LVEPECL DSE	
eHSTL DSE	
HSTL DSE	
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	
eHSTL DIF	
HSTL DIF	

Input	Output
2.5V LVTTL SE	eHSTL
1.8V LVTTL SE	
2.5V LVTTL DSE	
1.8V LVTTL DSE	
LVEPECL DSE	
eHSTL DSE	
HSTL DSE	
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	
eHSTL DIF	
HSTL DIF	
2.5V LVTTL SE	HSTL
1.8V LVTTL SE	
2.5V LVTTL DSE	
1.8V LVTTL DSE	
LVEPECL DSE	
eHSTL DSE	
HSTL DSE	
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	
eHSTL DIF	
HSTL DIF	

NOTE:
1. The INPUT/OUTPUT SELECTION Table describes the total possible combinations of input and output interfaces. Single-Ended (SE) inputs in a single-ended mode require the $\overline{A}/V_{REF}$ pin to be connected to GND. Differential Single-Ended (DSE) is for single-ended operation in differential mode, requiring a V_{REF}. Differential (DIF) inputs are used only in differential mode.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Max	Unit
V_{IHH}	Input HIGH Voltage Level(1)	3-Level Inputs Only		V_{DD} – 0.4	—	V
V_{IMM}	Input MID Voltage Level(1)	3-Level Inputs Only		$V_{DD}/2$ – 0.2	$V_{DD}/2$ + 0.2	V
V_{ILL}	Input LOW Voltage Level(1)	3-Level Inputs Only		—	0.4	V
I_3	3-Level Input DC Current (RxS, TxS)	$V_{IN} = V_{DD}$	HIGH Level	—	200	µA
		$V_{IN} = V_{DD}/2$	MID Level	–50	+50	
		V_{IN} = GND	LOW Level	–200	—	

NOTE:
1. These inputs are normally wired to V_{DD}, GND, or left floating. Internal termination resistors bias unconnected inputs to $V_{DD}/2$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR HSTL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(7)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current(9)	V_{DD} = 2.6V V_I = V_{DDQ}/GND	—	—	±5	µA
I_{IL}	Input LOW Current(9)	V_{DD} = 2.6V V_I = GND/V_{DDQ}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.4V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		+3.6	V
V_{DIF}	DC Differential Voltage(2,8)		0.2		—	V
V_{CM}	DC Common Mode Input Voltage(3,8)		680	750	900	mV
V_{IH}	DC Input HIGH(4,5,8)		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW(4,6,8)		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage(4,8)		—	750	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA	V_{DDQ} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQ} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation, in differential mode, $\overline{A}/V_{REF}$ is tied to the DC voltage V_{REF}.
5. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
6. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
7. Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.5V, +25°C ambient.
8. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
9. For differential mode (RxS = LOW), A and $\overline{A}/V_{REF}$ must be at the opposite rail.

POWER SUPPLY CHARACTERISTICS FOR HSTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	20	30	µA/MHz
I_{DDDQ}	Dynamic V_{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	30	50	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	V_{DDQ} = 1.5V, $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	20	40	mA
		V_{DDQ} = 1.5V, $F_{REFERENCE\ CLOCK}$ = 250MHz, C_L = 15pF	35	50	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	V_{DDQ} = 1.5V, $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	35	70	mA
		V_{DDQ} = 1.5V, $F_{REFERENCE\ CLOCK}$ = 250MHz, C_L = 15pF	60	120	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing[1]	1	V
V_X	Differential Input Signal Crossing Point[2]	750	mV
V_{THI}	Input Timing Measurement Reference Level[3]	Crossing Point	V
t_R, t_F	Input Signal Edge Rate[4]	1	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR eHSTL[1]

Symbol	Parameter	Test Conditions	Min.	Typ.[7]	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current[9]	V_{DD} = 2.6V V_I = V_{DDQ}/GND	—	—	±5	µA
I_{IL}	Input LOW Current[9]	V_{DD} = 2.6V V_I = GND/V_{DDQ}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.4V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		+3.6	V
V_{DIF}	DC Differential Voltage[2,8]		0.2		—	V
V_{CM}	DC Common Mode Input Voltage[3,8]		800	900	1000	mV
V_{IH}	DC Input HIGH[4,5,8]		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW[4,6,8]		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage[4,8]		—	900	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA	V_{DDQ} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQ} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation, in a differential mode, $\overline{A}$/V_{REF} is tied to the DC voltage V_{REF}.
5. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
6. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
7. Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.8V, +25°C ambient.
8. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
9. For differential mode (RxS = LOW), A and $\overline{A}$/V_{REF} must be at the opposite rail.

POWER SUPPLY CHARACTERISTICS FOR eHSTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	20	30	µA/MHz
I_{DDDQ}	Dynamic V_{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	40	60	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	V_{DDQ} = 1.8V, $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	20	40	mA
		V_{DDQ} = 1.8V, $F_{REFERENCE\ CLOCK}$ = 250MHz, C_L = 15pF	35	50	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	V_{DDQ} = 1.8V, $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	40	80	mA
		V_{DDQ} = 1.8V, $F_{REFERENCE\ CLOCK}$ = 250MHz, C_L = 15pF	80	160	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	1	V
V_X	Differential Input Signal Crossing Point(2)	900	mV
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	1	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVEPECL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(2)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current(6)	V_{DD} = 2.6V V_I = V_{DDQ}/GND	—	—	±5	µA
I_{IL}	Input LOW Current(6)	V_{DD} = 2.6V V_I = GND/V_{DDQ}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.4V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3	—	3.6	V
V_{CM}	DC Common Mode Input Voltage(3,5)		915	1082	1248	mV
V_{REF}	Single-Ended Reference Voltage(4,5)		—	1082	—	mV
V_{IH}	DC Input HIGH		1275	—	1620	mV
V_{IL}	DC Input LOW		555	—	875	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V_{DD} = 2.5V, +25°C ambient.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation while in differential mode, $\overline{A}/V_{REF}$ is tied to the DC Voltage V_{REF}.
5. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
6. For differential mode (RxS = LOW), A and $\overline{A}/V_{REF}$ must be at the opposite rail.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing[1]	732	mV
V_X	Differential Input Signal Crossing Point[2]	1082	mV
V_{THI}	Input Timing Measurement Reference Level[3]	Crossing Point	V
t_R, t_F	Input Signal Edge Rate[4]	1	V/ns

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A 1082mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR 2.5V LVTTL[1]

Symbol	Parameter	Test Conditions	Min.	Typ.[8]	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current[10]	V_{DD} = 2.6V V_I = V_{DDQ}/GND	—	—	±5	µA
I_{IL}	Input LOW Current[10]	V_{DD} = 2.6V V_I = GND/V_{DDQ}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.4V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		+3.6	V
Single-Ended Inputs[2]						
V_{IH}	DC Input HIGH		1.7		—	V
V_{IL}	DC Input LOW		—		0.7	V
Differential Inputs						
V_{DIF}	DC Differential Voltage[3,9]		0.2		—	V
V_{CM}	DC Common Mode Input Voltage[4,9]		1150	1250	1350	mV
V_{IH}	DC Input HIGH[5,6,9]		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW[5,7,9]		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage[5,9]		—	1250	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA	V_{DDQ} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQ} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 12mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. For 2.5V LVTTL single-ended operation, the RxS pin is tied HIGH and $\overline{A}/V_{REF}$ is tied to GND.
3. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
5. For single-ended operation, in differential mode, $\overline{A}/V_{REF}$ is tied to the DC voltage V_{REF}.
6. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
7. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
8. Typical values are at V_{DD} = 2.5V, V_{DDQ} = V_{DD}, +25°C ambient.
9. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
10. For differential mode (RxS = LOW), A and $\overline{A}/V_{REF}$ must be at the opposite rail.

POWER SUPPLY CHARACTERISTICS FOR 2.5V LVTTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	25	40	µA/MHz
I_{DDDQ}	Dynamic V_{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	45	70	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	V_{DDQ} = 2.5V., $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	25	40	mA
		V_{DDQ} = 2.5V., $F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 15pF	45	70	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	V_{DDQ} = 2.5V., $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	40	80	mA
		V_{DDQ} = 2.5V., $F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 15pF	100	200	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR 2.5V LVTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	V_{DD}	V
V_X	Differential Input Signal Crossing Point(2)	$V_{DD}/2$	V
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	2.5	V/ns

NOTES:

1. A nominal 2.5V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 1.25V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2.5V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

SINGLE-ENDED INPUT AC TEST CONDITIONS FOR 2.5V LVTTL

Symbol	Parameter	Value	Units
V_{IH}	Input HIGH Voltage	V_{DD}	V
V_{IL}	Input LOW Voltage	0	V
V_{THI}	Input Timing Measurement Reference Level(1)	$V_{DD}/2$	V
t_R, t_F	Input Signal Edge Rate(2)	2	V/ns

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR 1.8V LVTTL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(8)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current(12)	V_{DD} = 2.6V V_I = V_{DDQ}/GND	—	—	±5	µA
I_{IL}	Input LOW Current(12)	V_{DD} = 2.6V V_I = GND/V_{DDQ}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.4V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		V_{DDQ} + 0.3	V
Single-Ended Inputs(2)						
V_{IH}	DC Input HIGH		1.073(11)		—	V
V_{IL}	DC Input LOW		—		0.683(11)	V
Differential Inputs						
V_{DIF}	DC Differential Voltage(3,9)		0.2		—	V
V_{CM}	DC Common Mode Input Voltage(4,9)		825	900	975	mV
V_{IH}	DC Input HIGH(5,6,9)		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW(5,7,9)		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage(5,9)		—	900	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -6mA	V_{DDQ} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQ} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 6mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. For 1.8V LVTTL single-ended operation, the RxS pin is allowed to float or tied to V_{DD}/2 and $\overline{A}$/V_{REF} is tied to GND.
3. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
5. For single-ended operation in differential mode, $\overline{A}$/V_{REF} is tied to the DC voltage V_{REF}. The input is guaranteed to toggle within ±200mV of V_{REF} when V_{REF} is constrained within +600mV and V_{DDI}-600mV, where V_{DDI} is the nominal 1.8V power supply of the device driving the A input. To guarantee switching in voltage range specified in the JEDEC 1.8V LVTTL interface specification, V_{REF} must be maintained at 900mV with appropriate tolerances.
6. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
7. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
8. Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.8V, +25°C ambient.
9. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. The correct input interface table should be referenced.
10. This value is the worst case minimum V_{IH} over the specification range of the 1.8V power supply. The 1.8V LVTTL specification is V_{IH} = 0.65 • V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IH} = 0.65 • [1.8 - 0.15V]) rather than reference against a nominal 1.8V supply.
11. This value is the worst case maximum V_{IL} over the specification range of the 1.8V power supply. The 1.8V LVTTL specification is V_{IL} = 0.35 • V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IL} = 0.35 • [1.8 + 0.15V]) rather than reference against a nominal 1.8V supply.
12. For differential mode (RxS = LOW), A and $\overline{A}$/V_{REF} must be at the opposite rail.

POWER SUPPLY CHARACTERISTICS FOR 1.8V LVTTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	V_{DDQ} = Max., Reference Clock = LOW(3) Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	20	40	µA/MHz
I_{DDDQ}	Dynamic V_{DDQ} Power Supply Current per Output	V_{DD} = Max., V_{DDQ} = Max., C_L = 0pF	55	80	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	V_{DDQ} = 1.8V., $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	25	40	mA
		V_{DDQ} = 1.8V., $F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 15pF	40	60	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	V_{DDQ} = 1.8V., $F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 15pF	50	100	mA
		V_{DDQ} = 1.8V., $F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 15pF	120	240	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR 1.8V LVTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	V_{DDI}	V
V_X	Differential Input Signal Crossing Point(2)	$V_{DDI}/2$	mV
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	1.8	V/ns

NOTES:

1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input. A nominal 1.8V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1.8V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

SINGLE-ENDED INPUT AC TEST CONDITIONS FOR 1.8V LVTTL

Symbol	Parameter	Value	Units
V_{IH}	Input HIGH Voltage(1)	V_{DDI}	V
V_{IL}	Input LOW Voltage	0	V
V_{THI}	Input Timing Measurement Reference Level(2)	$V_{DDI}/2$	mV
t_R, t_F	Input Signal Edge Rate(3)	2	V/ns

NOTES:

1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input.
2. A nominal 900mV timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
3. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE(5)

Symbol	Parameter		Min.	Typ.	Max	Unit
Skew Parameters						
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew(1)	Single-Ended and Differential Modes	—	—	60	ps
		Single-Ended in Differential Mode (DSE)	—	60	—	
$t_{SK(INV)}$	Inverting Skew(2)	Single-Ended and Differential Modes	—	—	300	ps
		Single-Ended in Differential Mode (DSE)	—	300	—	
$t_{SK(P)}$	Pulse Skew(3)	Single-Ended and Differential Modes	—	—	300	ps
		Single-Ended in Differential Mode (DSE)	—	300	—	
$t_{SK(PP)}$	Part-to-Part Skew(4)	Single-Ended and Differential Modes	—	—	300	ps
		Single-Ended in Differential Mode (DSE)	—	300	—	
V_{OX}	HSTL and eHSTL Differential True and Complementary Output Crossing Voltage Level		$V_{DDQ}/2 - 200$	$V_{DDQ}/2$	$V_{DDQ}/2 + 200$	mV
Propagation Delay						
t_{PLH} t_{PHL}	Propagation Delay A to Qn/$\overline{Qn}$	2.5V / 1.8V LVTTL Outputs	—	—	2.5	ns
		HSTL / eHSTL Outputs	—	—	2	
t_R	Output Rise Time (20% to 80%)	2.5V / 1.8V LVTTL Outputs	350	—	1050	ps
		HSTL / eHSTL Outputs	350	—	1350	
t_F	Output Fall Time (20% to 80%)	2.5V / 1.8V LVTTL Outputs	350	—	1050	ps
		HSTL / eHSTL Outputs	350	—	1350	
f_O	Frequency Range (HSTL/eHSTL outputs)		—	—	250	MHz
	Frequency Range (2.5V/1.8V LVTTL outputs)		—	—	200	
Output Gate Enable/Disable Delay						
t_{PGE}	Output Gate Enable to Qn/$\overline{Qn}$		—	—	3.5	ns
t_{PGD}	Output Gate Enable to Qn/$\overline{Qn}$ Driven to GL Designated Level		—	—	3	ns

NOTES:

1. Skew measured between all outputs or output pairs under identical input and output interfaces, transitions and load conditions on any one device. For single ended and differential LVTTL outputs, this measurement is made when each output voltage passes through $V_{DDQ}/2$. For differential LVTTL outputs, the true outputs are compared only with other true outputs and the complementary outputs are compared only with other complementary outputs. For differential HSTL outputs, the measurement takes place at the crossing point of the true and complementary signals.
2. For operating with either 1.8V or 2.5V LVTTL output interfaces with both true and complementary outputs enabled. Inverting skew is the skew between true and complementary outputs switching in opposite directions under identical input and output interfaces, transitions and load conditions on any one device.
3. Skew measured is the difference between propagation delay times t_{PHL} and t_{PLH} of any output or output pair under identical input and output interfaces, transitions and load conditions on any one device. For single ended and differential LVTTL outputs, this measurement is made when each output voltage passes through $V_{DDQ}/2$. The measurement applies to both true and complementary signals. For differential HSTL outputs, the measurement takes place at the crossing point of the true and complementary signals.
4. Skew measured is the magnitude of the difference in propagation times between any outputs or output pairs of two devices, given identical transitions and load conditions at identical V_{DD}/V_{DDQ} levels and temperature.
5. Guaranteed by design.

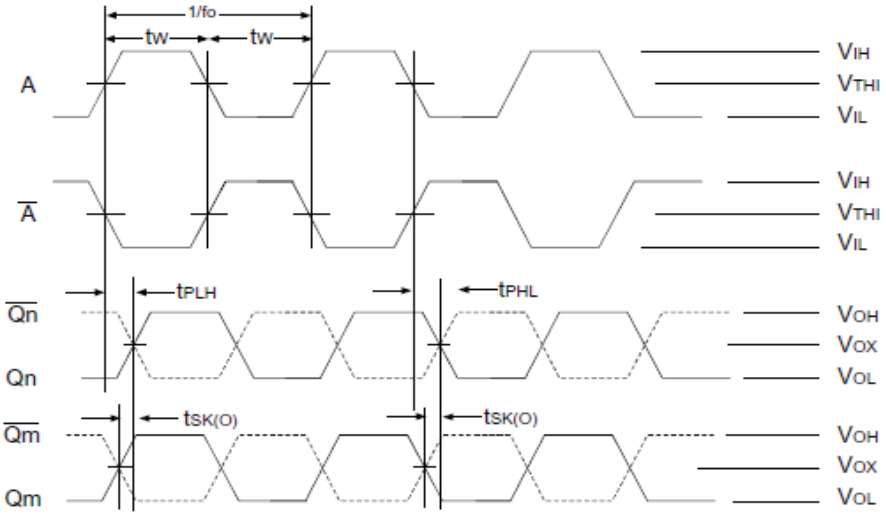
AC DIFFERENTIAL INPUT SPECIFICATIONS(1)

Symbol	Parameter	Min.	Typ.	Max	Unit
t_W	Reference Clock Pulse Width HIGH or LOW (HSTL/eHSTL outputs)(2)	1.73	—	—	ns
	Reference Clock Pulse Width HIGH or LOW (2.5V / 1.8V LVTTL outputs)(2)	2.17	—	—	
HSTL/eHSTL/1.8V LVTTL/2.5V LVTTL					
V_{DIF}	AC Differential Voltage(3)	400	—	—	mV
V_{IH}	AC Input HIGH(4,5)	Vx + 200	—	—	mV
V_{IL}	AC Input LOW(4,6)	—	—	Vx - 200	mV
LVEPECL					
V_{DIF}	AC Differential Voltage(3)	400	—	—	mV
V_{IH}	AC Input HIGH(4)	1275	—	—	mV
V_{IL}	AC Input LOW(4)	—	—	875	mV

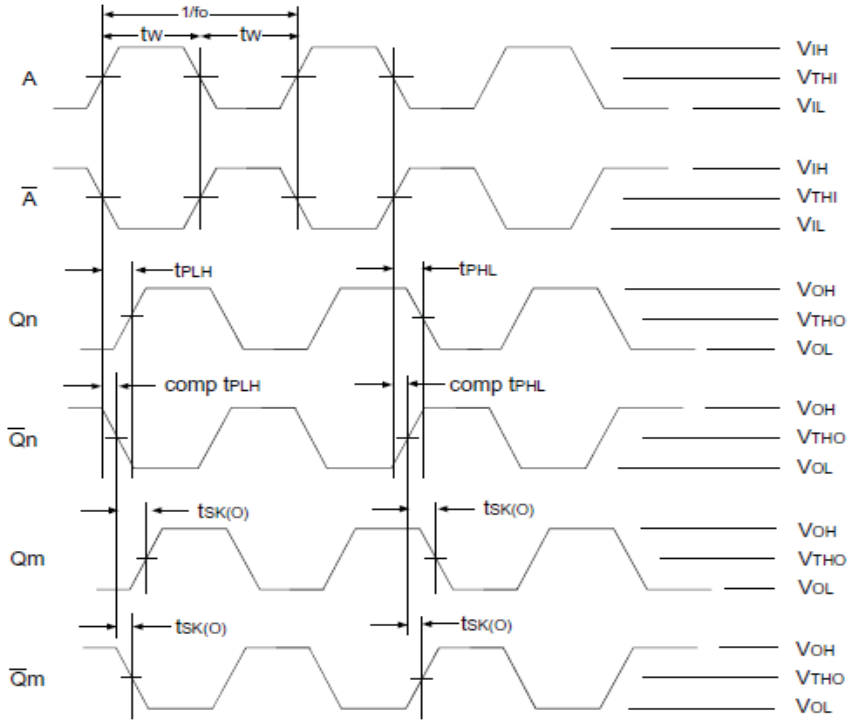
NOTES:

1. For differential input mode, RxS is tied to GND.
2. Both differential input signals should not be driven to the same level simultaneously. The input will not change state until the inputs have crossed and the voltage range defined by V_{DIF} has been met or exceeded.
3. Differential mode only. V_{DIF} specifies the minimum input voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
4. For single-ended operation, $\overline{A}/V_{REF}$ is tied to DC voltage (V_{REF}). Refer to each input interface's DC specification for the correct V_{REF} range.
5. Voltage required to switch to a logic HIGH, single-ended operation only.
6. Voltage required to switch to a logic LOW, single-ended operation only.

DIFFERENTIAL AC TIMING WAVEFORMS



HSTL and eHSTL Output Propagation and Skew Waveforms



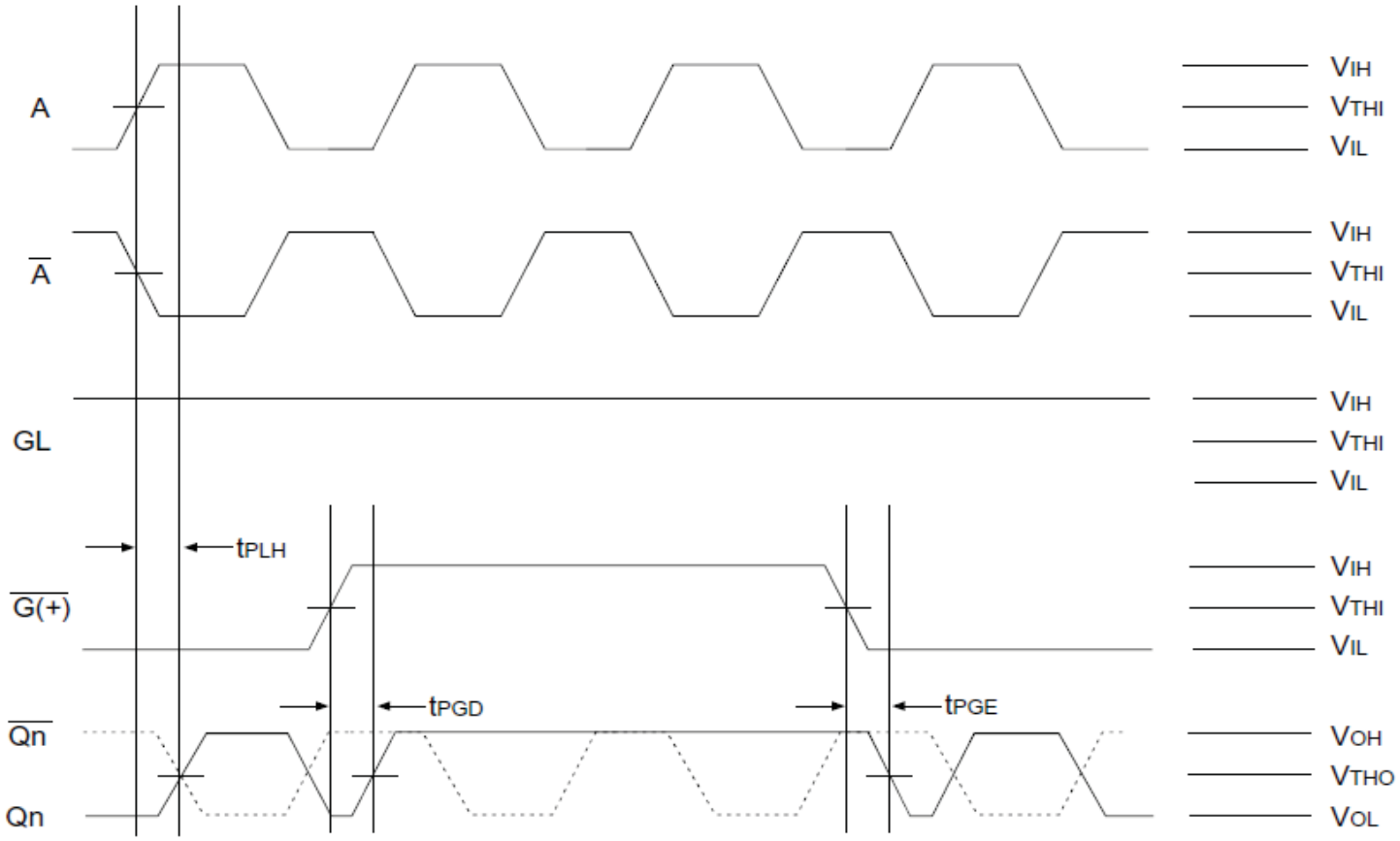
1.8V or 2.5V LVTTL Output Propagation and Skew Waveforms

NOTES:

1. For the HSTL and eHSTL outputs, t_{PHL} and t_{PLH} are measured from the input passing through V_{THI} or input pair crossing to the crossing point of each Qn and $\overline{Q}$n.
2. For 1.8V and 2.5V LVTTL outputs, t_{PHL} and t_{PLH} are measured from the input passing through V_{THI} or input pair crossing to the slower of Qn or $\overline{Q}$n passing through V_{THO}.
3. Pulse skew is calculated using the following expression:

   $t_{SK(P)} = | t_{PHL} - t_{PLH} |$

   where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from the rising and falling edges of a single pulse. Note that the t_{PHL} and t_{PLH} shown above are not valid measurements for this calculation because they are not taken from the same pulse.

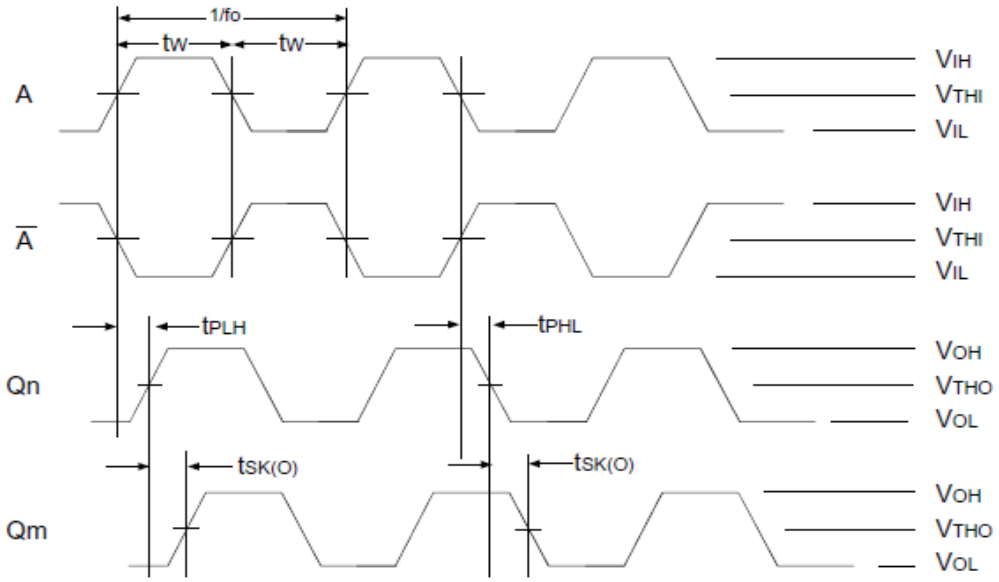


Differential Gate Disable/Enable Showing Runt Pulse Generation

NOTES:

1. The waveforms shown only gate "true" output, Qn.
2. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their $\overline{Gx}$ signals to avoid this problem.

SDR AC TIMING WAVEFORMS



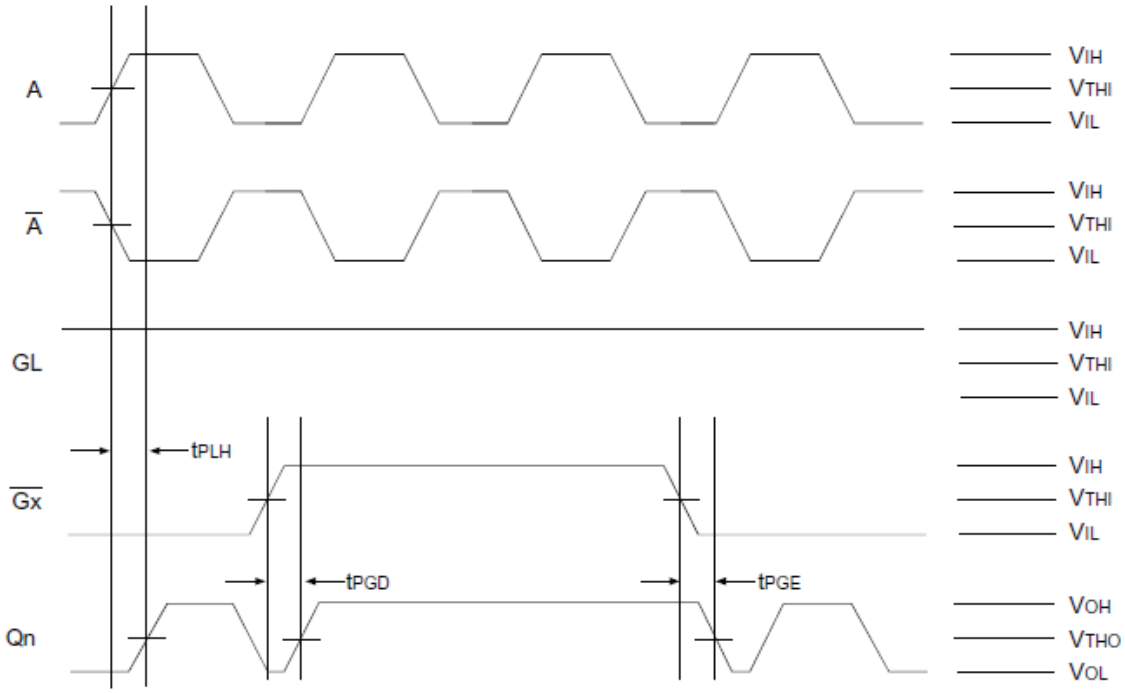
Propagation and Skew Waveforms

NOTES:

1. t_{PHL} and t_{PLH} signals are measured from the input passing through V_{THI} or input pair crossing to Qn passing through V_{THO}.
2. Pulse Skew is calculated using the following expression:

   $$t_{SK(P)} = | t_{PHL} - t_{PLH} |$$

   where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the t_{PHL} and t_{PLH} shown are not valid measurements for this calculation because they are not taken from the same pulse.

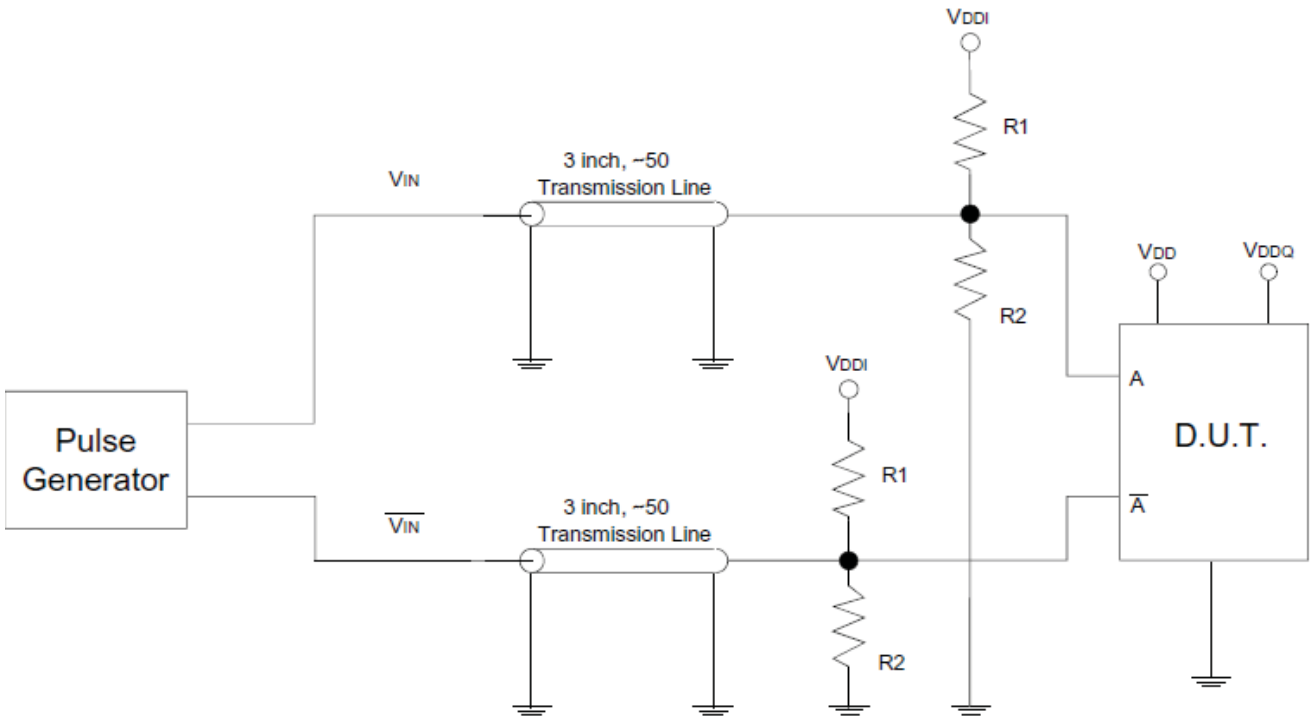


SDR Gate Disable/Enable Showing Runt Pulse Generation

NOTE:

As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their $\overline{Gx}$ signals to avoid this problem.

TEST CIRCUITS AND CONDITIONS



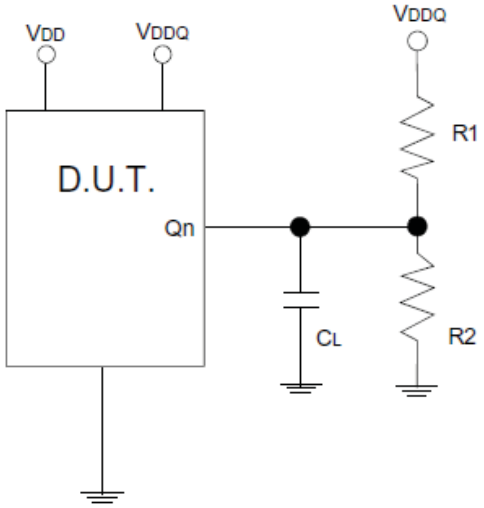
Test Circuit for Differential Input(1)

DIFFERENTIAL INPUT TEST CONDITIONS

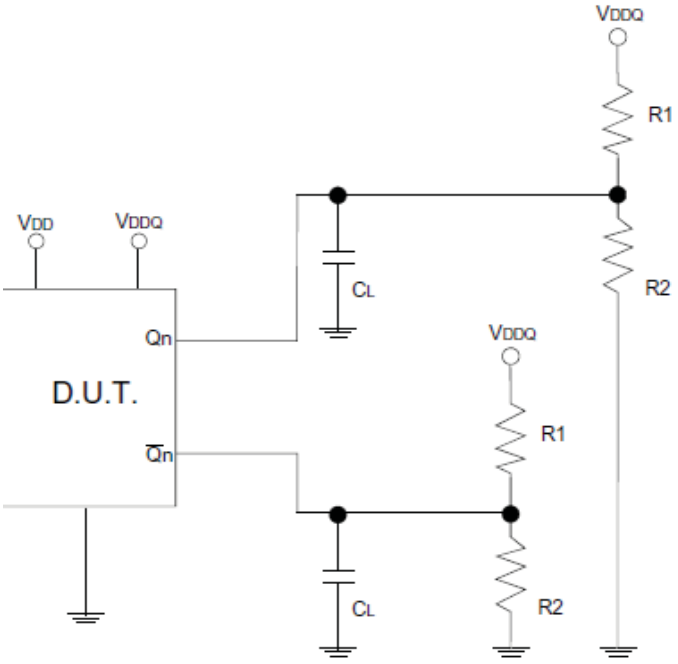
Symbol	V_{DD} = 2.5V ± 0.1V	Unit
R1	100	Ω
R2	100	Ω
V_{DDI}	V_{CM}*2	V
V_{THI}	HSTL: Crossing of A and $\overline{A}$ eHSTL: Crossing of A and $\overline{A}$ LVEPECL: Crossing of A and $\overline{A}$ 1.8V LVTTL: V_{DDI}/2 2.5V LVTTL: V_{DD}/2	V

NOTE:

1. This input configuration is used for all input interfaces. For single-ended testing, the V_{IN} input $\overline{\text{is}}$ tied to GND. For testing single-ended in differential input mode, the V_{IN} is left $\overline{\text{floating}}$.



Test Circuit for SDR Outputs



Test Circuit for Differential Outputs

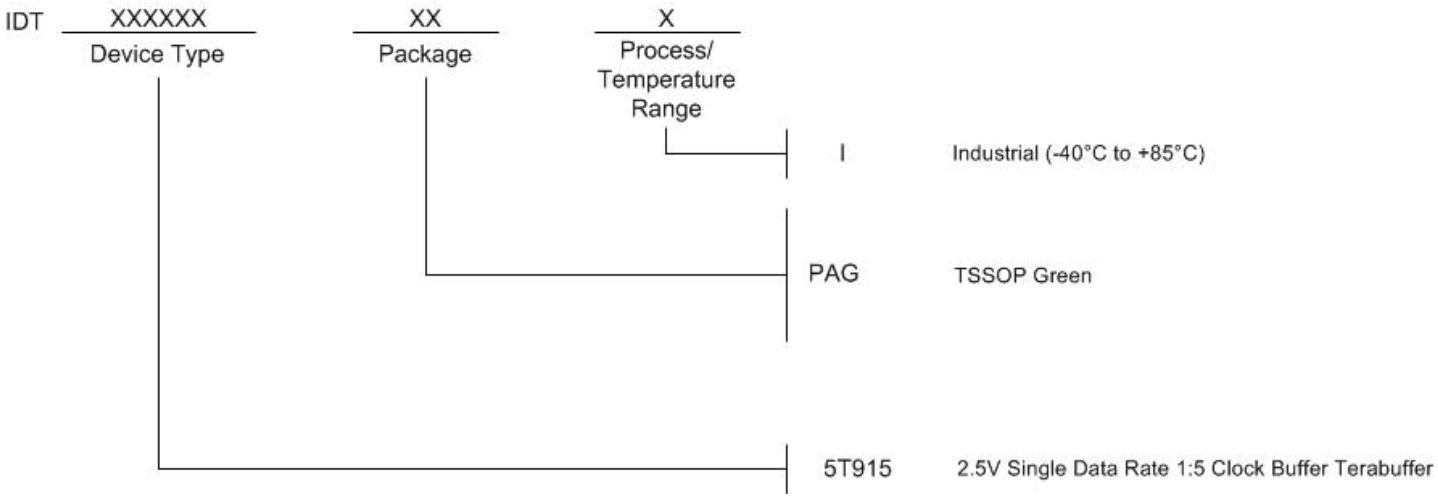
SDR OUTPUT TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.1V V_{DDQ} = Interface Specified	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{THO}	V_{DDQ} / 2	V

DIFFERENTIAL OUTPUT TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.1V V_{DDQ} = Interface Specified	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{OX}	HSTL: Crossing of Qn and $\overline{Qn}$ eHSTL: Crossing of Qn and $\overline{Qn}$	V
V_{THO}	1.8V LVTTL: V_{DDQ}/2 2.5V LVTTL: V_{DDQ}/2	V

ORDERING INFORMATION



REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
A		1	NRND - Not Recommended for New Designs	5/5/13
A		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05 Updated data sheet format	11/3/15

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