FEMTOCLOCK® CRYSTAL-TO-LVDS CLOCK GENERATOR

ICS844251-14

General Description

The ICS844251-14 is an Ethernet Clock Generator. The ICS844251-14 uses an 18pF parallel resonant crystal over the range of 23.2MHz – 30MHz. For Ethernet applications, a 25MHz crystal is used. The device has excellent <1ps phase jitter performance, over the 1.875MHz – 20MHz integration range. The ICS844251-14 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

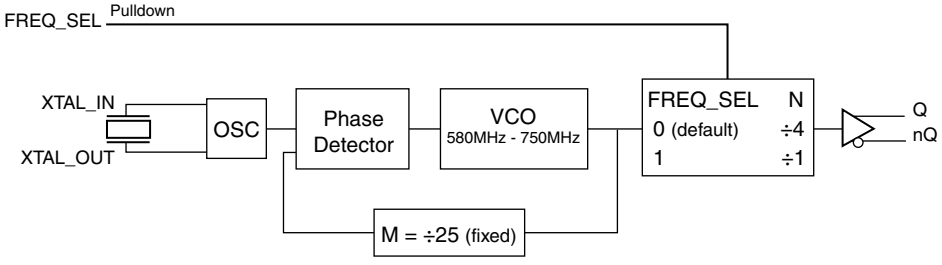
Features

- One differential LVDS output pair
- Crystal oscillator interface designed for 18pF, parallel resonant crystal (23.2MHz – 30MHz)
- Output frequency ranges: 145MHz – 187.5MHz and 580MHz – 750MHz
- VCO range: 580MHz – 750MHz
- RMS phase jitter at 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.53ps (typical)
- Full 3.3V or 2.5V output supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

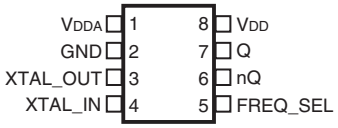
Common Configuration Table

Inputs					Output Frequency Range (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	1	25	1	25	625
26.67	1	25	1	25	666.67
25 (default)	0	25	4	6.25	156.25

Block Diagram



Pin Assignment



ICS844251-14
8 Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Output		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVDS interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLdown}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				10	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
I_{DD}	Power Supply Current				95	mA
I_{DDA}	Analog Supply Current				10	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 3.465V	2		V_{DD} + 0.3	V
		V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.465V	-0.3		0.8	V
		V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

Table 3D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.275		1.525	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 3E. LVDS DC Characteristics, $V_{DD} = V_{DDA}$ = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.0		1.4	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		23.2		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: It is not recommended to overdrive the crystal input with an external clock.

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 0	145		187.5	MHz
		FREQ_SEL = 1	580		750	MHz
$t_{jit}(\Phi)$	RMS Phase Jitter, Random; NOTE 1	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.53		ps
		625MHz, Integration Range: 1.875MHz – 20MHz		0.45		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	70		550	ps
odc	Output Duty Cycle	FREQ_SEL = 0	48		52	%
		FREQ_SEL = 1	46		54	%

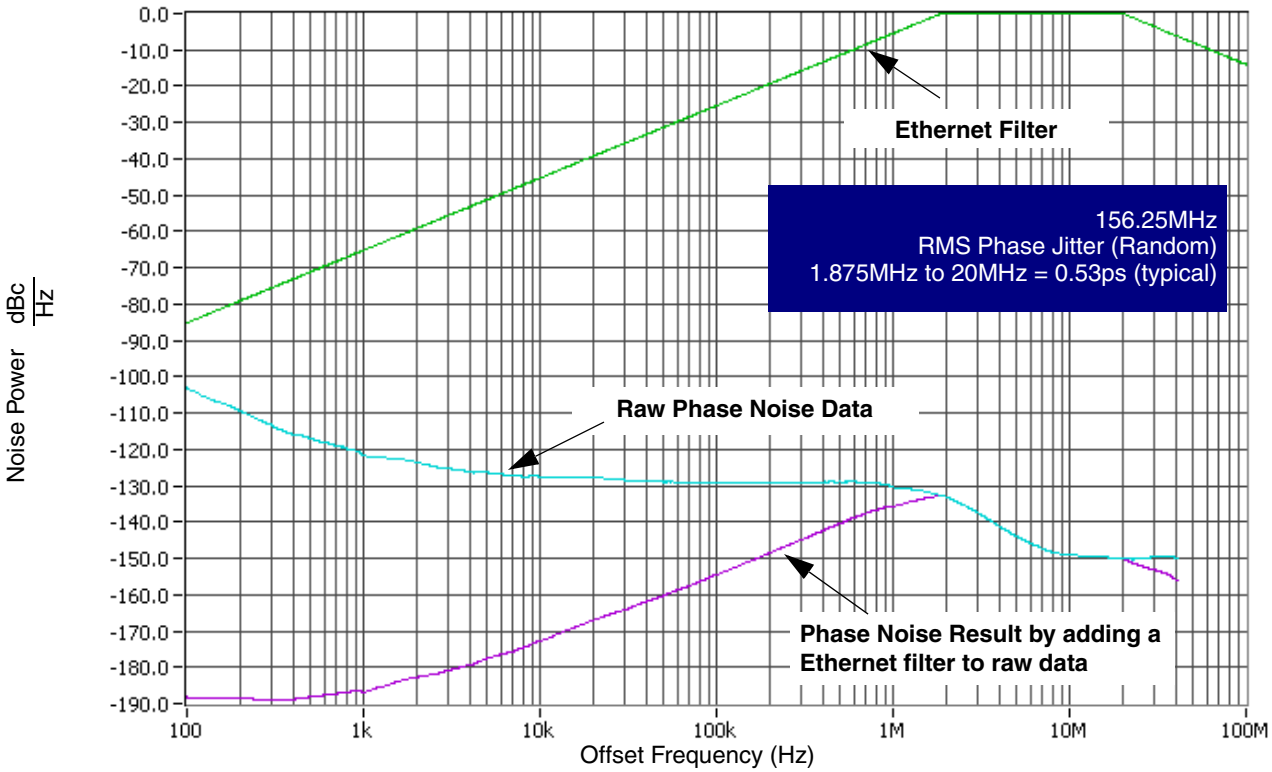
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

Table 5B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

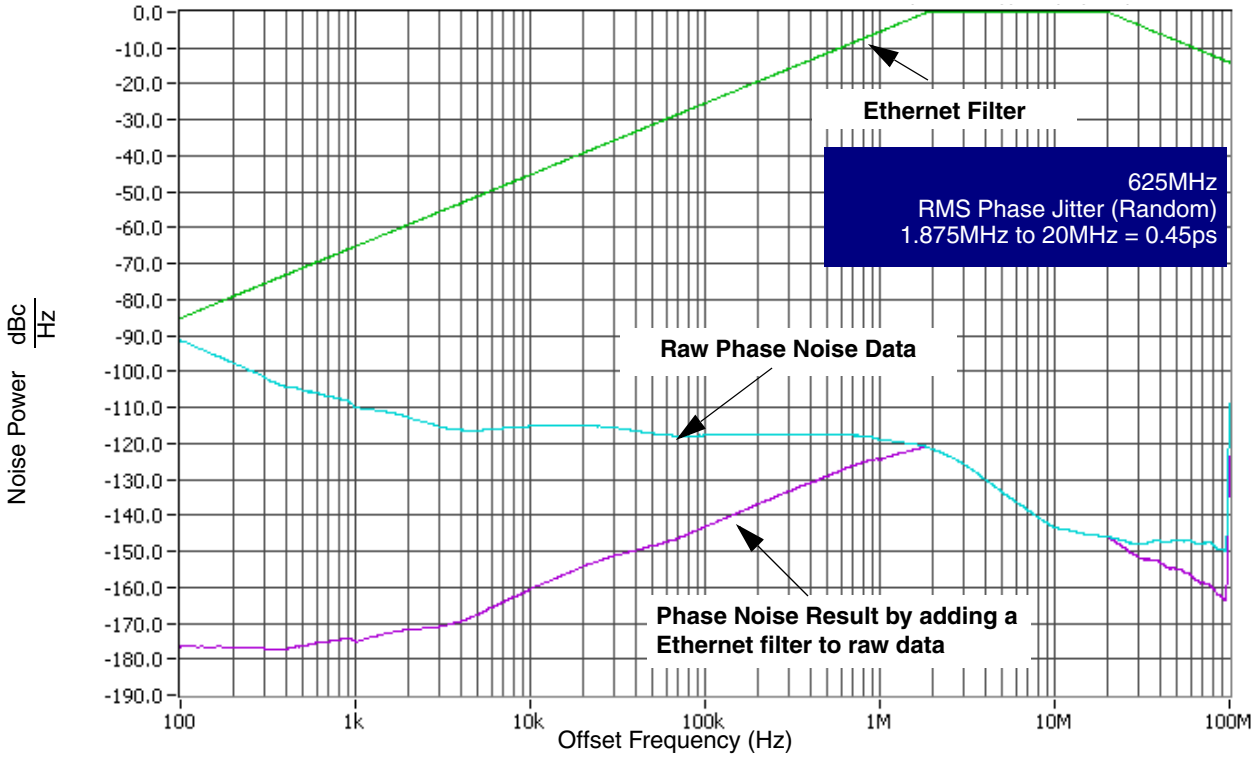
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 0	145		187.5	MHz
		FREQ_SEL = 1	580		750	MHz
$t_{jit}(\Phi)$	RMS Phase Jitter, Random; NOTE 1	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.54		ps
		625MHz, Integration Range: 1.875MHz – 20MHz		0.45		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	70		550	ps
odc	Output Duty Cycle	FREQ_SEL = 0	48		52	%
		FREQ_SEL = 1	46		54	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

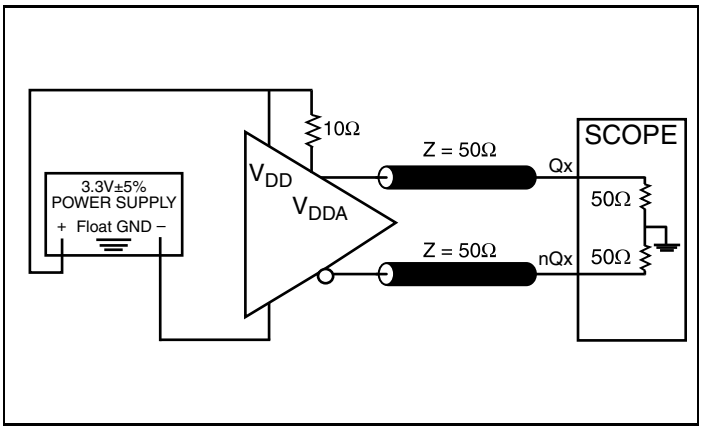
Typical Phase Noise at 156.25MHz (3.3V)



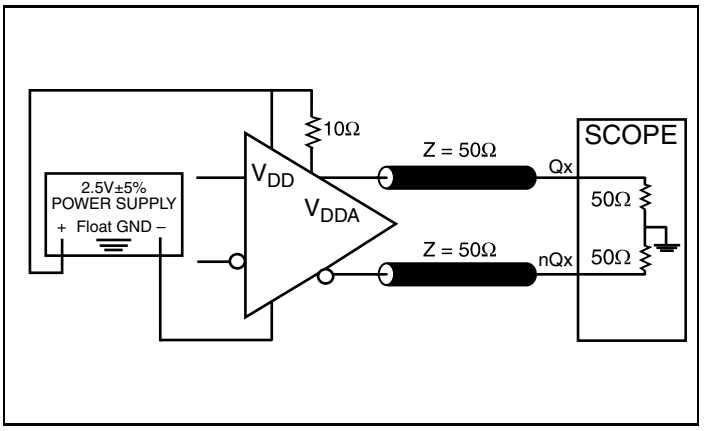
Typical Phase Noise at 625MHz (3.3V)



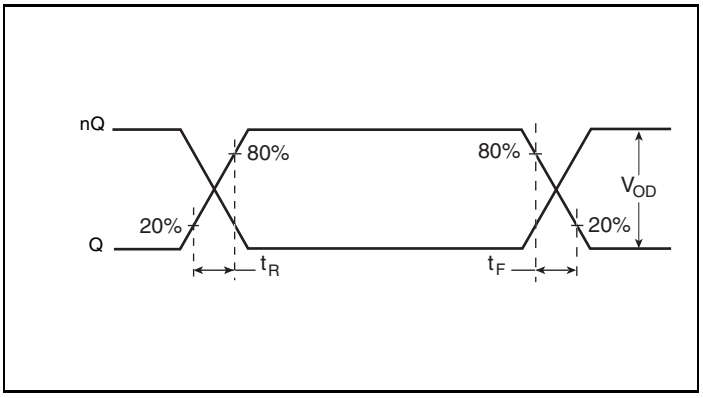
Parameter Measurement Information



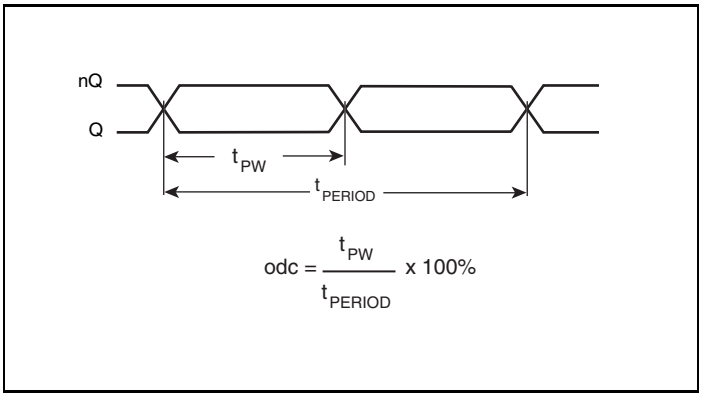
3.3V LVDS Output Load AC Test Circuit



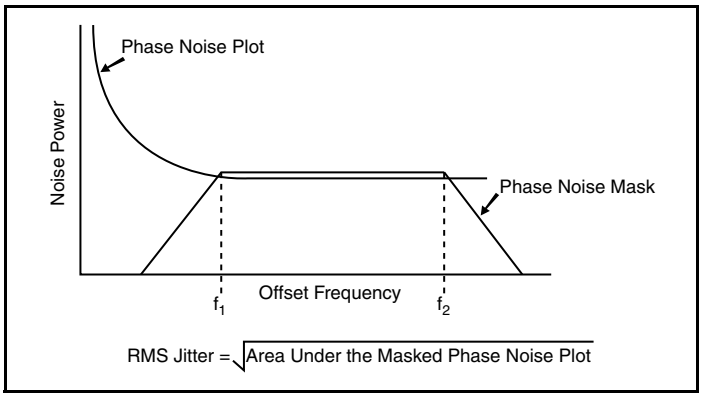
2.5V LVDS Output Load AC Test Circuit



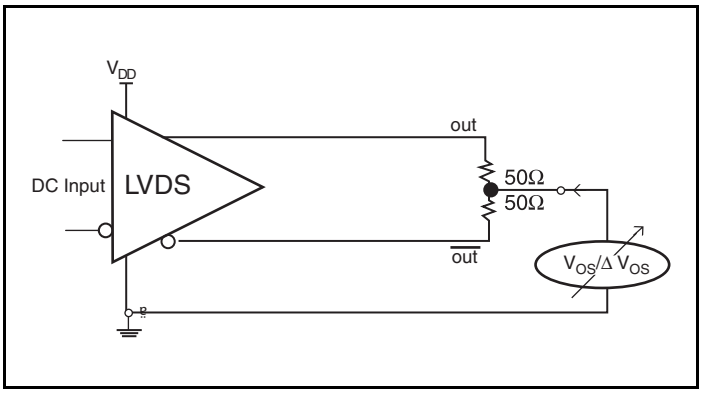
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

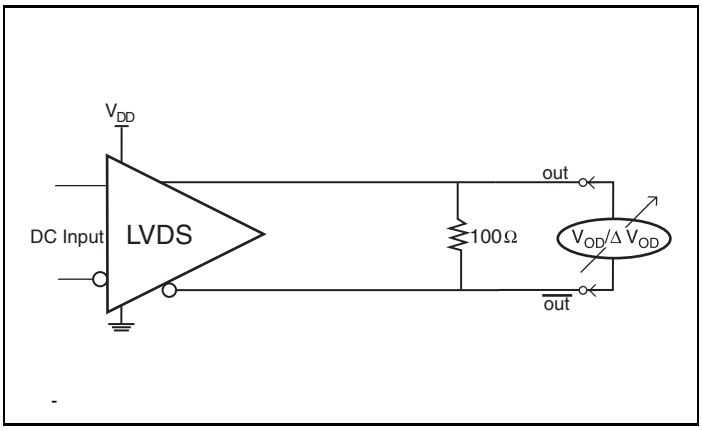


RMS Phase Jitter



OFFSET VOLTAGE SETUP

Parameter Measurement Information, continued



DIFFERENTIAL OUTPUT VOLTAGE SETUP

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844251-14 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

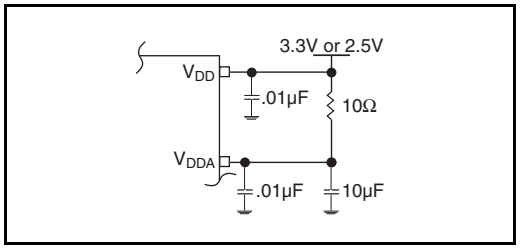


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS844251-14 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

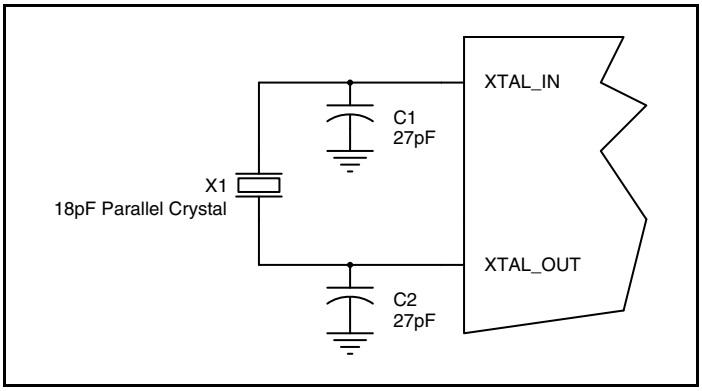


Figure 2. Crystal Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure XA* can be used with either type of output structure. *Figure XB*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

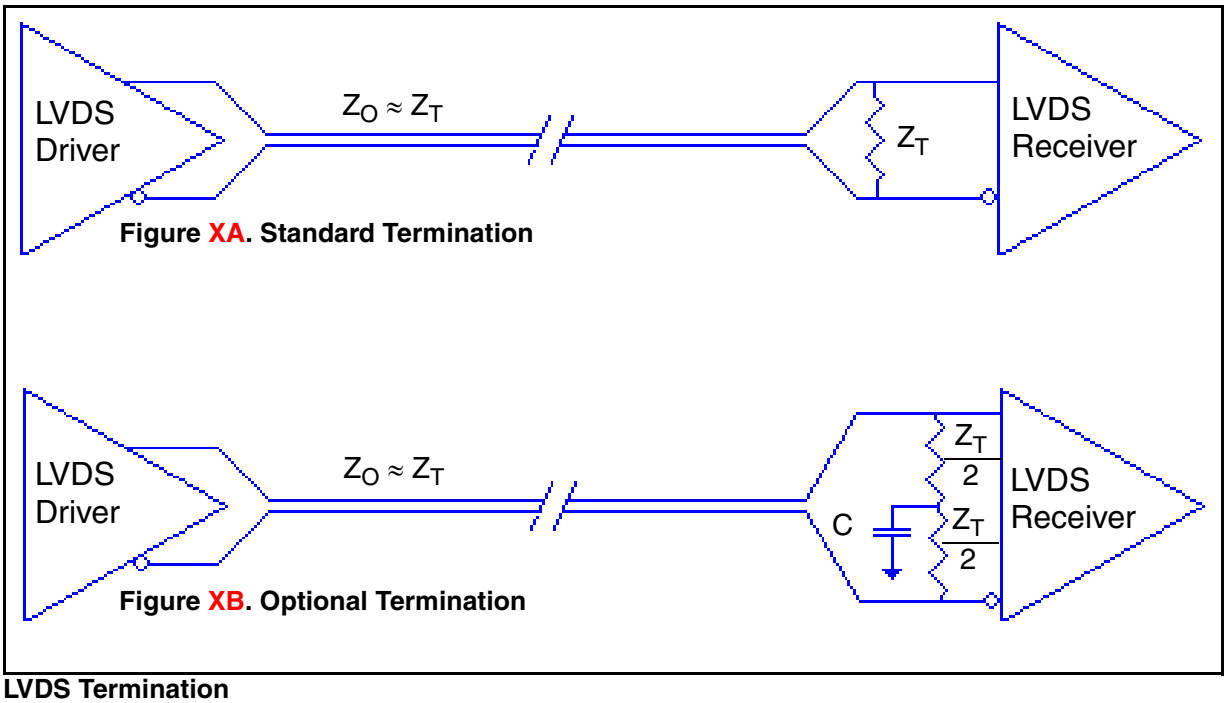


Figure XA. Standard Termination

Figure XB. Optional Termination

LVDS Termination

Schematic Example

Figure 5 shows an example of ICS844251-14 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitor should be located as close as possible to the power pin. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. For the LVDS output drivers, place a 100Ω resistor as close to the receiver as possible.

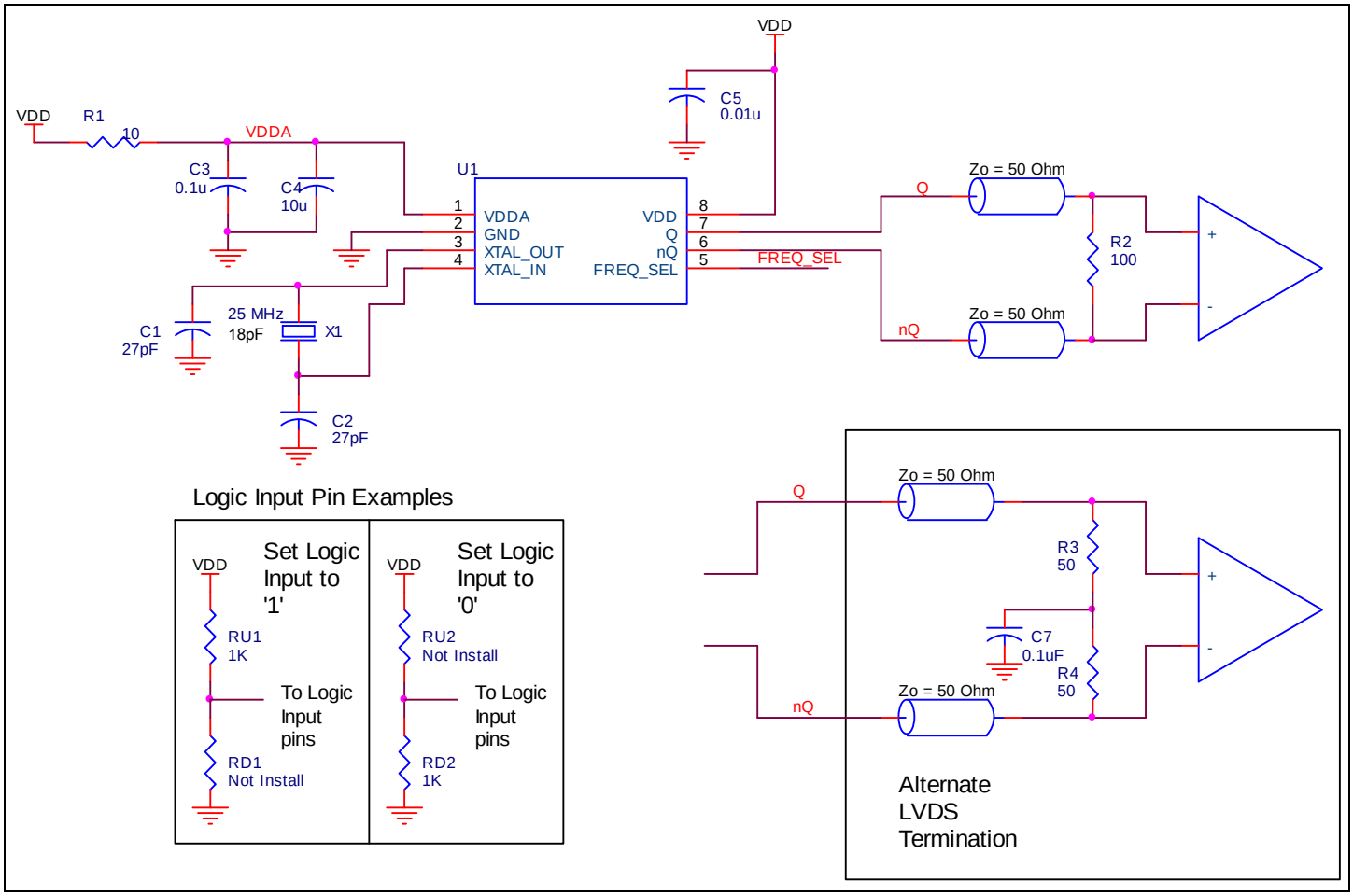


Figure 5. ICS844251-14 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844251-14.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844251-14 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (100mA + 10mA) = **381.15mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5.°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.381W *129.5°C/W = 119.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

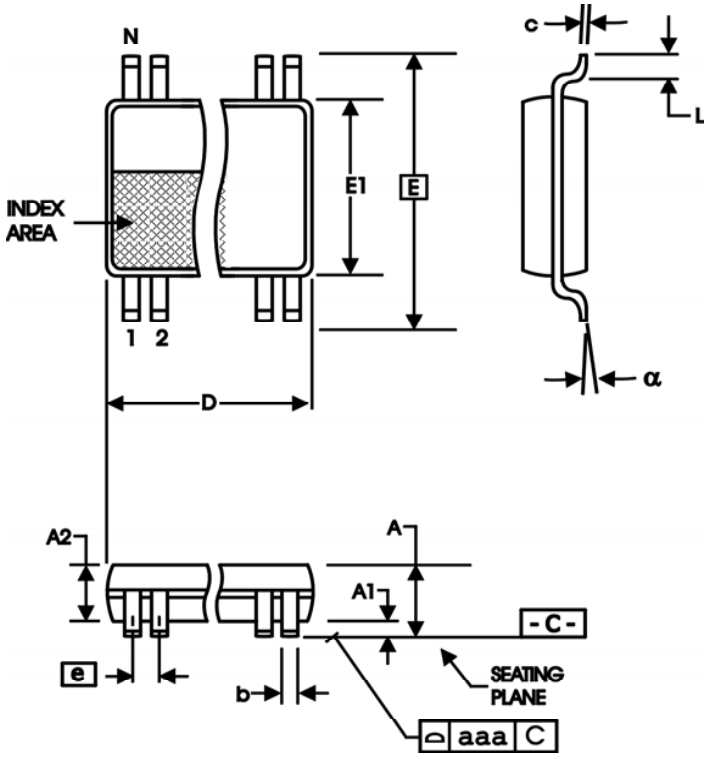
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for ICS844251-14 is: 2401

Package Outline and Package Dimensions

Table 8. Package Dimensions



Package Outline - G Suffix for 8 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844251BG-14	51B14	8 Lead TSSOP	Tube	0°C to 70°C
844251BG-14T	51B14	8 Lead TSSOP	Tape & Reel	0°C to 70°C
844251BG-14LF	1B14L	“Lead-Free” 8 Lead TSSOP	Tube	0°C to 70°C
844251BG-14LFT	1B14L	“Lead-Free” 8 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		11	Added schematic layout.	5/1/09
A		1	Deleted HiPerClockS references throughout.	11/2/12
	T4	4	Crystal Characteristics Table - added note.	
		8	Deleted application note, *LVCMOS to XTAL Interface*.	
		9	Updated Driver Termination Note.	
	T9	13	Deleted quantity from tape and reel. Deleted lead-free note.	

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