Low Skew, Dual, Differential-to-LVDS Fanout Buffer

ICS854S036

DATA SHEET

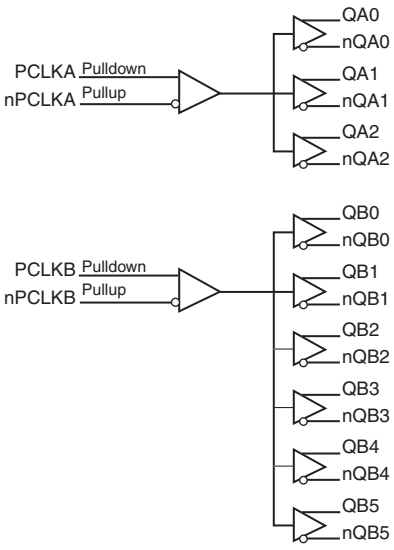
General Description

The ICS854S036 is a low skew, high performance Dual Differential-to-LVDS Fanout Buffer. One of the two fanout buffers has 3 LVDS outputs, the other has 6 LVDS outputs. The PCLKx, nPCLKx pairs can accept most standard differential input levels. The ICS854S036 is characterized to operate from a 3.3V power supply. Guaranteed output and bank skew characteristics make the ICS854S036 ideal for those clock distribution applications demanding well defined performance and repeatability.

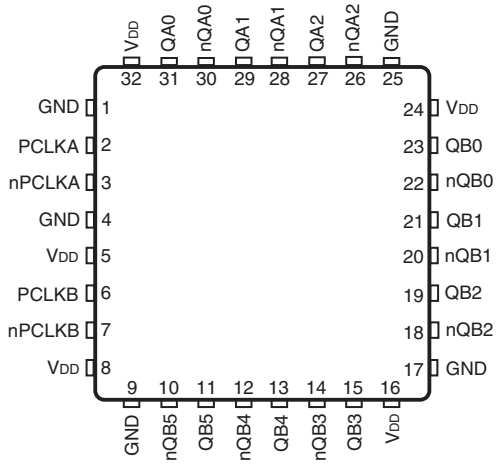
Features

- Two independent differential LVDS output buffers, buffer A with three outputs, buffer B with 6 outputs
- Two differential clock input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: 2GHz
- Translates any single ended input signal to LVDS levels with resistor bias on nPCLKx input
- Output skew: 100ps (maximum)
- Bank skew: 20ps (maximum)
- Propagation delay: 550ps (maximum)
- Additive phase jitter, RMS: 0.06ps (typical)
- Full 3.3V power supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS854S036
32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 4, 9, 17, 25	GND	Power		Power supply ground.
2	PCLKA	Input	Pulldown	Non-inverting differential clock input.
3	nPCLKA	Input	Pullup	Inverting differential clock input.
5, 8, 16, 24, 32	V_{DD}	Power		Power supply pins.
6	PCLKB	Input	Pulldown	Non-inverting differential clock input.
7	nPCLKB	Input	Pullup	Inverting differential clock input.
10, 11	nQB5, QB5	Output		Differential output pair. LVDS interface levels.
12, 13	nQB4, QB4	Output		Differential output pair. LVDS interface levels.
14, 15	nQB3, QB3	Output		Differential output pair. LVDS interface levels.
18, 19	nQB2, QB2	Output		Differential output pair. LVDS interface levels.
20, 21	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
22, 23	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
26, 27	nQA2, QA2	Output		Differential output pair. LVDS interface levels.
28, 29	nQA1, QA1	Output		Differential output pair. LVDS interface levels.
30, 31	nQA0, QA0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
PCLKA, PCLKB	nPCLKA, nPCLKB	QA[0:2], QB[0:5]	nQA[0:2], nQB[0:5]		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-ended to Differential	Inverting

NOTE 1: Refer to the Application Information Section, *Wiring the Differential Input to Accept Single-ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	42.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				210	mA

Table 4B. LVPECL Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLKA, PCLKB	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLKA, nPCLKB	$V_{DD} = V_{IN}$ = 3.465V			10	µA
I_{IL}	Input Low Current	PCLKA, PCLKB	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLKA, nPCLKB	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.25		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.25		V_{DD}	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4C. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

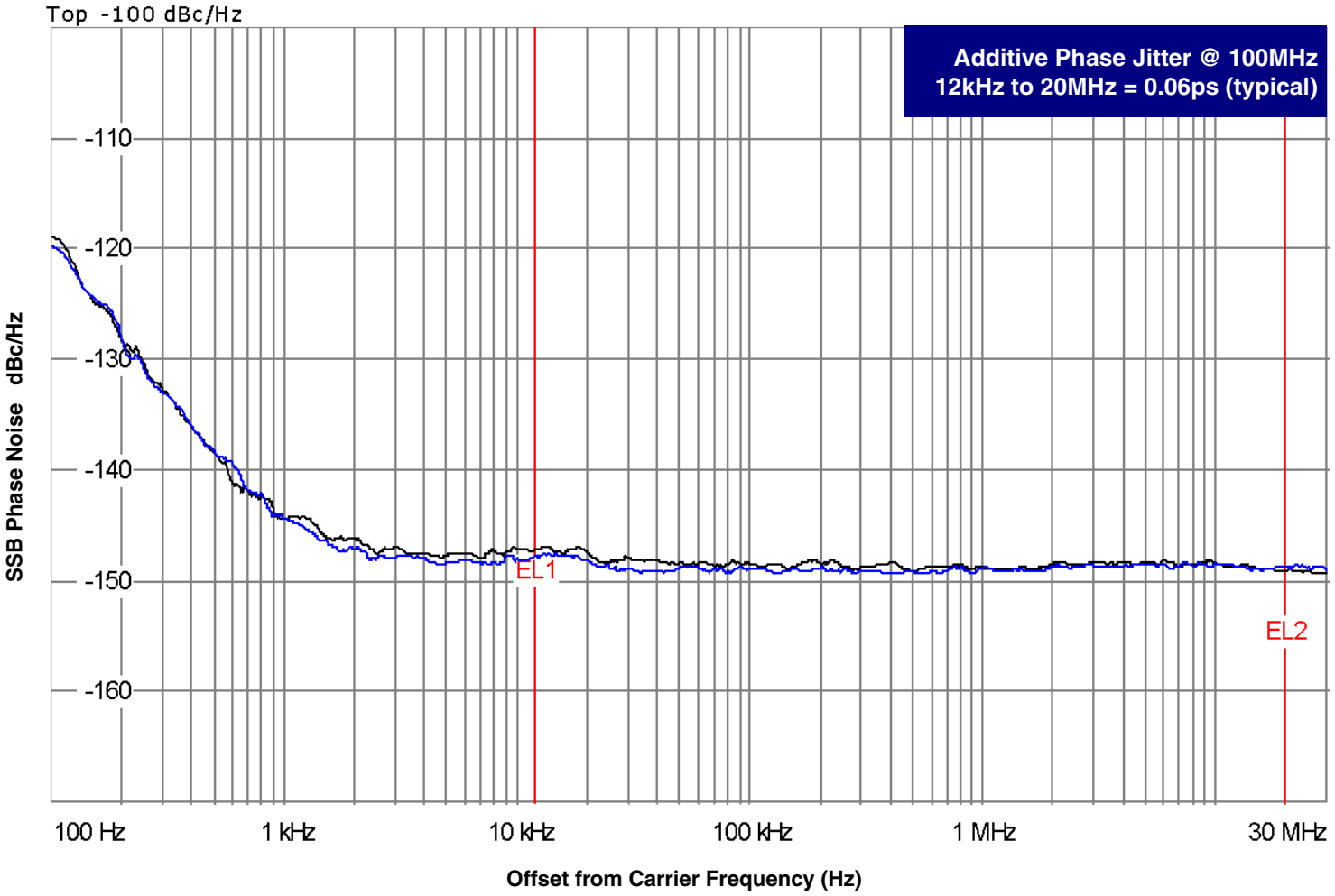
Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2	GHz
t_{PD}	Propagation Delay; NOTE 1		300		550	ps
tsk(o)	Output Skew; NOTE 2, 4				100	ps
tsk(b)	Bank Skew; NOTE 3, 4				20	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.06		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		250	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured from the output differential cross points.
NOTE 3: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

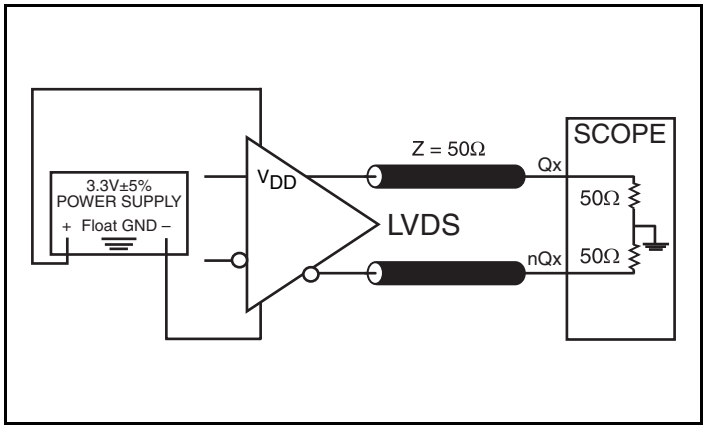
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



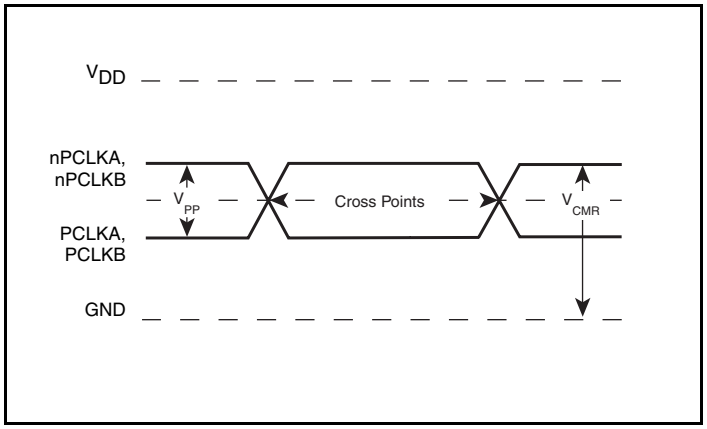
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

IFR2042 10kHz - 5.4GHz Low Noise Signal Generator as external input to a Hewlett Packard 8133A 3GHz Pulse Generator.

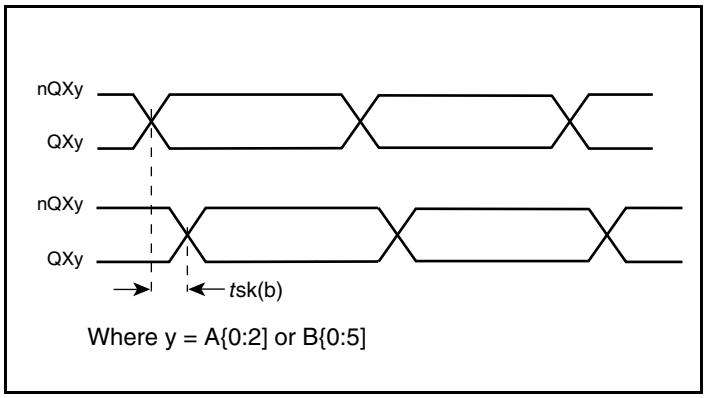
Parameter Measurement Information



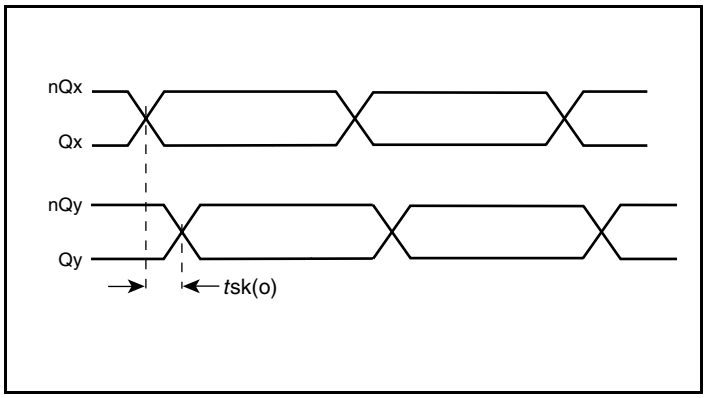
3.3V LVDS Output Load AC Test Circuit



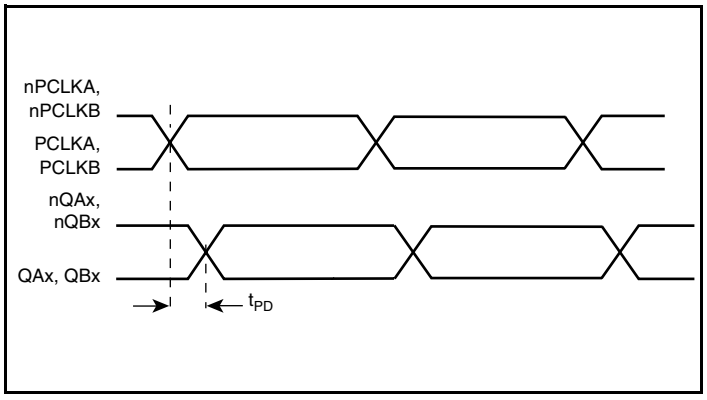
Differential Input Level



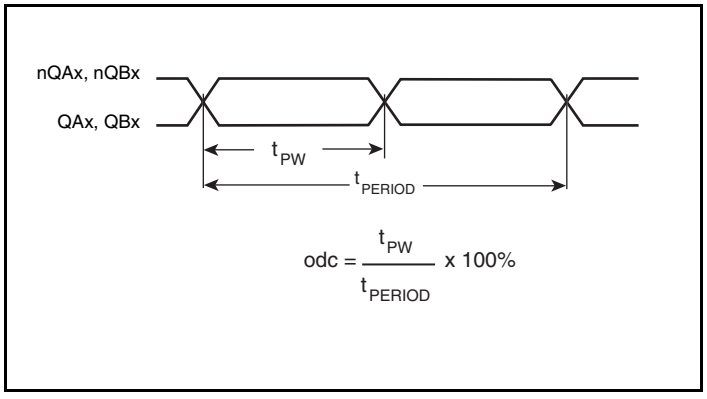
Bank Skew



Output Skew

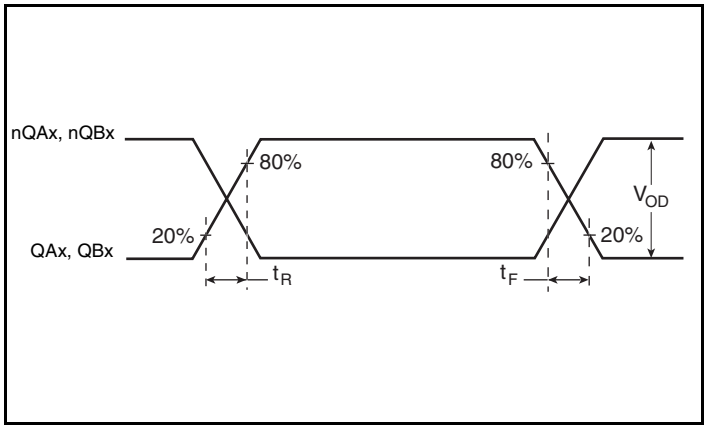


Propagation Delay

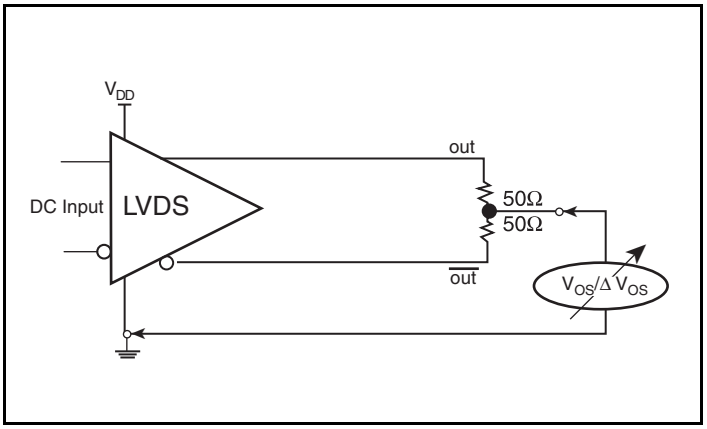


Output Duty Cycle/Pulse Width/Period

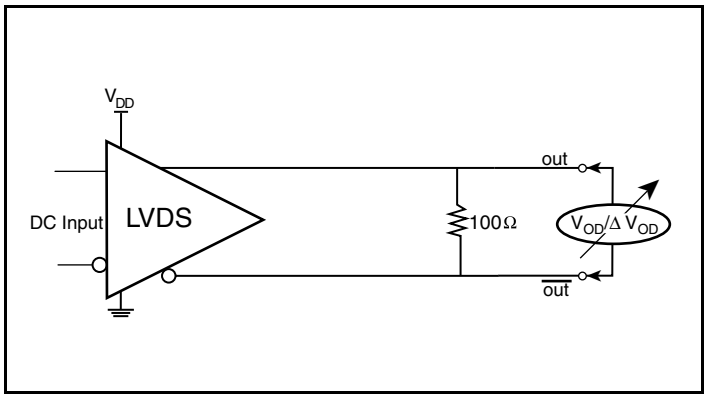
Parameter Measurement Information, continued



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

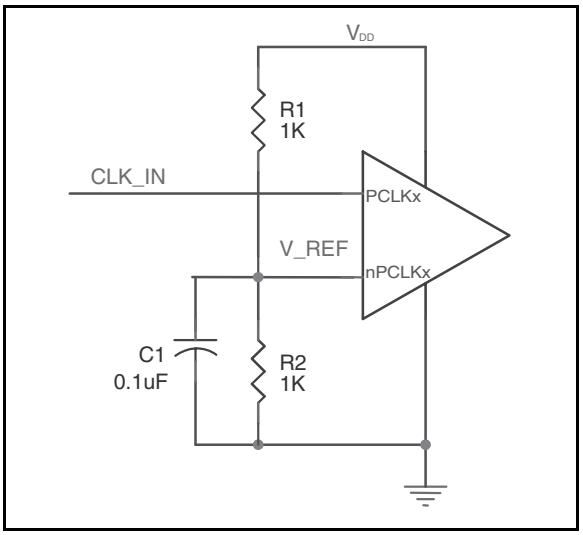


Figure 1. Single-Ended Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the PCLK/ nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

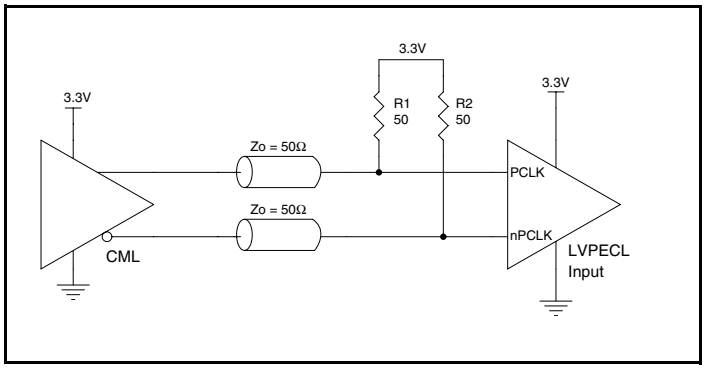


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

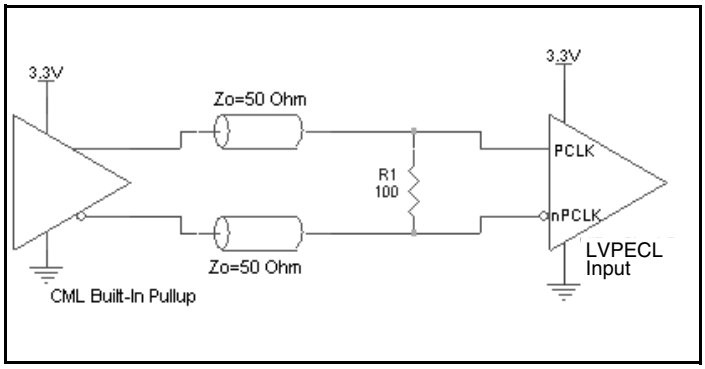


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

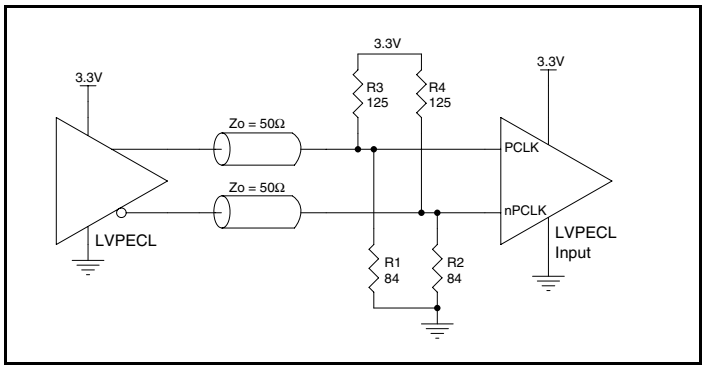


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

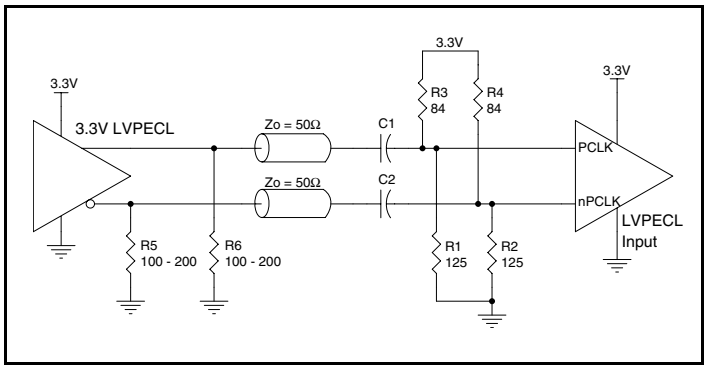


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

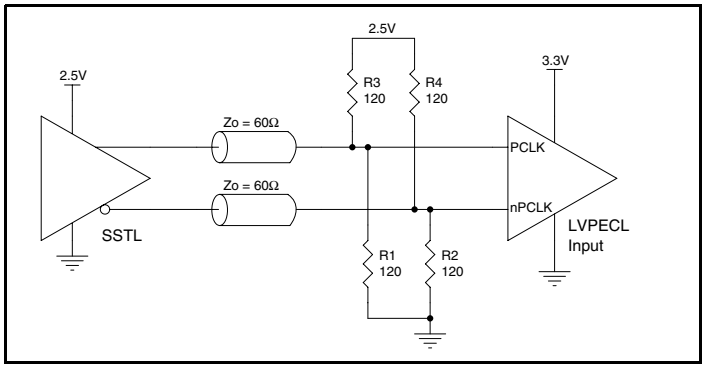


Figure 2E. PCLK/nPCLK Input Driven by an SSTL Driver

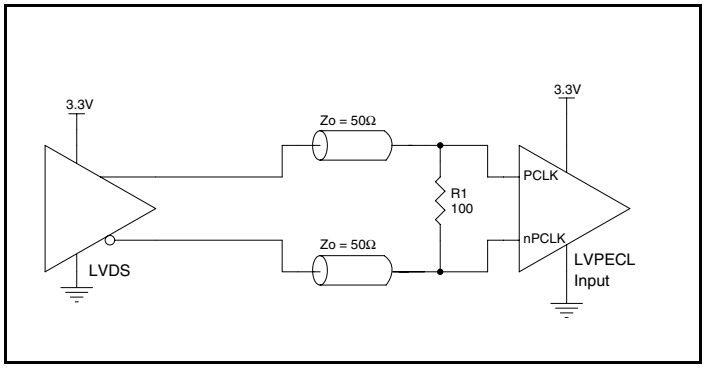


Figure 2F. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

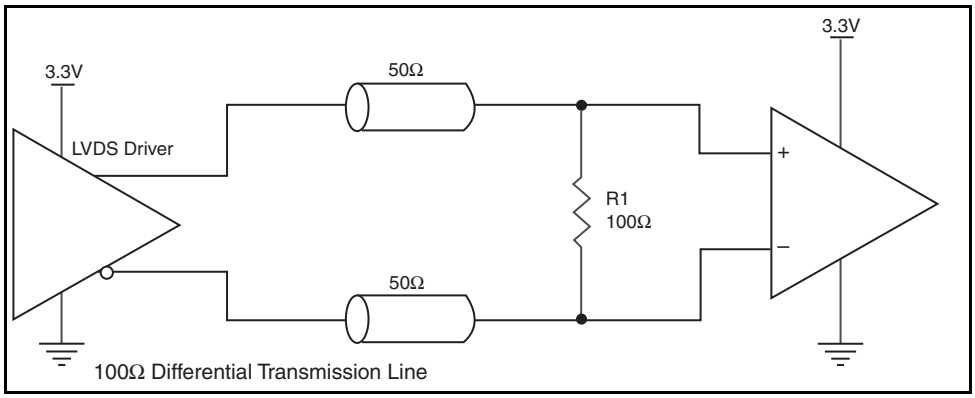


Figure 3. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

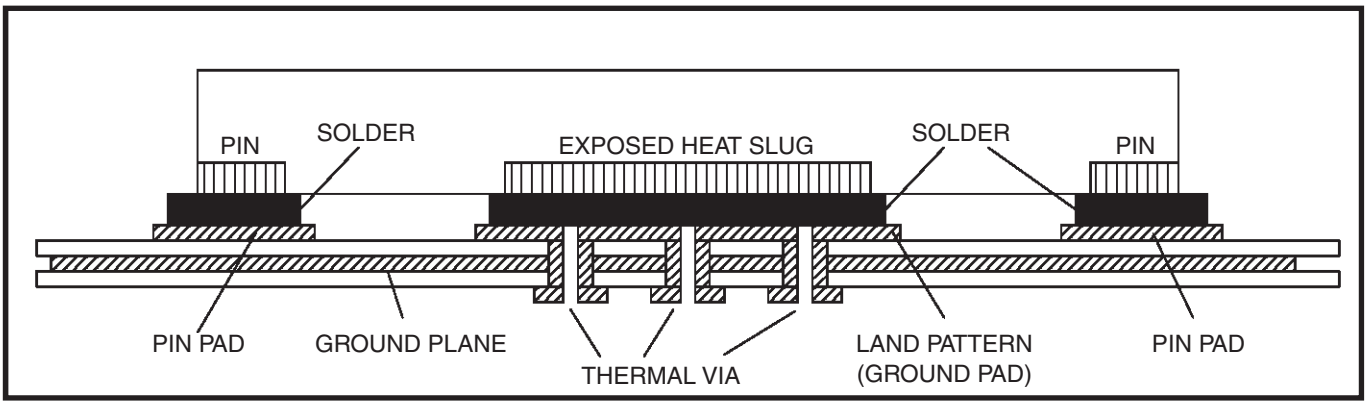


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S036.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S036 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 210mA = **727.65mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.728W * 42.7°C/W = 101.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

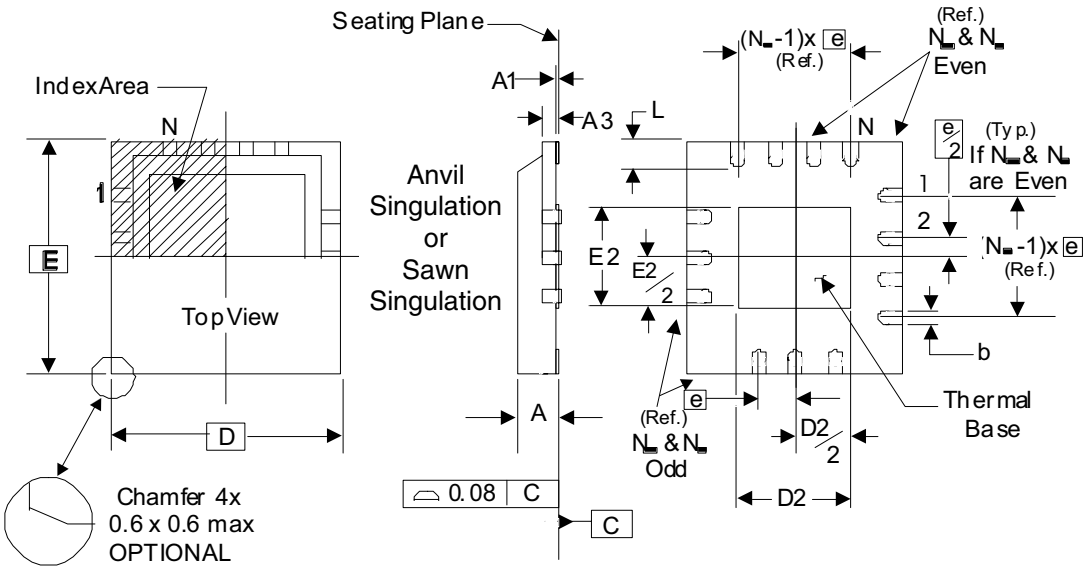
θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

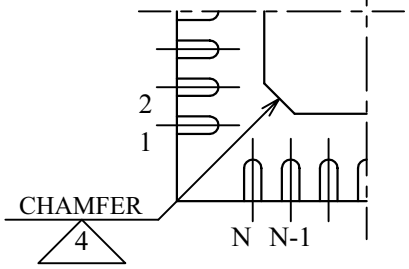
The transistor count for ICS854S036 is: 504

Package Outline and Package Dimensions

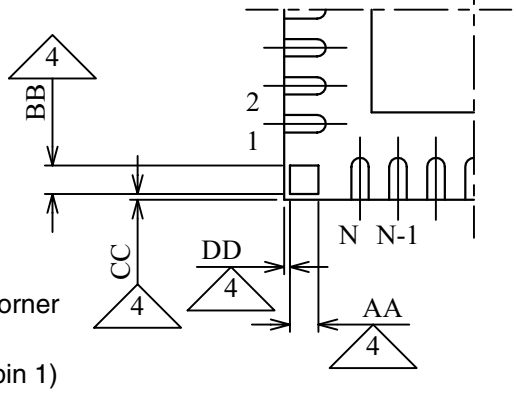
Package Outline - K Suffix for 32 Lead VFQFN



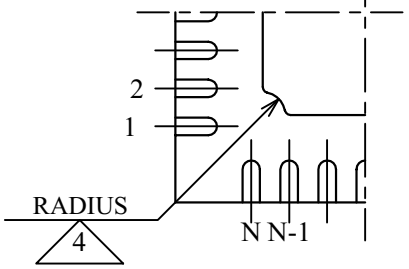
Bottom View w/Type A ID



Bottom View w/Type B ID



Bottom View w/Type C ID



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S036AKLF	ICS54S036AL	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
854S036AKLFT	ICS54S036AL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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