

GENERAL DESCRIPTION

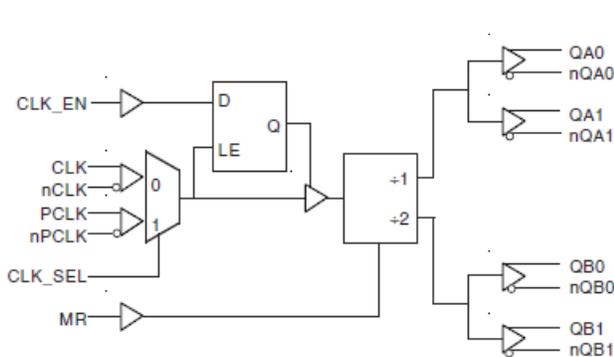
The 8737I-11 is a low skew, high performance Differential-to-3.3V LVPECL ClockGenerator/Divider. The 8737I-11 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8737I-11 ideal for clock distribution applications demanding well defined performance and repeatability.

FEATURES

- Two divide by 1 differential 3.3V LVPECL outputs; Two divide by 2 differential 3.3V LVPECL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single ended input signal (LVCMOS, LVTTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Output skew: 75ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Bank skew: Bank A - 30ps (maximum)
Bank B - 45ps (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS-compliant package

BLOCK DIAGRAM



PIN ASSIGNMENT

| | | | |
|-----------------|----|----|-----------------|
| V _{EE} | 1 | 20 | QA0 |
| CLK_EN | 2 | 19 | nQA0 |
| CLK_SEL | 3 | 18 | V _{CC} |
| CLK | 4 | 17 | QA1 |
| nCLK | 5 | 16 | nQA1 |
| PCLK | 6 | 15 | QB0 |
| nPCLK | 7 | 14 | nQB0 |
| nc | 8 | 13 | V _{CC} |
| MR | 9 | 12 | QB1 |
| V _{CC} | 10 | 11 | nQB1 |

8737I-11

20-Lead TSSOP

6.50mm x 4.40mm x 0.92 package body

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|------------|-----------------|--------|----------|--|
| 1 | V _{EE} | Power | | Negative supply pin. |
| 2 | CLK_EN | Power | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock Select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTTL interface levels. |
| 4 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 5 | nCLK | Input | Pullup | Inverting differential clock input. |
| 6 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 7 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 8 | nc | Unused | | No connect. |
| 9 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset. When LOW, the Master Reset is disabled. LVCMOS / LVTTTL interface levels. |
| 10, 13, 18 | V _{CC} | Power | | Positive supply pins. |
| 11, 12 | nQB1, QB1 | Output | | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQB0, QB0 | Output | | Differential output pair. LVPECL interface levels. |
| 16, 17 | nQA1, QA1 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQA0, QA0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

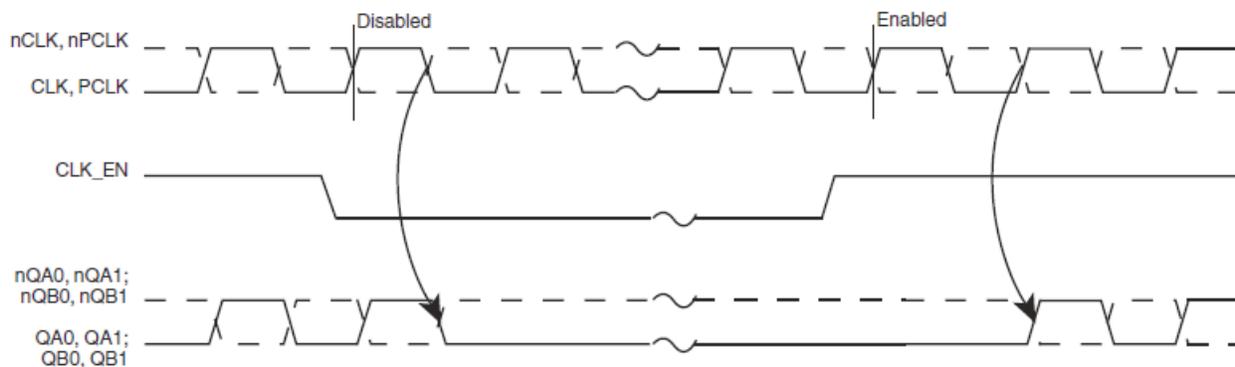
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

TABLE 3A. CONTROL INPUT FUNCTION TABLE

| Inputs | | | | Outputs | | | |
|--------|--------|---------|-----------------|---------------|----------------|---------------|----------------|
| MR | CLK_EN | CLK_SEL | Selected Source | QA0, QA1 | nQA0, nQA1 | QB0, QB1 | nQB0, nQB1 |
| 1 | X | X | X | LOW | HIGH | LOW | HIGH |
| 0 | 0 | 0 | CLK, nCLK | Disabled; LOW | Disabled; HIGH | Disabled; LOW | Disabled; HIGH |
| 0 | 0 | 1 | PCLK, nPCLK | Disabled; LOW | Disabled; HIGH | Disabled; LOW | Disabled; HIGH |
| 0 | 1 | 0 | CLK, nCLK | Enabled | Enabled | Enabled | Enabled |
| 0 | 1 | 1 | PCLK, nPCLK | Enabled | Enabled | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.


FIGURE 1 - CLK_EN TIMING DIAGRAM
TABLE 3B. CLOCK INPUT FUNCTION TABLE

| Inputs | | Outputs | | | | Input to Output Mode | Polarity |
|----------------|----------------|-----------------|------------------|-----------------|------------------|------------------------------|---------------|
| CLK or PCLK | nCLK or nPCLK | QA _x | nQA _x | QB _x | nQB _x | | |
| 0 | 0 | LOW | HIGH | LOW | HIGH | Differential to Differential | Non Inverting |
| 1 | 1 | HIGH | LOW | HIGH | LOW | Differential to Differential | Non Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | LOW | HIGH | Single Ended to Differential | Non Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | HIGH | LOW | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | HIGH | LOW | Single Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | LOW | HIGH | Single Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 73.2°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | | | | 55 | mA |

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK_EN | $V_{IN} = V_{CC} = 3.465V$ | | 5 | μA |
| | | CLK_SEL, MR | $V_{IN} = V_{CC} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | CLK_EN | $V_{IN} = 0V, V_{CC} = 3.465V$ | -150 | | μA |
| | | CLK_SEL, MR | $V_{IN} = 0V, V_{CC} = 3.465V$ | -5 | | μA |

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---|-----------------|--------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | nCLK | $V_{IN} = V_{CC} = 3.465V$ | | 5 | μA |
| | | CLK | $V_{IN} = V_{CC} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | nCLK | $V_{IN} = 0V, V_{CC} = 3.465V$ | -150 | | μA |
| | | CLK | $V_{IN} = 0V, V_{CC} = 3.465V$ | -5 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{CC} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|--------------------------------------|--------------------------------|----------------|---------|----------------|---------|
| I_{IH} | Input High Current | $V_{IN} = V_{CC} = 3.465V$ | | | 150 | μA |
| | | $V_{IN} = V_{CC} = 3.465V$ | | | 5 | μA |
| I_{IL} | Input Low Current | $V_{IN} = 0V, V_{CC} = 3.465V$ | -5 | | | μA |
| | | $V_{IN} = 0V, V_{CC} = 3.465V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.3 | | 1 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE} + 1.5$ | | V_{CC} | V |
| V_{OH} | Output High Voltage; NOTE 3 | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 3 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{CC} + 0.3V$.

NOTE 3: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|-----------|------------------------------|--------------------|-----------------|---------|---------|-------|----|
| f_{MAX} | Output Frequency | | | | 650 | MHz | |
| t_{PD} | Propagation Delay; NOTE 1 | CLK, nCLK | $f \leq 650MHz$ | 1.2 | | 1.8 | ns |
| | | PCLK, nPCLK | $f \leq 650MHz$ | 1.1 | | 1.7 | ns |
| tsk(o) | Output Skew; NOTE 2, 4 | | | | 75 | ps | |
| tsk(b) | Bank Skew; NOTE 4 | Bank A | | | 30 | ps | |
| | | Bank B | | | 45 | ps | |
| tsk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 300 | ps | |
| t_R | Output Rise Time | 20% to 80% @ 50MHz | 300 | | 700 | ps | |
| t_F | Output Fall Time | 20% to 80% @ 50MHz | 300 | | 700 | ps | |
| odc | Output Duty Cycle | | 47 | 50 | 53 | % | |

All parameters measured at 500MHz unless noted otherwise.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

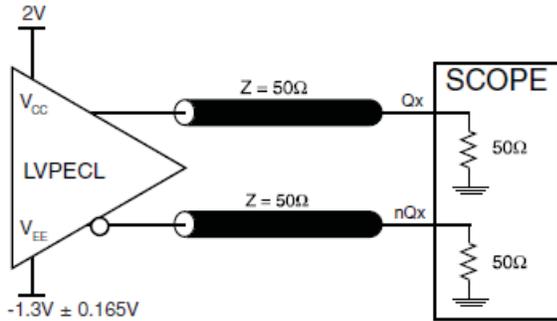
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

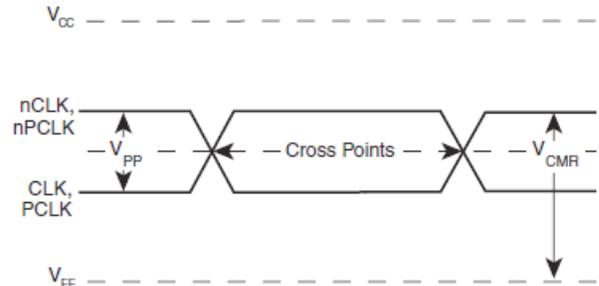
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

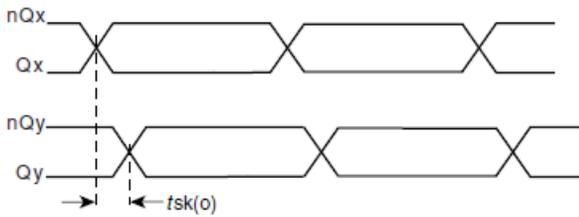
PARAMETER MEASUREMENT INFORMATION



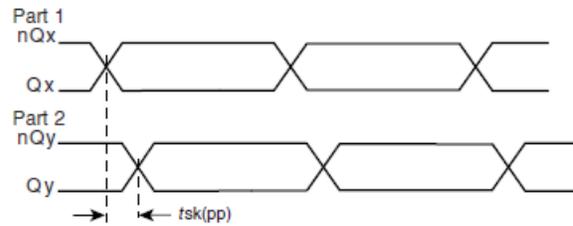
3.3V OUTPUT LOAD AC TEST CIRCUIT



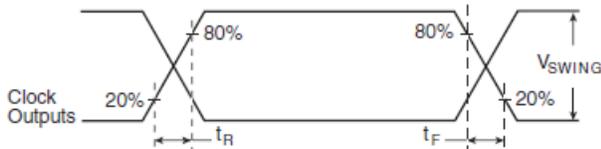
DIFFERENTIAL INPUT LEVEL



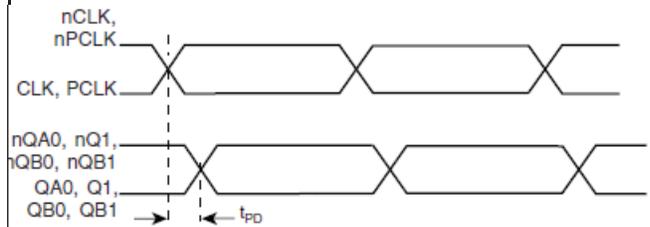
OUTPUT SKEW



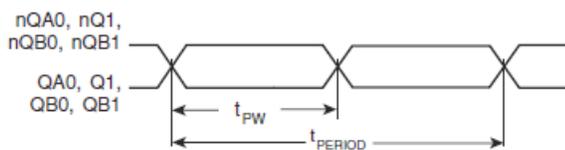
PART-TO-PART SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

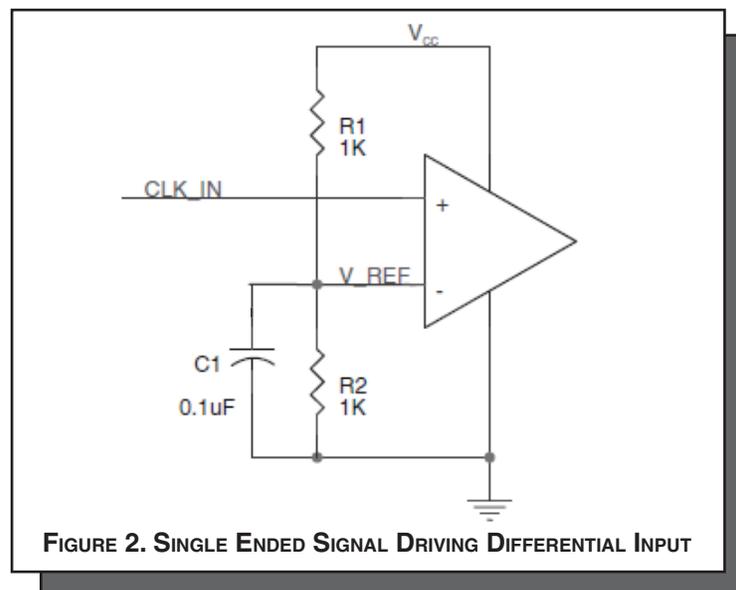
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} \approx V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from PCLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50 Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

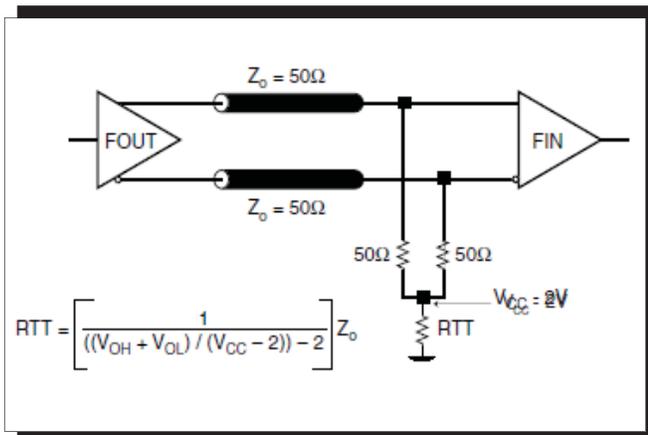


FIGURE 3A. LVPECL OUTPUT TERMINATION

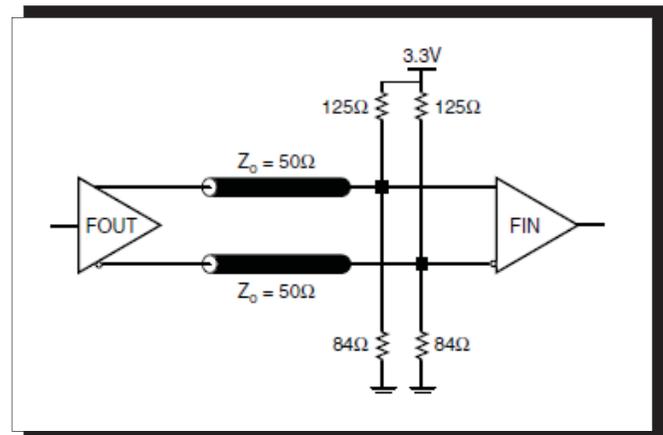


FIGURE 3B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8737I-11. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8737I-11 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{CC_MAX} = 3.465V * 55mA = 190.6mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 30mW = 120mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $190.6mW + 120mW = 310.6mW$

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.311W * 66.6^\circ C/W = 105.7^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 4*.

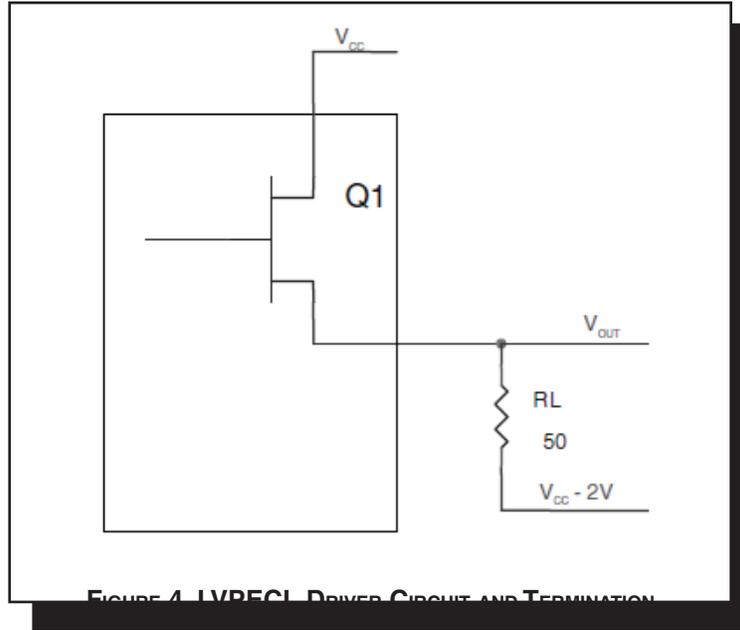


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 20 LEAD TSSOP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 8737I-11 is: 510

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

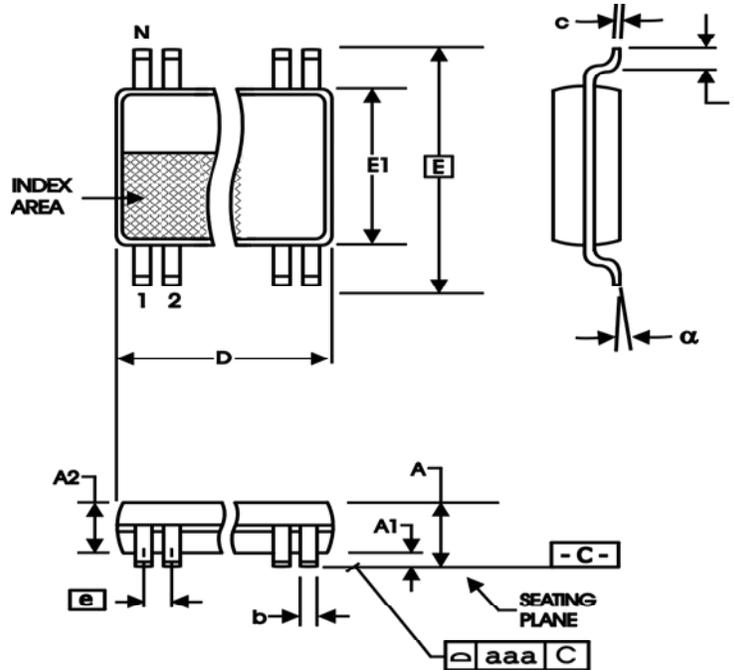


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 8737AGI-11LF | ICS8737AI11L | 20 lead "Lead-Free" TSSOP | Tube | -40°C to 85°C |
| 8737AGI-11LFT | ICS8737AI11L | 20 lead "Lead-Free" TSSOP | tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|------------------------|----------|-------------------|--|---------|
| Rev | Table | Page | Description of Change | Date |
| A | | 8 | Added Termination for LVPECL Outputs section. | 6/3/02 |
| A | 1 | 2 6 7 | Pin Description Table - revised MR description. 3.3V Output Load Test Circuit Diagram, revised VEE equation from “-1.3V ± 0.135V” to “-1.3V ± 0.165V”. Revised Output Rise/Fall Time Diagram. | 8/19/02 |
| B | T2 T9 | 1 2 8 13 | Features Section added Lead-Free bullet. Pin Characteristicst Table - changed C _{IN} from 4pF max. to 4pF typical. Added Recommendations for Unused Input and Output Pins. Ordering Information Table - added Lead-Free Part/Order Number, Marking and note. Updated format throughout the datasheet. | 1/12/06 |
| C | T4D | 5 9 - 10 | LVPECL DC Characteristics Table -corrected V _{OH} max. from V _{CC} - 1.0V to V _{CC} - 0.9V; and V _{SWING} max. from 0.9V to 1.0V. Power Considerations - corrected power dissipation to reflect V _{OH} max in Table 4D. | 4/13/07 |
| C | T9 | 13 15 | Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page. | 8/4/10 |
| C | T9 | 13 | Ordering Information - removed leaded devices. Updated data sheet format. | 7/16/15 |

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