64-Lane 16-Port PCIe® Gen3 System Interconnect Switch

89HPES64H16G3
Data Sheet

Device Overview

The 89HPES64H16G3 is a 64-lane, 16-port system interconnect switch optimized for PCI Express® Gen3 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

- **High Performance Non-Blocking Switch Architecture**
  - 64-lane 16-port PCIe switch
    - *Eight x8 switch ports each of which can bifurcate to two x4 ports (total of sixteen x4 ports)*
  - Integrated SerDes supports 8.0 GT/s Gen3, 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to 128 GBps (1024 Gbps) of switching capacity
  - Supports 128 Bytes to 2 KB maximum payload size
  - Low latency cut-through architecture
  - Supports one virtual channel and eight traffic classes
- **Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - Implements the following optional PCI Express features
    - *Advanced Error Reporting (AER) on all ports*
    - *End-to-End CRC (ECRC)*
    - *Access Control Services (ACS)*
    - *Power Budgeting Enhanced Capability*
    - *Device Serial Number Enhanced Capability*
    - *Sub-System ID and Sub-System Vendor ID Capability*
    - *Internal Error Reporting ECN*
    - *Atomic operations ECN*
    - *TLP processing hints ECN*
    - *Latency Tolerance Reporting (LTR) ECN*
    - *Optimized Buffer Flush/Fill (OBFF) ECN*
    - *ARI ECN*
    - *VGA and ISA enable*
    - *L0s and L1 ASPM*
- **Port Configurability**
  - x4 and x8 ports
    - *Ability to merge adjacent x4 ports to create a x8 port*
  - Automatic per port link width negotiation (x8 → x4 → x2 → x1)
  - Crosslink support
  - Automatic lane reversal
  - Autonomous and software managed link width and speed control
  - Per lane SerDes configuration
    - *Full back channel equalization support*
    - *Rx, 5 tap DFE*
    - *Rx, single tap has pulse shaping*
    - *Rx CTLE compensates for up to 25db @ 4G/s*
    - *Tx De-emphasis*
    - *Tx pre-shoot*
    - *Programmable Drive strength*
    - *Tx Margin*
- **Switch Partitioning**
  - IDT proprietary feature that creates logically independent switches in the device
  - Supports up to 16 fully independent switch partitions
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
    - *Dynamic port reconfiguration — downstream, upstream*
    - *Dynamic migration of ports between partitions*
    - *Movable upstream port within and between switch partitions*
- **Initialization / Configuration**
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
  - Common switch configurations are supported with pin strapping (no external components)
  - Supports in-system Serial EEPROM initialization/programming
- **Quality of Service (QoS)**
  - Port arbitration
    - *Round robin*
  - Request metering
    - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
  - High performance switch core architecture
    - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*
- **Clocking**
  - Supports 100 MHz reference clock frequency
  - Flexible port clocking modes
    - *Common clock*
    - *Non-common clock*
    - *Local port clock with SSC and port reference clock input*

- **Hot-Plug and Hot Swap**
  - Hot-plug controller on all ports
    - *Hot-plug supported on all downstream switch ports*
  - All ports support hot-plug using low-cost external SMBus I/O expanders
  - Direct package pin support for hot-plug on 5 ports
  - Configurable presence detect supports card and cable applications
  - GPE output pin for hot-plug event notification
    - *Enables SCI/SMI generation for legacy operating system support*
  - Hot-swap capable I/O
- **Power Management**
  - Supports D0, D3hot and D3 power management states
  - Active State Power Management (ASPM)
    - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
    - *Configurable L0s and L1 entry timers allow performance/ power-savings tuning*
  - Supports PCI Express Power Budgeting Capability
  - SerDes power savings
    - *Supports low swing / half-swing SerDes operation*
    - *SerDes optionally turned-off in D3hot*
    - *SerDes associated with unused ports are turned-off*
    - *SerDes associated with unused lanes are placed in a low power state*
- **54 General Purpose I/O**
- **Reliability, Availability and Serviceability (RAS)**
  - ECRC support
  - AER on all ports
  - SECDED ECC protection on all internal RAMs
  - End-to-end data path parity protection
  - Checksum Serial EEPROM content protected
  - Autonomous link reliability (preserves system operation in the presence of faulty links)
  - Ability to generate an interrupt (INTx or MSI) on link up/down transitions
- **Test and Debug**
  - On-die scope
  - On-chip link activity and status outputs available for several ports including the upstream ports
  - Per port link activity and status outputs available using external SMBus I/O expander for all remaining ports
  - SerDes test modes
  - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
- **Power Supplies**
  - Requires three power supply voltages (1.0V, 1.8V, and 3.3V)
  - No power sequencing requirements
- **Packaged in a 35mm x 35mm 1156-ball Flip Chip BGA with 1mm ball spacing**

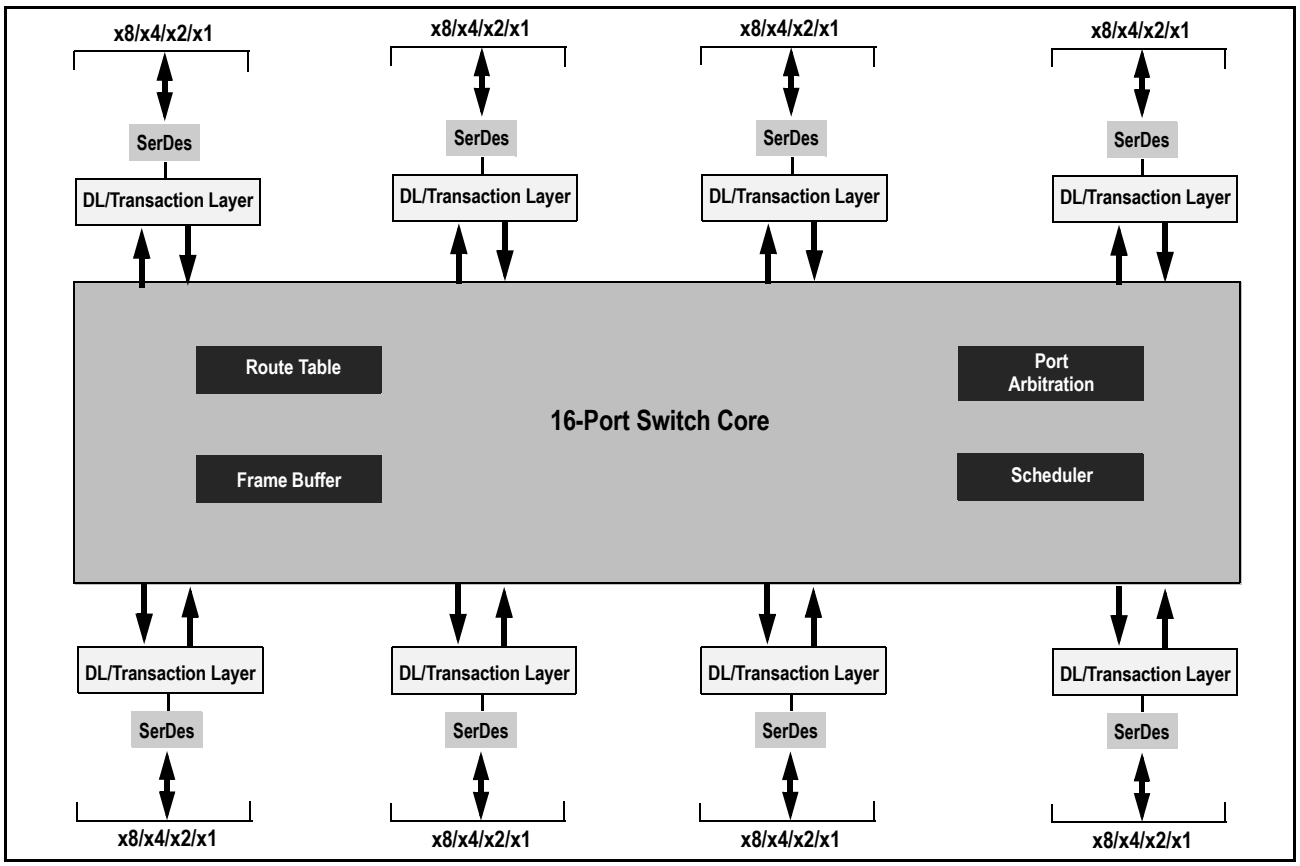
Product Description

Utilizing standard PCI Express interconnect, the PES64H16G3 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 128 GBps (1024 Gbps) of aggregated, full-duplex switching capacity through 64 integrated serial lanes, using proven and robust IDT technology. Each lane provides 8 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 3.0.

The PES64H16G3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 3.0. The PES64H16G3 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

The PES64H16G3 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES64H16G3 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES64H16G3 configuration.

Block Diagram



64 PCI Express Lanes
Up to 8 x8 ports or 16 x4 Ports

Figure 1 Internal Block Diagram

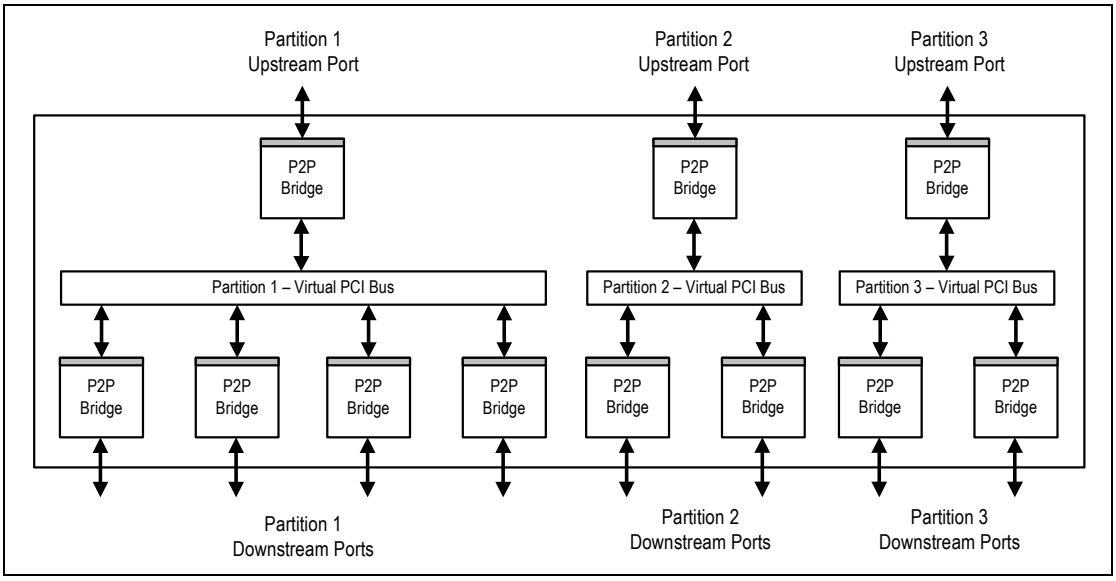


Figure 2 Example of Usage of Switch Partitioning

SMBus Interface

The PES64H16G3 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES64H16G3, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES64H16G3 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 3, the master and slave SMBuses may only be used in a split configuration.

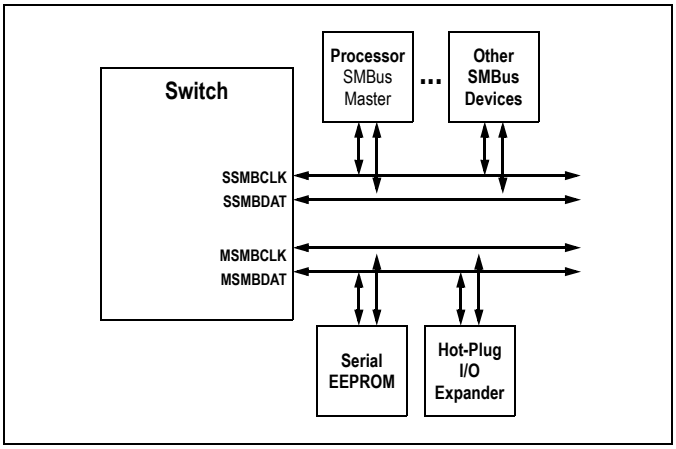


Figure 3 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES64H16G3 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES64H16G3 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES64H16G3 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES64H16G3. In response to an I/O expander interrupt, the PES64H16G3 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES64H16G3 provides 54 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES64H16G3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 3)

Signal	Type	Name/Description
PE01TP[3:0] PE01TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE05RP[3:0] PE05RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.
PE05TP[3:0] PE05TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RP[3:0] PE06RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE06TP[3:0] PE06TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE07RP[3:0] PE07RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE07TP[3:0] PE07TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PE08RP[3:0] PE08RN[3:0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pairs for port 8.
PE08TP[3:0] PE08TN[3:0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pairs for port 8.
PE09RP[3:0] PE09RN[3:0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pairs for port 9. When port 8 is merged with port 9, these signals become port 8 receive pairs for lanes 4 through 7.
PE09TP[3:0] PE09TN[3:0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pairs for port 9. When port 8 is merged with port 9, these signals become port 8 transmit pairs for lanes 4 through 7.
PE10RP[3:0] PE10RN[3:0]	I	**PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pairs for port 10.

Table 2 PCI Express Interface Pins (Part 2 of 3)

Signal	Type	Name/Description
PE10TP[3:0] PE10TN[3:0]	O	**PCI Express Port 10 Serial Data Transmit.** Differential PCI Express transmit pairs for port 10.
PE11RP[3:0] PE11RN[3:0]	I	**PCI Express Port 11 Serial Data Receive.** Differential PCI Express receive pairs for port 11. When port 10 is merged with port 11, these signals become port 10 receive pairs for lanes 4 through 7.
PE11TP[3:0] PE11TN[3:0]	O	**PCI Express Port 11 Serial Data Transmit.** Differential PCI Express transmit pairs for port 11. When port 10 is merged with port 11, these signals become port 10 transmit pairs for lanes 4 through 7.
PE12RP[3:0] PE12RN[3:0]	I	**PCI Express Port 12 Serial Data Receive.** Differential PCI Express receive pairs for port 12.
PE12TP[3:0] PE12TN[3:0]	O	**PCI Express Port 12 Serial Data Transmit.** Differential PCI Express transmit pairs for port 12.
PE13RP[3:0] PE13RN[3:0]	I	**PCI Express Port 13 Serial Data Receive.** Differential PCI Express receive pairs for port 13. When port 12 is merged with port 13, these signals become port 12 receive pairs for lanes 4 through 7.
PE13TP[3:0] PE13TN[3:0]	O	**PCI Express Port 13 Serial Data Transmit.** Differential PCI Express transmit pairs for port 13. When port 12 is merged with port 13, these signals become port 12 transmit pairs for lanes 4 through 7.
PE14RP[3:0] PE14RN[3:0]	I	**PCI Express Port 14 Serial Data Receive.** Differential PCI Express receive pairs for port 14.
PE14TP[3:0] PE14TN[3:0]	O	**PCI Express Port 14 Serial Data Transmit.** Differential PCI Express transmit pairs for port 14.
PE15RP[3:0] PE15RN[3:0]	I	**PCI Express Port 15 Serial Data Receive.** Differential PCI Express receive pairs for port 15. When port 14 is merged with port 15, these signals become port 14 receive pairs for lanes 4 through 7.
PE15TP[3:0] PE15TN[3:0]	O	**PCI Express Port 15 Serial Data Transmit.** Differential PCI Express transmit pairs for port 15. When port 14 is merged with port 15, these signals become port 14 transmit pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 3 of 3)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	**Global Reference Clock.** Differential reference clock input pairs. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is 100MHz. Note: Both pairs of the Global Reference Clocks must be connected to and derived from the same clock source. Refer to the Overview section of Chapter 3 in the PES64H16G3 User Manual for additional details.
P[15:0]CLKN P[15:0]CLKP	I	**Port x Reference Clock**. Differential reference clock pair associated with ports 0 through 15.[1]

Table 3 Reference Clock Pins

1. Unused port clock pins should be connected to Vss on the board.

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 4 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.

Table 5 General Purpose I/O Pins (Part 1 of 8)

Signal	Type	Name/Description
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Attention Push Button Input.
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Presence Detect Input.
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Fault Input.
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Power Good Input.
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0MRLN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 0 Manually Operated Retention Latch Input.
GPIO[14]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0AIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Attention Indicator Output.
GPIO[15]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PIN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Indicator Output.

Table 5 General Purpose I/O Pins (Part 2 of 8)

Signal	Type	Name/Description
GPIO[16]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0PEP Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Power Enable Output.
GPIO[17]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP0RSTN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 0 Reset Output.
GPIO[18]	I/O	General Purpose I/O. Alternate function pin name: HP1APN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Attention Push Button Input.
GPIO[19]	I/O	General Purpose I/O. Alternate function pin name: HP1PDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Presence Detect Input.
GPIO[20]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PFN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Fault Input.
GPIO[21]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP1PWRGDN Alternate function pin type: Input Alternate function: Hot Plug Signal Group 1 Power Enable Input.
GPIO[22]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 1 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P1LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Up Status Output.
GPIO[23]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Attention Indicator Output. 2nd Alternate function pin name: P1ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 1 Link Active Status Output.
GPIO[24]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Indicator Output. 2nd Alternate function pin name: P2LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 3 of 8)

Signal	Type	Name/Description
GPIO[25]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Power Enable Output. 2nd Alternate function pin name: P2ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 2 Link Active Status Output.
GPIO[26]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP1RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 1 Reset Output. 2nd Alternate function pin name: P3LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Up Status Output.
GPIO[27]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Attention Push Button Input. 2nd Alternate function pin name: P3ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 3 Link Active Status Output.
GPIO[28]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Presence Detect Input. 2nd Alternate function pin name: P4LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Up Status Output.
GPIO[29]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Fault Input. 2nd Alternate function pin name: P4ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Active Status Output.
GPIO[30]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Power Good Input. 2nd Alternate function pin name: P5LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 4 of 8)

Signal	Type	Name/Description
GPIO[31]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 2 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P5ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 5 Link Active Status Output.
GPIO[32]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Attention Indicator Output. 2nd Alternate function pin name: P6LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 6 Link Up Status Output.
GPIO[33]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Power Indicator Output. 2nd Alternate function pin name: P6ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 6 Link Active Status Output.
GPIO[34]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Power Enable Output. 2nd Alternate function pin name: P7LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 7 Link Up Status Output.
GPIO[35]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Reset Output. 2nd Alternate function pin name: P7ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 7 Link Active Status Output.
GPIO[36]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Attention Push Button Input. 2nd Alternate function pin name: P8LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 8 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 5 of 8)

Signal	Type	Name/Description
GPIO[37]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Presence Detect Input. 2nd Alternate function pin name: P8ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 8 Link Active Status Output.
GPIO[38]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Power Fault Input. 2nd Alternate function pin name: P9LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 9 Link Up Status Output.
GPIO[39]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Power Good Input. 2nd Alternate function pin name: P9ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 9 Link Active Status Output.
GPIO[40]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 3 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P10LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 10 Link Up Status Output.
GPIO[41]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Attention Indicator Output. 2nd Alternate function pin name: P10ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 10 Link Active Status Output.
GPIO[42]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Power Indicator Output. 2nd Alternate function pin name: P11LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 11 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 6 of 8)

Signal	Type	Name/Description
GPIO[43]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Power Enable Output. 2nd Alternate function pin name: P11ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 11 Link Active Status Output.
GPIO[44]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP3RSTN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 3 Reset Output. 2nd Alternate function pin name: P12LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 12 Link Up Status Output.
GPIO[45]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4APN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Attention Push Button Input. 2nd Alternate function pin name: P12ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 12 Link Active Status Output.
GPIO[46]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Presence Detect Input. 2nd Alternate function pin name: P13LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 13 Link Up Status Output.
GPIO[47]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PFN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Power Fault Input. 2nd Alternate function pin name: P13ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 13 Link Active Status Output.
GPIO[48]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PWRGDN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Power Good Input. 2nd Alternate function pin name: P14LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 14 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 7 of 8)

Signal	Type	Name/Description
GPIO[49]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4MRLN 1st Alternate function pin type: Input 1st Alternate function: Hot Plug Signal Group 4 Manually Operated Retention Latch Input. 2nd Alternate function pin name: P14ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 14 Link Active Status Output.
GPIO[50]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 4 Attention Indicator Output. 2nd Alternate function pin name: P15LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 15 Link Up Status Output.
GPIO[51]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP4PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 4 Power Indicator Output. 2nd Alternate function pin name: P15ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 15 Link Active Status Output.
GPIO[52]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP4PEP Alternate function pin type: Output Alternate function: Hot Plug Signal Group 4 Power Enable Output.
GPIO[53]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: HP4RSTN Alternate function pin type: Output Alternate function: Hot Plug Signal Group 4 Reset Output.

Table 5 General Purpose I/O Pins (Part 8 of 8)

Signal	Type	Name/Description
CLKMODE[2:0]		**Clock Mode.** These signals determine the port clocking mode used by ports of the device.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.

Table 6 System Pins (Part 1 of 3)

Signal	Type	Name/Description
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
P89MERGEN	I	**Port 8 and 9 Merge.** P89MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 8 is merged with port 9 to form a single x8 port. The Serdes lanes associated with port 9 become lanes 4 through 7 of port 8. When this pin is high, port 8 and port 9 are not merged, and each operates as a single x4 port.
P1011MERGEN	I	**Port 10 and 11 Merge.** P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 10 is merged with port 11 to form a single x8 port. The Serdes lanes associated with port 11 become lanes 4 through 7 of port 10. When this pin is high, port 10 and port 11 are not merged, and each operates as a single x4 port.
P1213MERGEN	I	**Port 12 and 13 Merge.** P1213MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 12 is merged with port 13 to form a single x8 port. The Serdes lanes associated with port 13 become lanes 4 through 7 of port 12. When this pin is high, port 12 and port 13 are not merged, and each operates as a single x4 port.
P1415MERGEN	I	**Port 14 and 15 Merge.** P1415MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 14 is merged with port 15 to form a single x8 port. The Serdes lanes associated with port 15 become lanes 4 through 7 of port 14. When this pin is high, port 14 and port 15 are not merged, and each operates as a single x4 port.

Table 6 System Pins (Part 2 of 3)

Signal	Type	Name/Description
PERSTN	I	**Global Reset.** Assertion of this signal resets all logic inside PES64H16G3.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES64H16G3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES64H16G3 switch operating mode. **Note:** These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition with port 0 selected as the upstream port 0x1 - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (i.e., port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (i.e., port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (i.e., port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (i.e., port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved

Table 6 System Pins (Part 3 of 3)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 7 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic (1.0V).
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply (3.3V).
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (1.8V).
V_{SS}	I	**Ground.**

Table 8 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any of these pins left floating can cause a slight increase in power consumption. Finally, unused Serdes (Rx and Tx) pins should be left floating.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe differential[2]	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				

Table 9 Pin Characteristics (Part 1 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (Cont.)	PE05TP[3:0]	O	PCIe differential	Serial Link		
	PE06RN[3:0]	I				
	PE06RP[3:0]	I				
	PE06TN[3:0]	O				
	PE06TP[3:0]	O				
	PE07RN[3:0]	I				
	PE07RP[3:0]	I				
	PE07TN[3:0]	O				
	PE07TP[3:0]	O				
	PE08RN[3:0]	I				
	PE08RP[3:0]	I				
	PE08TN[3:0]	O				
	PE08TP[3:0]	O				
	PE09RN[3:0]	I				
	PE09RP[3:0]	I				
	PE09TN[3:0]	O				
	PE09TP[3:0]	O				
	PE10RN[3:0]	I				
	PE10RP[3:0]	I				
	PE10TN[3:0]	O				
	PE10TP[3:0]	O				
	PE11RN[3:0]	I				
	PE11RP[3:0]	I				
	PE11TN[3:0]	O				
	PE11TP[3:0]	O				
	PE12RN[3:0]	I				
	PE12RP[3:0]	I				
	PE12TN[3:0]	O				
	PE12TP[3:0]	O				
	PE13RN[3:0]	I				
	PE13RP[3:0]	I				
	PE13TN[3:0]	O				
	PE13TP[3:0]	O				
	PE14RN[3:0]	I				
	PE14RP[3:0]	I				
	PE14TN[3:0]	O				
	PE14TP[3:0]	O				
	PE15RN[3:0]	I				
	PE15RP[3:0]	I				

Table 9 Pin Characteristics (Part 2 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (Cont.)	PE15TN[3:0]	O	PCIe differential	Serial Link		
	PE15TP[3:0]	O				
	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 16
	GCLKP[1:0]	I				
	P[15:0]CLKN	I				
	P[15:0]CLKP	I				
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-down	
	MSMBCLK	I/O		STI[3]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[53:0]	I/O	LVTTL	STI, High Drive	pull-up	
System Pins	CLKMODE[1:0]	I	LVTTL	Input	pull-up	
	CLKMODE[2]	I			pull-down	
	MSMBSMODE	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	P89MERGEN	I			pull-down	
	P1011MERGEN	I			pull-down	
	P1213MERGEN	I			pull-down	
	P1415MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 9 Pin Characteristics (Part 3 of 3)

1. Internal resistor values for pull-up and pull-down are in the range 27K – 34KΩ with 30KΩ being typical.

2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

3. Schmitt Trigger Input (STI).

Logic Diagram — PES64H16G3

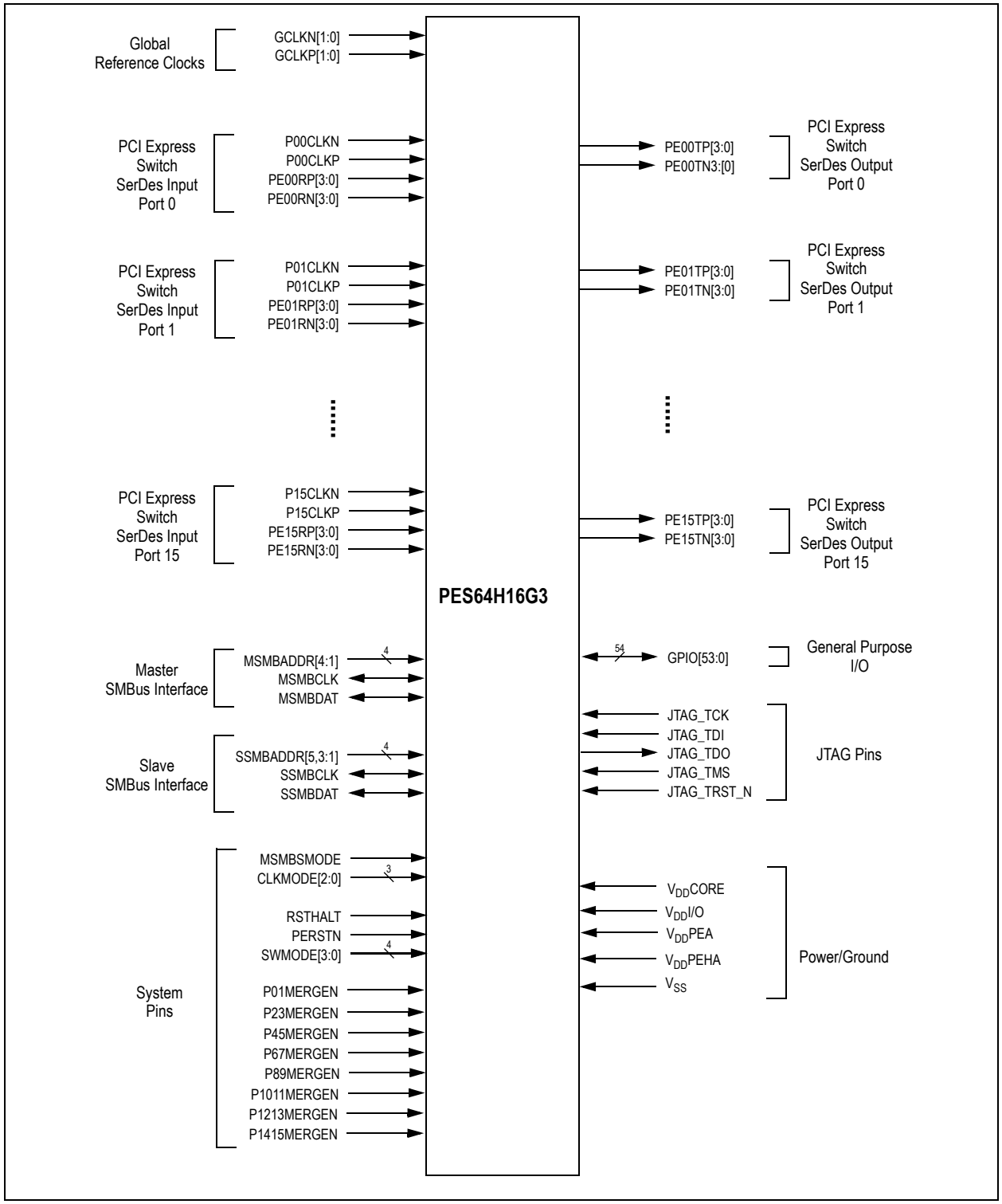


Figure 4 PES64H16G3 Logic Diagram

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 10 PES64H16G3 Operating Temperatures

Thermal Considerations

This section describes thermal considerations for the PES64H16G3 (35mm^2 FCBGA1156 package). The data in Table 11 below contains information that is relevant to the thermal performance of the PES64H16G3 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
		85	°C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	10.3	°C/W	Zero air flow
		6.7	°C/W	1 m/S air flow
		5.3	°C/W	2 m/S air flow
		4.7	°C/W	3 m/S air flow
		4.3	°C/W	4 m/S air flow
		4.1	°C/W	5 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.2	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.2	°C/W	
P	Power Dissipation of the Device	20.42	Watts	Maximum

Table 11 Thermal Specifications for PES64H16G3, 35x35 mm FCBGA1156 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 11. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 11), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range V_{DD}CORE	–0.5 to 1.35	V
Supply voltage range V_{DD}PEA	–0.5 to 1.35	V
Supply voltage range V_{DD}PEHA	–0.5 to 2.5	V
Supply voltage range V_{DD}I/O	–0.5 to 4.0	V
Voltage range Differential I/O	–0.5 to V_{DD}PEHA +0.5	V
3.3V Control IO	–0.5 to V_{DD}I/O + 0.5	V
ESD requirements: Electrostatic discharge Human body model	±2000	V
ESD requirements: Charged-Device Model (CDM)	±500	V
ESD requirements: Machine model	±200	V
Storage ambient temperature	-55 to 150	°C

Table 12 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Description	Min	Typical	Max	Unit
Power-Supply Pin Requirements					
V_{DD}CORE	1.0V DC digital core supply voltage	0.95	1.0	1.1	V
V_{DD}PEA[1]	1.0V DC analog supply voltage	0.95	1.0	1.1	V
V_{DD}PEHA[2]	1.8V DC analog high supply voltage	1.71	1.8	1.98	V
V_{DD}I/O	3.3V DC supply voltage for SMBus/JTAG/IO	3.0	3.3	3.6	V

Table 13 Recommended Operating Conditions

1. V_{DD}PEA should have no more than 25m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.8V nominal DC value.

Power-Up/Power-Down Sequence

There are no power-up or power-down sequence requirements for the various operating supply voltages for this device. Therefore, power supplies can be ramped up and ramped down in any order.

Power Consumption

Table 14 below lists power consumption values under typical and maximum operating conditions.

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.8V	Max 1.98V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/8/8/8/8/8/8/8 (Full Swing)	mA	5750	8625	4315	4962	2256	2594	72	94		
	Watts	5.75	9.49	4.32	5.46	4.06	5.14	0.24	0.34	14.36	20.42

Table 14 PES64H16G3 Power Consumption

Note 1: The above power consumption assumes that all ports are functioning at Gen3 (8.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DD}PEA and V_{DD}PEHA. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above two power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

Note 2: Using a port in Gen2 mode (5.0GT/S) results in approximately TBD % power savings for each power rail: V_{DD}PEA and V_{DD}PEHA.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately TBD % power savings for each power rail: V_{DD}PEA and V_{DD}PEHA.

Note 4: Tc (max case temp): 100°C.

DC Specifications

Parameter	Description	Min	Typical	Max	Unit
3.3V I/O Requirements					
V_{IL_VDDIO}	Digital Input Signal Voltage Low Level	-0.3	—	0.8	V
V_{IH_VDDIO}	Digital Input Signal Voltage High Level	2.1	—	V_{DD}I/O + 0.3	V
$V_{OL\_VDDIO\_HP}$	Digital Output Signal Voltage Low Level, High Power, IOL=4mA[1,2]	—	—	0.4	V
$V_{OL\_VDDIO\_LP}$	Digital Output Signal Voltage Low Level, Low Power, IOL=350uA	—	—	0.4	V
V_{HYS_VDDIO}	Hysteresis of Schmitt Trigger Input	0.1	—	—	V

Table 15 DC Specification

1. VOL low power and high power state is controlled via an external pull-up design in the end-application.
2. Applies to JTAG input pins.

Clock Specifications

The PES64H16G3 includes differential input clock buffers which are compatible with HCSL-type drivers and are designed to work with IDT standard 100 MHz PCIe reference clock generator devices (for information on IDT's Clock/Timing products, contact www.idt.com/go/clockhelp).

The standard 100 MHz PCIe input reference clock electrical specifications are shown in Table 16.

Parameter	Description	100 MHz Input		Unit
		Min	Max	
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150		mV
V_{IL}	Differential Input Low Voltage		-150	mV
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV
$V_{CROSSDELTA}$	Variation of Vcross over all rising clock edges		+140	mV
V_{RS}	Ring-back voltage margin	-100	+100	mV
V_{STABLE}	Time before V_{RS} is allowed	500		ps
$V_{PERIODAVG}$	Average Clock Period Accuracy	-300	+2800	ppm
$V_{PERIODABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns
$T_{CCJITTER}$	Cycle to Cycle jitter		150	ps
V_{MAX}	Absolute Max input voltage		+1.15	V
V_{MIN}	Absolute Min input voltage		-0.3	V
Duty Cycle	Duty Cycle	40	60	%
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%
Z_{C-DC}	Clock source DC impedance	40	60	Ω

Table 16 Input Reference Clock Buffer Electrical Specifications

AC Electrical Specifications

Note: For the tables in this section, please refer to PCI Express Base Specification 3.0 for setup and measurement conditions.

PCI Express Transmitter Specifications

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
BW_{TX-PLL}	Tx PLL BW for 2.5 GT/s	1.5	22	—	—	—	—	MHz	
$BW_{TX-PKG-PLL1}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL1}$ specified below.	—	—	8	16	2	4	MHz	
$BW_{TX-PKG-PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL2}$ specified below.	—	—	5	16	2	5	MHz	
$PKG_{TX-PLL1}$	Tx PLL peaking	—	—	—	3.0	—	2.0	dB	
$PKG_{TX-PLL2}$	Tx PLL peaking	—	—	—	1.0	—	1.0	dB	

Table 17 PLL Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0. Note that the values in this table apply to both Tx and Rx since both use the same PLL.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8	1.2	0.8	1.2	See $V_{TX-FS-NO-EQ}$ in Table 21		VPP	Defined by register settings in compliance with PCI Express Specification.
			1.8		>1.8		>1.8		Absolute maximum swing value across all possible register settings.
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	0.4	1.2	0.4	1.2	See $V_{TX-RS-NO-EQ}$ in Table 21		VPP	Defined by register settings in compliance with PCI Express Specification.
			1.8		1.8		1.8		Absolute maximum swing value across all possible register settings.
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio	2.5	4.5	2.5	4.5	See Table 21		dB	Programmable over a wide range with included registers.
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level	5.0	7.0	5.0	7.0	See Table 21		dB	Programmable over a wide range with included registers.
$V_{TX-CM-AC-PP}$	Tx AC peakpeak common mode voltage (5.0 GT/s)	—	—	—	150	—	150	mVPP	

Table 18 Transmitter Voltage and Current Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{TX-CM-AC-P}$	Tx AC peak common mode voltage (2.5 GT/s)	20	20	—	—	—	—	mV	
$I_{TX-SHORT}$	Transmitter short-circuit current limit	—	90	—	90	—	90	mA	
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0	3.6	0	3.6	0	3.6	V	
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0	100	0	100	0	100	mV	
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	25	0	25	0	25	mV	
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0	20	0	20	0	20	mV	
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	—	—	0	5	0	5	mV	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	600	—	600	—	600	mV	

Table 18 Transmitter Voltage and Current Specifications (Part 2 of 2)

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
UI	Unit Interval	399.88	400.12	199.94	200.06	124.96	125.03	ps	
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—	—	0.9	—	See Table 21		UI	
T_{TX-EYE}	Transmitter Eye including all jitter sources	0.75	—	0.75	—	See Table 21		UI	
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and max deviation from the median	—	0.125	—	—	—	—	UI	
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	See Table 21		UI	
$T_{TX-LF-RMS}$	Tx RMS jitter < 1.5 MHz	—	—	—	3.0	See Table 21		ps RMS	
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	—	—	—	0.1	—	—	UI	
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	20	—	20	—	20	—	ns	

Table 19 Transmitter Timing and Jitter Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an EIOS	—	8	—	8	—	8	ns	
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving Electrical Idle	—	8	—	8	—	8	ns	
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	500 ps + 2 UI	—	500 ps + 4 UI	—	500 ps + 6 UI	ps	

Table 19 Transmitter Timing and Jitter Specifications (Part 2 of 2)

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$T_{RES-ISI-5GBPS}$	Residual Deterministic ISI Jitter at output pins after a signal has passed through a 60-inch FR4 trace at 5Gbps	—	—	—	0.25	—		UI_{pkpk}	
$T_{RES-ISI-8GBPS}$	Residual Deterministic ISI Jitter at output pins after a signal has passed through a 40-inch FR4 trace at 8Gbps	—	—	—	—	—	0.25	UI_{pkpk}	
$RL_{TX-DIFF}$	Tx package plus Si differential return loss	10	—	10 for 0.05 - 1.25GHz	—	10 for 0.05 - 1.25GHz	—	dB	
				8 for >1.25 - 2.5GHz	—	8 for >1.25 - 2.5GHz	—		
						4 for 2.5 - 4GHz	—		
RL_{TX-CM}	Tx package plus Si common mode return loss	6	—	6 for 0.05 - 2.5GHz	—	6 for 0.05 - 2.5GHz	—	dB	
						3 for 2.5GHz - 4GHz	—		
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	80	120	—	120	—	120	Ω	
C_{TX}	AC Coupling Capacitor	75	265	75	265	176	265	nF	

Table 20 Miscellaneous Transmitter Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen3 8.0GT/s		Unit	Notes
		Min[1]	Max[1]		
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEq	800	1300	mVPP	Defined by register settings in compliance with PCI Express Specification. See $V_{TX-DIFF-PP}$ in Table 18 for absolute maximum swing value.
$V_{TX-RS-NO-EQ}$	Reduced swing Tx voltage with no TxEq	—	1300	mVPP	Defined by register settings in compliance with PCI Express Specification. See $V_{TX-DIFF-PP-LOW}$ in Table 18 for absolute maximum swing value.
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250	—	mVPP	Programmable over a wide range with included registers.
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232	—	mVPP	Programmable over a wide range with included registers.
$V_{TX-BOOST-FS}$	Tx boost ratio for full swing	8.0	—	dB	Programmable over a wide range with included registers.
$V_{TX-BOOST-RS}$	Tx boost ratio for reduced swing	2.5	—	dB	Programmable over a wide range with included registers.
T_{TX-UTJ}	Tx uncorrelated total jitter	—	31.25	ps PP @ 10^{-12}	
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	—	12	ps PP	
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	—	24	ps PP @ 10^{-12}	
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	—	10	ps PP	
T_{TX-DDJ}	Data dependent jitter	—	18	ps PP	
$EQ_{TX-COEFF-RES}$	Tx coefficient resolution	1/63	1/24	N/A	
$ps21_{TX}$	Pseudo package loss	-3.0	—	dB	
Preshoot_3.5dB	Preshoot (P7, P8, P9)	2.5	4.5	dB	
Preshoot_1.9dB	Preshoot (P5)	0.9	2.9	dB	
Preshoot_2.5dB	Preshoot (P6)	1.5	3.5	dB	
Deemphasis_3.5dB	Deemphasis (P1, P8)	2.5	4.5	dB	
Deemphasis_6dB	Deemphasis (P0, P7)	4.5	7.5	dB	
Deemphasis_2.5dB	Deemphasis (P3)	1.5	3.5	dB	
Deemphasis_4.4dB	Deemphasis (P2)	2.9	5.9	dB	

Table 21 Gen3-specific Transmitter Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen2 5.0 GT/s		Unit	Notes
		Min[1]	Max[1]		
UI	Unit interval without SSC	199.94	200.06	ps	
$T_{RX-HF-RMS}$	1.5 – 100 MHz RMS jitter	—	4.2	ps RMS	
$T_{RX-HF-DJ-DD}$	Max Dj impinging on Rx under tolerancing	—	88	ps	
$T_{RX-LF-RMS}$	10 kHz to 1.5 MHz RMS jitter	—	8.0	ps RMS	
$T_{RX-MIN-PULSE}$	Minimum single pulse applied at Rx	120	—	ps	
$V_{RX-MIN-MAXRATIO}$	Min/max pulse voltage ratio seen over an time interval of 2 UI	—	5		
V_{RX-EYE}	Receive eye voltage opening	100	—	mVPP diff	
$V_{RX-CM-CH-SRC}$	Common mode noise from Rx	—	300	mVPP	

Table 22 Gen 2 Tolerancing Limits for Data Clocked Rx Architecture

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

PCI Express Receiver Specifications

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{RX-DIFF-PP-DC}$	Differential Rx peak-peak voltage for data clocked Rx architecture	0.175	1.2	0.100	1.2	0.175	2.0	V	
		Closed eye	2.0	Closed eye	2.0	Closed eye	2.0		Extended specification of this device.
$V_{RX-MAX-MIN-RATIO}$	Min/Max pulse voltage on consecutive UI	—	—	—	5	—	—		
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	—	150	—	150	—	75 mV (EH <100 mVPP) 125 mV (EH ≥ 100 mVPP) See Table 4.22 in the PCIe Base Specification 3.0	mVP	

Table 23 Receiver Voltage and Current Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	175	65	175	65	175	mV	Programmable over a wide range with included registers

Table 23 Receiver Voltage and Current Specifications (Part 2 of 2)

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
UI	Unit Interval	399.88	400.12	199.94	200.06	124.96	125.03	ps	
T_{RX-EYE}	Receiver eye time opening	0.40	—	—	—	See Tables 4.22 and 4.23 in the PCIe Base Specification 3.0		UI	
$T_{RX-TJ-DC}$	Max Rx inherent timing error	—	—	—	0.34			UI	
$T_{RX-DJ-DD-DC}$	Max Rx inherent deterministic timing error	—	—	—	0.24			UI	
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Max time delta between median and deviation from median	—	0.3	—	—	—	—	UI	
$T_{RX-MIN-PULSE}$	Minimum width pulse at Rx	—	—	0.6	—	—	—	UI	
T_{RX-GND_FLOAT}	Rx termination ground float time	—	—	—	—	—	500	µs	
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	10	—	10	—	10	ms	
$L_{RX-SKEW}$	Lane to Lane input skew	—	20	—	8	—	6	ns	

Table 24 Receiver Timing and Jitter Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$RL_{RX-DIFF}$	Rx package plus Si differential return loss	10	—	10 for 0.05 - 1.25GHz	—	10 for 0.05 - 1.25GHz	—	dB	
				8 for >1.25 - 2.5GHz	—	8 for >1.25 - 2.5GHz	—		
						5 for 2.5GHz - 4GHz	—		
RL_{RX-CM}	Common mode Rx return loss	6	—	6 for 0.05 - 2.5GHz	—	6 for 0.05 - 2.5GHz	—	dB	
						5 for 2.5GHz - 4GHz	—		
Z_{RX-DC}	Receiver DC single ended impedance	40	60	40	60	—	—	Ω	
$Z_{RX-DIFF-DC}$	DC differential impedance	80	120	—	—	—	—	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	10 k or 20 k	—	10 k or 20 k	—	10 k or 20 k	—	Ω	
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input CM Input Impedance for V < 0 during Reset or power down	1.0 k	—	1.0 k	—	1.0 k	—	Ω	

Table 25 Miscellaneous Receiver Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

GPIO Timing Characteristics

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[53:0][1]	Tpw[2]	None	50	—	ns	

Table 26 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

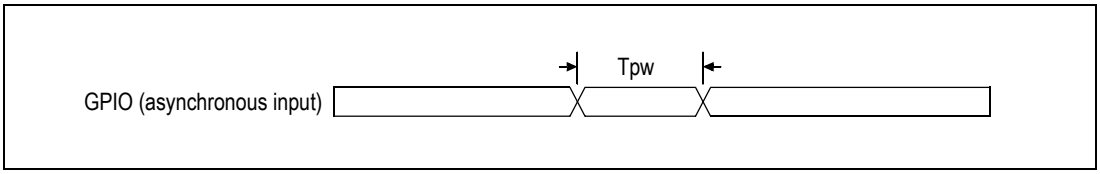


Figure 5 GPIO AC Timing Waveform

JTAG AC Timing Specifications

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 6.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 27 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

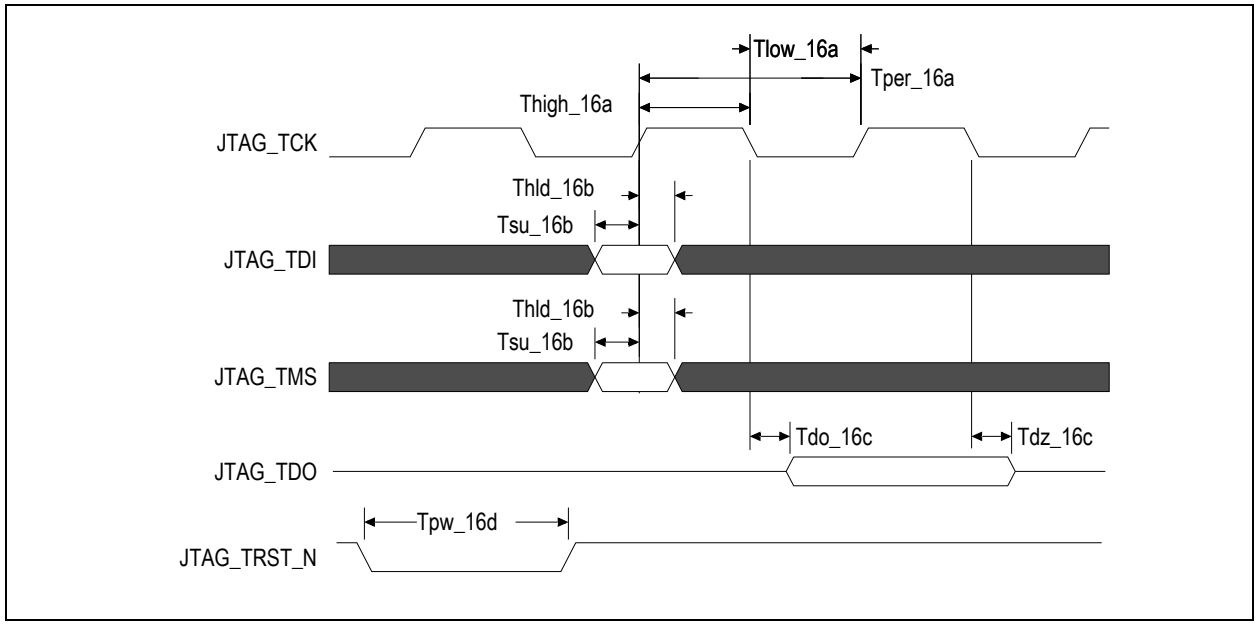


Figure 6 JTAG AC Timing Waveform

SMBus Characterization

Symbol	Parameter	Slow SMBus[1]		
		3.0V	3.3V	3.6V
DC Parameter for SDA Pin				
V_{IL}	Input Low	1.5	1.6	1.7
V_{IH}	Input High	1.6	1.7	1.9
$V_{OL@4mA}$	Output Low	245	230	220
$V_{OL@3mA}$	Output Low	185	175	165
$V_{OL@6mA}$	Output Low	380	350	330
$V_{OL@1mA}$	Output Low	65	65	65
$V_{OL@3350uA}$	Output Low	30	30	30
$I_{OL@0.4V}$		6.4	7	7.4
I_{Pullup}	Current Source	—	—	—
I_{IL_Leak}	Input Low Leakage	0	0.1	.01
I_{IH_Leak}	Input High Leakage	0	0.1	.01

Table 28 SMBus DC Characterization Data (Part 1 of 2)

Symbol	Parameter	Slow SMBus[1]		
		3.0V	3.3V	3.6V
DC Parameter for SCL Pin				
$V_{IL\ (V)}$	Input Low	1.5	1.6	1.7
$V_{IH\ (V)}$	Input High	1.6	1.7	1.9
I_{IL_Leak}	Input Low Leakage	0	0.1	0.1
I_{IH_Leak}	Input High Leakage	0	0.1	0.1

Table 28 SMBus DC Characterization Data (Part 2 of 2)

1. Data at room and hot temperature.

Symbol	Parameter	SMBus @3.3V ±10%[1]		Unit
		Min	Max	
F_{SCL}	Clock frequency	6	625	KHz
T_{BUF}	Bus free time between Stop and Start	3.7	—	µs
$T_{HD:STA}$	Start condition hold time	1.2	—	µs
$T_{SU:STA}$	Start condition setup time	1.2	—	µs
$T_{SU:STO}$	Stop condition setup time	1.2	—	µs
$T_{HD:DAT}$	Data hold time	1.2	—	ns
$T_{SU:DAT}$	Data setup time	1.2	—	ns
$T_{TIMEOUT}$	Detect clock low time out	—	74.7	ms
T_{LOW}	Clock low period	3.7	—	µs
T_{HIGH}	Clock high period	3.7	—	µs
T_F	Clock/Data fall time	—	68.4	ns
T_R	Clock/Data rise time	—	127.6	ns
$T_{POR@10kHz}$	Time which a device must be operational after power-on reset	20	—	ms

Table 29 SMBus AC Timing Data

1. Data at room and hot temperature.

Package Pinout — 1156-BGA Signal Pinout for PES64H16G3

The following table lists the pin numbers and signal names for the PES64H16G3 device. Note: NC stands for No Connection.

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
A1	V_{SS}		A27	PE02TP1		B19	PE03TN2	
A2	V_{SS}		A28	PE02TP0		B20	V_{SS}	
A3	GPIO19	1	A29	V_{SS}		B21	PE03TN1	
A4	V_{DD}IO		A30	V_{DD}IO		B22	PE03TN0	
A5	V_{SS}		A31	MSMBADDR1		B23	V_{SS}	
A6	PE09TP3		A32	MSMBSMODE		B24	PE02TN3	
A7	PE09TP2		A33	V_{SS}		B25	PE02TN2	
A8	V_{SS}		A34	V_{SS}		B26	V_{SS}	
A9	PE09TP1		B1	V_{SS}		B27	PE02TN1	
A10	PE09TP0		B2	V_{DD}IO		B28	PE02TN0	
A11	V_{SS}		B3	GPIO18	1	B29	V_{SS}	
A12	PE08TP3		B4	GPIO17	1	B30	MSMBADDR3	
A13	PE08TP2		B5	V_{SS}		B31	MSMBADDR2	
A14	V_{SS}		B6	PE09TN3		B32	PERSTN	
A15	PE08TP1		B7	PE09TN2		B33	V_{DD}IO	
A16	PE08TP0		B8	V_{SS}		B34	V_{SS}	
A17	V_{SS}		B9	PE09TN1		C1	GPIO29	2
A18	PE03TP3		B10	PE09TN0		C2	GPIO27	2
A19	PE03TP2		B11	V_{SS}		C3	GPIO21	1
A20	V_{SS}		B12	PE08TN3		C4	GPIO16	1
A21	PE03TP1		B13	PE08TN2		C5	V_{SS}	
A22	PE03TP0		B14	V_{SS}		C6	V_{SS}	
A23	V_{SS}		B15	PE08TN1		C7	V_{SS}	
A24	PE02TP3		B16	PE08TN0		C8	V_{SS}	
A25	PE02TP2		B17	V_{SS}		C9	V_{SS}	
A26	V_{SS}		B18	PE03TN3		C10	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 1 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
C11	V_{SS}		D3	$V_{DD}IO$		D29	V_{SS}	
C12	V_{SS}		D4	GPIO23	2	D30	JTAG_TMS	
C13	V_{SS}		D5	V_{SS}		D31	$V_{DD}IO$	
C14	V_{SS}		D6	PE09RN3		D32	SSMBADDR5	
C15	V_{SS}		D7	PE09RN2		D33	SSMBADDR3	
C16	V_{SS}		D8	V_{SS}		D34	$V_{DD}IO$	
C17	V_{SS}		D9	PE09RN1		E1	$V_{DD}IO$	
C18	V_{SS}		D10	PE09RN0		E2	GPIO30	2
C19	V_{SS}		D11	V_{SS}		E3	GPIO31	2
C20	V_{SS}		D12	PE08RN3		E4	GPIO24	2
C21	V_{SS}		D13	PE08RN2		E5	V_{SS}	
C22	V_{SS}		D14	V_{SS}		E6	PE09RP3	
C23	V_{SS}		D15	PE08RN1		E7	PE09RP2	
C24	V_{SS}		D16	PE08RN0		E8	V_{SS}	
C25	V_{SS}		D17	V_{SS}		E9	PE09RP1	
C26	V_{SS}		D18	PE03RN3		E10	PE09RP0	
C27	V_{SS}		D19	PE03RN2		E11	V_{SS}	
C28	V_{SS}		D20	V_{SS}		E12	PE08RP3	
C29	V_{SS}		D21	PE03RN1		E13	PE08RP2	
C30	MSMBADDR4		D22	PE03RN0		E14	V_{SS}	
C31	JTAG_TDI		D23	V_{SS}		E15	PE08RP1	
C32	JTAG_TRST_N		D24	PE02RN3		E16	PE08RP0	
C33	SSMBADDR2		D25	PE02RN2		E17	V_{SS}	
C34	SSMBADDR1		D26	V_{SS}		E18	PE03RP3	
D1	GPIO28	2	D27	PE02RN1		E19	PE03RP2	
D2	GPIO26	2	D28	PE02RN0		E20	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 2 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
E21	PE03RP1		F13	V_{SS}		G5	PE10RP0	
E22	PE03RP0		F14	P08CLKP		G6	V_{SS}	
E23	V_{SS}		F15	V_{SS}		G7	GPIO46	2
E24	PE02RP3		F16	V_{SS}		G8	GPIO45	2
E25	PE02RP2		F17	NC		G9	V_{SS}	
E26	V_{SS}		F18	V_{SS}		G10	V_{SS}	
E27	PE02RP1		F19	NC		G11	P09CLKN	
E28	PE02RP0		F20	P03CLKP		G12	NC	
E29	V_{SS}		F21	V_{SS}		G13	V_{SS}	
E30	V_{SS}		F22	V_{SS}		G14	P08CLKN	
E31	V_{SS}		F23	P02CLKP		G15	NC	
E32	V_{SS}		F24	V_{SS}		G16	V_{SS}	
E33	V_{SS}		F25	V_{SS}		G17	GCLKN0	
E34	V_{SS}		F26	V_{SS}		G18	GCLKP0	
F1	V_{SS}		F27	V_{SS}		G19	NC	
F2	V_{SS}		F28	V_{SS}		G20	P03CLKN	
F3	V_{SS}		F29	V_{SS}		G21	V_{SS}	
F4	V_{SS}		F30	PE01RP3		G22	NC	
F5	V_{SS}		F31	PE01RN3		G23	P02CLKN	
F6	V_{SS}		F32	V_{SS}		G24	V_{SS}	
F7	V_{SS}		F33	PE01TN3		G25	V_{SS}	
F8	V_{SS}		F34	PE01TP3		G26	GPIO33	2
F9	V_{SS}		G1	PE10TP0		G27	MSMBCLK	
F10	NC		G2	PE10TN0		G28	GPIO32	2
F11	P09CLKP		G3	V_{SS}		G29	V_{SS}	
F12	V_{SS}		G4	PE10RN0		G30	PE01RP2	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 3 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
G31	PE01RN2		H23	V_{SS}		J15	NC	
G32	V_{SS}		H24	V_{SS}		J16	V_{SS}	
G33	PE01TN2		H25	V_{SS}		J17	V_{DD}PEHA	
G34	PE01TP2		H26	MSMBDAT		J18	V_{DD}PEHA	
H1	PE10TP1		H27	V_{DD}IO		J19	V_{SS}	
H2	PE10TN1		H28	SSMBCLK		J20	V_{SS}	
H3	V_{SS}		H29	V_{SS}		J21	V_{DD}PEA	
H4	PE10RN1		H30	V_{SS}		J22	V_{SS}	
H5	PE10RP1		H31	V_{SS}		J23	V_{SS}	
H6	V_{SS}		H32	V_{SS}		J24	V_{SS}	
H7	GPIO48	2	H33	V_{SS}		J25	JTAG_TDO	
H8	GPIO20	1	H34	V_{SS}		J26	V_{DD}IO	
H9	V_{DD}IO		J1	V_{SS}		J27	SSMBDAT	
H10	GPIO47	2	J2	V_{SS}		J28	GPIO34	2
H11	V_{SS}		J3	V_{SS}		J29	V_{SS}	
H12	V_{SS}		J4	V_{SS}		J30	PE01RP1	
H13	V_{DD}PEHA		J5	V_{SS}		J31	PE01RN1	
H14	V_{SS}		J6	GPIO50	2	J32	V_{SS}	
H15	V_{DD}PEA		J7	GPIO51	2	J33	PE01TN1	
H16	V_{SS}		J8	V_{SS}		J34	PE01TP1	
H17	V_{SS}		J9	GPIO25	2	K1	PE10TP2	
H18	V_{SS}		J10	GPIO49	2	K2	PE10TN2	
H19	V_{SS}		J11	V_{SS}		K3	V_{SS}	
H20	V_{DD}PEA		J12	V_{SS}		K4	PE10RN2	
H21	NC		J13	V_{SS}		K5	PE10RP2	
H22	V_{DD}PEHA		J14	V_{DD}PEA		K6	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 4 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
K7	GPIO53	1	K33	PE01TN0		L25	V_{SS}	
K8	GPIO52	1	K34	PE01TP0		L26	V_{SS}	
K9	V_{DD}IO		L1	PE10TP3		L27	V_{SS}	
K10	GPIO22	2	L2	PE10TN3		L28	V_{SS}	
K11	V_{SS}		L3	V_{SS}		L29	V_{SS}	
K12	V_{SS}		L4	PE10RN3		L30	V_{SS}	
K13	V_{DD}PEHA		L5	PE10RP3		L31	V_{SS}	
K14	V_{SS}		L6	V_{SS}		L32	V_{SS}	
K15	V_{DD}PEA		L7	V_{SS}		L33	V_{SS}	
K16	V_{SS}		L8	V_{SS}		L34	V_{SS}	
K17	V_{DD}PEHA		L9	V_{SS}		M1	V_{SS}	
K18	V_{DD}PEHA		L10	V_{SS}		M2	V_{SS}	
K19	V_{SS}		L11	V_{SS}		M3	V_{SS}	
K20	V_{DD}PEA		L12	V_{SS}		M4	V_{SS}	
K21	V_{SS}		L13	V_{DD}PEA		M5	V_{SS}	
K22	V_{DD}PEHA		L14	V_{DD}PEA		M6	V_{SS}	
K23	V_{SS}		L15	V_{DD}PEA		M7	V_{SS}	
K24	V_{SS}		L16	V_{SS}		M8	V_{SS}	
K25	CLKMODE1		L17	V_{DD}PEA		M9	V_{SS}	
K26	JTAG_TCK		L18	V_{DD}PEA		M10	V_{SS}	
K27	GPIO36	2	L19	V_{SS}		M11	V_{SS}	
K28	GPIO35	2	L20	V_{DD}PEA		M12	V_{SS}	
K29	V_{SS}		L21	V_{DD}PEA		M13	V_{DD}PEA	
K30	PE01RP0		L22	V_{DD}PEA		M14	V_{SS}	
K31	PE01RN0		L23	V_{SS}		M15	V_{DD}PEA	
K32	V_{SS}		L24	V_{SS}		M16	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 5 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
M17	V_{DD}PEA		N9	V_{SS}		P1	PE11TP1	
M18	V_{DD}PEA		N10	V_{DD}PEHA		P2	PE11TN1	
M19	V_{SS}		N11	V_{DD}PEA		P3	V_{SS}	
M20	V_{DD}PEA		N12	V_{DD}PEA		P4	PE11RN1	
M21	V_{SS}		N13	V_{DD}CORE		P5	PE11RP1	
M22	V_{DD}PEA		N14	V_{DD}CORE		P6	V_{SS}	
M23	V_{SS}		N15	V_{DD}CORE		P7	P10CLKP	
M24	V_{SS}		N16	V_{SS}		P8	P10CLKN	
M25	V_{SS}		N17	V_{DD}CORE		P9	V_{DD}PEA	
M26	V_{SS}		N18	V_{SS}		P10	V_{SS}	
M27	V_{SS}		N19	V_{DD}CORE		P11	V_{DD}PEA	
M28	NC		N20	V_{DD}CORE		P12	V_{SS}	
M29	V_{SS}		N21	V_{DD}CORE		P13	V_{DD}CORE	
M30	PE00RP3		N22	V_{DD}CORE		P14	V_{SS}	
M31	PE00RN3		N23	V_{DD}PEA		P15	V_{DD}CORE	
M32	V_{SS}		N24	V_{DD}PEA		P16	V_{SS}	
M33	PE00TN3		N25	V_{DD}PEHA		P17	V_{DD}CORE	
M34	PE00TP3		N26	V_{SS}		P18	V_{SS}	
N1	PE11TP0		N27	V_{DD}PEHA		P19	V_{DD}CORE	
N2	PE11TN0		N28	NC		P20	V_{SS}	
N3	V_{SS}		N29	V_{SS}		P21	V_{DD}CORE	
N4	PE11RN0		N30	PE00RP2		P22	V_{DD}CORE	
N5	PE11RP0		N31	PE00RN2		P23	V_{SS}	
N6	V_{SS}		N32	V_{SS}		P24	V_{DD}PEA	
N7	NC		N33	PE00TN2		P25	V_{SS}	
N8	V_{DD}PEHA		N34	PE00TP2		P26	V_{DD}PEA	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 6 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
P27	P01CLKN		R19	V_{SS}		T11	V_{SS}	
P28	P01CLKP		R20	V_{DD}CORE		T12	V_{SS}	
P29	V_{SS}		R21	V_{SS}		T13	V_{SS}	
P30	V_{SS}		R22	V_{DD}CORE		T14	V_{SS}	
P31	V_{SS}		R23	V_{DD}PEA		T15	V_{DD}CORE	
P32	V_{SS}		R24	V_{DD}PEA		T16	V_{SS}	
P33	V_{SS}		R25	V_{DD}PEA		T17	V_{DD}CORE	
P34	V_{SS}		R26	V_{SS}		T18	V_{SS}	
R1	V_{SS}		R27	V_{DD}PEA		T19	V_{DD}CORE	
R2	V_{SS}		R28	V_{SS}		T20	V_{SS}	
R3	V_{SS}		R29	NC		T21	V_{DD}CORE	
R4	V_{SS}		R30	PE00RP1		T22	V_{DD}CORE	
R5	V_{SS}		R31	PE00RN1		T23	V_{SS}	
R6	V_{SS}		R32	V_{SS}		T24	V_{SS}	
R7	NC		R33	PE00TN1		T25	V_{SS}	
R8	V_{DD}PEA		R34	PE00TP1		T26	V_{SS}	
R9	V_{SS}		T1	PE11TP2		T27	P00CLKN	
R10	V_{DD}PEA		T2	PE11TN2		T28	P00CLKP	
R11	V_{DD}PEA		T3	V_{SS}		T29	NC	
R12	V_{DD}PEA		T4	PE11RN2		T30	PE00RP0	
R13	V_{DD}CORE		T5	PE11RP2		T31	PE00RN0	
R14	V_{DD}CORE		T6	NC		T32	V_{SS}	
R15	V_{SS}		T7	P11CLKP		T33	PE00TN0	
R16	V_{DD}CORE		T8	P11CLKN		T34	PE00TP0	
R17	V_{SS}		T9	NC		U1	PE11TP3	
R18	V_{DD}CORE		T10	V_{SS}		U2	PE11TN3	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 7 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
U3	V_{SS}		U29	V_{SS}		V21	V_{DD}CORE	
U4	PE11RN3		U30	V_{SS}		V22	V_{DD}CORE	
U5	PE11RP3		U31	V_{SS}		V23	V_{DD}PEA	
U6	V_{SS}		U32	V_{SS}		V24	V_{DD}PEA	
U7	NC		U33	V_{SS}		V25	V_{DD}PEHA	
U8	V_{SS}		U34	V_{SS}		V26	V_{DD}PEHA	
U9	V_{DD}PEHA		V1	V_{SS}		V27	V_{SS}	
U10	V_{DD}PEHA		V2	V_{SS}		V28	NC	
U11	V_{DD}PEA		V3	V_{SS}		V29	V_{SS}	
U12	V_{DD}PEA		V4	V_{SS}		V30	PE15RP3	
U13	V_{DD}CORE		V5	V_{SS}		V31	PE15RN3	
U14	V_{DD}CORE		V6	V_{SS}		V32	V_{SS}	
U15	V_{SS}		V7	NC		V33	PE15TN3	
U16	V_{DD}CORE		V8	V_{SS}		V34	PE15TP3	
U17	V_{SS}		V9	V_{DD}PEHA		W1	PE04TP0	
U18	V_{DD}CORE		V10	V_{DD}PEHA		W2	PE04TN0	
U19	V_{SS}		V11	V_{DD}PEA		W3	V_{SS}	
U20	V_{DD}CORE		V12	V_{DD}PEA		W4	PE04RN0	
U21	V_{SS}		V13	V_{SS}		W5	PE04RP0	
U22	V_{SS}		V14	V_{SS}		W6	V_{SS}	
U23	V_{DD}PEA		V15	V_{DD}CORE		W7	P04CLKP	
U24	V_{DD}PEA		V16	V_{SS}		W8	P04CLKN	
U25	V_{DD}PEHA		V17	V_{DD}CORE		W9	V_{SS}	
U26	V_{DD}PEHA		V18	V_{SS}		W10	V_{SS}	
U27	V_{SS}		V19	V_{DD}CORE		W11	V_{SS}	
U28	NC		V20	V_{SS}		W12	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 8 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
W13	V_{DD}CORE		Y5	PE04RP1		Y31	V_{SS}	
W14	V_{DD}CORE		Y6	NC		Y32	V_{SS}	
W15	V_{SS}		Y7	NC		Y33	V_{SS}	
W16	V_{DD}CORE		Y8	V_{DD}PEA		Y34	V_{SS}	
W17	V_{SS}		Y9	V_{SS}		AA1	V_{SS}	
W18	V_{DD}CORE		Y10	V_{DD}PEA		AA2	V_{SS}	
W19	V_{SS}		Y11	V_{DD}PEA		AA3	V_{SS}	
W20	V_{DD}CORE		Y12	V_{DD}PEA		AA4	V_{SS}	
W21	V_{SS}		Y13	V_{DD}CORE		AA5	V_{SS}	
W22	V_{SS}		Y14	V_{SS}		AA6	V_{SS}	
W23	V_{SS}		Y15	V_{DD}CORE		AA7	P05CLKP	
W24	V_{SS}		Y16	V_{SS}		AA8	P05CLKN	
W25	V_{SS}		Y17	V_{DD}CORE		AA9	V_{DD}PEA	
W26	NC		Y18	V_{SS}		AA10	V_{SS}	
W27	P15CLKN		Y19	V_{DD}CORE		AA11	V_{DD}PEA	
W28	P15CLKP		Y20	V_{SS}		AA12	V_{SS}	
W29	NC		Y21	V_{DD}CORE		AA13	V_{DD}CORE	
W30	PE15RP2		Y22	V_{DD}CORE		AA14	V_{DD}CORE	
W31	PE15RN2		Y23	V_{DD}PEA		AA15	V_{SS}	
W32	V_{SS}		Y24	V_{DD}PEA		AA16	V_{DD}CORE	
W33	PE15TN2		Y25	V_{DD}PEA		AA17	V_{SS}	
W34	PE15TP2		Y26	V_{SS}		AA18	V_{DD}CORE	
Y1	PE04TP1		Y27	V_{DD}PEA		AA19	V_{SS}	
Y2	PE04TN1		Y28	V_{SS}		AA20	V_{DD}CORE	
Y3	V_{SS}		Y29	NC		AA21	V_{SS}	
Y4	PE04RN1		Y30	V_{SS}		AA22	V_{DD}CORE	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 9 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AA23	V_{SS}		AB15	V_{DD}CORE		AC7	V_{SS}	
AA24	V_{DD}PEA		AB16	V_{DD}CORE		AC8	V_{SS}	
AA25	V_{SS}		AB17	V_{SS}		AC9	V_{SS}	
AA26	V_{DD}PEA		AB18	V_{DD}CORE		AC10	V_{SS}	
AA27	P14CLKN		AB19	V_{SS}		AC11	V_{SS}	
AA28	P14CLKP		AB20	V_{DD}CORE		AC12	V_{SS}	
AA29	NC		AB21	V_{DD}CORE		AC13	V_{DD}PEA	
AA30	PE15RP1		AB22	V_{DD}CORE		AC14	V_{SS}	
AA31	PE15RN1		AB23	V_{DD}PEA		AC15	V_{DD}PEA	
AA32	V_{SS}		AB24	V_{DD}PEA		AC16	V_{SS}	
AA33	PE15TN1		AB25	V_{DD}PEHA		AC17	V_{DD}PEA	
AA34	PE15TP1		AB26	V_{SS}		AC18	V_{DD}PEA	
AB1	PE04TP2		AB27	V_{DD}PEHA		AC19	V_{SS}	
AB2	PE04TN2		AB28	V_{SS}		AC20	V_{DD}PEA	
AB3	V_{SS}		AB29	V_{SS}		AC21	V_{SS}	
AB4	PE04RN2		AB30	PE15RP0		AC22	V_{DD}PEA	
AB5	PE04RP2		AB31	PE15RN0		AC23	V_{SS}	
AB6	NC		AB32	V_{SS}		AC24	V_{SS}	
AB7	NC		AB33	PE15TN0		AC25	V_{SS}	
AB8	V_{DD}PEHA		AB34	PE15TP0		AC26	V_{SS}	
AB9	V_{SS}		AC1	PE04TP3		AC27	V_{SS}	
AB10	V_{DD}PEHA		AC2	PE04TN3		AC28	V_{SS}	
AB11	V_{DD}PEA		AC3	V_{SS}		AC29	V_{SS}	
AB12	V_{DD}PEA		AC4	PE04RN3		AC30	V_{SS}	
AB13	V_{DD}CORE		AC5	PE04RP3		AC31	V_{SS}	
AB14	V_{DD}CORE		AC6	V_{SS}		AC32	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 10 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AC33	V_{SS}		AD25	GPIO39	2	AE17	V_{DD}PEHA	
AC34	V_{SS}		AD26	GPIO38	2	AE18	V_{DD}PEHA	
AD1	V_{SS}		AD27	GPIO37	2	AE19	V_{SS}	
AD2	V_{SS}		AD28	V_{SS}		AE20	V_{DD}PEA	
AD3	V_{SS}		AD29	V_{SS}		AE21	V_{SS}	
AD4	V_{SS}		AD30	PE14RP3		AE22	V_{DD}PEHA	
AD5	V_{SS}		AD31	PE14RN3		AE23	V_{SS}	
AD6	V_{SS}		AD32	V_{SS}		AE24	V_{SS}	
AD7	V_{SS}		AD33	PE14TN3		AE25	GPIO06	
AD8	V_{SS}		AD34	PE14TP3		AE26	V_{DD}IO	
AD9	NC		AE1	PE05TP0		AE27	GPIO40	2
AD10	NC		AE2	PE05TN0		AE28	V_{SS}	
AD11	V_{SS}		AE3	V_{SS}		AE29	V_{SS}	
AD12	V_{SS}		AE4	PE05RN0		AE30	PE14RP2	
AD13	V_{DD}PEA		AE5	PE05RP0		AE31	PE14RN2	
AD14	V_{DD}PEA		AE6	V_{SS}		AE32	V_{SS}	
AD15	V_{DD}PEA		AE7	V_{SS}		AE33	PE14TN2	
AD16	V_{SS}		AE8	V_{DD}IO		AE34	PE14TP2	
AD17	V_{DD}PEA		AE9	V_{DD}IO		AF1	PE05TP1	
AD18	V_{DD}PEA		AE10	V_{DD}IO		AF2	PE05TN1	
AD19	V_{SS}		AE11	V_{SS}		AF3	V_{SS}	
AD20	V_{DD}PEA		AE12	V_{SS}		AF4	PE05RN1	
AD21	V_{DD}PEA		AE13	V_{DD}PEHA		AF5	PE05RP1	
AD22	V_{DD}PEA		AE14	V_{SS}		AF6	V_{SS}	
AD23	V_{SS}		AE15	V_{DD}PEA		AF7	V_{SS}	
AD24	V_{SS}		AE16	V_{SS}		AF8	V_{SS}	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 11 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AF9	$V_{DD}IO$		AG1	V_{SS}		AG27	GPIO04	1
AF10	$V_{DD}IO$		AG2	V_{SS}		AG28	GPIO43	2
AF11	V_{SS}		AG3	V_{SS}		AG29	V_{SS}	
AF12	V_{SS}		AG4	V_{SS}		AG30	PE14RP1	
AF13	V_{SS}		AG5	V_{SS}		AG31	PE14RN1	
AF14	$V_{DD}PEA$		AG6	V_{SS}		AG32	V_{SS}	
AF15	V_{SS}		AG7	CLKMODE0		AG33	PE14TN1	
AF16	V_{SS}		AG8	$V_{DD}IO$		AG34	PE14TP1	
AF17	$V_{DD}PEHA$		AG9	$V_{DD}IO$		AH1	PE05TP2	
AF18	$V_{DD}PEHA$		AG10	V_{SS}		AH2	PE05TN2	
AF19	V_{SS}		AG11	V_{SS}		AH3	V_{SS}	
AF20	V_{SS}		AG12	V_{SS}		AH4	PE05RN2	
AF21	$V_{DD}PEA$		AG13	$V_{DD}PEHA$		AH5	PE05RP2	
AF22	V_{SS}		AG14	V_{SS}		AH6	V_{SS}	
AF23	V_{SS}		AG15	$V_{DD}PEA$		AH7	CLKMODE2	
AF24	V_{SS}		AG16	V_{SS}		AH8	NC	
AF25	GPIO42	2	AG17	V_{SS}		AH9	V_{SS}	
AF26	GPIO09	1	AG18	V_{SS}		AH10	V_{SS}	
AF27	GPIO41	2	AG19	V_{SS}		AH11	V_{SS}	
AF28	V_{SS}		AG20	$V_{DD}PEA$		AH12	P06CLKN	
AF29	V_{SS}		AG21	NC		AH13	V_{SS}	
AF30	V_{SS}		AG22	$V_{DD}PEHA$		AH14	NC	
AF31	V_{SS}		AG23	V_{SS}		AH15	P07CLKN	
AF32	V_{SS}		AG24	V_{SS}		AH16	NC	
AF33	V_{SS}		AG25	GPIO44	2	AH17	GCLKP1	
AF34	V_{SS}		AG26	$V_{DD}IO$		AH18	GCLKN1	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 12 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AH19	V_{SS}		AJ11	V_{SS}		AK3	V_{SS}	
AH20	NC		AJ12	P06CLKP		AK4	V_{SS}	
AH21	P12CLKN		AJ13	V_{SS}		AK5	V_{SS}	
AH22	NC		AJ14	NC		AK6	V_{SS}	
AH23	NC		AJ15	P07CLKP		AK7	PE06RP0	
AH24	P13CLKN		AJ16	NC		AK8	PE06RP1	
AH25	V_{SS}		AJ17	V_{SS}		AK9	V_{SS}	
AH26	V_{SS}		AJ18	V_{SS}		AK10	PE06RP2	
AH27	V_{SS}		AJ19	V_{SS}		AK11	PE06RP3	
AH28	V_{SS}		AJ20	V_{SS}		AK12	V_{SS}	
AH29	V_{SS}		AJ21	P12CLKP		AK13	PE07RP0	
AH30	PE14RP0		AJ22	V_{SS}		AK14	PE07RP1	
AH31	PE14RN0		AJ23	V_{SS}		AK15	V_{SS}	
AH32	V_{SS}		AJ24	P13CLKP		AK16	PE07RP2	
AH33	PE14TN0		AJ25	V_{SS}		AK17	PE07RP3	
AH34	PE14TP0		AJ26	V_{SS}		AK18	V_{SS}	
AJ1	PE05TP3		AJ27	V_{SS}		AK19	PE12RP0	
AJ2	PE05TN3		AJ28	V_{SS}		AK20	PE12RP1	
AJ3	V_{SS}		AJ29	V_{SS}		AK21	V_{SS}	
AJ4	PE05RN3		AJ30	V_{SS}		AK22	PE12RP2	
AJ5	PE05RP3		AJ31	V_{SS}		AK23	PE12RP3	
AJ6	V_{SS}		AJ32	V_{SS}		AK24	V_{SS}	
AJ7	V_{SS}		AJ33	V_{SS}		AK25	PE13RP0	
AJ8	V_{SS}		AJ34	V_{SS}		AK26	PE13RP1	
AJ9	V_{SS}		AK1	V_{SS}		AK27	V_{SS}	
AJ10	V_{SS}		AK2	V_{SS}		AK28	PE13RP2	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 13 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AK29	PE13RP3		AL21	V_{SS}		AM13	V_{SS}	
AK30	V_{SS}		AL22	PE12RN2		AM14	V_{SS}	
AK31	GPIO08	1	AL23	PE12RN3		AM15	V_{SS}	
AK32	GPIO15	1	AL24	V_{SS}		AM16	V_{SS}	
AK33	GPIO14	1	AL25	PE13RN0		AM17	V_{SS}	
AK34	V_{DD}IO		AL26	PE13RN1		AM18	V_{SS}	
AL1	V_{DD}IO		AL27	V_{SS}		AM19	V_{SS}	
AL2	P01MERGEN		AL28	PE13RN2		AM20	V_{SS}	
AL3	P45MERGEN		AL29	PE13RN3		AM21	V_{SS}	
AL4	V_{DD}IO		AL30	V_{SS}		AM22	V_{SS}	
AL5	P89MERGEN		AL31	GPIO07		AM23	V_{SS}	
AL6	V_{SS}		AL32	V_{DD}IO		AM24	V_{SS}	
AL7	PE06RN0		AL33	GPIO10	1	AM25	V_{SS}	
AL8	PE06RN1		AL34	GPIO12	1	AM26	V_{SS}	
AL9	V_{SS}		AM1	P23MERGEN		AM27	V_{SS}	
AL10	PE06RN2		AM2	P67MERGEN		AM28	V_{SS}	
AL11	PE06RN3		AM3	P1415MERGEN		AM29	V_{SS}	
AL12	V_{SS}		AM4	P1011MERGEN		AM30	V_{SS}	
AL13	PE07RN0		AM5	SWMODE3		AM31	GPIO00	1
AL14	PE07RN1		AM6	V_{SS}		AM32	GPIO05	2
AL15	V_{SS}		AM7	V_{SS}		AM33	GPIO11	1
AL16	PE07RN2		AM8	V_{SS}		AM34	GPIO13	1
AL17	PE07RN3		AM9	V_{SS}		AN1	V_{SS}	
AL18	V_{SS}		AM10	V_{SS}		AN2	V_{DD}IO	
AL19	PE12RN0		AM11	V_{SS}		AN3	P1213MERGEN	
AL20	PE12RN1		AM12	V_{SS}		AN4	SWMODE0	

Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 14 of 15)

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AN5	SWMODE2		AN27	V_{SS}		AP15	V_{SS}	
AN6	V_{SS}		AN28	PE13TN2		AP16	PE07TP2	
AN7	PE06TN0		AN29	PE13TN3		AP17	PE07TP3	
AN8	PE06TN1		AN30	V_{SS}		AP18	V_{SS}	
AN9	V_{SS}		AN31	GPIO01	1	AP19	PE12TP0	
AN10	PE06TN2		AN32	GPIO02	1	AP20	PE12TP1	
AN11	PE06TN3		AN33	$V_{DD}IO$		AP21	V_{SS}	
AN12	V_{SS}		AN34	V_{SS}		AP22	PE12TP2	
AN13	PE07TN0		AP1	V_{SS}		AP23	PE12TP3	
AN14	PE07TN1		AP2	V_{SS}		AP24	V_{SS}	
AN15	V_{SS}		AP3	RSTHALT		AP25	PE13TP0	
AN16	PE07TN2		AP4	SWMODE1		AP26	PE13TP1	
AN17	PE07TN3		AP5	$V_{DD}IO$		AP27	V_{SS}	
AN18	V_{SS}		AP6	V_{SS}		AP28	PE13TP2	
AN19	PE12TN0		AP7	PE06TP0		AP29	PE13TP3	
AN20	PE12TN1		AP8	PE06TP1		AP30	V_{SS}	
AN21	V_{SS}		AP9	V_{SS}		AP31	$V_{DD}IO$	
AN22	PE12TN2		AP10	PE06TP2		AP32	GPIO03	1
AN23	PE12TN3		AP11	PE06TP3		AP33	V_{SS}	
AN24	V_{SS}		AP12	V_{SS}		AP34	V_{SS}	
AN25	PE13TN0		AP13	PE07TP0				
AN26	PE13TN1		AP14	PE07TP1				

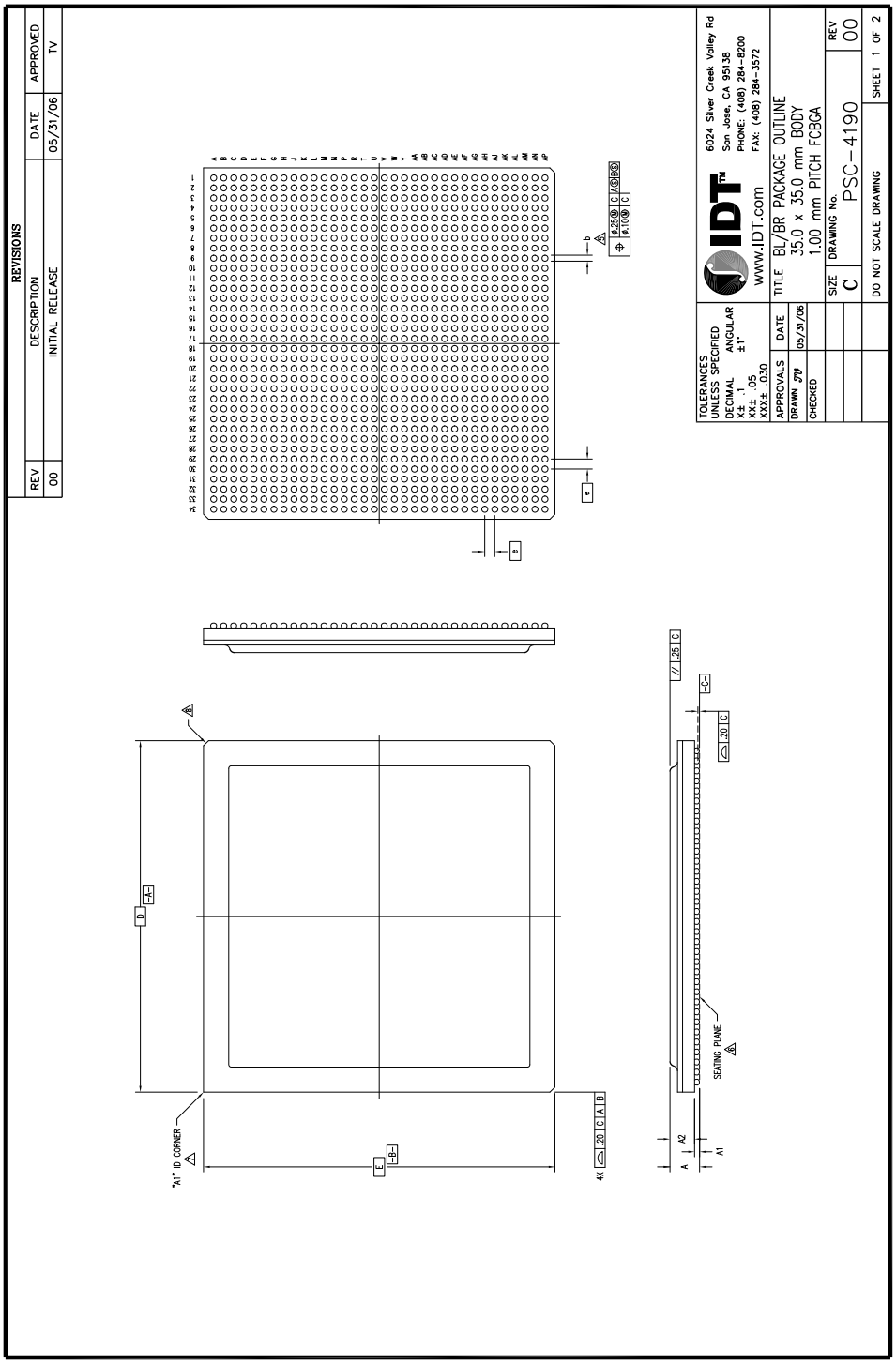
Table 30 PES64H16G3 1156-Pin Signal Pin-out (Part 15 of 15)

Alternate Signal Functions

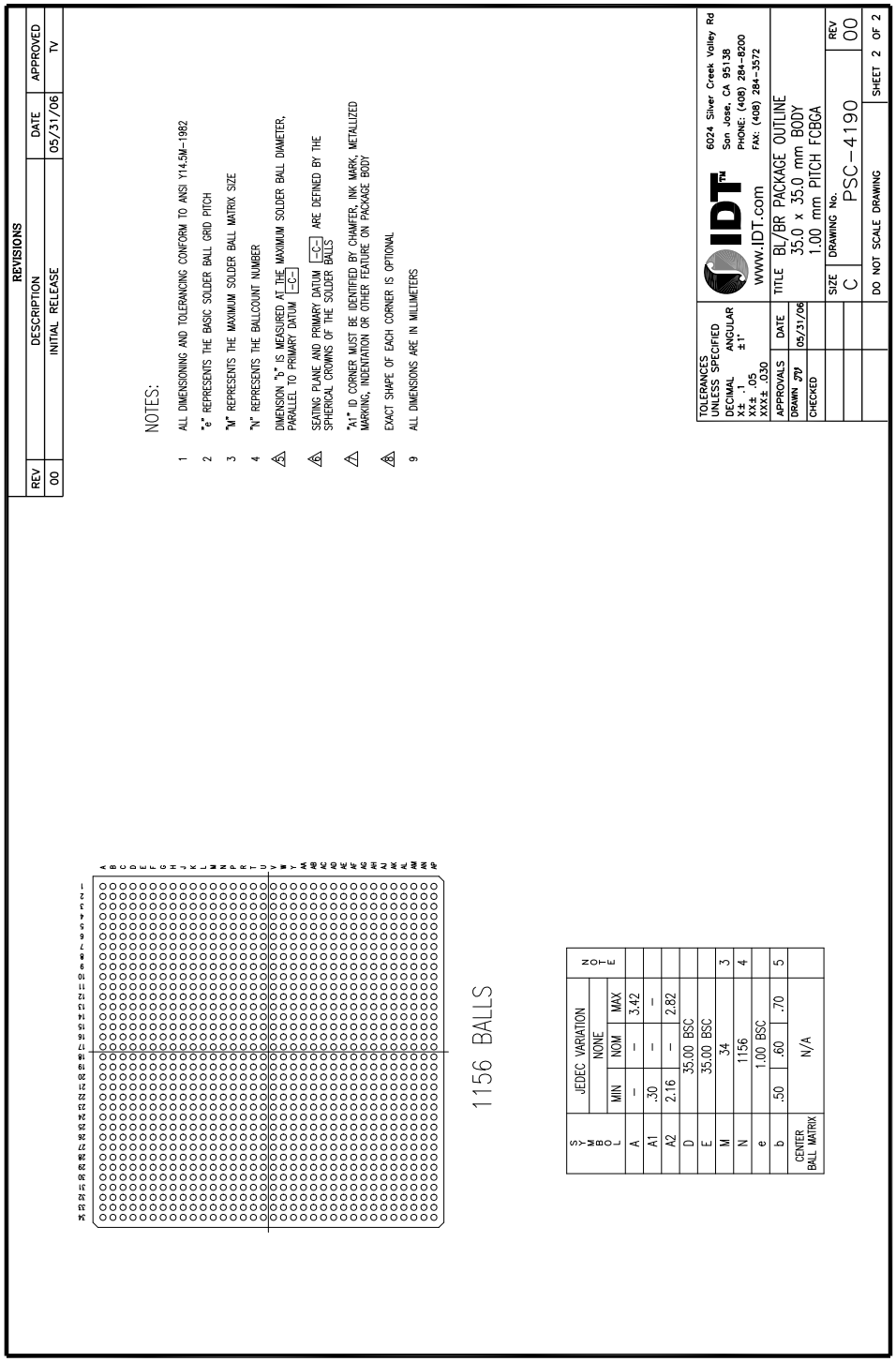
Pin	GPIO	1st Alternate	2nd Alternate	Pin	GPIO	1st Alternate	2nd Alternate
AM31	GPIO00	PART0PERSTN	—	D1	GPIO28	HP2PDN	P4LINKUPN
AN31	GPIO01	PART1PERSTN	—	C1	GPIO29	HP2PFN	P4ACTIVEN
AN32	GPIO02	PART2PERSTN	—	E2	GPIO30	HP2PWRGDN	P5LINKUPN
AP32	GPIO03	PART3PERSTN		E3	GPIO31	HP2MRLN	P5ACTIVEN
AG27	GPIO04	—	P0LINKUPN	G28	GPIO32	HP2AIN	P6LINKUPN
AM32	GPIO05	GPEN	P0ACTIVEN	G26	GPIO33	HP2PIN	P6ACTIVEN
AK31	GPIO08	IOEXPINTN	—	J28	GPIO34	HP2PEP	P7LINKUPN
AF26	GPIO09	HP0APN	—	K28	GPIO35	HP2RSTN	P7ACTIVEN
AL33	GPIO10	HP0PDN	—	K27	GPIO36	HP3APN	P8LINKUPN
AM33	GPIO11	HP0PFN	—	AD27	GPIO37	HP3PDN	P8ACTIVEN
AL34	GPIO12	HP0PWRGDN	—	AD26	GPIO38	HP3PFN	P9LINKUPN
AM34	GPIO13	HP0MRLN	—	AD25	GPIO39	HP3PWRGDN	P9ACTIVEN
AK33	GPIO14	HP0AIN	—	AE27	GPIO40	HP3MRLN	P10LINKUPN
AK32	GPIO15	HP0PIN	—	AF27	GPIO41	HP3AIN	P10ACTIVEN
C4	GPIO16	HP0PEP	—	AF25	GPIO42	HP3PIN	P11LINKUPN
B4	GPIO17	HP0RSTN	—	AG28	GPIO43	HP3PEP	P11ACTIVEN
B3	GPIO18	HP1APN	—	AG25	GPIO44	HP3RSTN	P12LINKUPN
A3	GPIO19	HP1PDN	—	G8	GPIO45	HP4APN	P12ACTIVEN
H8	GPIO20	HP1PFN	—	G7	GPIO46	HP4PDN	P13LINKUPN
C3	GPIO21	HP1PWRGDN	—	H10	GPIO47	HP4PFN	P13ACTIVEN
K10	GPIO22	HP1MRLN	P1LINKUPN	H7	GPIO48	HP4PWRGDN	P14LINKUPN
D4	GPIO23	HP1AIN	P1ACTIVEN	J10	GPIO49	HP4MRLN	P14ACTIVEN
E4	GPIO24	HP1PIN	P2LINKUPN	J6	GPIO50	HP4AIN	P15LINKUPN
J9	GPIO25	HP1PEP	P2ACTIVEN	J7	GPIO51	HP4PIN	P15ACTIVEN
D2	GPIO26	HP1RSTN	P3LINKUPN	K8	GPIO52	HP4PEP	—
C2	GPIO27	HP2APN	P3ACTIVEN	K7	GPIO53	HP4RSTN	—

Table 31 PES64H16G3 Alternate Signal Functions

PES64H16G3 Package Drawing — 1156-Pin BL1156/BLG1156



PES64H16G3 Package Drawing — Page Two

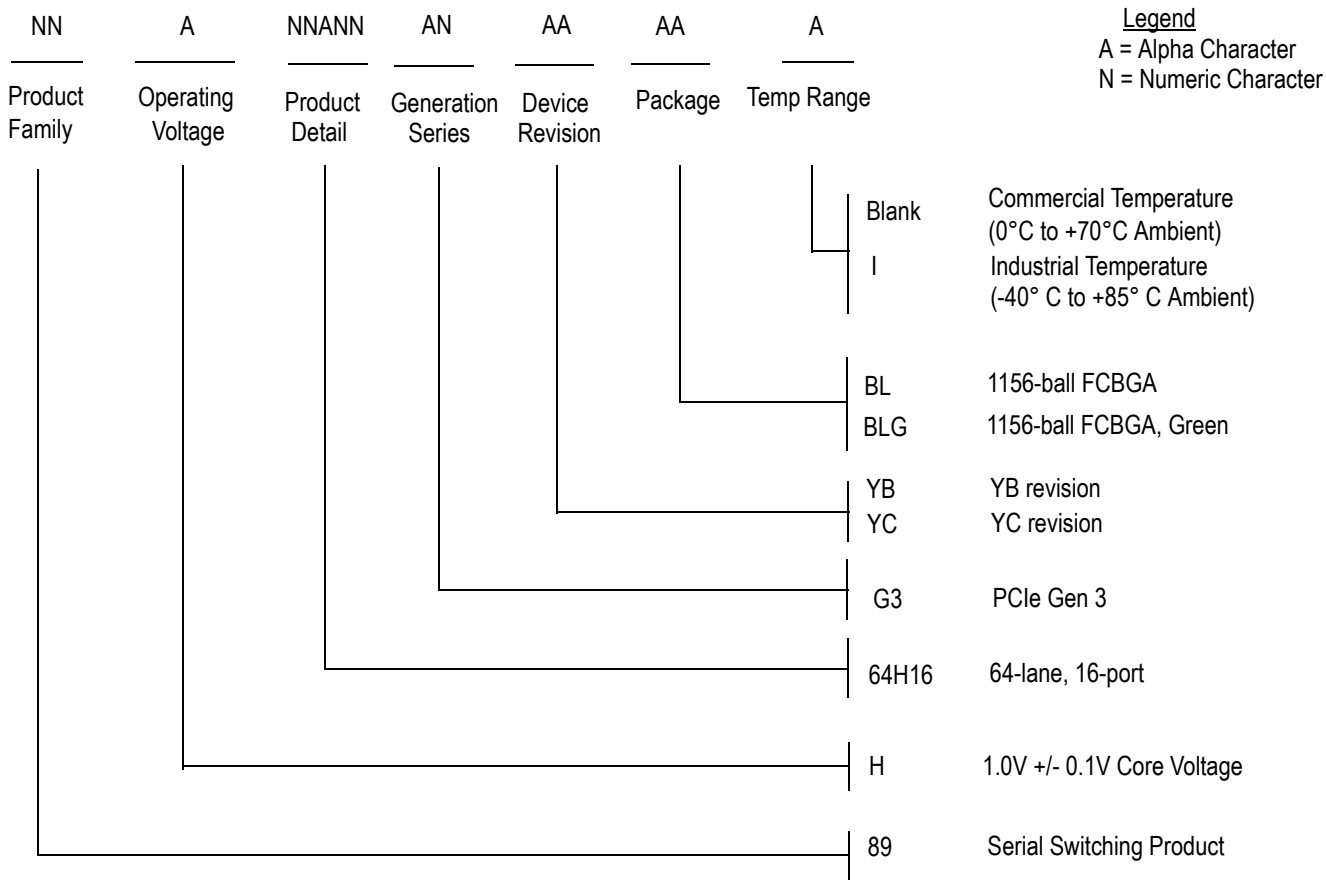


Revision History

March 12, 2013: Initial publication of final data sheet.

April 17, 2013: In Power Consumption table (Table 14) footnotes, added Note #4 Tc (max case temp).

Ordering Information



Valid Combinations

89H64H16G3YBBL	1156-ball FCBGA package, Commercial Temp.	89H64H16G3YCBL	1156-ball FCBGA package, Commercial Temp.
89H64H16G3YBBLG	1156-ball Green FCBGA package, Commercial Temp.	89H64H16G3YCBLG	1156-ball Green FCBGA package, Commercial Temp.
89H64H16G3YBBLI	1156-ball FCBGA package, Industrial Temp.	89H64H16G3YCBLI	1156-ball FCBGA package, Industrial Temp.
89H64H16G3YBBLGI	1156-ball Green FCBGA package, Industrial Temp.	89H64H16G3YCBLGI	1156-ball Green FCBGA package, Industrial Temp.

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