

General Description

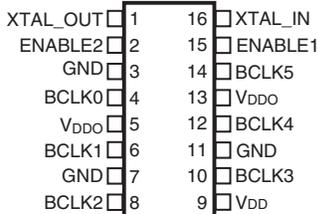
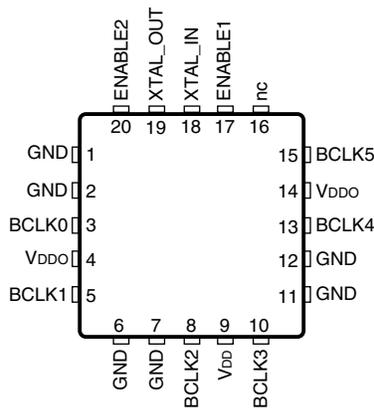


The ICS83905 is a low skew, 1-to-6 LVCMOS / LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 6 to 12 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83905 is characterized at full 3.3V, 2.5V, and 1.8V, mixed 3.3V/2.5V, 3.3V/1.8V and 2.5V/1.8V output operating supply mode. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the ICS83905 ideal for high performance, single ended applications that also require a limited output voltage.

Pin Assignments

ICS83905
20-Lead VFQFN
4mm x 4mm x 0.925mm
package body
K Package
Top View



ICS83905
16-Lead SOIC, 150 Mil
3.9mm x 9.9mm x 1.38mm
package body
M Package
Top View

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm
package body
G Package
Top View

Features

- Six LVCMOS / LVTTL outputs
- Outputs able to drive 12 series terminated lines
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Output skew: 80ps (maximum)
- RMS phase jitter @ 25MHz, (100Hz – 1MHz): 0.26ps (typical), $V_{DD} = V_{DD0} = 2.5V$
- **Offset** **Noise Power**
- 100Hz.....-129.7 dBc/Hz
- 1kHz.....-144.4 dBc/Hz
- 10kHz.....-147.3 dBc/Hz
- 100kHz.....-157.3 dBc/Hz
- 5V tolerant enable inputs
- Synchronous output enables
- Operating power supply modes:
 Full 3.3V, 2.5V, 1.8V
 Mixed 3.3V core/2.5V output operating supply
 Mixed 3.3V core/1.8V output operating supply
 Mixed 2.5V core/1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram

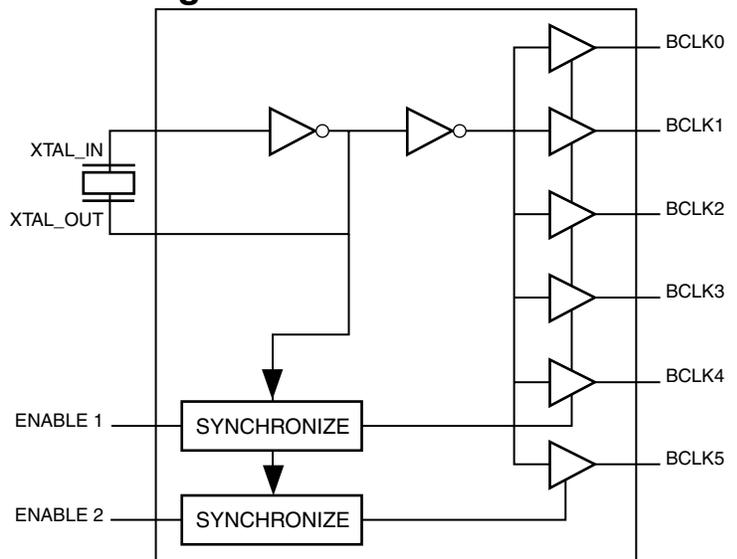


Table 1. Pin Descriptions

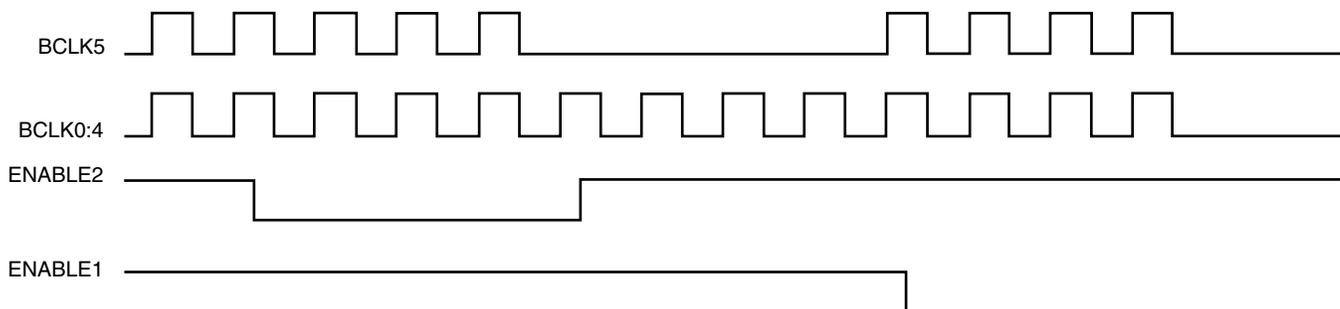
| Name | Type | Description |
|--|--------|---|
| XTAL_OUT | Output | Crystal oscillator interface. XTAL_OUT is the output. |
| XTAL_IN | Input | Crystal oscillator interface. XTAL_IN is the input. |
| ENABLE1, ENABLE2 | Input | Clock enable. LVCMOS/LVTTL interface levels. See Table 3. |
| BCLK0, BCLK1, BCLK2, BCLK3, BCLK4, BCLK5 | Output | Clock outputs. LVCMOS/LVTTL interface levels. |
| GND | Power | Power supply ground. |
| V _{DD} | Power | Power supply pin. |
| V _{DDO} | Power | Output supply pin. |
| nc | Unused | No connect. |

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------|--|--------------------------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance (per output) | V _{DDO} = 3.465V | | | 19 | pF |
| | | V _{DDO} = 2.625V | | | 18 | pF |
| | | V _{DDO} = 2.0V | | | 16 | pF |
| R _{OUT} | Output Impedance | V _{DDO} = 3.3V ± 5% | | 7 | | Ω |
| | | V _{DDO} = 2.5V ± 5% | | 7 | | Ω |
| | | V _{DDO} = 1.8V ± 0.2V | | 10 | | Ω |

Function Table**Table 3. Clock Enable Function Table**

| Control Inputs | | Outputs | |
|----------------|---------|-----------|----------|
| ENABLE 1 | ENABLE2 | BCLK[0:4] | BCLK5 |
| 0 | 0 | LOW | LOW |
| 0 | 1 | LOW | Toggling |
| 1 | 0 | Toggling | LOW |
| 1 | 1 | Toggling | Toggling |

**Figure 1. Enable Timing Diagram**

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|---|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} 16 Lead SOIC package 16 Lead TSSOP package 20 Lead VFQFN package | 78.8°C/W (0 mps) 100.3°C/W (0 mps) 57.5°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | ENABLE [1:2] = 00 | | | 10 | mA |
| I_{DDO} | Output Supply Current | ENABLE [1:2] = 00 | | | 5 | mA |

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | ENABLE [1:2] = 00 | | | 8 | mA |
| I_{DDO} | Output Supply Current | ENABLE [1:2] = 00 | | | 4 | mA |

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| V_{DDO} | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| I_{DD} | Power Supply Current | ENABLE [1:2] = 00 | | | 5 | mA |
| I_{DDO} | Output Supply Current | ENABLE [1:2] = 00 | | | 3 | mA |

Table 4D. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | ENABLE [1:2] = 00 | | | 10 | mA |
| I_{DDO} | Output Supply Current | ENABLE [1:2] = 00 | | | 4 | mA |

Table 4E. Power Supply DC Characteristics, $3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V\%$, $T_A = 0^\circ\text{C}$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| I_{DD} | Power Supply Current | ENABLE [1:2] = 00 | | | 10 | mA |
| I_{DDO} | Output Supply Current | ENABLE [1:2] = 00 | | | 3 | mA |

Table 4F. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V\%$, $T_A = 0^\circ\text{C}$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-------------------|---------|---------|---------|-------|
| V_{DD} | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DDO} | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| I_{DD} | Power Supply Current | ENABLE [1:2] = 00 | | | 8 | mA |
| I_{DDO} | Output Supply Current | ENABLE [1:2] = 00 | | | 3 | mA |

Table 4G. LVCMOS/LVTTL DC Characteristics, $T_A = 0^\circ\text{C}$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|----------|----------------------------|---------------------|---|-----------------|---------|-----------------|---|
| V_{IH} | Input High Voltage | ENABLE1, ENABLE2 | $V_{DD} = 3.3V \pm 5\%$ | 2 | | $V_{DD} + 0.3$ | V |
| | | | $V_{DD} = 2.5V \pm 5\%$ | 1.7 | | $V_{DD} + 0.3$ | V |
| | | | $V_{DD} = 1.8V \pm 0.2V$ | $0.65 * V_{DD}$ | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | ENABLE1, ENABLE2 | $V_{DD} = 3.3V \pm 5\%$ | -0.3 | | 0.8 | V |
| | | | $V_{DD} = 2.5V \pm 5\%$ | -0.3 | | 0.7 | V |
| | | | $V_{DD} = 1.8V \pm 0.2V$ | -0.3 | | $0.35 * V_{DD}$ | V |
| V_{OH} | Output High Voltage | | $V_{DDO} = 3.3V \pm 5\%$; NOTE 1 | 2.6 | | | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$; $I_{OH} = -1\text{mA}$ | 2.0 | | | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$; NOTE 1 | 1.8 | | | V |
| | | | $V_{DDO} = 1.8V \pm 0.2V$; NOTE 1 | $V_{DDO} - 0.3$ | | | |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{DDO} = 3.3V \pm 5\%$; NOTE 1 | | | 0.5 | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$; $I_{OL} = 1\text{mA}$ | | | 0.4 | V |
| | | | $V_{DDO} = 2.5V \pm 5\%$; NOTE 1 | | | 0.45 | V |
| | | | $V_{DDO} = 1.8V \pm 0.2V$; NOTE 1 | | | 0.35 | |

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, *Output Load Test Circuit diagrams*.

Table 5. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 10 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------------------|------------------------------------|---|---------|---------|---------|--------|
| f_{MAX} | Output Frequency | Using External Crystal | | 10 | | 40 | MHz |
| | | Using External Clock Source NOTE 1 | | DC | | 100 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | | 80 | ps |
| $t_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 4 | | 25MHz, Integration Range: 100Hz – 1MHz | | 0.13 | | ps |
| t_R / t_F | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | | | 48 | | 52 | % |
| t_{EN} | Output Enable Time; NOTE 5 | ENABLE1 | | | | 4 | cycles |
| | | ENABLE2 | | | | 4 | cycles |
| t_{DIS} | Output Disable Time; NOTE 5 | ENABLE1 | | | | 4 | cycles |
| | | ENABLE2 | | | | 4 | cycles |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

Table 6B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|------------------------------------|---|---------|---------|---------|--------|
| f_{MAX} | Output Frequency | Using External Crystal | | 10 | | 40 | MHz |
| | | Using External Clock Source NOTE 1 | | DC | | 100 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | | 80 | ps |
| t_{jit} | RMS Phase Jitter (Random); NOTE 4 | | 25MHz, Integration Range: 100Hz – 1MHz | | 0.26 | | ps |
| t_R / t_F | Output Rise/Fall Time | | 20% to 80% | 200 | | 800 | ps |
| odc | Output Duty Cycle | | | 47 | | 53 | % |
| t_{EN} | Output Enable Time; NOTE 5 | ENABLE1 | | | | 4 | cycles |
| | | ENABLE2 | | | | 4 | cycles |
| t_{DIS} | Output Disable Time; NOTE 5 | ENABLE1 | | | | 4 | cycles |
| | | ENABLE2 | | | | 4 | cycles |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

Table 6C. AC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V, T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------------|---|---------|---------|---------|--------|
| f_{MAX} | Output Frequency | Using External Crystal | 10 | | 40 | MHz |
| | | Using External Clock Source NOTE 1 | DC | | 100 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | 80 | ps |
| $t_{jit}(\emptyset)$ | RMS Phase Jitter (Random) | 25MHz, Integration Range: 100Hz – 1MHz | | 0.27 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 900 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |
| t_{EN} | Output Enable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | 4 | cycles |
| t_{DIS} | Output Disable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | 4 | cycles |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65..

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

Table 6D. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------|---|---------|---------|---------|--------|
| f_{MAX} | Output Frequency | Using External Crystal | 10 | | 40 | MHz |
| | | Using External Clock Source NOTE 1 | DC | | 100 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | 80 | ps |
| t_{jit} | RMS Phase Jitter (Random) | 25MHz, Integration Range: 100Hz – 1MHz | | 0.14 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 48 | | 52 | ps |
| odc | Output Duty Cycle | | 200 | | 800 | % |
| t_{EN} | Output Enable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | 4 | cycles |
| t_{DIS} | Output Disable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | 4 | cycles |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

Table 6E. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------|---|---------|---------|---------|--------|
| f_{MAX} | Output Frequency | Using External Crystal | 10 | | 40 | MHz |
| | | Using External Clock Source NOTE 1 | DC | | 100 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | 80 | ps |
| t_{jit} | RMS Phase Jitter (Random) | 25MHz, Integration Range: 100Hz – 1MHz | | 0.18 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 900 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |
| t_{EN} | Output Enable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | | cycles |
| t_{DIS} | Output Disable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | | cycles |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65..

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

Table 6F. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ to $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------|---|---------|---------|---------|--------|
| f_{MAX} | Output Frequency | Using External Crystal | 10 | | 40 | MHz |
| | | Using External Clock Source NOTE 1 | DC | | 100 | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | 80 | ps |
| t_{jit} | RMS Phase Jitter (Random) | 25MHz, Integration Range: 100Hz – 1MHz | | 0.19 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | | 900 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |
| t_{EN} | Output Enable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | 4 | cycles |
| t_{DIS} | Output Disable Time; NOTE 4 | ENABLE1 | | | 4 | cycles |
| | | ENABLE2 | | | 4 | cycles |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

Terminated at 50Ω to $V_{DDO}/2$.

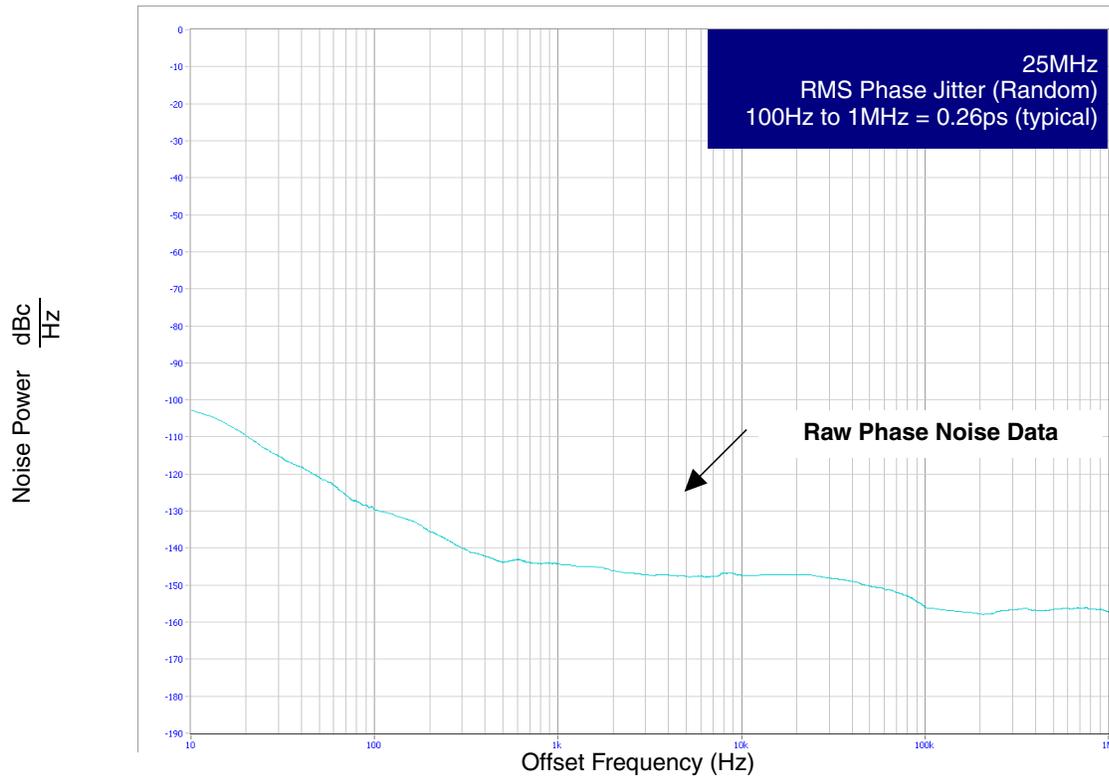
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

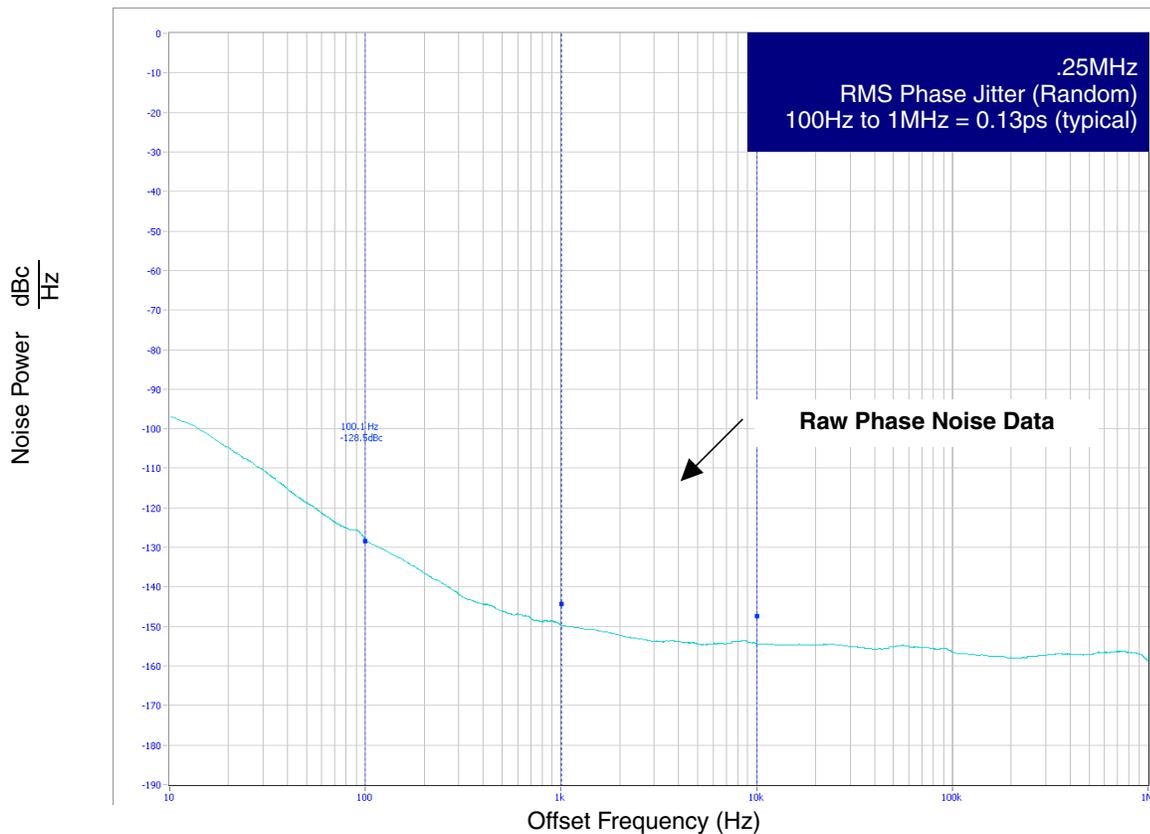
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

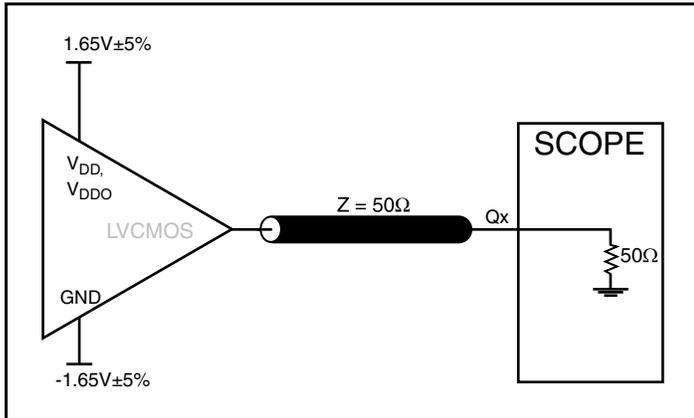
Typical Phase Noise at 25MHz (2.5V Core/2.5V Output)



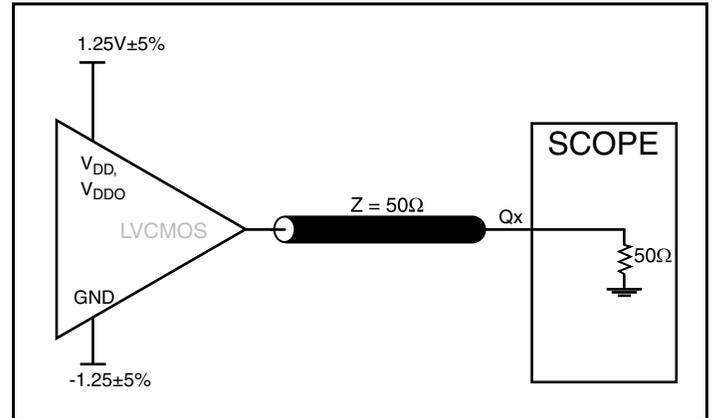
Typical Phase Noise at 25MHz (3.3V Core/3.3V Output)



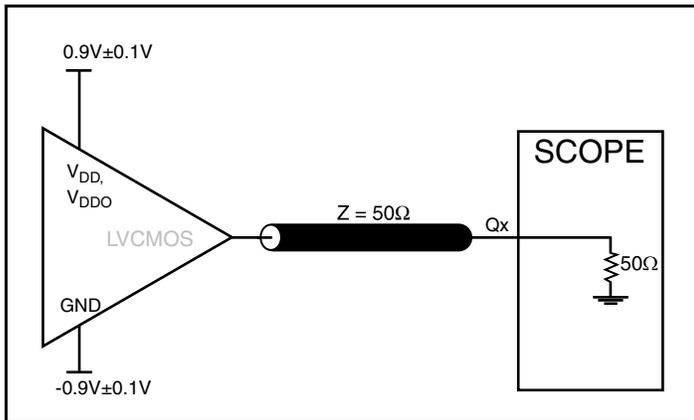
Parameter Measurement Information



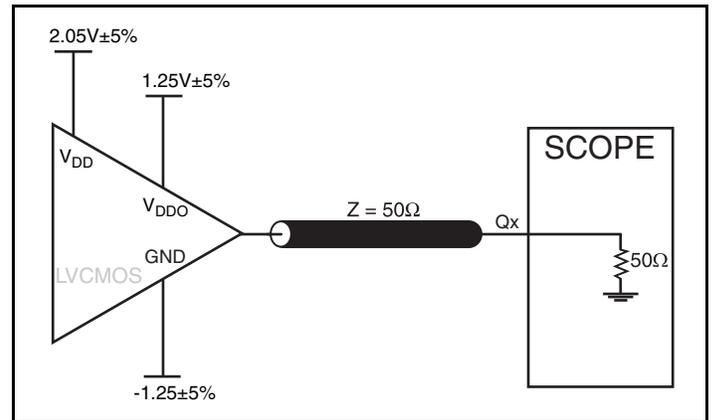
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



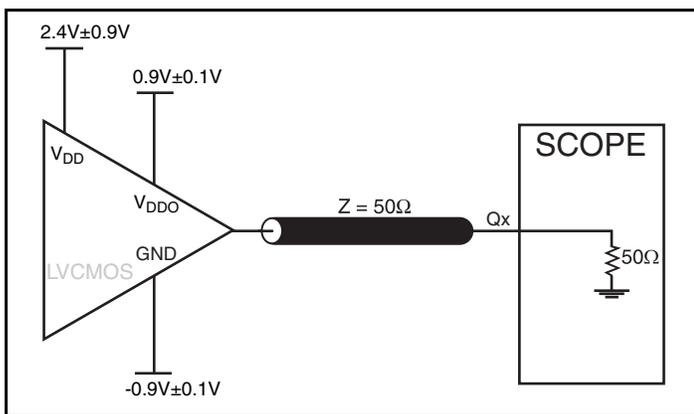
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



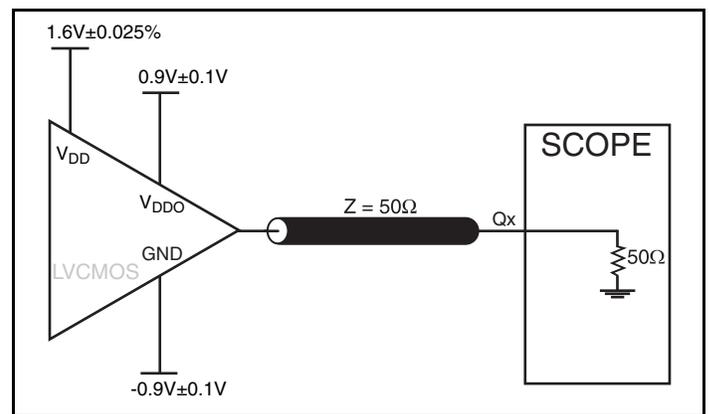
1.8V Core/1.8V LVCMOS Output Load AC Test Circuit



3.3V Core/2.5V LVCMOS Output Load AC Test Circuit

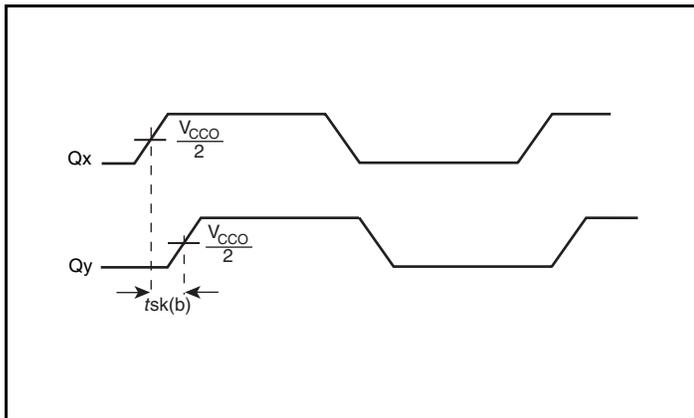


3.31.8V Core/1.8V LVCMOS Output Load AC Test Circuit

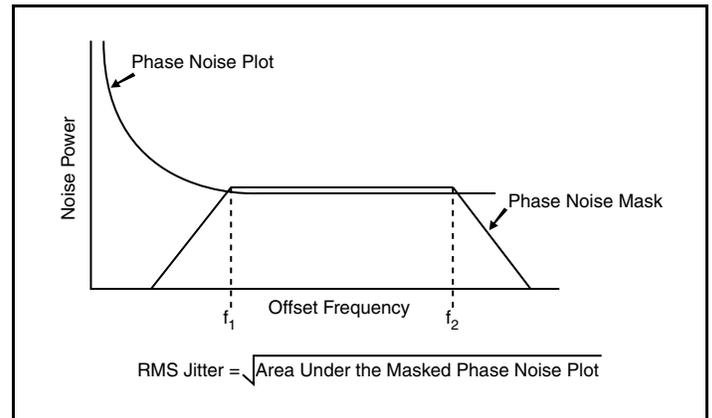


2.5V Core/1.8V LVCMOS Output Load AC Test Circuit

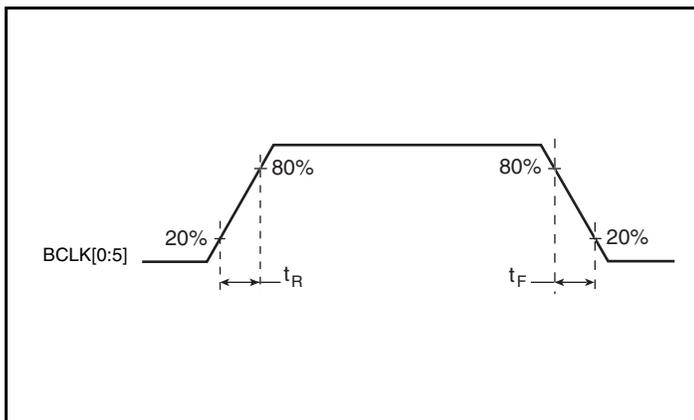
Parameter Measurement Information, continued



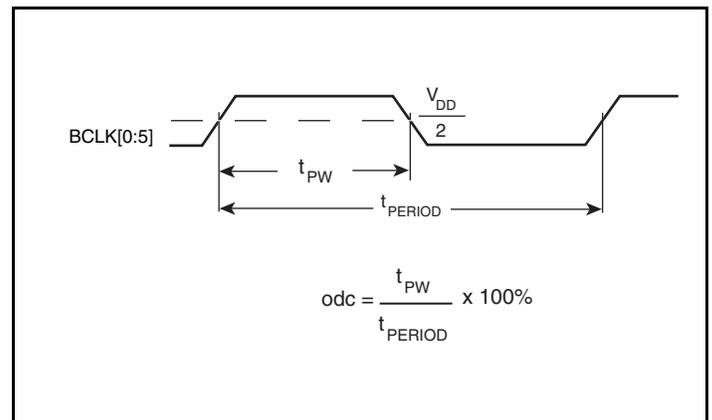
Output Skew



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Crystal Input Interface

Figure 2 shows an example of ICS83905 crystal interface with a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For a parallel crystal with loading capacitance $C_L = 18\text{pF}$, to start with, we suggest $C_1 = 15\text{pF}$ and $C_2 = 15\text{pF}$. These values may be slightly fine tuned further to optimize

the frequency accuracy for different board layouts. Slightly increasing the C1 and C2 values will slightly reduce the frequency. Slightly decreasing the C1 and C2 values will slightly increase the frequency. For the oscillator circuit below, R1 can be used, but is not required. For new designs, it is recommended that R1 not be used.

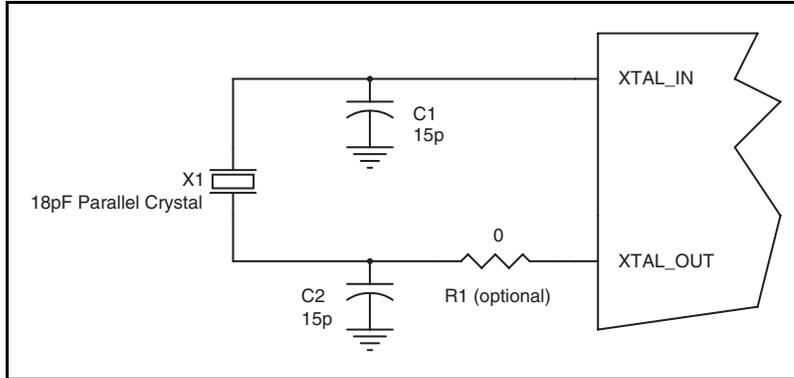


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 3. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals

the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω . This can also be accomplished by removing R1 and making R2 50Ω . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

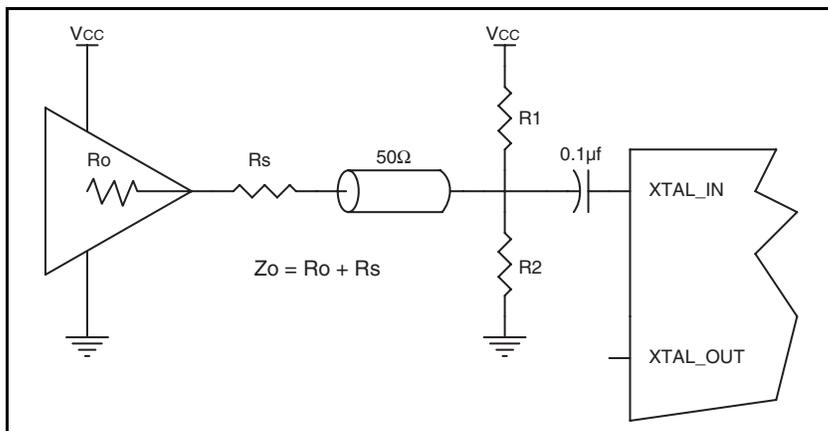


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

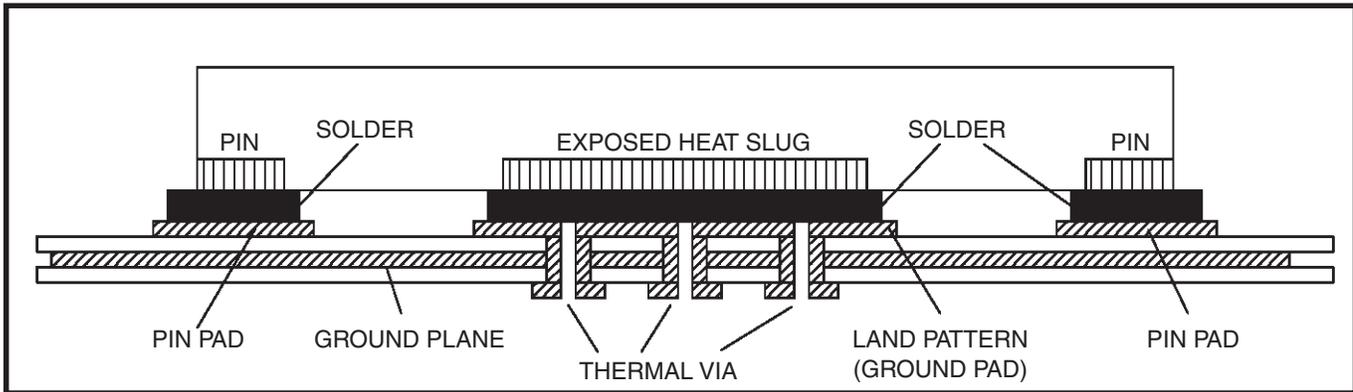


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

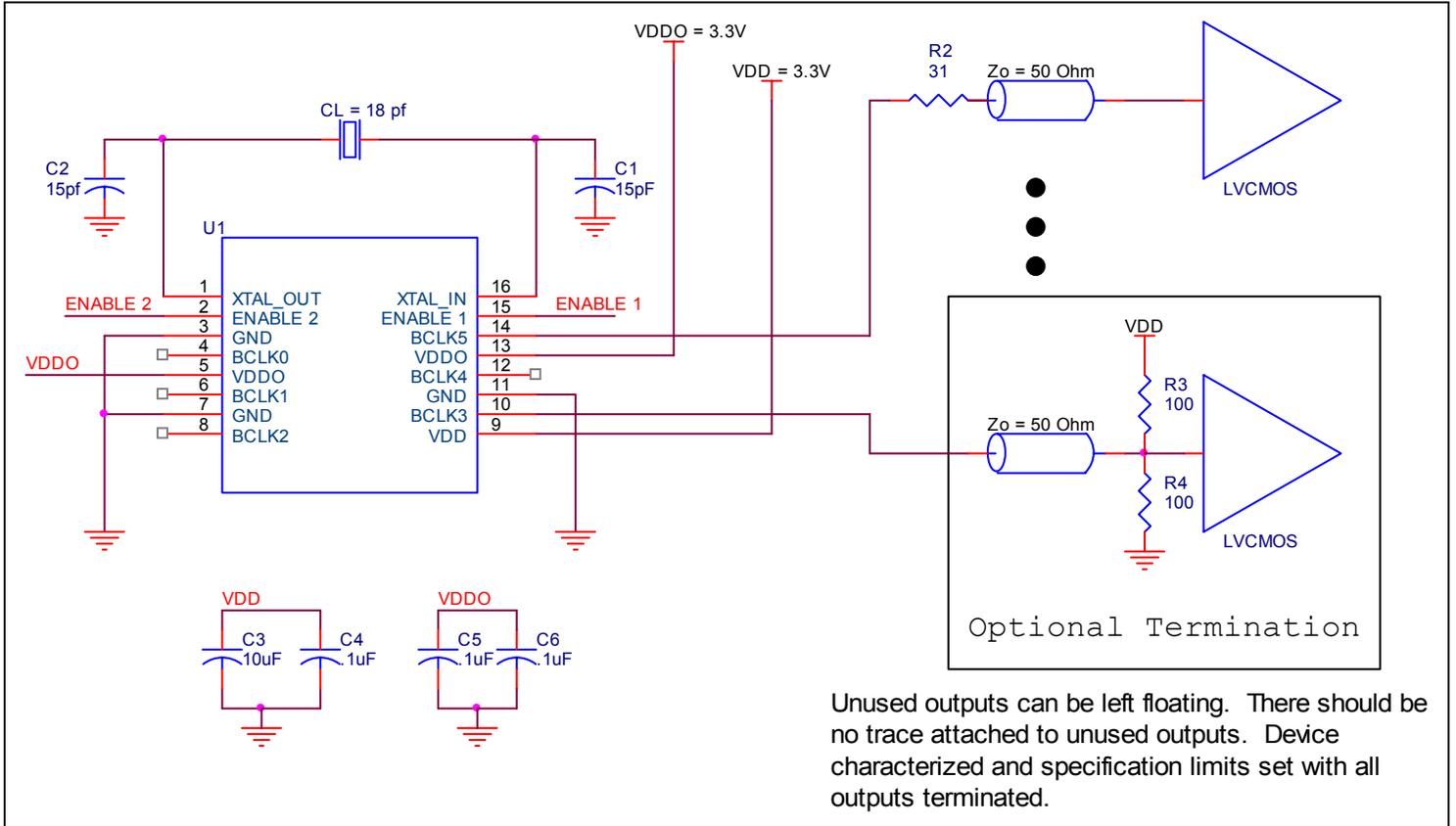
LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Layout Guideline

Figure 5 shows an example of ICS83905 applications schematic. In this example, the device is operated at $V_{DD} = 3.3V$ and $V_{DDO} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pins. The input is driven by an 18pF load resonant quartz crystal. The tuning capacitors (C1, C2) are fairly accurate, but minor

adjustments might be required. For the LVCMOS output drivers, two termination examples are shown in the schematic. For additional termination, examples are shown in the LVCMOS Termination Applications Note.



Unused outputs can be left floating. There should be no trace attached to unused outputs. Device characterized and specification limits set with all outputs terminated.

Figure 5. Schematic of Recommended Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS83905. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS83905 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD} + I_{DDO}) = 3.465V * (10mA + 5mA) = \mathbf{51.9mW}$
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
Output Current $I_{OUT} = V_{DD_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 7\Omega)] = \mathbf{30.4mA}$
- Power Dissipation on the R_{OUT} per LVCMOS output
Power (R_{OUT}) = $R_{OUT} * (I_{OUT})^2 = 7\Omega * (30.4mA)^2 = \mathbf{6.5mW \text{ per output}}$
- Total Power Dissipation on the R_{OUT}
Total Power (R_{OUT}) = $6.5mW * 6 = \mathbf{39mW}$

Dynamic Power Dissipation at 25MHz

$$\text{Power (25MHz)} = C_{PD} * \text{Frequency} * (V_{DD})^2 = 19pF * 25MHz * (3.465V)^2 = \mathbf{5.70mW \text{ per output}}$$

$$\mathbf{\text{Total Power (25MHz)} = 5.70mW * 6 = \mathbf{34.2mW}}$$

Total Power Dissipation

- Total Power**
= Power (core)_{MAX} + Total Power (R_{OUT}) + Total Power (25MHz)
= $51.98mW + 39mW + 34.2mW$
= **125.1mW**

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C .

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.125W * 100.3^\circ\text{C/W} = 82.5^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

| Meters per Second | θ_{JA} by Velocity | | |
|---|---------------------------|------------------------|------------------------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 100.3°C/W | 96.0°C/W | 93.9°C/W |

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

| θ_{JA} vs. Air Flow | | | |
|---|-----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 100.3°C/W | 96.0°C/W | 93.9°C/W |

Table 8B. θ_{JA} vs. Air Flow Table for a 16 Lead SOIC

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 78.8°C/W | 71.1°C/W | 66.2°C/W |

Table 8C. θ_{JA} vs. Air Flow Table for a 20 Lead VFQFN

| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 57.5°C/W | 50.3°C/W | 45.1°C/W |

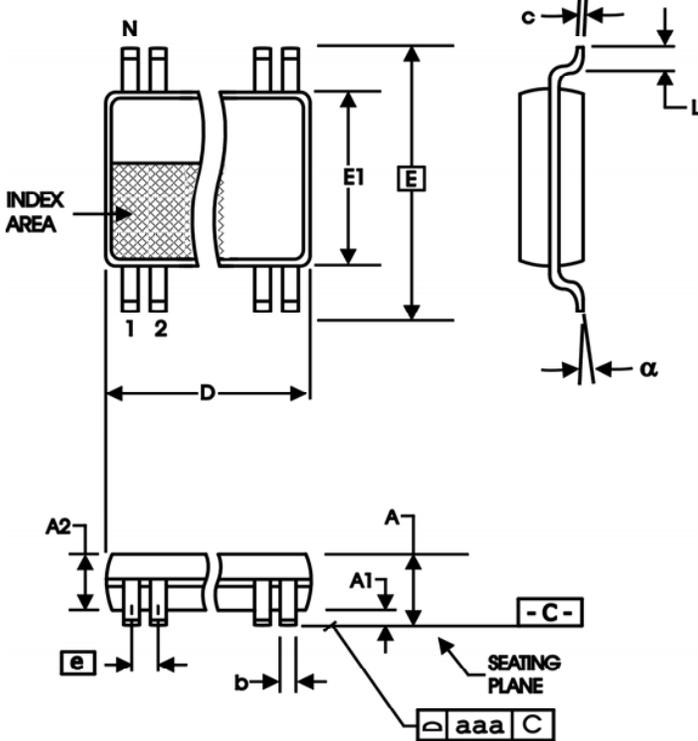
Transistor Count

The transistor count for ICS83905: 339

Pin compatible to MPC905

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP



Package Outline - M Suffix for 16 Lead SOIC

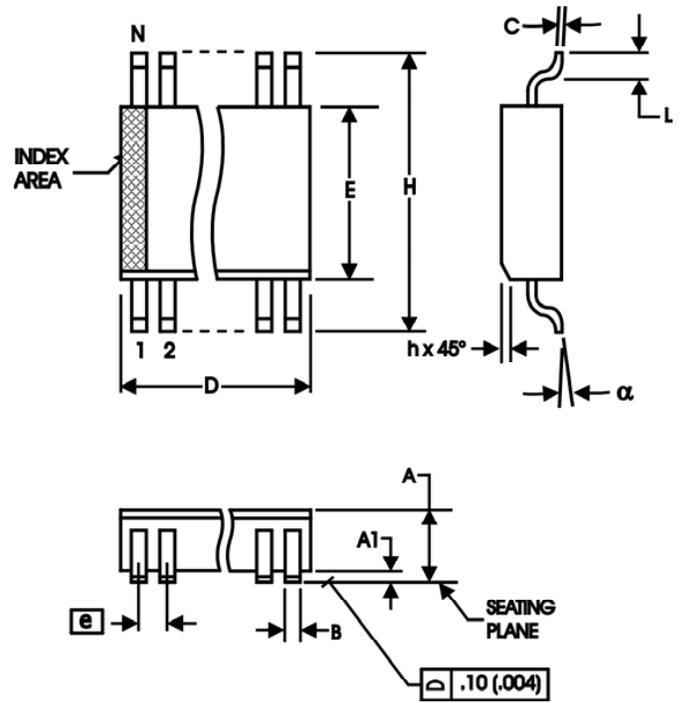


Table 9A. Package Dimensions for 16 Lead TSSOP

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 16 | |
| A | | 1.20 |
| A1 | 0.5 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 4.90 | 5.10 |
| E | 6.40 Basic | |
| E1 | 4.30 | 4.50 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

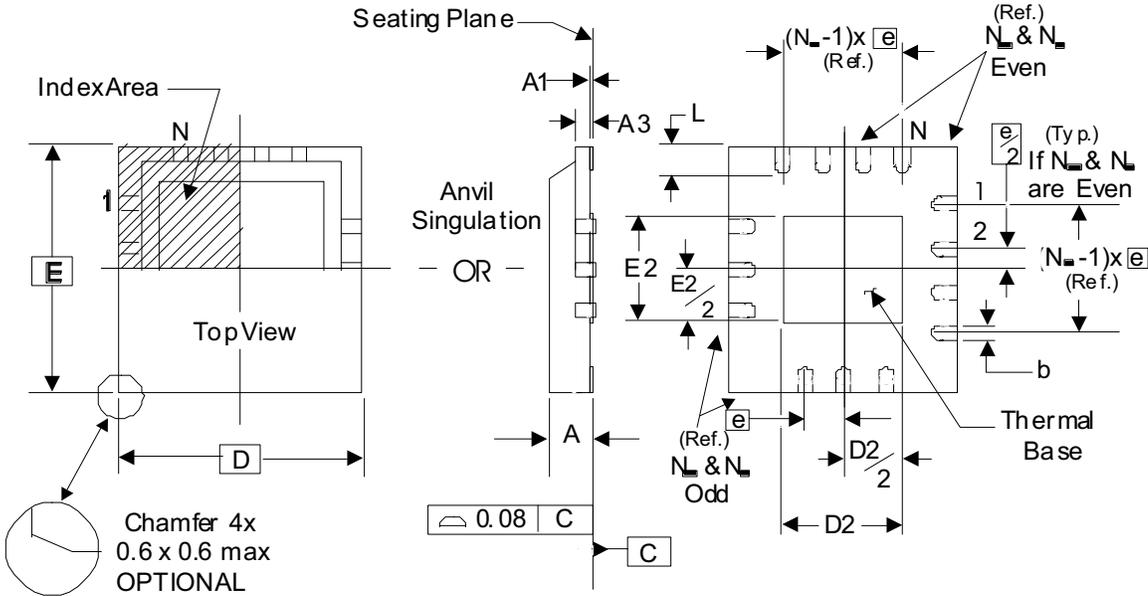
Table 9B. Package Dimensions for 16 Lead SOIC

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 16 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 9.80 | 10.00 |
| E | 3.80 | 4.00 |
| e | 1.27 Basic | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this

device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9C below.

Table 9C. Package Dimensions

| JEDEC Variation: VGGD-1/-5 All Dimensions in Millimeters | | | |
|---|------------|---------|---------|
| Symbol | Minimum | Nominal | Maximum |
| N | 20 | | |
| A | 0.80 | | 1.00 |
| A1 | 0 | | 0.05 |
| A3 | 0.25 Ref. | | |
| b | 0.18 | | 0.30 |
| N_D & N_E | 5 | | |
| D & E | 4.00 Basic | | |
| D2 & E2 | 1.95 | | 2.25 |
| e | 0.50 Basic | | |
| L | 0.35 | | 0.75 |

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------|---------------------------|--------------------|-------------|
| 83905AM | 83905AM | 16 Lead SOIC | Tube | 0°C to 70°C |
| 83905AMT | 83905AM | 16 Lead SOIC | 2500 Tape & Reel | 0°C to 70°C |
| 83905AMLF | 83905AML | "Lead-Free" 16 Lead SOIC | Tube | 0°C to 70°C |
| 83905AMLFT | 83905AML | "Lead-Free" 16 Lead SOIC | 2500 Tape & Reel | 0°C to 70°C |
| 83905AG | 83905AG | 16 Lead TSSOP | Tube | 0°C to 70°C |
| 83905AGT | 83905AG | 16 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |
| 83905AGLF | 83905AGL | "Lead-Free" 16 Lead TSSOP | Tube | 0°C to 70°C |
| 83905AGLFT | 83905AGL | "Lead-Free" 16 Lead TSSOP | 2500 Tape & Reel | 0°C to 70°C |
| 83905AK | 83905A | 20 Lead VFQFN | Tray | 0°C to 70°C |
| 83905AKT | 83905A | 20 Lead VFQFN | 2500 Tape & Reel | 0°C to 70°C |
| 83905AKLF | 3905AL | "Lead-Free" 20 Lead VFQFN | Tray | 0°C to 70°C |
| 83905AKLFT | 3905AL | "Lead-Free" 20 Lead VFQFN | 2500 Tape & Reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-----------|---------------------|--|---------|
| A | | 2 | Added Enable Timing Diagram. | 3/28/05 |
| B | T6A - T6F | 1 5 - 7 8 | Features Section - added RMS Phase Jitter bullet. AC Characteristics Tables - added RMS Phase Jitter specs. Added Phase Noise Plot. | 4/8/05 |
| B | T9 | 14 | Ordering Information Table - added TSSOP, non-LF part number. | 4/25/05 |
| B | | 11 12 | Added Crystal Input Interface in Application Section. Added Schematic layout. | 5/16/05 |
| B | | 3 11 13 | Absolute Maximum Ratings - corrected 20 lead VFQFN package Thermal Impedance. Added Recommendations for <i>Unused Input and Output Pins</i> . Corrected Theta JA Air Flow Table for 20 lead VFQFN. | 10/2/06 |
| B | T9 | 11 12 17 | Added <i>LVCMOS to XTAL Interface section</i> . Added <i>Thermal Release Path section</i> . AC Characteristics Table - added lead-free marking for 20 lead VFQFN package. | 7/9/07 |
| B | T7B - T7C | 3 12 14 16 | Absolute Maximum Ratings - updated TSSOP and VFQFN Thermal Impedance. Updated Thermal Release Path section. Updated TSSOP and VFQFN Thermal Impedance. Added note to VFQFN Package Outline. | 1/24/08 |
| B | | 15 | Added Power Considerations section. Converted datasheet format. | 7/20/09 |



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