() IDT.

2.5V LVDS 1:16 CLOCK BUFFER TERABUFFER™ II

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES ON OCTOBER 28, 2014

FEATURES:

- Guaranteed Low Skew < 25ps (max)
- Very low duty cycle distortion < 125ps (max)
- High speed propagation delay < 1.75ns (max)
- Up to 1GHz operation
- Selectable inputs
- · Hot insertable and over-voltage tolerant inputs
- 3.3V / 2.5V LVTTL, HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input interface
- · Selectable differential inputs to sixteen LVDS outputs
- Power-down mode
- 2.5V VDD
- Available in VFQFPN package
- use replacement part: 8516FYILF, (8T349316NLGI)

APPLICATIONS:

· Clock distribution

FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION:

The IDT5T93162.5V differential clock buffer is a user-selectable differential input to sixteen LVDS outputs. The fanout from a differential input to sixteen LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9316 can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

IDT5T9316

The IDT5T9316 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.



The IDT logo is a registered trademark of Integrated Device Technology, Inc. INDUSTRIAL TEMPERATURE RANGE

MARCH 20, 2014

PINCONFIGURATION



VFQFPN TOP VIEW Storage Temperature

Junction Temperature

Symbol Description Max Unit Vdd Power Supply Voltage -0.5 to +3.6 V Vı Input Voltage -0.5 to +3.6 V Output Voltage⁽²⁾ V Vo -0.5 to VDD +0.5

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

CAPACITANCE⁽¹⁾ (TA = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Тур.	Max.	Unit
CIN	Input Capacitance	_	_	3	pF

NOTE:

°C

°C

1. This parameter is measured at characterization but not tested

NOTES:

Tstg Tj

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

-65 to +150

150

2. Not to exceed 3.6V.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Тур.	Max.	Unit
TA	Ambient Operating Temperature	-40	+25	+85	°C
Vdd	Internal Power Supply Voltage	2.3	2.5	2.7	V

PINDESCRIPTION

Symbol	I/O	Туре	Description
A[1:2]	Ι	Adjustable ^(1,4)	Clock input. A[1:2] is the "true" side of the differential clock input.
Ā[1:2]	I	Adjustable ^(1,4)	Complementary clock inputs. $\overline{A}_{1:2}$ is the complementary side of A[1:2]. For LVTTL single-ended operation, $\overline{A}_{1:2}$ should be set to the desired toggle voltage for A[1:2]:
			3.3V LVTTL VREF = 1650mV
			2.5V LVTTL VREF = 1250mV
G1	I	LVTTL	Gate control for differential outputs Q1 and \overline{Q} 1 through Q8 and \overline{Q} 8. When \overline{G} 1 is LOW, the differential outputs are active. When \overline{G} 1 is HIGH, the differential outputs are asynchronously driven to the level designated by GL ⁽²⁾ .
G2	I	LVTTL	Gate control for differential outputs Q9 and \overline{Q} 9 through Q16 and \overline{Q} 16. When \overline{G} 2 is LOW, the differential outputs are active. When \overline{G} 2 is HIGH, the differential outputs are asynchronously driven to the level designated by GL ⁽²⁾ .
GL	I	LVTTL	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
Qn	0	LVDS	Clock outputs
Qn	0	LVDS	Complementary clock outputs
SEL	Ι	LVTTL	Reference clock select. When LOW, selects A2 and $\overline{A}2$. When HIGH, selects A1 and $\overline{A}1$.
PD	I	LVTTL	Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to VDD. Set HIGH for normal operation. ⁽³⁾
Vdd		PWR	Power supply for the device core and inputs
GND		PWR	Power supply return for all power
NC			No connect; recommended to connect to GND

NOTES:

1. Inputs are capable of translating the following interface standards:

Single-ended 3.3V and 2.5V LVTTL levels

Differential HSTL and eHSTL levels

Differential LVEPECL (2.5V) and LVPECL (3.3V) levels

Differential LVDS levels

Differential CML levels

2. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

3. It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting PD.

4. The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

INDUSTRIAL TEMPERATURE RANGE

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTL⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Тур. ⁽²⁾	Max	Unit		
Input Chara	Input Characteristics							
Ін	Input HIGH Current	Vdd = 2.7V	_	—	±5	μA		
lil	Input LOW Current	VDD = 2.7V	_	—	±5			
Vik	Clamp Diode Voltage	Vdd = 2.3V, IIN = -18mA	_	- 0.7	- 1.2	V		
Vin	DC Input Voltage		- 0.3	—	+3.6	V		
Vih	DC Input HIGH		1.7	—	_	V		
Vil	DC Input LOW		_	—	0.7	V		
Vthi	DC Input Threshold Crossing Voltage		_	Vdd /2	_	V		
Vref	Single-Ended Reference Voltage ⁽³⁾	3.3VLVTTL	_	1.65	_	V		
		2.5V LVTTL	-	1.25	—			

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Typical values are at VDD = 2.5V, +25°C ambient.

3. For A_[1:2] single-ended operation, \overline{A} _[1:2] is tied to a DC reference voltage.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR DIFFER-ENTIAL INPUTS⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Тур. ⁽²⁾	Max	Unit			
Input Charac	Input Characteristics								
Ін	Input HIGH Current	$V_{DD} = 2.7V$	—	—	±5	μA			
lıL	Input LOW Current	$V_{DD} = 2.7V$	—	—	±5				
Vik	Clamp Diode Voltage	Vdd = 2.3V, Iin = -18mA	—	- 0.7	- 1.2	V			
Vin	DC Input Voltage		- 0.3	—	+3.6	V			
Vdif	DC Differential Voltage ⁽³⁾		0.1	—	—	V			
Vсм	DC Common Mode Input Voltage ⁽⁴⁾		0.05	_	Vdd	V			

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Typical values are at VDD = 2.5V, +25°C ambient.

XDIF specifies the minimum input differential voltage (VTR - VCP) required for switching where VTR is the "true" input level and VCP is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
 VCM specifies the maximum allowable range of (VTR + VCP) /2.

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING RANGE FOR LVDS⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽²⁾	Max	Unit			
Output Char	Output Characteristics								
Vot(+)	Differential Output Voltage for the True Binary State		247	_	454	mV			
Vot(-)	Differential Output Voltage for the False Binary State		247	_	454	mV			
ΔV от	Change in VoT Between Complementary Output States		—	_	50	mV			
Vos	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V			
ΔVos	Change in Vos Between Complementary Output States		—	_	50	mV			
los	Outputs Short Circuit Current	Vout + and Vout - = 0V	—	12	24	mA			
losd	Differential Outputs Short Circuit Current	Vout + = Vout -	_	6	12	mA			

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Typical values are at VDD = 2.5V, TA = +25°C ambient.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
Vdif	Input Signal Swing ⁽¹⁾	1	V
Vx	Differential Input Signal Crossing Point ⁽²⁾	750	mV
Dн	Duty Cycle	50	%
Vthi	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
tr, tr	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
Vdif	Input Signal Swing ⁽¹⁾	1	V
Vx	Differential Input Signal Crossing Point ⁽²⁾	900	mV
Dн	Duty Cycle	50	%
Vthi	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
tr, tr	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL (2.5V) AND LVPECL (3.3V)

Parameter		Value	Units
Input Signal Swing ⁽¹⁾		732	mV
Differential Input Signal Crossing Point ⁽²⁾	LVEPECL	1082	mV
	LVPECL	1880	
Duty Cycle		50	%
Input Timing Measurement Reference Level ⁽³⁾		Crossing Point	V
Input Signal Edge Rate ⁽⁴⁾		2	V/ns
-	Input Signal Swing ⁽¹⁾ Differential Input Signal Crossing Point ⁽²⁾ Duty Cycle Input Timing Measurement Reference Level ⁽³⁾	Input Signal Swing ⁽¹⁾ Differential Input Signal Crossing Point ⁽²⁾ LVEPECL LVPECL Duty Cycle Input Timing Measurement Reference Level ⁽³⁾	Input Signal Swing ⁽¹⁾ 732 Differential Input Signal Crossing Point ⁽²⁾ LVEPECL 1082 LVPECL 1880 Duty Cycle 50 Input Timing Measurement Reference Level ⁽³⁾ Crossing Point

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point levels are specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVDS

Symbol	Parameter	Value	Units
Vdif	Input Signal Swing ⁽¹⁾	400	mV
Vx	Differential Input Signal Crossing Point ⁽²⁾	1.2	V
Dн	Duty Cycle	50	%
Vthi	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
tr, tr	Input Signal Edge Rate ⁽⁴⁾	2	V/ns

NOTES:

1. The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

AC DIFFERENTIAL INPUT SPECIFICATIONS⁽¹⁾

Symbol	Parameter	Min.	Тур.	Max	Unit
Vdif	AC Differential Voltage ⁽²⁾	0.1	—	3.6	V
Vix	Differential Input Crosspoint Voltage	0.05	_	Vdd	V
Vсм	Common Mode Input Voltage Range ⁽³⁾	0.05	_	Vdd	V
Vin	InputVoltage	- 0.3		+3.6	V

NOTES:

1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by VDIF has been met or exceeded.

2. VDIF specifies the minimum input voltage (VTR - VCP) required for switching where VTR is the "true" input level and VCP is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.

3. Vcm specifies the maximum allowable range of (VTR + VcP) /2.

POWER SUPPLY CHARACTERISTICS FOR LVDS OUTPUTS⁽¹⁾

Symbol	Parameter	Test Conditions	Тур.	Max	Unit
Iddq	Quiescent Vod Power Supply Current	VDD = Max., All Input Clocks = LOW ⁽²⁾	-	350	mA
		Outputs enabled			
Ітот	Total Power Vod Supply Current	Vdd = 2.7V., Freference clock = 1GHz	-	360	mA
IPD	Total Power Down Supply Current	PD = LOW	_	5	mA

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.

2. The true input is held LOW and the complementary input is held HIGH.

INDUSTRIAL TEMPERATURE RANGE

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE^(1,5)

Symbol	Parameter	Min.	Тур.	Max	Unit
Skew Parameters			-		
tsк(o)	Same Device Output Pin-to-Pin Skew ⁽²⁾	—	-	25	ps
tsк(p)	Pulse Skew ⁽³⁾	—	-	125	ps
tsk(pp)	Part-to-Part Skew ⁽⁴⁾	_	-	300	ps
Propagation Delay	y .		•		
t PLH	Propagation Delay A, A Crosspoint to Qn, Qn Crosspoint	_	1.25	1.75	ns
T PHL					
fo	Frequency Range ⁽⁶⁾	_	-	1	GHz
Output Gate Enab	e/Disable Delay		•		
T PGE	Output Gate Enable Crossing VTHI to Qn/Qn Crosspoint	_	_	3.5	ns
tpgd	Output Gate Disable Crossing VTHI to Qn/Qn Crosspoint Driven to GL Designated Level	_	_	3.5	ns
Power Down Tim	ing				
t PWRDN	\overline{PD} Crossing VTHI to Qn = VDD, \overline{Qn} = VDD	_	- 1	100	μS
t PWRUP	Output Gate Disable Crossing VTHI to Qn/Qn Driven to GL Designated Level	_	_	100	μS

NOTES:

1. AC propagation measurements should not be taken within the first 100 cycles of startup.

2. Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.

3. Skew measured is the difference between propagation delay times tPHL and tPLH of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.

4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical VDD levels and temperature.

5. All parameters are tested with a 50% input duty cycle.

6. Guaranteed by design but not production tested.

DIFFERENTIAL AC TIMING WAVEFORMS



Output Propagation and Skew Waveforms

NOTES:

1. Pulse skew is calculated using the following expression:

tsk(p) = | tphl - tplh |

- Note that the tPHL and tPLH shown above are not valid measurements for this calculation because they are not taken from the same pulse.
- 2. AC propagation measurements should not be taken within the first 100 cycles of startup.

IDT5T9316 2.5V LVDS1:16 CLOCK BUFFER TERABUFFER II

INDUSTRIAL TEMPERATURE RANGE



Differential Gate Disable/Enable Showing Runt Pulse Generation

NOTE:

1. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time their Gx signals to avoid this problem.



Power Down Timing

NOTES:

1. It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting PD.

2. The POWER DOWN TIMING diagram assumes that GL is HIGH.

3. It should be noted that during power-down mode, the outputs are both pulled to VDD. In the POWER DOWN TIMING diagram this is shown when Qn-Qn goes to VDIF = 0.

TEST CIRCUITS AND CONDITIONS



Test Circuit for Differential Input

DIFFERENTIAL INPUT TEST CONDITIONS

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
Vтні	Crossing of A and \overline{A}	V



Test Circuit for DC Outputs and Power Down Tests



Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
CL	O ⁽¹⁾	pF
	8(1,2)	
R∟	50	Ω

LVDS OUTPUT TEST CONDITION

NOTES:

1. Specifications only apply to "Normal Operations" test condition. The TIA/EIA specification load is for reference only.

2. The scope inputs are assumed to have a 2pF load to ground. TIA/EIA - 644 specifies 5pF between the output pair. With CL = 8pF, this gives the test circuit appropriate 5pF equivalent load.

RECOMMENDED LANDING PATTERN



NL 52 pin

NOTE: All dimensions are in millimeters.



REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
А		1	NRND - Not Recommended for New Designs	5/16/13
А		1	Product Discontinuation Notice - Last Time Buy Expires on October 28, 2014, PDN# CQ-13-02	11/27/13
А		1	Added new additional replacement part number	3/21/14

We've Got Your Timing Solution.



6024 Silver Creek Valley Road San Jose, CA 95138

Sales 800-345-7015 (inside USA) +408-284-8200 (outside USA) Fax: 408-284-2775 www.IDT.com/go/contactIDT Tech Support netcom@idt.com +480-763-2056

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners.

Copyright 2014 All rights reserved.