NOTICE OF REVISION (NOR) THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.	1. DATE *(YYMMDD)* 96-06-18	*Form Approved OMB No. 0704-0188*

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSED. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/ PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.

			2. PROCURING ACTIVITY NO.
			3. DODAAC
4. ORIGINATOR	b. ADDRESS *(Street, City, State, Zip Code)* Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5765	5. CAGE CODE 67268	6. NOR NO. 5962-R145-96
a. TYPED NAME *(First, Middle Initial, Last)*		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-90946**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
MICROCIRCUIT, DIGITAL, 32-BIT MICROPROCESSOR, FLOATING POINT UNIT AND MEMORY MANAGEMENT UNIT, MONOLITHIC SILICON	a. CURRENT C	b. NEW D	N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "B".
Revisions description column; add "Changes in accordance with NOR 5962-R145-96".
Revisions date column; add "96-06-18".
Revision level block; change from "C" to 'D".
Rev status of sheets; for sheet 1, 8 change from "C" to "D".

Sheet 8: Add the following:
Note: A terminal 1 identification mark shall be located in the index corner. However, terminal 1 shall be located on the first side clockwise from the index corner and is the terminal in the center of the side. Terminal numbers shall increase in a counterclockwise direction when viewed from the top (See figure 2).

Change status of revision level to "D".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME *(First, Middle Initial, Last)*
DESC-ELD	Monica L. Poelking

d. TITLE	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)*
Chief, Custom Microelectronics	Monica L. Poelking	96-06-18

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)*
DESC-ELD	Thomas M. Hess	96-06-18

NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE *(YYMMDD)* 93-11-04

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME (First, Middle Initial, Last)

b. ADDRESS *(Street, City, State, Zip Code)*
Defense Electronics Supply Center
1507 Wilmington Pike
Dayton, OH 45444-5765

5. CAGE CODE 67268

7. CAGE CODE 67268

6. NOR NO. 5962-R012-96

8. DOCUMENT NO. **5962-90946**

9. TITLE OF DOCUMENT
MICROCIRCUIT, DIGITAL, 32-BIT MICROPROCESSOR, FLOATING POINT UNIT AND MEMORY MANAGEMENT UNIT, MONOLITHIC SILICON

10. REVISION LETTER

a. CURRENT B

b. NEW C

11. ECP NO.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "C".
Revisions description column; add "Changes in accordance with NOR 5962-R012-94".
Revisions date column; add "93-11-04".
Revision level block; add "C".
Rev status of sheets; For sheets 1, 13, and 14 add "C".

Sheet 13: Figure 2. Terminal connections:

Change signal pin# 1 from:BE_0 to: $\overline{BE}_0$.

Change signal pin# 2 from: BE_3 to:$\overline{BE}_3$.

Change signal pin# 3 from: READY to: $\overline{READY}$.

Change signal pin# 4 from: BE_1 to: $\overline{BE}_1$.

Change signal pin# 6 from: DT/R to:DT/$\overline{R}$

Change signal pin# 8 from: W/R to: W/$\overline{R}$.

Change signal pin# 13 from: ALE to: $\overline{ALE}$.

Change signal pin # 15 from: ADS to: $\overline{ADS}$.

Revison level block; add"C".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT
DESC-ECC

c. TYPED NAME *(First, Middle Initial, Last)*
Monica L. Poelking

d. TITLE
Chief, Custom Microelectronics

e. SIGNATURE
Monica L. Poelking

f. DATE SIGNED *(YYMMDD)* 93/11/04

15a. ACTIVITY ACCOMPLISHING REVISION
DESC-ECC

b. REVISION COMPLETED *(Signature)*
Jeffery Tunstall

c. DATE SIGNED *(YYMMDD)* 93/11/04

DD Form 1695, APR 92 *Previous editions are obsolete.*

10. Description of Revision- Continued.

Change signal pin # 28 from: BADAC to: $\overline{\text{BACDC}}$.
Change signal pin # 56 from: LAD_1 to LAD_0.

Change signal pin # 58 from: INT_3 to $\overline{INT}_3$.

Change signal pin # 75 from: INT_0 to $\overline{INT}_0$.

Change signal pin # 160 from: LOCK to $\overline{LOCK}$.

Change signal pin # 161 from: FAIL to $\overline{FAIL}$.

Change signal pin # 162 from: DEN to $\overline{DEN}$.

Change signal pin # 163 from: BE to $\overline{BE}_2$.

Revision level block; add "C".

Sheet 14: Figure 2. Terminal connections:

Change signal pin # 1 from: BE_0 to: $\overline{BE}_0$.

Change signal pin # 2 from: BE_3 to: $\overline{BE}_3$.

Change signal pin # 3 from: READY to: $\overline{READY}$.

Change signal pin # 4 from: BE_1 to: $\overline{BE}_1$.

Change signal pin # 6 from:DT/R to: DT/$\overline{R}$.

Change signal pin # 8 from: W/R to: W/$\overline{R}$.

Change signal pin # 13 from: ALE to: $\overline{ALE}$.

Change signal pin # 15 from: ADS to: $\overline{ADS}$.

Change signal pin # 28 from: BADAC to: $\overline{BADAC}$.

Change signal pin # 56 from: LAD_1 to:LAD_0.

Change signal pin # 58 from: INT_3 to: $\overline{INT}_3$.

Change signal pin # 75 from: INT_0 to: $\overline{INT}_0$.

Change signal pin # 160 from: LOCK to: $\overline{LOCK}$.

Change signal pin # 161 from: FAIL to: $\overline{FAIL}$.

Change signal pin # 162 from: DEN to: $\overline{DEN}$.

Change signal pin # 163 from: BE to: $\overline{BE}_2$.

Revision level block; add "C".

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y, correct associated paragraphs and tables. Editorial changes throughout.	92-06-24	Tim Noh
B	Add device 04, 05, 06. Editorial changes throughout.	93-02-12	Monica Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
Tim Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
91/05/30

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, 32-BIT MICROPROCESSOR, FLOATING POINT UNIT AND MEMORY MANAGEMENT UNIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-90946**

SHEET 1 OF 32

DESC FORM 193
JUL 91

5962-E096-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	90946	01	M	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
_____ Drawing number _____/						

1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	80960MC-16	32-bit microprocessor with floating point and MMU	16 MHz
02	80960MC-20	32-bit microprocessor with floating point and MMU	20 MHz
03	80960MC-25	32-bit microprocessor with floating point and MMU	25 MHz
04	80960XA-16	32-bit microprocessor with floating point and MMU	16 MHz 1/
05	80960XA-20	32-bit microprocessor with floating point and MMU	20 MHz 1/
06	80960XA-25	32-bit microprocessor with floating point and MMU	25 MHz 1/

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	P-AF (132-pin, 1.480" x 1.480" x .345"), pin grid array package
Y	See figure 1 (164-terminal, 1.140" x 1.140" x .115"), leaded chip carrier with unformed leads.

1/ Devices 04, 05 and 06 have a 33rd tag bit to distinguish data from object pointer.

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/

Storage temperature range	-65°C to +150°C
Voltage on any pin with respect to ground	-0.5 V to V_{CC} +0.5 V
Power dissipation (P_D)	2.6 W
Lead temperature (soldering, 10 seconds)	+275°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Case Y	8°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	4.75 V dc to 5.25 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input low voltage	V_{IL}		1,2,3	All	2/ -0.3	+0.8	V
Input high voltage	V_{IH}				2.0	2/ V_{CC} +0.3	
CLK2 input low voltage	V_{CL}				-0.3	+0.8	
CLK2 input high voltage	V_{CH}				0.55 V_{CC}	V_{CC} +0.3	
Output low voltage	V_{OL}	Address/data = 4.0 mA Control = 5.0 mA Open-drain outputs = 25 mA				0.45	
Output high voltage 3/	V_{OH}	Address/data = -1.0 mA Control = -0.9 mA ALE = -5.0 mA			2.4		
Power supply current	I_{CC}	$V_{CC} = V_{CC}$ Max 16 MHz 20 MHz 25 MHz		01,04 02,05 03,06		375 420 480	mA
Input leakage current	I_{LI}	$V_{IN} = V_{CC}$ max		All	0	+15	µA
		$V_{IN} = 0.0$ V			0	-15	
Output leakage current	I_{LO}	$V_{OUT} = V_{CC}$ max			0	+15	
		$V_{OUT} = 0.0$ V			0	-15	
Input and clock capacitance	C_{IN}, C_{CLK}	f_c = 1 MHz see 4.4.1c	4			10	pF
I/O or output capacitance	C_{OUT}					12	
Functional testing		See 4.4.1b	7,8				
Processor clock period	T_1	$V_{IN} = 1.5$ V	9,10,11	01,04 02,05 03,06	31.25 25 20	125 125 125	ns
Processor clock low time	T_2	$V_{IL} = 1.0$ V		01,04 02,05 03,06	8 6 5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Processor clock high time	T_3	V_{IH} = 2.55 V	9,10,11	01,04 02,05 03,06	8 6 5		ns
Processor clock fall time 2/	T_4	V_{IN} = 90% to 10% point		All		10	
Processor clock rise time 2/	T_5	V_{IN} = 10% to 90% point		All		10	
Output valid delay	T_6	C_L = 100 pF (LAD) C_L = 75 pF (controls)		01,04	2	25	
		C_L = 60 pF (LAD) C_L = 50 pF (controls)		02,05 03,06	2 2	20 19	
Holda output valid delay	T_{6h}	C_L = 75 pF		01,04 05,06	4	31	
		C_L = 50 pF		02 03	4 4	26 24	
$\overline{ALE}$ width	T_7	C_L = 75 pF		01,04	15		
		C_L = 50 pF		02,05 03,06	12 12		
$\overline{ALE}$ invalid delay 2/ 4/	T_8	C_L = 75 pF		01,04	0	20	
		C_L = 50 pF		02,05 03,06	0 0	20 20	
Output float delay 2/ 4/	T_9	C_L = 100 pF (LAD) C_L = 75 pF (controls)		01,04	2	20	
		C_L = 60 pF (LAD) C_L = 50 pF (controls)		02,05 03,06	2 2	20 19	
Holda output float delay	T_{9h}	C_L = 75 pF		01,04 05,06	4	20	
		C_L = 50 pF		02 03	4	20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input setup 1 5/	T_{10}		9,10,11	All	3		ns
Input hold 5/	T_{11}			All	5		
Hold input hold	T_{11h}	C_L = 50 pF		All	4		
Input setup 2	T_{12}			01,04 02,05 03,06	8 7 7		
Setup to $\overline{ALE}$ inactive	T_{13}	C_L = 100 pF (LAD) C_L = 75 pF (controls)		01,04	10		
		C_L = 60 pF (LAD) C_L = 50 pF (controls)		02,05 03,06	10 8		
Hold after $\overline{ALE}$ inactive	T_{14}	C_L = 100 pF (LAD) C_L = 75 pF (controls)		01,04	8		
		C_L = 60 pF (LAD) C_L = 50 pF (controls)		02,05 03,06	8 8		
Reset hold	T_{15}			All	3		
Reset setup	T_{16}			All	5		
Reset width	T_{17}	41 CLK2 periods minimum		01,04 02,05 03,06	1281 1025 820		

1/ All testing to be performed using worst-case test conditions. For all devices V_{CC}: $4.75 \le V_{CC} \le 5.25$ V
2/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.
3/ Not measured on open-drain outputs.
4/ A float condition occurs when the maximum output current becomes less than I_{LO}.
5/ IAC/INT0, INT1, INTR, INT3, can be asynchronous.

Case Y

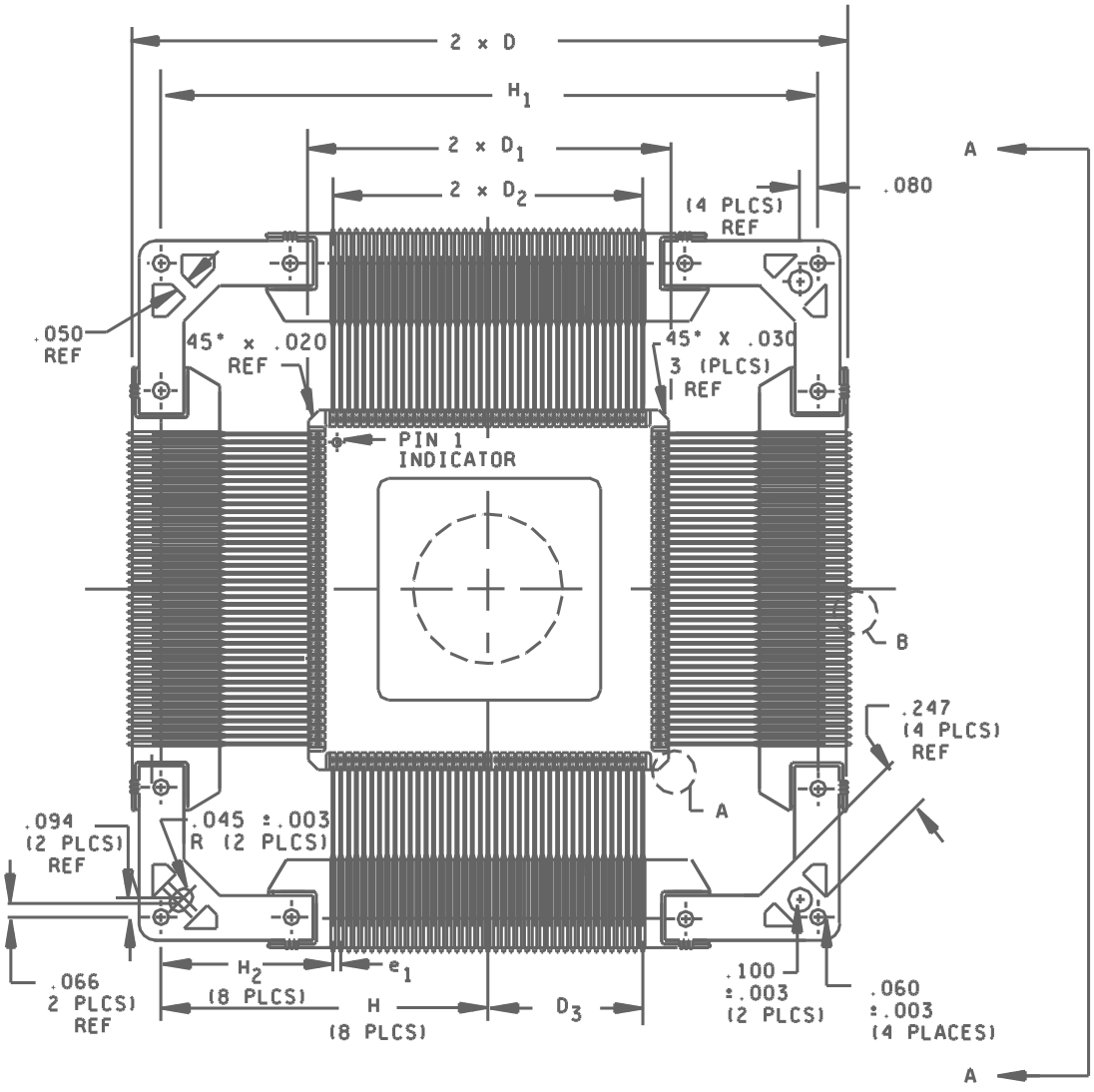
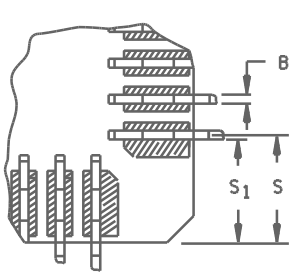


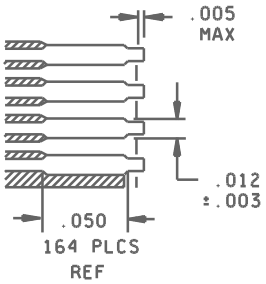
FIGURE 1. Case outline.

STANDARD MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**5962-90946**
		REVISION LEVEL B	SHEET **8**

Case Y

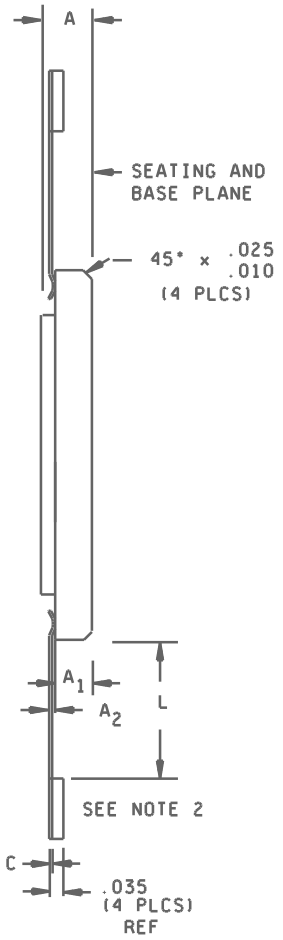


DETAIL A



DETAIL B

Inches	mm
.003	0.08
.005	0.13
.010	0.25
.012	0.30
.025	0.64
.035	0.89
.050	1.27



DETAIL A-A

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.088	.115	2.23	2.92
A_1	.078	.094	1.98	2.39
A_2	.006	.012	0.15	0.30
B	.007	.010	0.18	0.25
C	.004	.006	0.10	0.15
D	2.500	2.520	63.50	64.01
D_1	1.120	1.140	28.45	28.96
D_2	1.00 BASIC		25.40 BASIC	
D_3	.500 BASIC		12.70 BASIC	
e_1	.023	.027	0.58	0.69
H	1.150 BASIC		29.21 BASIC	
H_1	2.30 BASIC		58.42 BASIC	
H_2	.650 BASIC		16.51 BASIC	
L	.365	.395	9.27	10.03
N	164 TERMINALS			
S	.060	.080	1.52	2.03
S_1	.060	.076	1.52	1.93

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbols B and C dimensions shall be increased by .002 inch when solder coat is added.

FIGURE 1. Case outline - Continued.

Case X

Devices 01, 02, 03

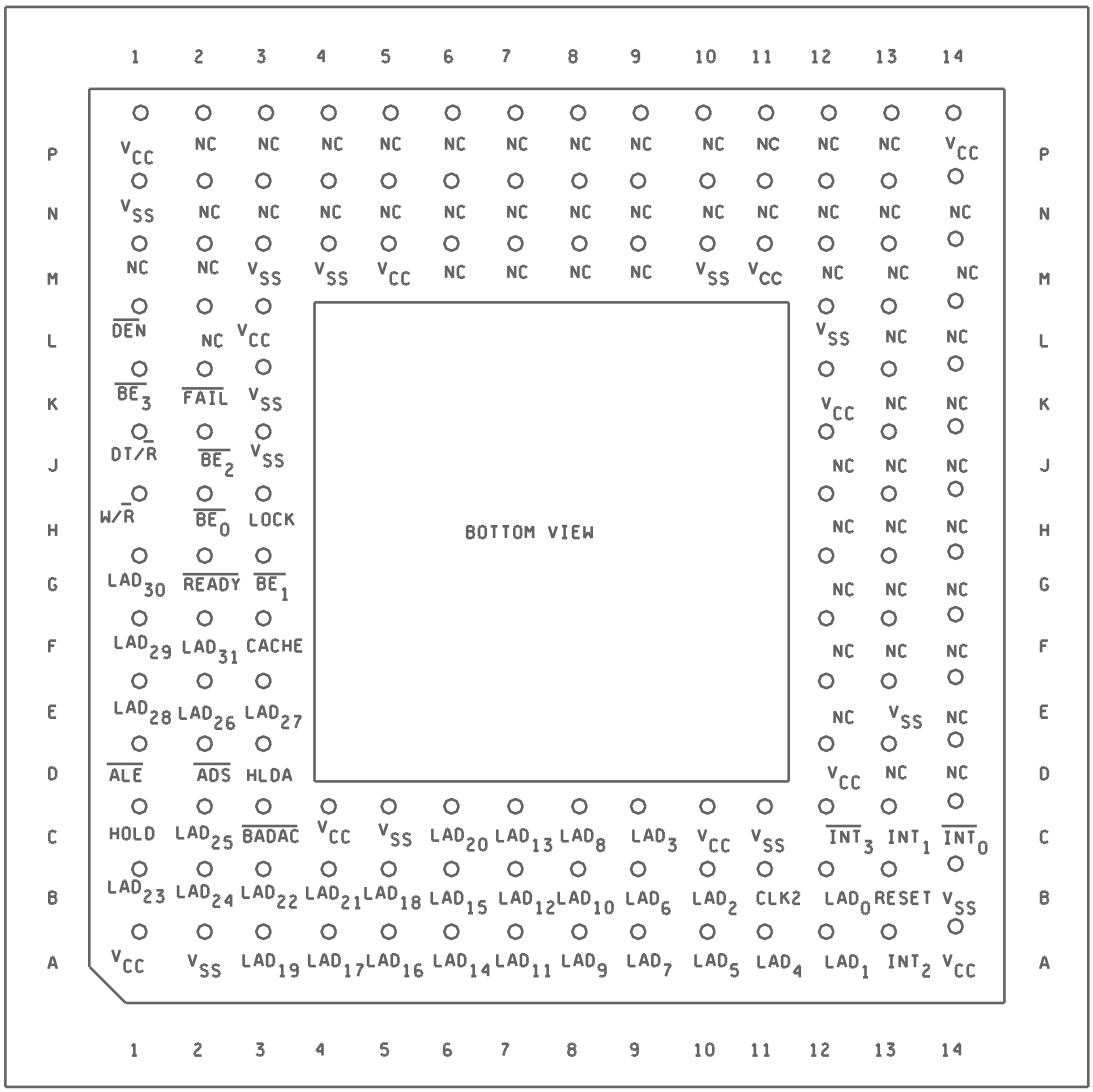


FIGURE 2. Terminal connections.

Case X

Devices 04, 05, 06

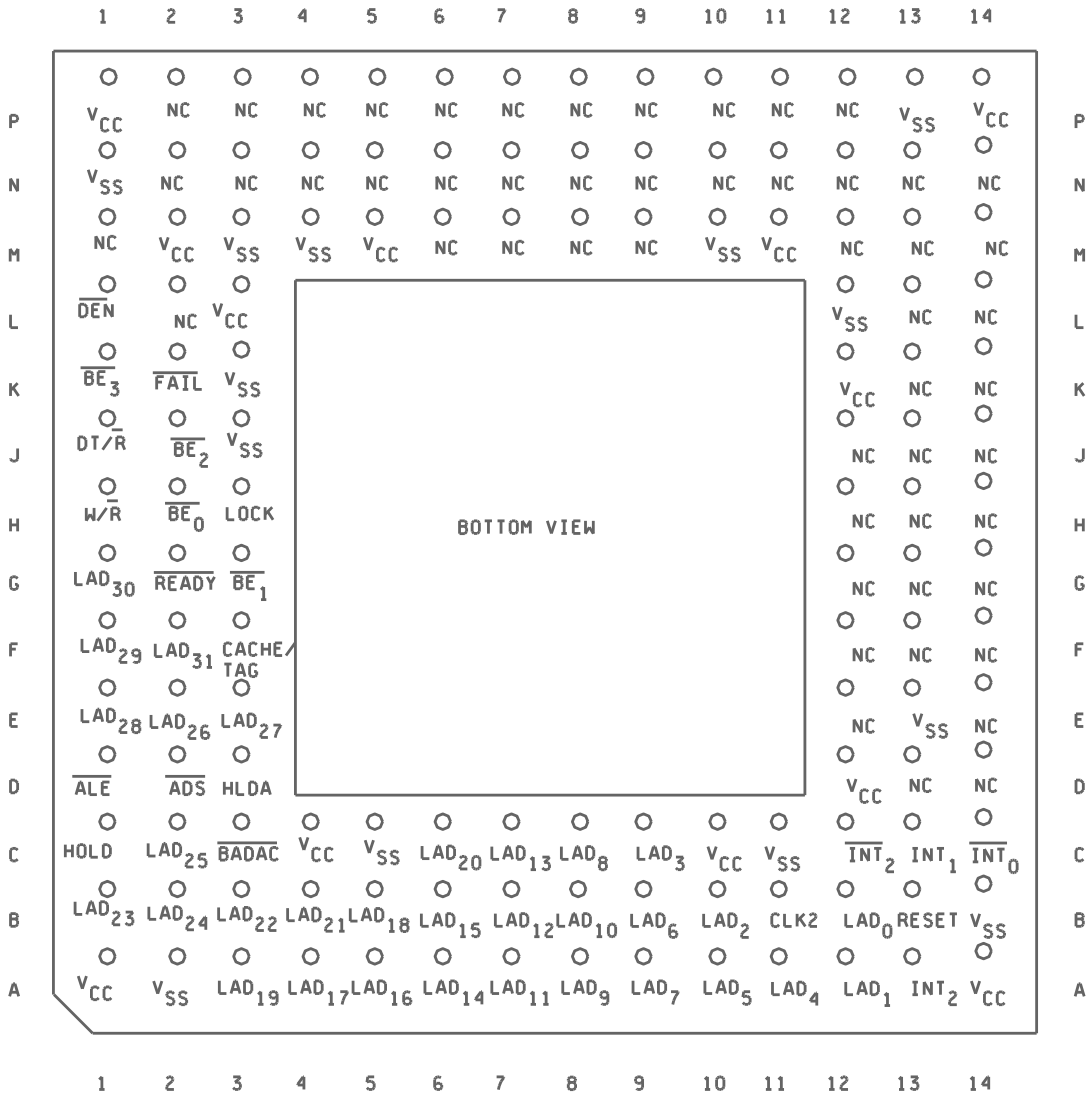
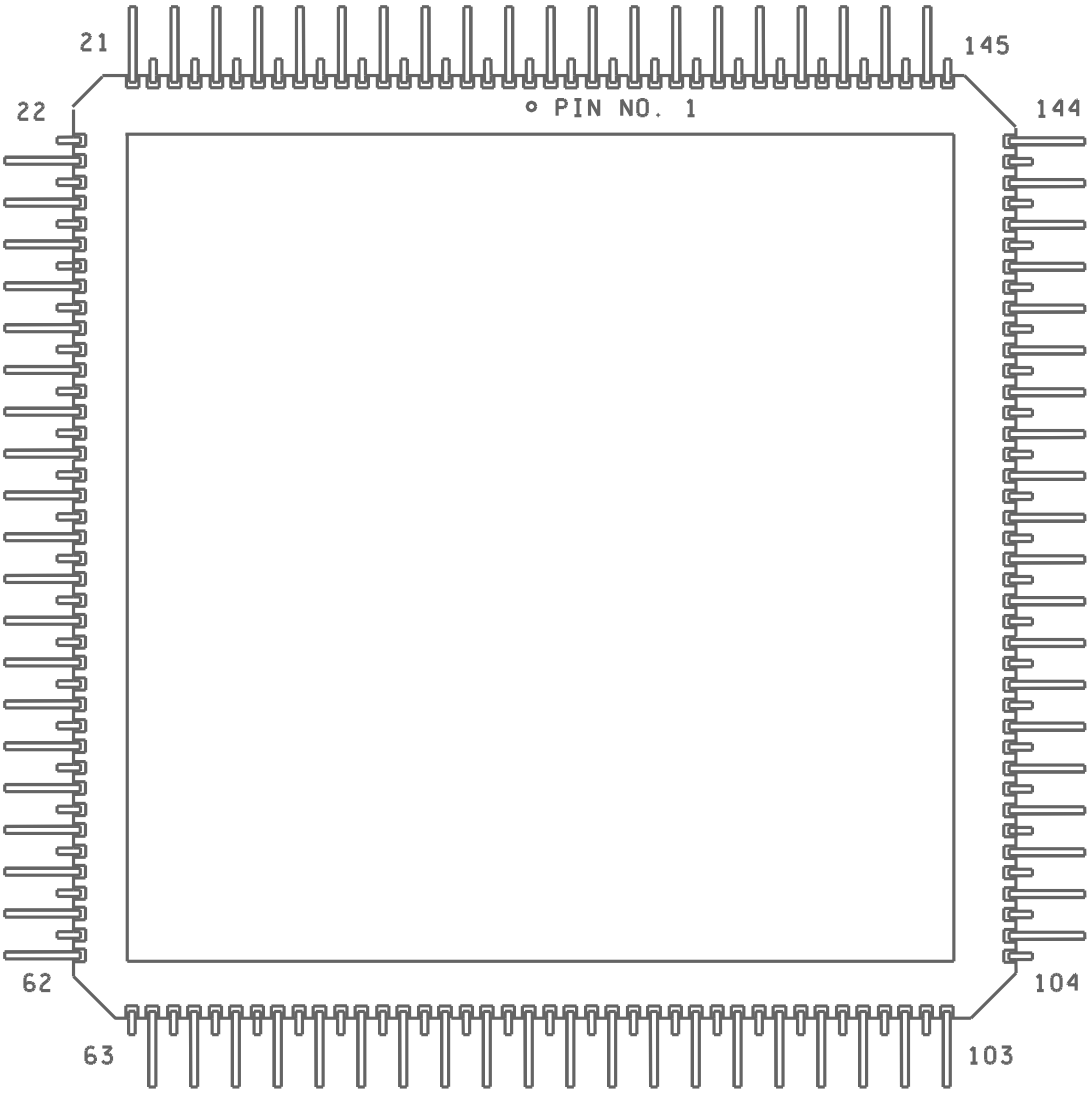


FIGURE 2. Terminal connections - Continued.

Case Y

All devices



NOTE: Staggered pin arrangement is shown for clarity only. Actual package has pins of equal length.

FIGURE 2. Terminal connections - Continued.

Case Y

Devices 01, 02, 03

Pin	Signal	Pin	Signal	Pin	Signal	pin	Signal
1	BE_0	42	LAD_{11}	83	NC	124	NC
2	BE_3	43	LAD_{12}	84	V_{CC}	125	V_{SS}
3	READY	44	LAD_9	85	NC	126	V_{CC}
4	BE_1	45	LAD_{10}	86	NC	127	NC
5	CACHE	46	LAD_7	87	V_{SS}	128	NC
6	DT/R	47	LAD_8	88	NC	128	NC
7	LAD_{31}	48	LAD_5	89	NC	130	NC
8	W/R	49	LAD_6	90	NC	131	NC
9	LAD_{29}	50	LAD_4	91	NC	132	NC
10	LAD_{30}	51	LAD_1	92	NC	133	NC
11	LAD_{27}	52	CLK_2	93	NC	134	NC
12	LAD_{28}	53	INT_2	94	NC	135	NC
13	ALE	54	LAD_3	95	NC	136	NC
14	LAD_{26}	55	LAD_2	96	NC	137	NC
15	ADS	56	LAD_1	97	NC	138	NC
16	HLDA	57	RESET	98	NC	139	NC
17	NC	58	INT_3	99	NC	140	NC
18	V_{SS}	59	INT_1	100	V_{CC}	141	NC
19	V_{CC}	60	V_{SS}	101	NC	142	NC
20	V_{SS}	61	V_{CC}	102	NC	143	NC
21	V_{CC}	62	V_{SS}	103	V_{SS}	144	NC
22	V_{CC}	63	V_{CC}	104	NC	145	NC
23	V_{SS}	64	V_{SS}	105	NC	146	NC
24	V_{CC}	65	V_{CC}	106	NC	147	NC
25	V_{SS}	66	V_{SS}	107	NC	148	NC
26	V_{CC}	67	V_{CC}	108	NC	149	NC
27	HOLD	68	NC	109	NC	150	NC
28	BADAC	69	NC	110	NC	151	NC
29	LAD_{25}	70	NC	111	NC	152	NC
30	LAD_{24}	71	NC	112	NC	153	V_{SS}
31	LAD_{23}	72	NC	113	NC	154	V_{CC}
32	LAD_{21}	73	NC	114	NC	155	NC
33	LAD_{22}	74	NC	115	NC	156	NC
34	LAD_{19}	75	INT_0	116	NC	157	NC
35	LAD_{20}	76	NC	117	NC	158	V_{SS}
36	LAD_{17}	77	NC	118	NC	159	NC
37	LAD_{18}	78	NC	119	V_{SS}	160	LOCK
38	LAD_{16}	79	NC	120	V_{CC}	161	FAIL
39	LAD_{15}	80	NC	121	NC	162	DEN
40	LAD_{14}	81	NC	122	NC	163	BE
41	LAD_{13}	82	NC	123	NC	164	V_{SS}

FIGURE 2. Terminal connections - Continued.

Case Y

Devices 04, 05, 06

Pin	Signal	Pin	Signal	Pin	Signal	pin	Signal
1	BE_0	42	LAD_{11}	83	NC	124	NC
2	BE_3	43	LAD_{12}	84	V_{CC}	125	V_{SS}
3	READY	44	LAD_9	85	NC	126	V_{CC}
4	BE_1	45	LAD_{10}	86	NC	127	NC
5	CACHE/TAG	46	LAD_7	87	V_{SS}	128	NC
6	DT/R	47	LAD_8	88	NC	128	NC
7	LAD_{31}	48	LAD_5	89	NC	130	NC
8	W/R	49	LAD_6	90	NC	131	NC
9	LAD_{29}	50	LAD_4	91	NC	132	NC
10	LAD_{30}	51	LAD_1	92	NC	133	NC
11	LAD_{27}	52	CLK_2	93	NC	134	NC
12	LAD_{28}	53	INT_2	94	NC	135	NC
13	ALE	54	LAD_3	95	NC	136	NC
14	LAD_{26}	55	LAD_2	96	NC	137	NC
15	ADS	56	LAD_1	97	NC	138	NC
16	HLDA	57	RESET	98	NC	139	NC
17	NC	58	INT_3	99	NC	140	NC
18	V_{SS}	59	INT_1	100	V_{CC}	141	NC
19	V_{CC}	60	V_{SS}	101	NC	142	NC
20	V_{SS}	61	V_{CC}	102	NC	143	NC
21	V_{CC}	62	V_{SS}	103	V_{SS}	144	NC
22	V_{CC}	63	V_{CC}	104	NC	145	NC
23	V_{SS}	64	V_{SS}	105	NC	146	NC
24	V_{CC}	65	V_{CC}	106	NC	147	NC
25	V_{SS}	66	V_{SS}	107	NC	148	NC
26	V_{CC}	67	V_{CC}	108	NC	149	NC
27	HOLD	68	NC	109	NC	150	NC
28	BADAC	69	NC	110	NC	151	NC
29	LAD_{25}	70	NC	111	NC	152	NC
30	LAD_{24}	71	NC	112	NC	153	V_{SS}
31	LAD_{23}	72	NC	113	NC	154	V_{CC}
32	LAD_{21}	73	NC	114	NC	155	NC
33	LAD_{22}	74	NC	115	NC	156	NC
34	LAD_{19}	75	INT_0	116	NC	157	NC
35	LAD_{20}	76	NC	117	NC	158	V_{SS}
36	LAD_{17}	77	NC	118	NC	159	NC
37	LAD_{18}	78	NC	119	V_{SS}	160	LOCK
38	LAD_{16}	79	NC	120	V_{CC}	161	FAIL
39	LAD_{15}	80	NC	121	NC	162	DEN
40	LAD_{14}	81	NC	122	NC	163	BE
41	LAD_{13}	82	NC	123	NC	164	V_{SS}

FIGURE 2. Terminal connections - Continued.

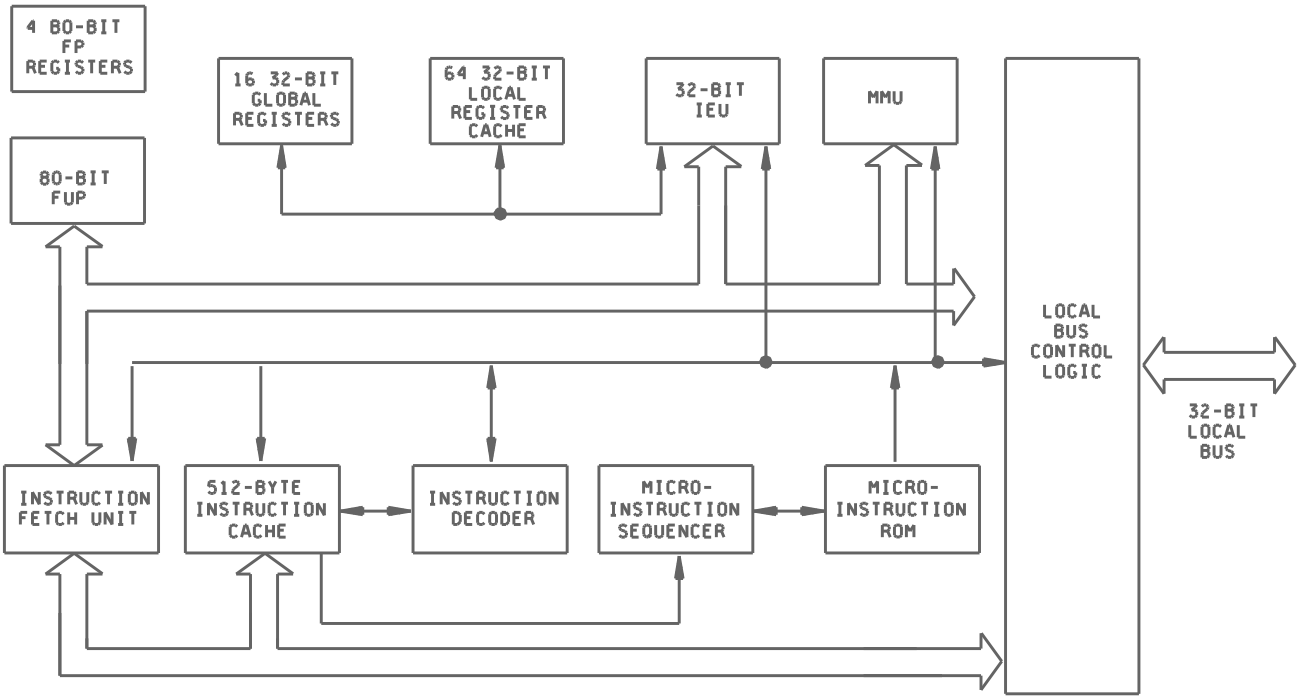


FIGURE 3. Functional block diagram.

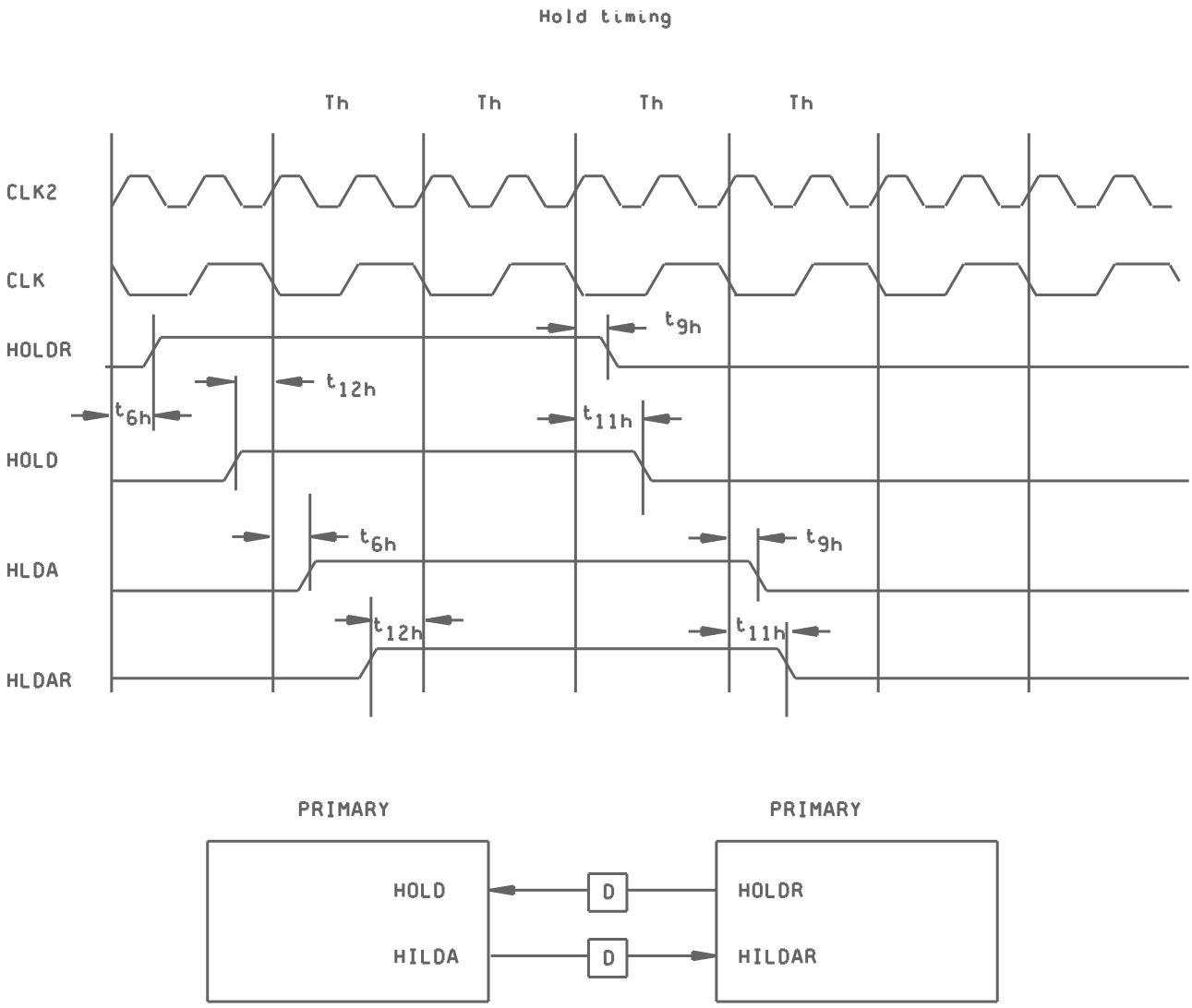
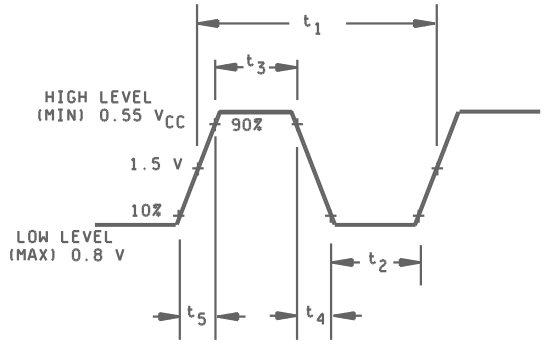
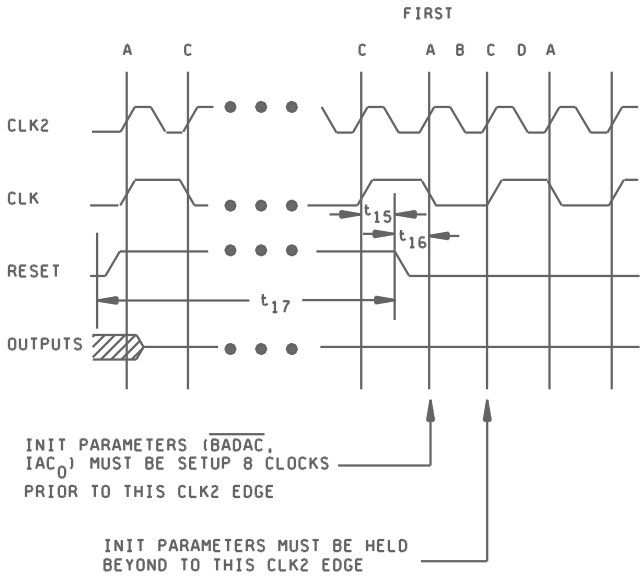


FIGURE 4. Switching waveforms and test circuit.

STANDARD MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE **A**		**5962-90946**
		REVISION LEVEL B	SHEET **16**



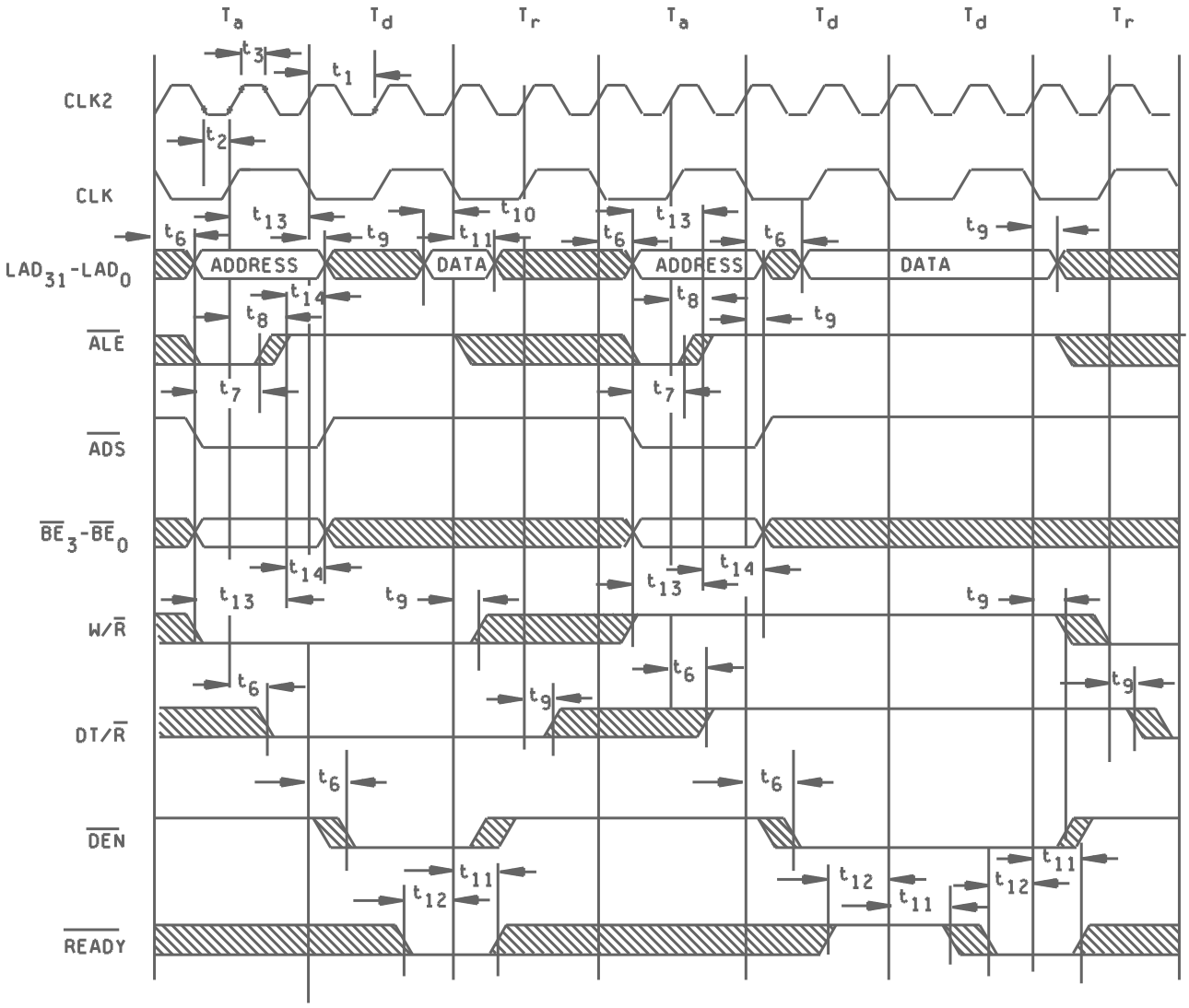
Processor clock pulse (CLK2)



T_{15} = reset hold
T_{16} = reset setup
T_{17} = reset width

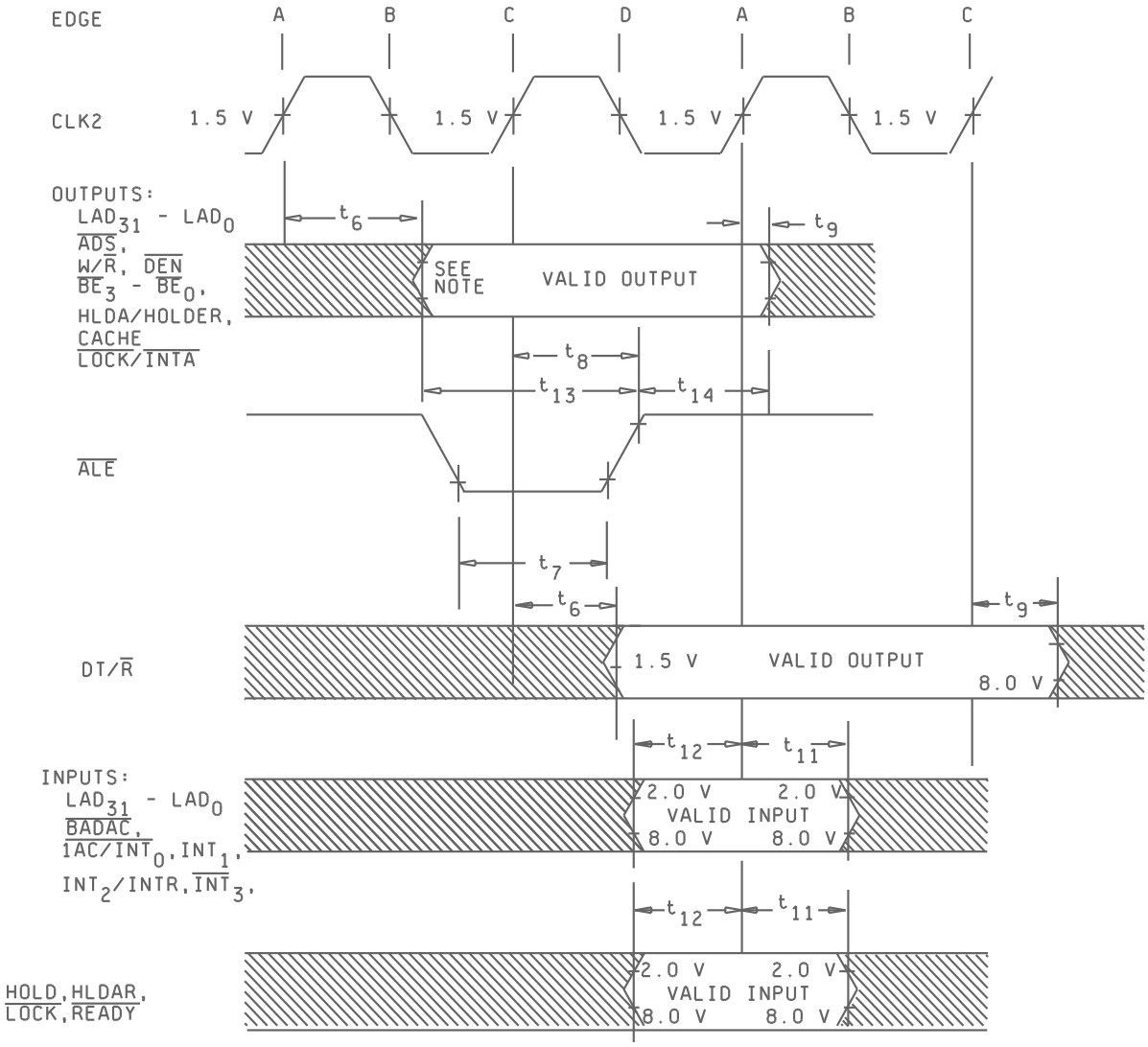
RESET signal timing

FIGURE 4. Switching waveforms and test circuit - Continued.



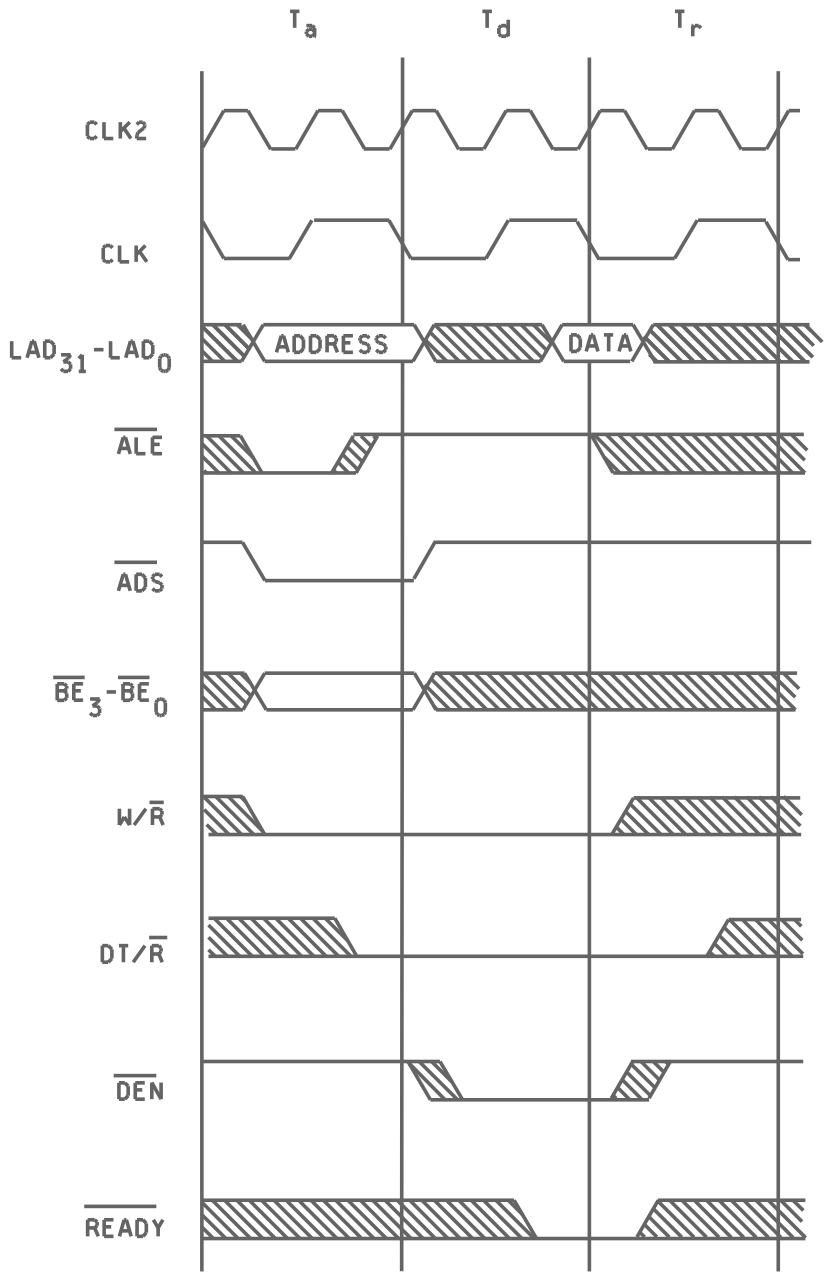
Timing relationship of L-bus signals

FIGURE 4. Switching waveforms and test circuit - Continued.



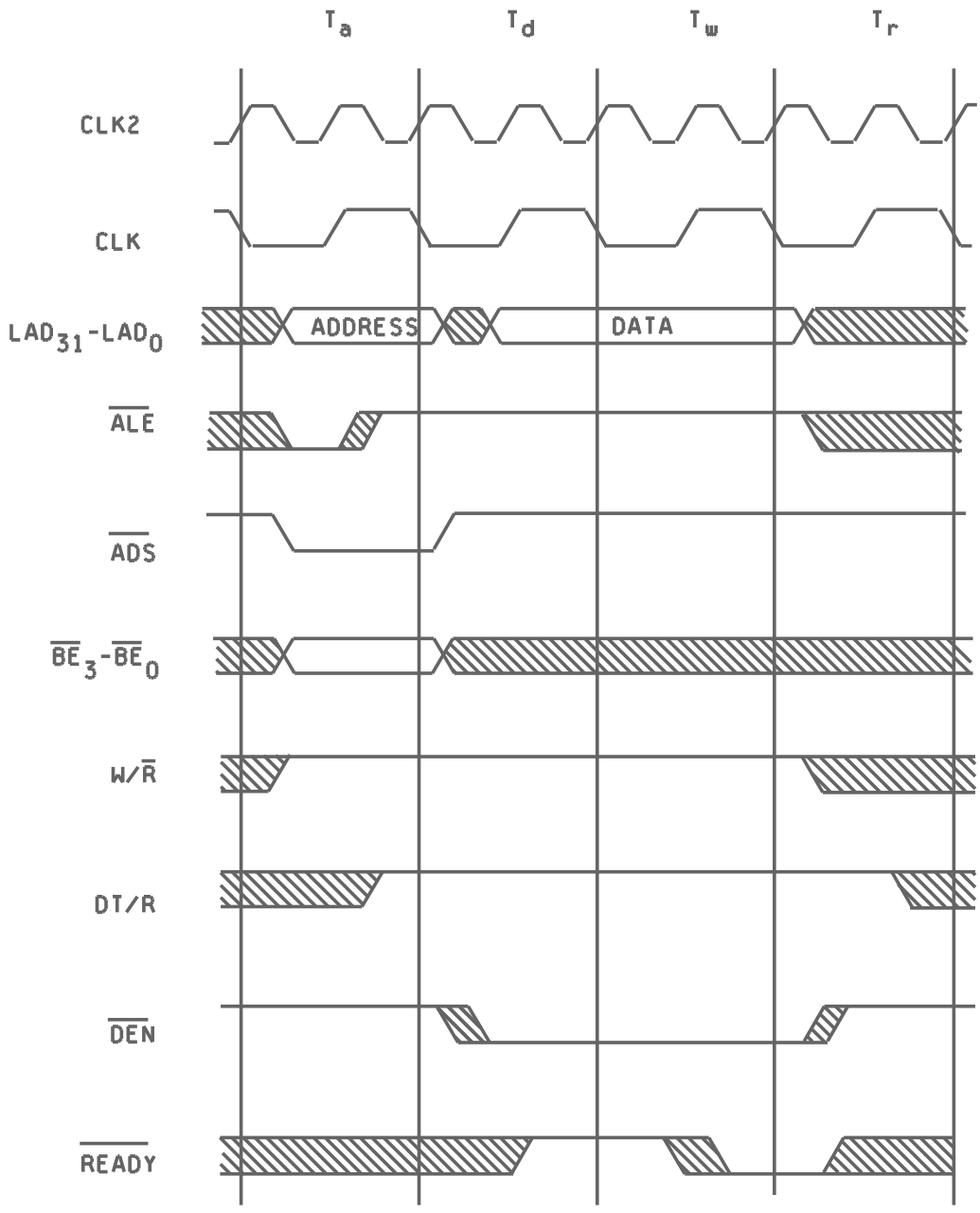
NOTE: For tri-state pins, T_6 and T_9 are measured at 1.5 V. For open-drain pins, T_6 is measured at 1.5 V, T_9 at 0.8 V.

FIGURE 4. Switching waveforms and test circuit - Continued.



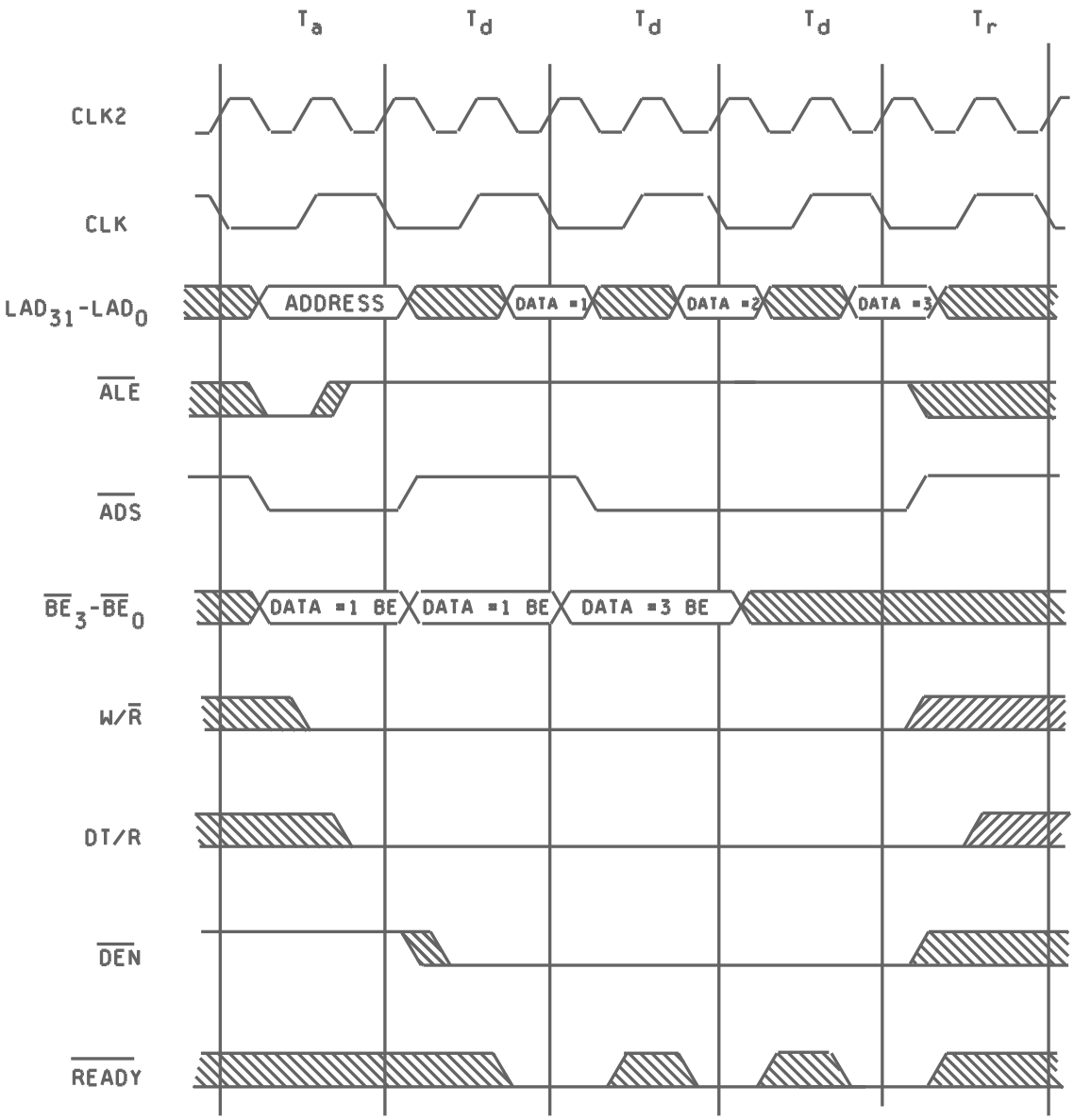
Read transaction

FIGURE 4. Switching waveforms and test circuit - Continued.



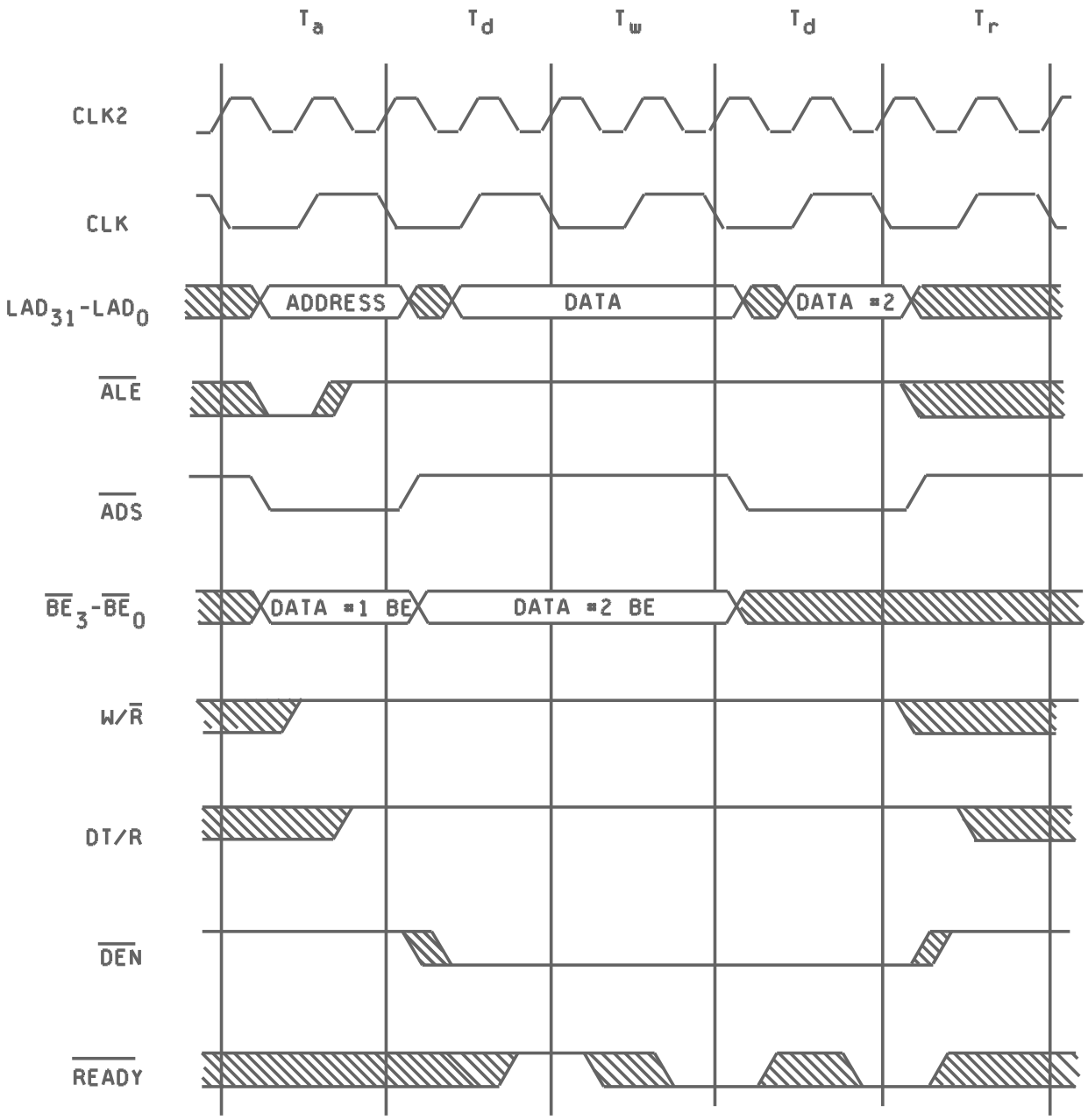
Write transaction with one wait state

FIGURE 4. Switching waveforms and test circuit - Continued.



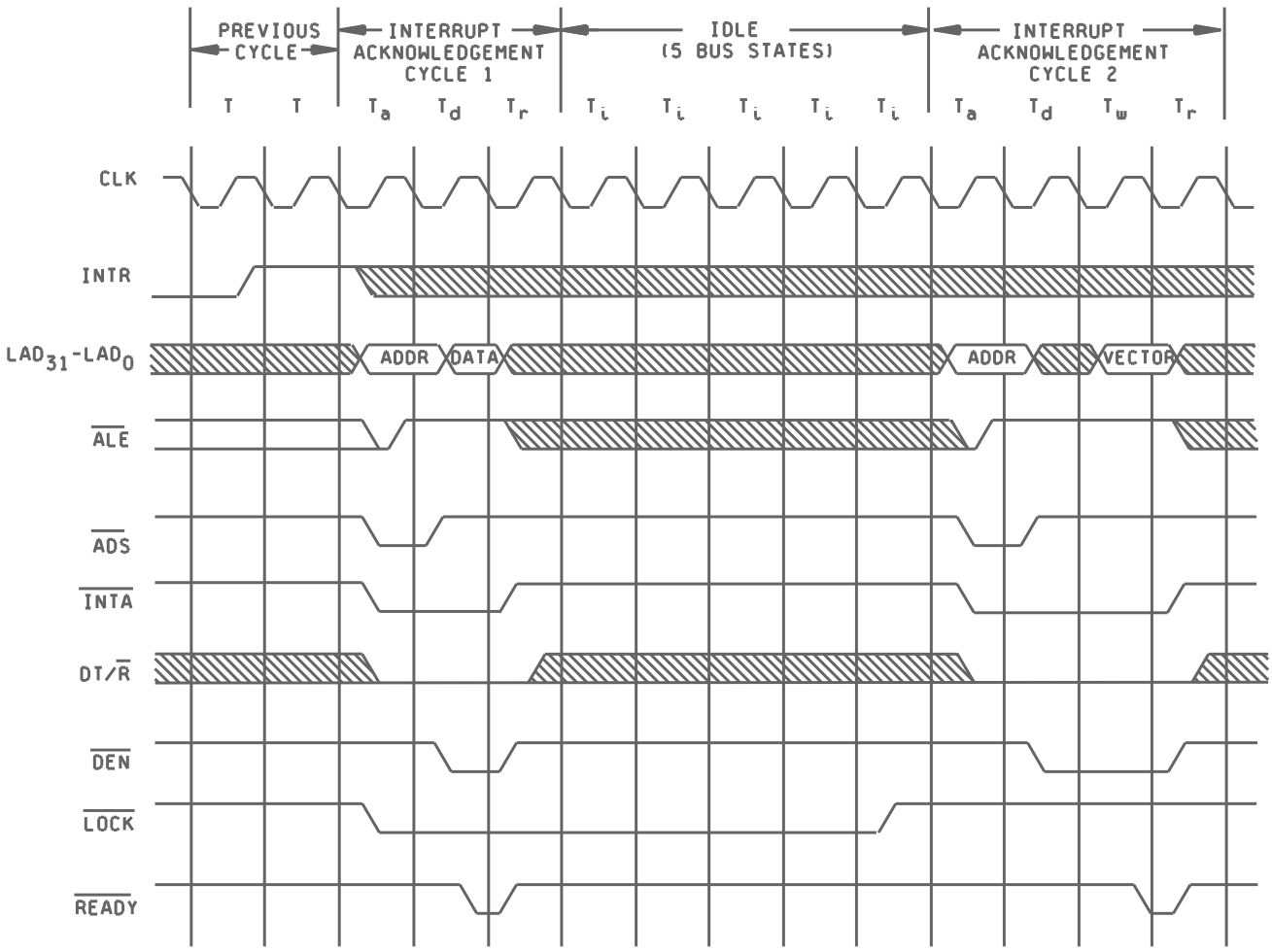
Burst read transaction

FIGURE 4. Switching waveforms and test circuit - Continued.



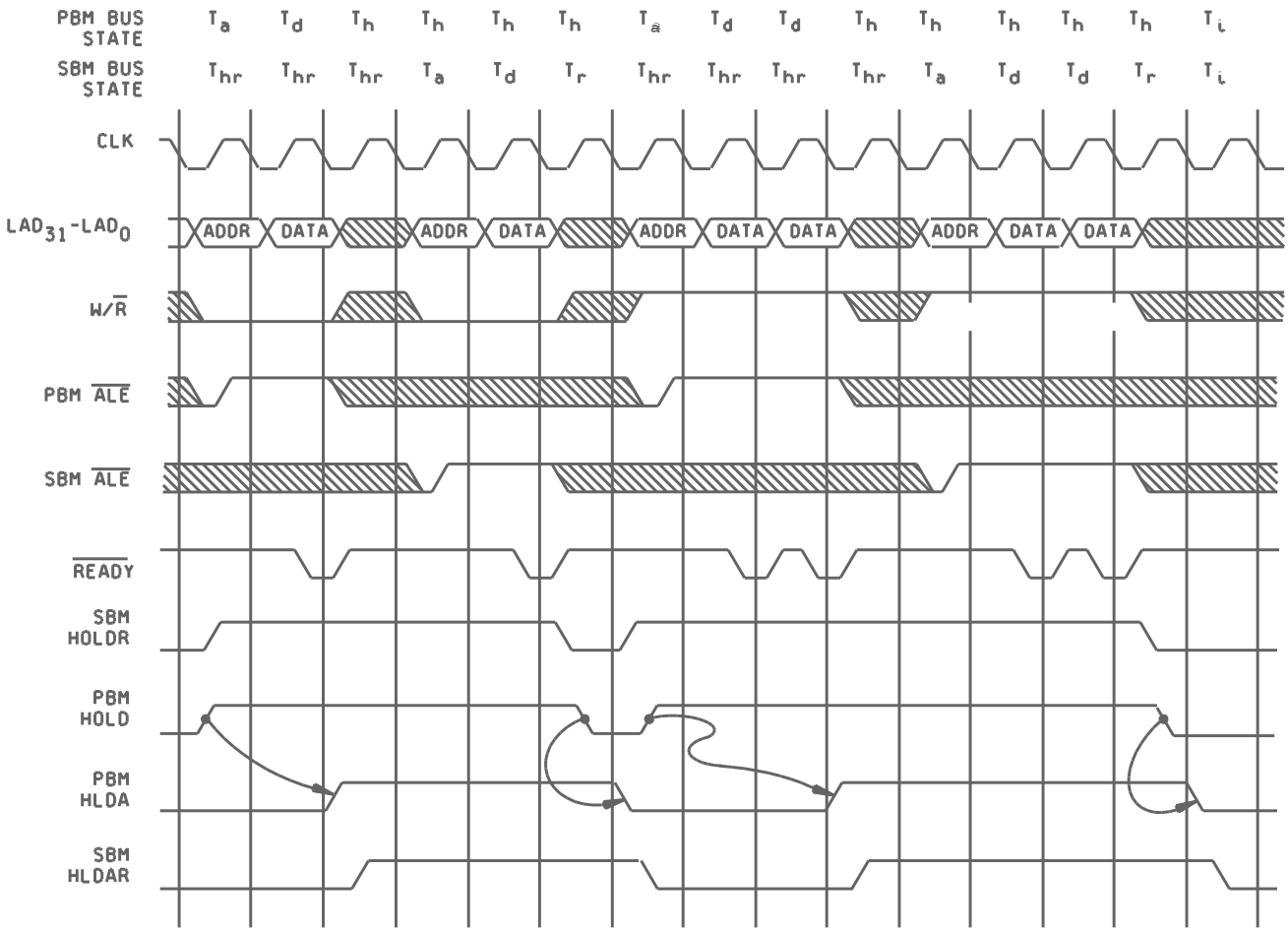
Burst write transaction with one wait state

FIGURE 4. Switching waveforms and test circuit - Continued.



Interrupt acknowledge transaction

FIGURE 4. Switching waveforms and test circuit - Continued.



Bus exchange transaction
(PBM = primary bus master, SBM = secondary bus master)

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{CLK}, and C_{OUT}) shall be measured only for the inital qualification and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1,7		1,7
Final electrical parameters (see 4.2)	1/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,2,3		
Group C end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,7,8a,10	2,8a,10	2,7,8a,10
Group D end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,7,8a,10	2,8a,10	2,8a,10
Group E end-point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiograpnic	2012	100%

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Pin functions.

Symbol	Type	Name and function
CLK21		SYSTEM CLOCK: Provides the fundamental timing for 5962-90946. It is divided by two inside the device to generate the internal processor clock.
LAD_{31} - LAD_0	I/O T.S.	LOCAL ADDRESS/DATA BUS: Carries 32-bit physical addresses and data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bites 0-1 indicate SIZE; see below). During a data (T_d) cycle, bits 0-31 contain read or write data. The LAD lines are active HIGH and float to a high impedance state when not active. SIZE, which is comprised of bits 0-1 of the LAD lines during a T_a cycle, specifies the size of a transfer in words for a burst transaction. LAD 1 / LAD 0 0 0 — 1 word 0 0 — 2 words 1 0 — 3 words 1 1 — 4 words
$\overline{ALE}$	0 T.S.	ADDRESS-LATCH ENABLE: Indicates the transfer of a physical address. $\overline{ALE}$ is asserted during a T_a cycle and deserted before the beginning of the T_d state. It is active LOW and floats to a high impedance state when the processor is idle or is at the end of any bus access.
$\overline{ADS}$	0 O.D.	ADDRESS STATUS: Indicates an address state. $\overline{ADS}$ is asserted every T_a state and deserted during the following T_d state. For a burst transaction, ADS is asserted again every T_d state where $\overline{READY}$ was asserted in the previous cycle.
W/$\overline{R}$	0 O.D.	WRITE/READ: Specifies, during a T_a cycle, whether the operation is a write or read. It is latched on-chip and remains valid during T_d and T_w states.
DT/$\overline{R}$	0 O.D.	DATA TRANSMIT/RECEIVE: Indicates the direction of data transfer to and from the L-bus. It is low during T_a, T_w, and T_d cycles for a read or interrupt acknowledgement; it is high during T_a, T_w, and T_d cycles for a write. DT/$\overline{R}$ never changes state when $\overline{DEN}$ is asserted.
$\overline{DEN}$	0 O.D.	DATA ENABLE: Is asserted during T_d and T_w cycles and indicates transfer of data on the LAD bus lines.
$\overline{READY}$	I	$\overline{READY}$: Indicates that data on LAD lines can be sampled or removed. If $\overline{READY}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting wait state (T_w), and ADS is not asserted in the next cycle.

6.5 Pin functions - Continued.

Symbol	Type	Name and function
$\overline{\text{LOCK}}$	I/O O.D.	BUS LOCK: Prevents other bus masters from gaining control of the L-bus following the current cycle (if they would assert LOCK to do so). LOCK is used by the processor or any bus agent when it performs indivisible Read/Modify/Write (RMW) operations. For a read that is designated as a RMW-read, $\overline{\text{LOCK}}$ is examined. If asserted, the processor waits until it is not asserted; if not asserted, the processor asserts LOCK during the T_a cycle and leaves it asserted. A write that is designated as an RMW-write desserts $\overline{\text{LOCK}}$ in the t_a cycle.
BADAC	1	BAD ACCESS: If asserted in the cycle following the one in which the last $\overline{\text{READY}}$ of a transaction is asserted, indicates that an unrecoverable error has occurred on the current bus transaction, or that a synchronous load/store instruction has not been acknowledged. STARTUP: During system reset, the BADAC signal is interpreted differently. If the signal is high, it indicates that this processor will perform system initialization. If it is low, another processor in the system will perform system initialization instead.
RESET	I	RESET: Clears the internal logic of the processor and causes it to re-initialize. During RESET assertion, the input pins are ignored (except for $\overline{\text{RADAC}}$ and $\overline{\text{IAC}}/\overline{\text{INT}}_0$), the tri-state output pins are placed in a high impedance state, and other output pins are placed in their non-asserted state. RESET must be asserted for at least 41 CLK2 cycles for a predictable RESET. The HIGH to LOW transition of RESET should occur after the rising edge of both CLK2 and the external bus CLK, and before the next rising edge of CLK2.
$\overline{\text{FAILURE}}$	0 O.D.	INITIALIZATION FAILURE: Indicates that the processor has failed to initialize correctly. After RESET is deasserted and before the first bus transaction begins. $\overline{\text{FAILURE}}$ is asserted while the processor performs a self-test. If the self-test completes successfully, then $\overline{\text{FAILURE}}$ is deasserted. Next, the processor performs a zero checksum on the first eight words of memory. If it fails, $\overline{\text{FAILURE}}$ is asserted for a second time and remains asserted; if it passes, system initialization continues and $\overline{\text{FAILURE}}$ remains deasserted.
N C	N/A	NOT CONNECTED: Indicates pins should not be connected. Never connect any pin marked N C.
$\overline{\text{IAC}}$	I	INTERAGENT COMMUNICATION REQUEST/INTERRUPT: 0 indicates either that there is a ($\overline{\text{INT}}_0$)pending IAC message for the processor or an interrupt. The bus interrupt control register determines in which way the signal should be interpreted. To signal an interrupt or IAC request in a synchronous system, this pin (as well as the other interrupt pins) must be enabled by being deasserted for at least one bus cycle and then asserted for at least one additional bus cycle; in an asynchronous system, the pin must remain deasserted for at least two bus cycles and then be asserted for at least two more bus cycles. LOCAL PROCESSOR NUMBER: This signal is interpreted differently during system reset. If the signal is at a high voltage level, it indicates that this processor is a primary bus master (local processor number = 0); if it is at a low voltage level, it indicates that this processor is a secondary bus master (local processor number = 1).
$\overline{\text{INT}}_1$	I	INTERRUPT 1: Like $\overline{\text{INT}}_0$, provides direct interrupt signaling.
$\overline{\text{INT}}_2$ ($\overline{\text{INTR}}$)	I	INTERRUPT 2/INTERRUPT REQUEST: The bus control register determines how this pin is interpreted. If $\overline{\text{INT}}_2$, it has the same interpretation as the $\overline{\text{INT}}_0$ and INT1 pins. If $\overline{\text{INTR}}$, it is used to receive an interrupt request from an external interrupt controller.

6.5 Pin functions - Continued.

Symbol	Type	Name and function
$\overline{INT}_3$ determines	I/O	INTERRUPT 3/INTERRUPT ACKNOWLEDGE: The bus interrupt control register
($\overline{INTA}$)	O.D.	how this pin is interpreted. If INT_3, it has the same interpretation as the INT_0, INT_1, and INT_2 pins. If INTA, it is used as an output to control interrupt acknowledge bus transactions. The output is latched on-chip and remains valid during T_d cycles; as an output, it is open-drain.
$\overline{BE}_3$-$\overline{BE}_0$	0 O.D.	BYTE ENABLE LINES: Specify which data bytes (up to four) on the bus take part in the current bus cycle. $\overline{BE}_3$ corresponds to LAD_{31}-LAD_{24} and $\overline{BE}_0$ corresponds to LAD_7-LAD_0. The byte enables are provided in advance of data. The byte enables asserted during T_a specify the bytes of the first data word. The byte enables asserted during T_d specify the bytes of the next data word (if any), that is, the word to be transmitted following the next assertion of READY. The byte enables during the T_d cycles preceding the last assertion of READY are undefined. The byte enables are latched on-chip and remain constant from one T_d cycle to the next when READY is not asserted. For reads, the byte enables specify the byte(s) that the processor will actually use. The device will assert only adjacent byte enables (e.g., asserting just $\overline{BE}_0$ and $\overline{BE}_2$ is not permitted), and are required to assert at least one byte enable. Accesses must also be naturally aligned (e.g., asserting $\overline{BE}_1$ and $\overline{BE}_2$ is not allowed even though they are adjacent). To produce address bits A_0 and A_1 externally, they can be decoded from the byte enables.
HOLD	1	HOLD: Indicates a request from a secondary bus master to acquire the bus. If the processor is initialized as the primary bus master this input will be interpreted as HOLD. When the processor receives HOLD and grants another master control of the bus, it floats its three-state bus lines, asserts HOLD ACKNOWLEDGE, and enters the T_h state. When HOLD is deasserted, the processor will deassert HOLD ACKNOWLEDGE and go to either the T_1 or T_a state. HOLD ACKNOWLEDGE RECEIVED: Indicates that the processor has acquired the bus. If the processor is initialized as the secondary bus master this input is interpreted as HLDAR.
HLDA (HOLDR)	0 T.S.	HOLD ACKNOWLEDGE: Relinquishes control of the bus to another bus master. If the processor is initialized as the primary bus master this output will be interpreted as HLDA. When HOLD is deasserted, the processor will deassert HLDA and go to either T_1 or T_a state. HOLD REQUEST: Indicates a request to acquire the bus. If the processor is initialized as the secondary bus master this output will be interpreted as HOLDR.
CACHE/TAG	I/0	CACHE: An output signal that indicates if an access is cacheable during a T_a cycle. The CACHE signal T.S. floats to a high impedance state when the processor is idle. TAG is an input/output signal that during T_d and T_w cycles identifies the contents of a 32-bit word as either data (TAG = 0) or an access descriptor (TAG = 1).

I/O = Input/output
T.S. = Three state
$T_r = T_{RECOVERY}$

O = Output
$T_a = T_{ADDRESS}$
$T_1 = T_{IDLE}$

I = Input
$T_d = T_{DATA}$
$T_h = T_{HOLD}$

O.D. = Open-drain
$T_w = T_{WAIT}$

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-02-12

Approved sources of supply for SMD 5962-90946 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9094601MXX	34649	MG80960MC-16/B
5962-9094601MYX	34649	MQ80960MC-16/B
5962-9094602MXX	34649	MG80960MC-20/B
5962-9094602MYX	34649	MQ80960MC-20/B
5962-9094603MXX	34649	MG80960MC-25/B
5962-9094603MYX	34649	MQ80960MC-25/B
5962-9094604MXX	34649	MG80960XA-16/B
5962-9094604MYX	34649	MQ80960XA-16/B
5962-9094605MXX	34649	MG80960XA-20/B
5962-9094605MYX	34649	MQ80960XA-20/B
5962-9094606MXX	34649	MG80960XA-25/B
5962-9094606MYX	34649	MQ80960XA-25/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 W. Chandler Blvd. Chandler, AZ 85226

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.