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Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology[1]

Datasheet

2 GHz – 3.40 GHz Frequencies Supporting Hyper-Threading Technology[1] at 3.06 GHz with 533 MHz System Bus and All Frequencies with 800 MHz System Bus

- Available at 2 GHz, 2.20 GHz, 2.26 GHz, 2.40 GHz, 2.50 GHz, 2.53 GHz, 2.60 GHz, 2.66 GHz, 2.80 GHz, 3 GHz, 3.06 GHz, 3.20 GHz, and 3.40 GHz
- Supports Hyper-Threading Technology (HT Technology) at 3.06 GHz with 533 MHz system bus and all frequencies with 800 MHz system bus
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel NetBurst® microarchitecture
- System bus frequency at 400 MHz, 533 MHz, and 800 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper-Pipelined Technology
  —Advance Dynamic Execution
  —Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems

- 8-KB Level 1 data cache
- Level 1 Execution Trace Cache stores 12-K micro-ops and removes decoder latency from main execution loops
- 512-KB Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 2-MB Integrated Level 3 (L3) cache with 8-way associativity that is supported by Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  —System Management mode
  —Multiple low-power states
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 478-Pin Package

The Intel® Pentium® 4 processor family supporting Hyper-Threading Technology[1] (HT Technology) delivers Intel's most advanced, most powerful processors for desktop PCs and entry-level workstations, which are based on the Intel NetBurst® microarchitecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end-users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multimedia, and multitasking user environments. The Intel® Pentium® 4 processor Extreme Edition supporting HT Technology features 2 MB of L3 cache and offers high levels of performance targeted specifically for high-end gamers and computing power users.

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Revision History

Revision	Description	Date
-005	Added Thermal and Electrical Specifications for frequencies through 3.06 GHz and included multiple VID specifications. Updated the THERMTRIP# and DBI# signal descriptions. Removed Deep Sleep State section. Updated Boxed Processor Fan Heatsink Set Points table and figure. Update Power-on Configuration Option pins table.	November 2002
-006	Minor update to DC specifications	December 2002
-007	Corrected Table 4-3, Signal Description. Item TRST#, last sentence. Measurement changed from 680 W pull-down resistor to 680 Ω pull-down resistor.	January 2003
-008	Added 800 MHz system bus specifications. Added IMPSEL definition. Updated Stop-Grant, HALT, and AutoHALT states	April 2003
-009	Added thermal and electrical specifications for 2.40C GHz, 2.60C GHz, and 2.80C GHz with 800 MHz system bus. Updated thermal specifications and thermal monitor chapter. Updated PROCHOT# pin definition.	May 2003
-010	Added thermal and electrical specifications for 3.20C GHz. Updated processor markings.	June 2003
-011	Added Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology	November 2003
-012	Added 3.40 GHz thermal and electrical specifications for the Intel Pentium 4 Processor Extreme Edition and Intel Pentium 4 Processor with 512-KB L2 Cache on 0.13 Micron Process	February 2004

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Introduction 1

The Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel® Pentium® 4 processor Extreme Edition supporting Hyper-Threading Technology are follow-on processors to the Intel® Pentium® 4 processor in the 478-pin package with Intel NetBurst® microarchitecture. These processors use Flip-Chip Pin Grid Array (FC-PGA2) package technology, and plug into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology, like the Pentium 4 processor in the 478-pin package, are based on the same Intel 32-bit microarchitecture and maintain the tradition of compatibility with IA-32 software. The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process contains an on-die 512-KB advanced transfer L2 cache. The Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology contains an on-die 512-KB level 2 (L2) advanced transfer cache and an on-die 2-MB integrated level 3 (L3) cache. Both processors are on a 0.13 micron process.

This document covers the Pentium 4 processors with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.

Note: Unless otherwise specified in this document, the term "Pentium 4 processor on 0.13 micron process" (or simply processor) refers to both the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.

Hyper-Threading Technology[1] is a new feature in the Pentium 4 processor on 0.13 micron process at 800 MHz system bus. It is also on the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process at 3.06 GHz/533 MHz system bus. HT Technology allows a single, physical Pentium 4 processor on 0.13 micron process to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architecture state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multi-threaded applications. Intel recommends enabling HT Technology with Microsoft Windows* XP Professional or Windows* XP Home, and disabling HT Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see www.intel.com/info/hyperthreading. Refer to Section 6.1 for HT Technology configuration details.

The Intel NetBurst microarchitecture features include hyper-pipelined technology, a rapid execution engine, a 400 MHz, 533 MHz, or 800 MHz system bus, and an execution trace cache. The hyper-pipelined technology doubles the pipeline depth in the Pentium 4 processor on 0.13 micron process, allowing the processor to reach much higher core frequencies. The rapid execution engine allows the two integer ALUs in the processor to run at twice the core frequency; this allows many integer instructions to execute in 1/2 clock cycle. The 400 MHz, 533 MHz, or 800 MHz system bus is a quad-pumped bus running off a 100 MHz or a 133 MHz system clock, making 3.2 Gbytes/sec, 4.3 Gbytes/sec, or 6.4 Gbytes/sec data transfer rates possible. The execution trace cache is a first-level cache that stores approximately 12-K decoded micro-operations that removes the instruction decoding logic from the main execution path, thereby increasing performance.

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Additional features within the Intel NetBurst microarchitecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 512-KB, on-die level 2 (L2) cache. A new floating point and multi-media unit has been implemented that provides superior performance for multi-media and mathematically intensive applications. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management. Power management capabilities (such as AutoHALT, Stop-Grant, and Sleep) have been retained.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multi-media applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques (such as ray tracing).

The 2-MB L3 cache is available with only the Pentium 4 processor Extreme Edition. The additional third level of cache is located on the processor die and is designed specifically to meet the compute needs of high-end gamers and other power users. The integrated level 3 cache is available in 2-MB and is coupled with the 800 MHz system bus to provide a high bandwidth path to memory. The efficient design of the integrated Level 3 cache provides a faster path to large data sets stored in cache on the processor. This results in reduced average memory latency and increased throughput for larger workloads.

The Intel NetBurst microarchitecture system bus on the Pentium 4 processor on 0.13 micron process uses a split-transaction, deferred reply protocol like the Pentium 4 processor in the 478-pin package. This system bus is not compatible with the P6 processor family bus. The Intel NetBurst microarchitecture system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 6.4 Gbytes/second.

Intel will enable support components for the Pentium 4 processor on 0.13 micron process including heatsinks, heatsink retention mechanisms, and sockets. Manufacturability is a high priority; hence, mechanical assembly can be completed from the top of the motherboard, and should not require any special tooling.

The processor system bus uses a variant of GTL+ signalling technology called Assisted Gunning Transceiver Logic (AGTL+) signal technology.

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1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating that the signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol indicates that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "System Bus" refers to the interface between the processor and system core logic (also known as the chipset components). The system bus is a multiprocessing interface to processors, memory, and I/O.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel Pentium 4 processor in the 478-pin package** — 0.18-micron Pentium 4 processor core in the FC-PGA2 package.
- **Intel Pentium 4 processor in the 423-pin package** — 0.18-micron Pentium 4 processor core in the PGA package.
- **Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process** — 0.13 micron version of Pentium 4 processor in the 478-pin package core in the FC-PGA2 package with a 512-KB L2 cache.
- **Intel Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology** — 0.13 micron version of Pentium 4 processor in the 478-pin package core in the FC-PGA2 package with a 512-KB L2 cache and a 2-MB L3 cache.
- **Processor** — For this document, the term processor shall mean Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.
- **Keep-out zone** — The area on or near the processor that system design can not utilize. This area must be kept free of all components to make room for the processor package, retention mechanism, heatsink, and heatsink clips.
- **Hyper-Threading Technology** — Hyper-Threading Technology allows a single, physical Pentium 4 processor to function as two logical processors when the necessary system ingredients are present. For more information, see: www.intel.com/info/hyperthreading.
- **Intel® 875P chipset** — Chipset that supports DDR memory technology for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. This chipset also supports the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology in platforms that meet the thermal design guidelines for this processor.
- **Intel® 865G/865GV/865PE chipset** — Chipset that supports DDR memory technology for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
- **Intel® 865P chipset** — Chipset that supports DDR memory technology for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
- **Intel® 850 chipset** — Chipset that supports Rambus RDRAM* memory technology for Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and Pentium 4 processor in the 478-pin package.
- **Intel® 845 chipset** — Chipset that supports PC133 and DDR memory technologies for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and Pentium 4 processor in the 478-pin package.

- **Processor core** — Pentium 4 processor with 512-KB L2 cache on 0.13 micron process core die with integrated L2 cache and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology core die with integrated L2 and L3 caches.
- **FC-PGA2 package** — Flip-Chip Pin Grid Array package with 50-mil pin pitch and integrated heat spreader.
- **mPGA478B socket** — Surface mount, 478 pin, Zero Insertion Force (ZIF) socket with 50-mil pin pitch. The socket mates the processor to the system board.
- **Integrated heat spreader** — The surface used to make contact between a heatsink or other thermal solution and the processor. Integrated heat spreader is abbreviated IHS.
- **Retention mechanism** — The structure mounted on the system board that provides support and retention of the processor heatsink.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. References (Sheet 1 of 2)

Document	Location
Intel® 875P Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/252527.htm
Intel® 865G/865PE/865P Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/252518.htm
Intel® Pentium® 4 Processor in the 478-Pin Package / Intel® 850 Chipset Platform Family Design Guide	http://developer.intel.com/design/pentium4/guides/249888.htm
Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845 Chipset Platform for DDR Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298605.htm
Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845E Chipset Platform for DDR Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298652.htm
Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845 Chipset Platform for SDR Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298354.htm
Intel® Pentium® 4 Processor in the 478-Pin Package and Intel® 845GE/845PE Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/251925.htm
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845G/845GL/845GV Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/designex/298654.htm
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines	http://developer.intel.com/design/pentium4/guides/252161.htm
Mechanical Enabling for the Intel® Pentium® 4 Processor in the 478-pin Package	http://developer.intel.com/design/pentium4/guides/290728.htm
Assembling Intel Reference Components for the Intel® Pentium® 4 Processor in the 478-pin Package	http://developer.intel.com/design/pentium4/guides/298590.htm
Voltage Regulator-Down (VRD) 10.0: for Desktop Socket 478 Design Guide	http://developer.intel.com/design/pentium4/guides/252885.htm
Voltage Regulator Module (VRM) 9.0 DC-DC Converter Design Guidelines	http://developer.intel.com/design/pentium4/guides/249205.htm
Intel® Pentium® 4 Processor VR-Down Design Guidelines	http://developer.intel.com/design/Pentium4/guides/249891.htm
CK00 Clock Synthesizer/Driver Design Guidelines	http://developer.intel.com/design/pentium4/guides/249206.htm
Intel® Pentium®4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines	http://developer.intel.com/design/pentium4/guides/249890.htm

Table 1-1. References (Sheet 2 of 2)

Document	Location
IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture	http://developer.intel.com/design/ pentium4/manuals/245470.htm
IA-32 Intel® Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	http://developer.intel.com/design/ pentium4/manuals/245471.htm
IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programming Guide	http://developer.intel.com/design/ pentium4/manuals/245472.htm
AP-485 Intel® Processor Identification and the CPUID Instruction	http://developer.intel.com/design/ xeon/applnots/241618.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/ Xeon/guides/249679.htm

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Electrical Specifications 2

2.1 System Bus and GTLREF

Most Pentium 4 processor on 0.13 micron process system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signalling technology. As with the P6 family of microprocessors, this signalling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Like the Pentium 4 processor in the 478-pin package, the termination voltage level for the Pentium 4 processor on 0.13 micron process AGTL+ signals is V_{CC}, which is the operating voltage of the processor core. The use of a termination voltage that is determined by the processor core allows better voltage scaling on the system bus for the Pentium 4 processor on 0.13 micron process. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Design guidelines for the Pentium 4 processor on 0.13 micron process system bus are detailed in the appropriate platform design guide (refer to Table 1-1*)*.

The AGTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board.

Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). The Intel® 875P chipset, Intel® 865G/865GV/865PE/865P chipsets, Intel® 850 chipset, and the Intel® 845 chipset also provide on-die termination. This eliminates the need to terminate the bus on the system board for most AGTL+ signals. However, some AGTL+ signals do not include on-die termination and must be terminated on the system board. For more information, refer to the appropriate platform design guide.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system. For more information, refer to the appropriate platform design guide.

2.2 Power and Ground Pins

For clean on-chip power distribution, the Pentium 4 processor on 0.13 micron process has 85 VCC (power) and 180 VSS (ground) inputs. All power pins must be connected to V_{CC}, while all V_{SS} pins must be connected to a system ground plane.The processor VCC pins must be supplied with the voltage defined by the VID (Voltage ID) pins and the loadline specifications (see Figure 2-4).

2.3 Decoupling Guidelines

Because of the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-6. Failure to do so can result in timing violations and/or affect the long term reliability of the processor. For further information and design guidelines, refer to the appropriate platform design guide and the *Intel® Pentium® 4 Processor VR-Down Design Guidelines.*

2.3.1 V$_{CC}$ Decoupling

VCC regulator solutions need to provide sufficient decoupling capacitance to satisfy processor voltage specifications. This includes bulk capacitance with low effective series resistance (ESR) to keep the voltage rail within specifications during large swings in load current. In addition, ceramic decoupling capacitors are required to filter high frequency content generated by bus and processor activity. Consult the Voltage Regulator Down design guide and appropriate platform design guide for further information.

2.3.2 System Bus AGTL+ Decoupling

Pentium 4 processors on 0.13 micron process integrate signal termination on the die and incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation. For more information, refer to the appropriate platform design guide.

2.4 Voltage Identification

The VID specification for Pentium 4 processors on 0.13 micron process is supported by the *Intel® Pentium® 4 Processor VR-Down Design Guidelines, Voltage Regulator-Down (VRD) 10.0 Design Guide*, and *Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum*. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 2-6 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Pentium 4 processors on 0.13 micron process use five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. The VID pins for the Pentium 4 processor on 0.13 micron process are open drain outputs driven by the processor VID circuitry. The VID signals rely on pull-up resistors tied to a 3.3 V (maximum) supply to set the signal to a logic high level. These pull-up resistors may be either external logic on the motherboard, or internal to the Voltage Regulator. Table 2-2 specifies the voltage level corresponding to the state of VID[4:0]. A '1' in this table refers to a high voltage level, and a '0' refers to low voltage level. The definition provided in Table 2-2 is not related in any way to previous P6 processors or VRs, but is compatible with the Pentium 4 processor in the 478-pin package. If the processor socket is empty (VID[4:0] = 11111) or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *Intel® Pentium® 4 Processor VR-Down Design Guidelines, Voltage Regulator-Down (VRD) 10.0 Design Guide*, or *Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum* for more details.

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Power source characteristics must be stable when the supply to the voltage regulator is stable. Refer to the appropriate platform design guide for timing details of the power up sequence. Refer to the appropriate platform design guide for implementation details.

The Voltage Identification circuit requires an independent 1.2 V supply. This voltage must be routed to the processor $V_{CC}VID$ pin. Figure 2-1 and Table 2-1 show the voltage and current requirements of the $V_{CC}VID$ pin.

Table 2-1. V_{CC}VID Pin Voltage Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{CC}VID$	V_{CC} for Voltage Identification circuit	–5%	1.2	+10%	V	1

NOTE:
1. This specification applies to both static and transient components. The rising edge of $V_{CC}VID$ must be monotonic from 0 to 1.1 V. See Figure 2-1 for current requirements. In this case, monotonic is defined as continuously increasing with less than 50 mV of peak to peak noise for any width greater than 2 ns superimposed on the rising edge.

Figure 2-1. V_{CC}VID Pin Voltage and Current Requirements
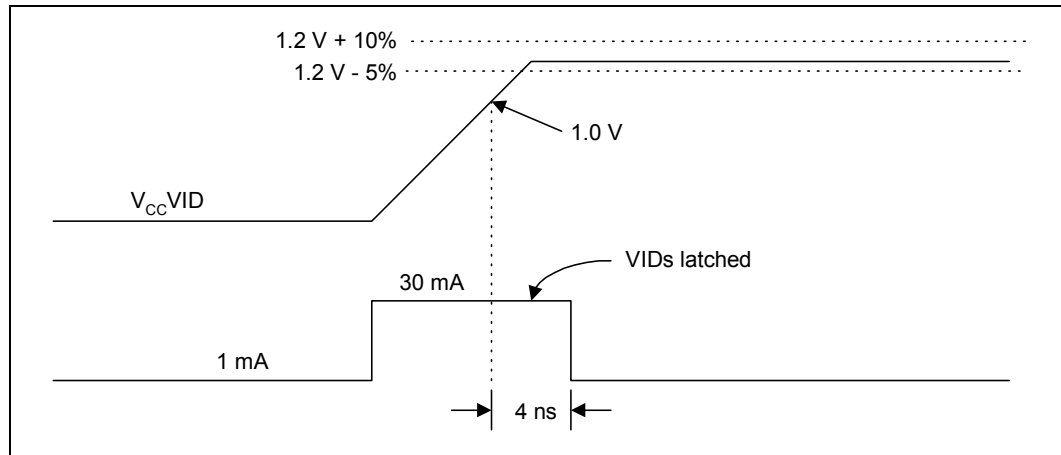
Table 2-2. Voltage Identification Definition

VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
	Proce	ssor Pins			
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600

2.4.1 Phase Lock Loop (PLL) Power and Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Pentium 4 processor on 0.13 micron process. Since these PLLs are analog, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. A typical filter topology is shown in Figure 2-2.

The AC low-pass requirements, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 2-2), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

Refer to the appropriate platform design guide for recommendations on implementing the filter.

Figure 2-2. Typical V_{CCIOPLL}, V_{CCA} and V_{SSA} Power Distribution
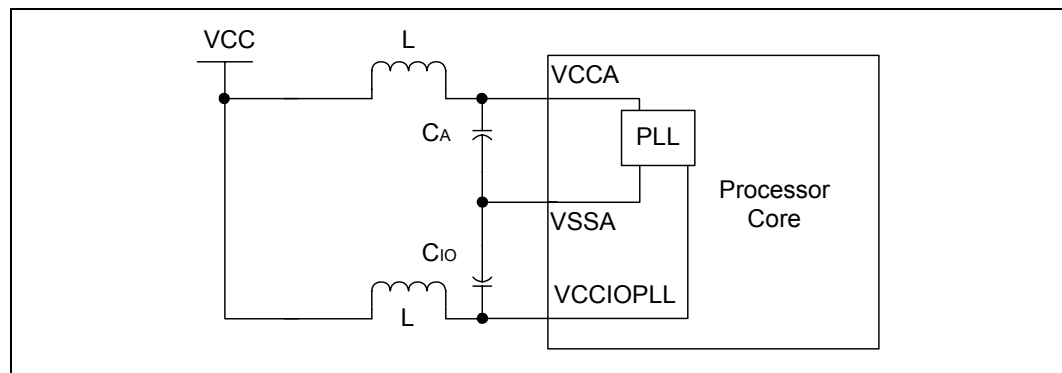
Figure 2-3. Phase Lock Loop (PLL) Filter Requirements
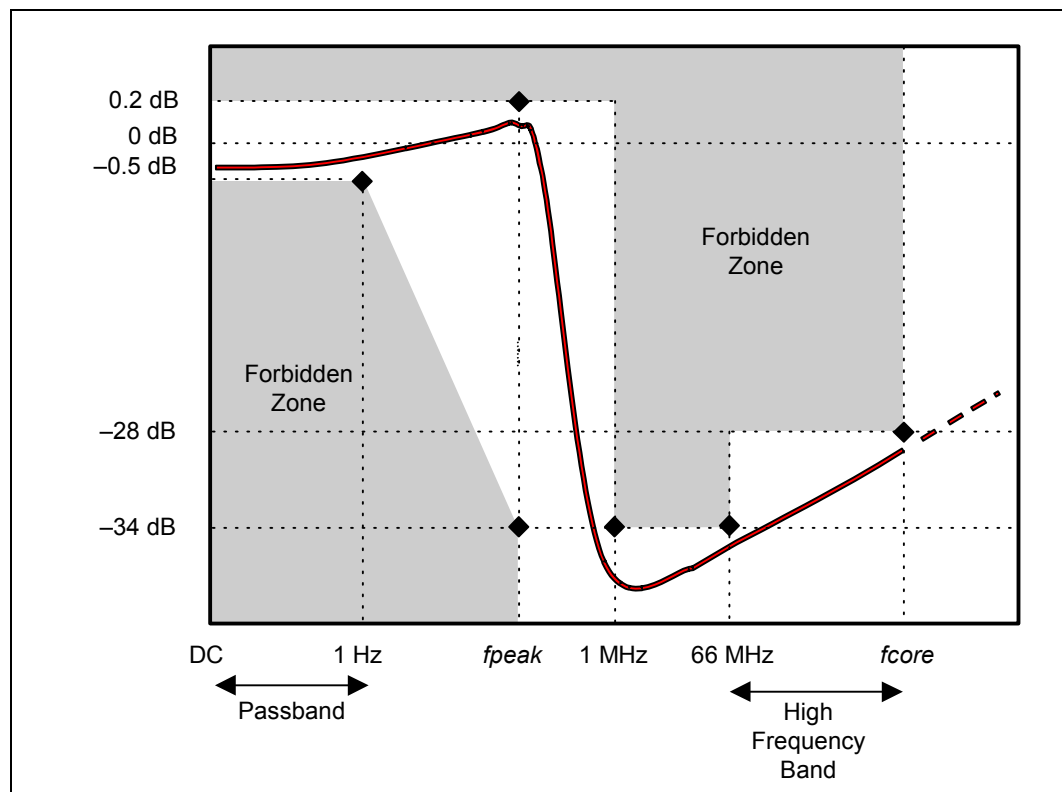
NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.

2.5   Reserved, Unused Pins, and TESTHI[12:0]

All RESERVED pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium 4 processors on 0.13 micron process. See Chapter 4 for a pin listing of the processor and the location of all RESERVED pins.

For reliable operation, always connect unused inputs or bidirectional signals that are not terminated on the die to an appropriate signal level. Note that on-die termination has been included on the Pentium 4 processor on 0.13 micron process to allow signals to be terminated within the processor silicon. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Table 2-3 lists details on AGTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Refer to the appropriate platform design guide for the appropriate resistor values.

Unused outputs can be left unconnected. However, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals that don't have on-die termination, use pull-up resistors of the same value in place of the on-die termination resistors (RTT). See Table 2-14.

The TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused output unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate platform design guide listed in Table 1-1.

The TESTHI pins should be tied to the processor V_{CC} using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or may be grouped together as follows:

1. TESTHI[1:0]
2. TESTHI[5:2]
3. TESTHI[10:8]
4. TESTHI[12:11]

A matched resistor should be used for each group.

Additionally, if the ITPCLKOUT[1:0] pins are not used, they may be connected individually to V_{CC} using matched resistors or may be grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 kΩ resistors is required. Tying ITPCLKOUT[1:0] directly to V_{CC} or sharing a pull-up resistor to V_{CC} will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an inboard debug port.

As an alternative, group2 (TESTHI[5:2]) and the ITPCLKOUT[1:0] pins may be tied directly to the processor V_{CC}. This has no impact on system functionality. TESTHI0 and TESTHI12 may also be tied directly to the processor V_{CC} if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0] pins, direct tie to V_{CC} is strongly discouraged for system boards that do not implement an inboard debug port.

Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing.

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2.6   System Bus Signal Groups

To simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers that use GTLREF as a reference level. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals that are dependent on the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.), and the second set is for the source synchronous signals that are relative to their respective strobe lines (data and address), as well as the rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-3 identifies which signals are common clock, source synchronous, and asynchronous signals.

Table 2-3. System Bus Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Common Clock	BPRI#, DEFER#, RESET#[2], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#[2], BR0#[2], DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
AGTL+ Source Synchronous I/O	Source Synchronous	**Signals** **Associated Strobe** REQ[4:0]#, A[16:3]#[5] ADSTB0# A[35:17]#[5] ADSTB1# D[15:0]#, DBI0# DSTBP0#, DSTBN0# D[31:16]#, DBI1# DSTBP1#, DSTBN1# D[47:32]#, DBI2# DSTBP2#, DSTBN2# D[63:48]#, DBI3# DSTBP3#, DSTBN3#
AGTL+ Strobes	Common Clock	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Asynchronous GTL+ Input[4,5]	Asynchronous	A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#
Asynchronous GTL+ Output[4]	Asynchronous	FERR#, IERR#[2], THERMTRIP#
Asynchronous GTL+ Input/ Output[4]	Asynchronous	PROCHOT#
TAP Input[4]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[4]	Synchronous to TCK	TDO
System Bus Clock	N/A	BCLK[1:0], ITP_CLK[1:0][3]
Power/Other	N/A	V_{CC}, V_{CCA}, $V_{CCIOPLL}$, V_{CC}VID, VID[4:0], V_{SS}, V_{SSA}, GTLREF[3:0], COMP[1:0], RESERVED, TESTHI[5:0, 12:8], ITPCLKOUT[1:0], THERMDA, THERMDC, IMPSEL, DBR#[3], PWRGOOD, SKTOCC#, V_{CC_SENSE}, V_{SS_SENSE}, BSEL[1:0],

NOTES:
1. Refer to Section 5.2 for signal descriptions.
2. These AGTL+ signals do not have on-die termination. Refer to Section 2.5 and the *ITP700 Debug Port Design Guide* for termination requirements.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. These signal groups are not terminated by the processor. Refer to Section 2.5, the *ITP700 Debug Port Design Guide,* and the appropriate Platform Design Guide for termination requirements and further details.
5. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 6.1 for details.

2.7 Asynchronous GTL+ Signals

The Pentium 4 processor on 0.13 micron process does not use CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals (such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK#) use GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP#) use GTL+ output buffers. PROCHOT# uses GTL+ input/output buffer. All of these signals follow the same DC requirements as AGTL+ signals; however, the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs for the processor to recognize them. See Section 2.11 for the DC specifications for the Asynchronous GTL+ signal groups. See Section 6.2 for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Because of the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium 4 processor on 0.13 micron process be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required, with each driving a different voltage level.

2.9 System Bus Frequency Select Signals (BSEL[1:0])

The BSEL[1:0] are output signals used to select the frequency of the processor input clock (BCLK[1:0]). Table 2-4 defines the possible combinations of the signals, and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process currently operates at a 400 MHz, 533 MHz, or 800 MHz system bus frequency. The Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology currently operates at 800 MHz system bus frequency. Individual processors will operate only at their specified system bus frequency.

For more information about these pins, refer to Section 4.2 and the appropriate platform design guidelines.

Table 2-4. BSEL[1:0] Frequency Table for BCLK[1:0]

BSEL1	BSEL0	Function
L	L	100 MHz
L	H	133 MHz
H	L	200 MHz
H	H	RESERVED

2.10 Maximum Ratings

Table 2-5 lists the processor's maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from Electro Static Discharge (ESD), one should always take precautions to avoid high static voltages or electric fields.

Table 2-5. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	2
V_{CC}	Any processor supply voltage with respect to V_{SS}	–0.3	1.75	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.1	1.75	V	
$V_{inAsynch\_GTL+}$	Asynch GTL+ buffer DC input voltage with respect to V_{SS}	–0.1	1.75	V	
I_{VID}	Max VID pin current		5	mA	

NOTES:
1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon unless noted otherwise. See Chapter 4 for the pin signal definitions and signal pin assignments. Most of the signals on the processor system bus are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 2-9.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 2-10.

Table 2-6 through Table 2-10 list the DC specifications for the Pentium 4 processor on 0.13 micron process, and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Processors with multiple VID have I_{CC_MAX} of the highest VID for the specified frequency. For example, for processors through 2.80 GHz, the I_{CC_MAX} would be the one at VID=1.525 V.

Table 2-6. Voltage and Current Specifications (Sheet 1 of 4)

Symbol	Parameter	Min	Typ	Max	Unit	Notes[10]
V_{CC} (400 MHz FSB)	**V_{CC} for Processor at VID=1.475 V**		Refer to [Table 2-7](#) and [Figure 2-4](#)		V	1, 2, 3, 4
	2A GHz	1.315		1.390		
	2.20 GHz	1.310		1.385		
	2.40 GHz	1.300		1.380		
	2.50 GHz	1.300		1.375		
	2.60 GHz	1.295		1.375		
	V_{CC} for Processor at VID=1.500 V					
	2A GHz	1.340		1.415		
	2.20 GHz	1.335		1.410		
	2.40 GHz	1.330		1.405		
	2.50 GHz	1.325		1.400		
	2.60 GHz	1.320		1.400		
	V_{CC} for Processor at VID=1.525 V					
	2A GHz	1.365		1.440		
	2.20 GHz	1.360		1.435		
	2.40 GHz	1.350		1.430		
	2.50 GHz	1.350		1.430		
	2.60 GHz	1.345		1.425		
V_{CC} (533 MHz FSB)	**V_{CC} for Processor at VID=1.475 V**		Refer to [Table 2-7](#) and [Figure 2-4](#)		V	1, 2, 3, 4
	2.26 GHz	1.305		1.380		
	2.40B GHz	1.300		1.380		
	2.53 GHz	1.295		1.375		
	2.66 GHz	1.295		1.370		
	2.80 GHz	1.290		1.370		
	3.06 GHz	1.265		1.345		
	V_{CC} for Processor at VID=1.500 V					
	2.26 GHz	1.330		1.405		
	2.40B GHz	1.330		1.405		
	2.53 GHz	1.325		1.400		
	2.66 GHz	1.320		1.395		
	2.80 GHz	1.315		1.395		
	3.06 GHz	1.290		1.370		
	V_{CC} for Processor at VID=1.525 V					
	2.26 GHz	1.355		1.435		
	2.40B GHz	1.350		1.430		
	2.53 GHz	1.345		1.430		
	2.66 GHz	1.345		1.420		
	2.80 GHz	1.340		1.420		
	3.06 GHz	1.315		1.395		
	V_{CC} for Processor at VID=1.550 V					
	3.06 GHz	1.340		1.425		

Table 2-6. Voltage and Current Specifications (Sheet 2 of 4)

Symbol	Parameter	Min	Typ	Max	Unit	Notes[10]
V_{CC} (800 MHz FSB with 512-KB L2 Cache Only)	**V_{CC} for Processor at VID=1.475 V** 2.40C GHz 2.60C GHz 2.80C GHz 3 GHz 3.20C GHz 3.40 GHz	1.295 1.290 1.288 1.265 1.260 1.280	Refer to Table 2-7, Figure 2-4. and Table 2-8, Figure 2-5	1.375 1.370 1.369 1.350 1.345 1.350	V	1, 2, 3, 4,13
	V_{CC} for Processor at VID=1.500 V 2.40C GHz 2.60C GHz 2.80C GHz 3 GHz 3.20C GHz 3.40 GHz	1.320 1.315 1.313 1.290 1.285 1.305		1.400 1.395 1.394 1.375 1.370 1.375		
	V_{CC} for Process or at VID=1.525 V 2.40C GHz 2.60C GHz 2.80C GHz 3 GHz 3.20C GHz 3.40 GHz	1.345 1.340 1.338 1.315 1.310 1.330		1.425 1.420 1.419 1.400 1.395 1.400		
	V_{CC} for Processor at VID=1.550 V 3 GHz 3.20C GHz 3.40 GHz	1.340 1.335 1.355		1.425 1.420 1.425		
V_{CC} (800 MHz FSB with 2 MB L3 Cache)	**Vcc for Processor at VID=1.475 V:** 3.20 GHz	1.285	Refer to Table 2-8 and Figure 2-5	1.340	V	1,2,4,13
	Vcc for Processor at VID=1.500 V: 3.20 GHz	1.310		1.365		
	Vcc for Processor at VID=1.525 V 3.20 GHz 3.40 GHz	1.335 1.325		1.390 1.380		
	Vcc for Processor at VID=1.550 V 3.20 GHz 3.40 GHz	1.360 1.350		1.415 1.405		
	Vcc for Processor at VID=1.575 V 3.40 GHz	1.375		1.430		
	Vcc for Processor at VID=1.600 V 3.40 GHz	1.400		1.455		
V_{CC}VID	V_{CC} for voltage identification circuit	−5%	1.2	+10%	V	9

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Table 2-6. Voltage and Current Specifications (Sheet 3 of 4)

Symbol	Parameter	Min	Typ	Max	Unit	Notes[10]
I_{CC} (400 MHz FSB)	**I_{CC} for Processor at VID=1.500 V** 2A GHz 2.20 GHz 2.40 GHz 2.50 GHz			44.3 47.1 49.8 51.3	A	3,4,6,10
	I_{CC} for Processor at VID=1.525 V 2A GHz 2.20 GHz 2.40 GHz 2.50 GHz 2.60 GHz			45.1 47.9 50.7 52.0 53.5		
	I_{CC} for Processor with multiple VIDs 2A GHz 2.20 GHz 2.40 GHz 2.50 GHz 2.60 GHz			45.1 47.9 50.7 52.0 53.5		
I_{CC} (533 MHz FSB)	**I_{CC} for Processor at VID=1.500 V** 2.26 GHz 2.40B GHz 2.53 GHz			48 49.8 51.5	A	3,4,6,10
	I_{CC} for Processor at VID=1.525 V 2.26 GHz 2.40B GHz 2.53 GHz 2.66 GHz 2.80 GHz			48.6 50.7 52.5 53.9 55.9		
	I_{CC} for Processor with multiple VIDs 2.26 GHz 2.40B GHz 2.53 GHz 2.66 GHz 2.80 GHz 3.06 GHz			48.6 50.7 52.5 53.9 55.9 65.4		
I_{CC} (800 MHz FSB with 512-KB L2 Cache Only)	**I_{CC} for Processor with multiple VIDs** 2.40C GHz 2.60C GHz 2.80C GHz 3 GHz 3.20C GHz 3.40 GHz			52.4 55.0 55.9 64.8 67.4 71.6	A	3,4,6,10
I_{CC} (800 MHz FSB with 2-MB L3 Cache)	**I_{CC} for Processor with multiple VIDs:** 3.20 GHz 3.40 GHz			71.5 77.7	A	4,6,10,13

Table 2-6. Voltage and Current Specifications (Sheet 4 of 4)

Symbol	Parameter	Min	Typ	Max	Unit	Notes[10]
I_{SGNT} Islp	I_{CC} Stop-Grant			23	A	5,7,8
				27		5,7,11
				32		5,7,12
				35		5,7,14
I_{TCC}	I_{CC} TCC active			I_{CC}	A	6
$I_{CC\ PLL}$	I_{CC} for PLL pins			60	mA	

NOTES:

1. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Table 2-2 for more information. The VID bits will set the maximum V_{CC} with the minimum being defined according to current consumption at that voltage.
2. The voltage specification requirements are measured across V_{CC_SENSE} and V_{SS_SENSE} pins at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Refer to Table 2-7 and Figure 2-4 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current. Failure to adhere to this specification can affect the long term reliability of the processor.
4. V_{CC_MIN} is defined at I_{CC_MAX}.
5. The current specified is also for AutoHALT State.
6. The maximum instantaneous current that the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
7. I_{CC} Stop-Grant and I_{CC} Sleep are specified at V_{CC_MAX}.
8. These specifications apply to the processor with maximum VID setting of 1.525 V for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
9. This specification applies to both static and transient components. The rising edge of V_{CC}VID must be monotonic from 0 to 1.1 V. See Figure 2-1 for current requirements. In this case monotonic is defined as continuously increasing with less than 50 mV of peak to peak noise for any width greater than 2 ns superimposed on the rising edge.
10. I_{CC_MAX} is specified for highest VID only. The processor will be shipped under multiple VIDs listed for each frequency; however, the I_{CC_MAX} specifications will be the same as highest VID specified in table.
11. These specifications apply to the processor with maximum VID setting of 1.550 V for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
12. This specification applies to processors with maximum VID setting of 1.550 V for the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.
13. Refer to Table 2-8 and Figure 2-5 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC}exceeds V_{CC_MAX} for a given current. Failure to adhere to this specification can affect the long term reliability of the processor.
14. These specifications apply to processors with maximum VID setting of 1.600 V for the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.

Table 2-7. V$_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor With 512-KB L2 Cache on 0.13 Micron Process at Frequencies up to and Including 3.2 GHz)

Icc (A)	Voltage Deviation from VID Setting (V)[1,2,3]		
	Maximum	Typical	Minimum
0	0.000	−0.025	−0.050
5	−0.010	−0.036	−0.062
10	−0.019	−0.047	−0.075
15	−0.029	−0.058	−0.087
20	−0.038	−0.069	−0.099
25	−0.048	−0.079	−0.111
30	−0.057	−0.090	−0.124
35	−0.067	−0.101	−0.136
40	−0.076	−0.112	−0.148
45	−0.085	−0.123	−0.160
50	−0.095	−0.134	−0.173
55	−0.105	−0.145	−0.185
60	−0.114	−0.156	−0.197
65	−0.124	−0.166	−0.209
70	−0.133	−0.177	−0.222

NOTES:
1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on the following loadline figure.
3. The loadlines specify voltage limits at the die measured at V$_{CC\_SENSE}$ and V$_{SS\_SENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V$_{CC}$ and V$_{SS}$ pins. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* for V$_{CC}$ and V$_{SS}$ socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is required to ensure reliable processor operation.

Figure 2-4. V$_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor With 512-KB L2 Cache on 0.13 Micron Process at Frequencies up to and Including 3.2 GHz)
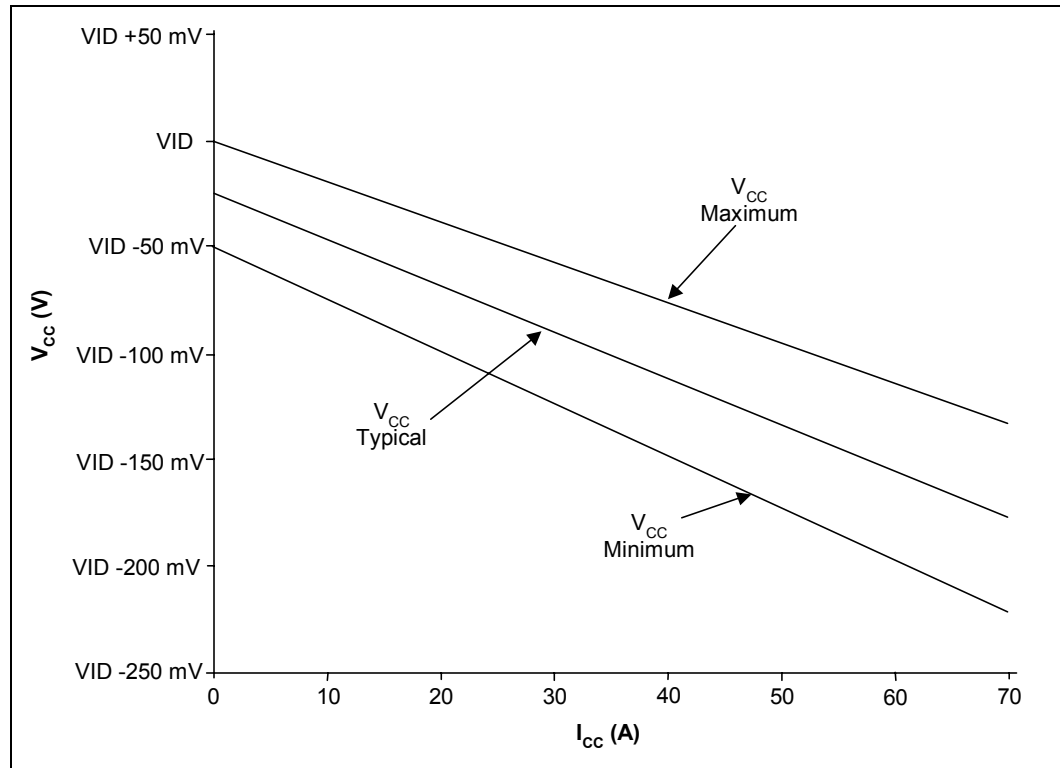
NOTES:
1. The loadline specification includes both static and transient limits.
2. Refer to Table 2-7 for specific offsets from VID voltage which apply to all VID settings.
3. The loadlines specify voltage limits at the die measured at V$_{CC\_SENSE}$ and V$_{SS\_SENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V$_{CC}$ and V$_{SS}$ pins. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* V$_{CC}$ and V$_{SS}$ socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is required to ensure reliable processor operation.

Table 2-8. Vcc Static and Transient Tolerance (For Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology, and Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 3.4 GHz)

Icc (A)	Voltage Deviation from VID Setting (V)[1,2,3]		
	Maximum	Typical	Minimum
0	0	-0.019	-0.038
5	-0.009	-0.029	-0.049
10	-0.019	-0.039	-0.059
15	-0.028	-0.049	-0.070
20	-0.037	-0.059	-0.080
25	-0.046	-0.068	-0.091
30	-0.056	-0.078	-0.101
35	-0.065	-0.088	-0.112
40	-0.074	-0.098	-0.122
45	-0.083	-0.108	-0.133
50	-0.093	-0.118	-0.143
55	-0.102	-0.128	-0.154
60	-0.111	-0.138	-0.164
65	-0.120	-0.147	-0.175
70	-0.130	-0.157	-0.185
75	-0.139	-0.167	-0.196
80	-0.148	-0.177	-0.206
85	-0.157	-0.187	-0.217
90	-0.167	-0.197	-0.227

NOTES:
1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on the following loadline figure.
3. The loadlines specify voltage limits at the die measured at V_{CC_SENSE} and V_{SS_SENSE} pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum* for V_{CC} and V_{SS} socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.

Figure 2-5. V$_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology, and Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 3.4 GHz)
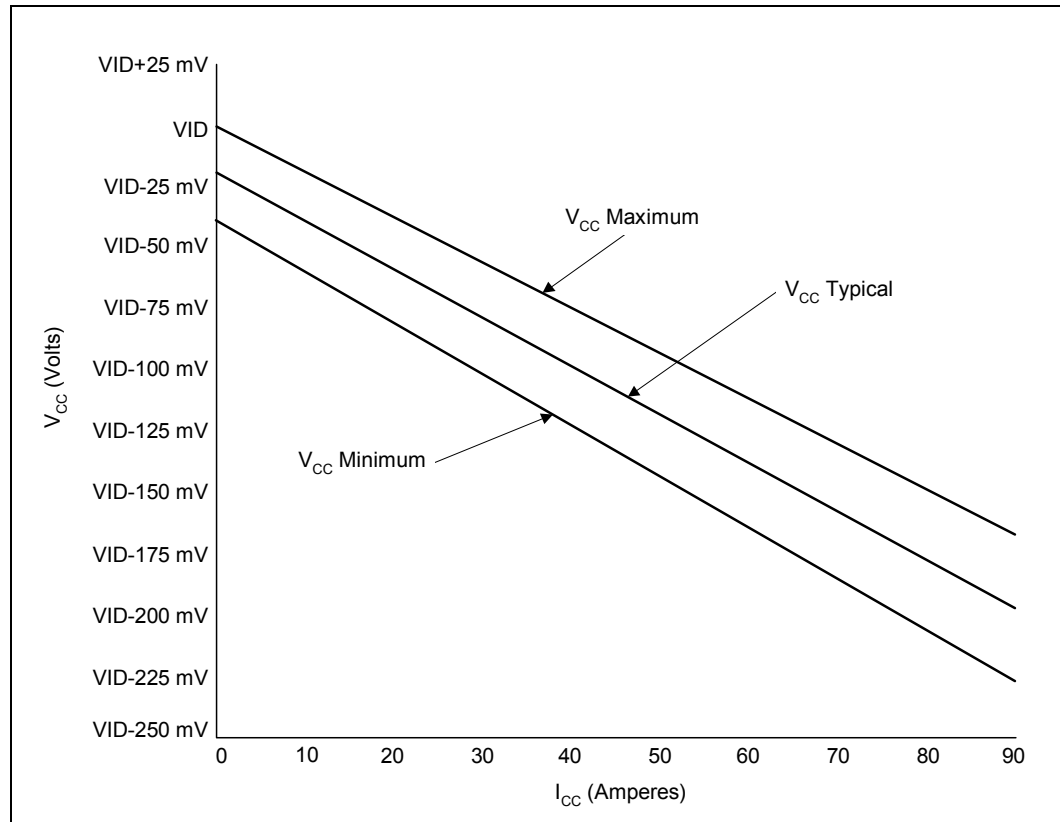
NOTES:
1. The loadline specification includes both static and transient limits.
2. Refer to Table 2-8 for specific offsets from VID voltage which apply to all VID settings.
3. The loadlines specify voltage limits at the die measured at V$_{CC\_SENSE}$ and V$_{SS\_SENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V$_{CC}$ and V$_{SS}$ pins. Refer to the *Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum* V$_{CC}$ and V$_{SS}$ socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.

Table 2-9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
GTLREF	Reference Voltage	2/3 V_{CC} – 2%	2/3 V_{CC} + 2%	V	
GTLREF Compatible	Reference Voltage	0.63 V_{CC} – 2%	0.63 V_{CC} +2%	V	10
V_{IH}	Input High Voltage	1.10*GTLREF	V_{CC}	V	2,5
V_{IL}	Input Low Voltage	0.0	0.9*GTLREF	V	3,5
V_{OH}	Output High Voltage	N/A	V_{CC}	V	6
I_{OL}	Output Low Current	N/A	50	mA	5
I_{HI}	Pin Leakage High	N/A	100	µA	7
I_{LO}	Pin Leakage Low	N/A	500	µA	8
R_{ON}	Buffer On Resistance	7	11	Ω	4
R_{ON} Compatible	Buffer On Resistance	8.4	13.2	Ω	4, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. Refer to processor I/O Buffer Models for I/V characteristics.
5. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
6. Vol max of 0.450 V is guaranteed when driving into a test load of 50 Ω as indicated in Figure 2-7.
7. Leakage to V_{SS} with pin held at V_{CC}.
8. Leakage to V_{CC} with Pin held at 300 mV.
9. R_{ON} value is defined for a platform that is forward compatible with future processors.
10. GTLREF value is defined for a platform that is forward compatible with future processors.

Table 2-10. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IH}	Input High Voltage Asynch GTL+	1.10*GTLREF	V_{CC}	V	3, 4
V_{IL}	Input Low Voltage Asynch GTL+	0	0.9*GTLREF	V	4
V_{OH}	Output High Voltage		V_{CC}	V	2, 3
I_{OL}	Output Low Current		50	mA	5, 7
I_{HI}	Pin Leakage High	N/A	100	µA	8
I_{LO}	Pin Leakage Low	N/A	500	µA	9
R_{on}	Buffer On Resistance Asynch GTL+	7	11	Ω	4,6
R_{ON} Compatible	Buffer On Resistance Asynch GTL+	8.4	13.2	Ω	4,6,10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
4. This specification applies to the asynchronous GTL+ signal group.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in Figure 2-7.
6. Refer to the processor I/O Buffer Models for I/V characteristics.
7. Vol max of 0.270 Volts is guaranteed when driving into a test load of 50 Ω as indicated in Figure 2-7 for the Asynchronous GTL+ signals.
8. Leakage to V_{SS} with pin held at V_{CC}.
9. Leakage to V_{CC} with Pin held at 300 mV.
10. R_{ON} value is defined for a platform that is forward compatible with future processors.

Table 2-11. PWRGOOD and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{HYS}	Input Hysteresis	200	300	mV	6
V_{T+}	Input Low to High Threshold Voltage	$1/2*(V_{CC}+V_{HYS\_MIN})$	$1/2*(V_{CC}+V_{HYS\_MAX})$	V	4
V_{T-}	Input High to Low Threshold Voltage	$1/2*(V_{CC}-V_{HYS\_MAX})$	$1/2*(V_{CC}-V_{HYS\_MIN})$	V	5
V_{OH}	Output High Voltage	N/A	V_{CC}	V	2,3,4
I_{OL}	Output Low Current	N/A	40	mA	5,6
I_{HI}	Pin Leakage High	N/A	100	µA	8
I_{LO}	Pin Leakage Low	N/A	500	µA	9
R_{ON}	Buffer On Resistance	8.75	13.75	Ω	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. Refer to I/O Buffer Models for I/V characteristics.
4. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in Figure 2-7.
6. Vol max of 0.320 V is guaranteed when driving into a test load of 50 Ω as indicated in Figure 2-7 for the TAP Signals.
7. V_{HYS} represents the amount of hysteresis, nominally centered about 1/2 V_{CC} for all TAP inputs.
8. Leakage to V_{SS} with pin held at V_{CC}.
9. Leakage to V_{CC} with Pin held at 300 mV.

Table 2-12. ITPCLKOUT[1:0] DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
Ron	Buffer On Resistance	27	46	Ω	2,3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. See Figure 2-6 for ITPCLKOUT[1:0] output buffer diagram.

Figure 2-6. ITPCLKOUT[1:0] Output Buffer Diagram
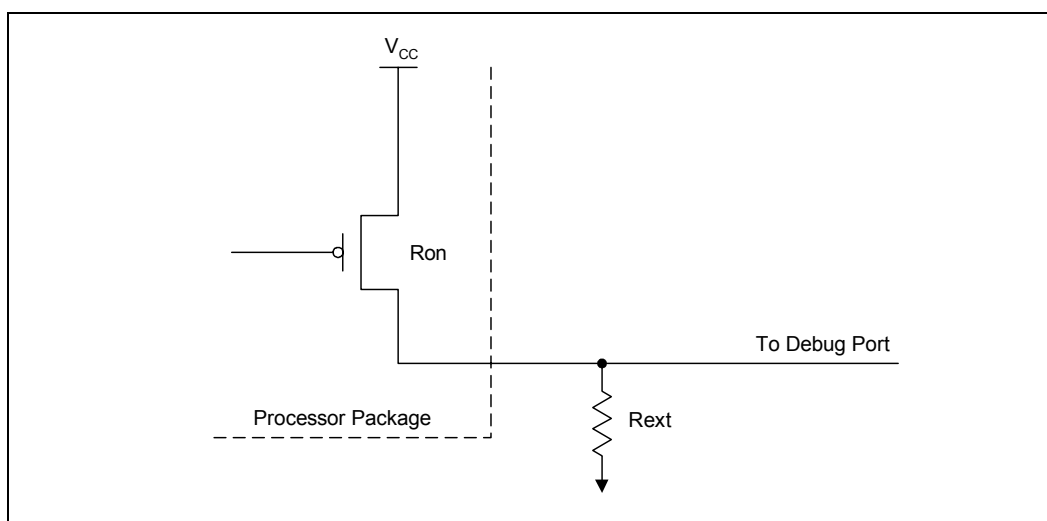
NOTES:
 1. See Table 2-12 for range of Ron.
 2. The V_{CC} referred to in this figure is the instantaneous Vcc.
 3. Refer to the *ITP 700 Debug Port Design Guide* and the appropriate platform design guidelines for the value of Rext.

Table 2-13. BSEL [1:0] and VID[4:0] DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
Ron (BSEL)	Buffer On Resistance	9.2	14.3	Ω	2
Ron (VID)	Buffer On Resistance	7.8	12.8	Ω	2
I_{HI}	Pin Leakage High	N/A	100	µA	3

NOTES:
 1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
 2. These parameters are not tested and are based on design simulations.
 3. Leakage to Vss with pin held at 2.50 V.

2.12 AGTL+ System Bus Specifications

Routing topology recommendations may be found in the appropriate platform design guide listed in Table 1-1. Termination resistors are not required for most AGTL+ signals because they are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

Table 2-14 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and is well-controlled. For more details on platform design, see the appropriate platform design guide.

Table 2-14. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF	Bus Reference Voltage	2/3 V_{CC} –2%	2/3 V_{CC}	2/3 V_{CC} +2%	V	2, 3, 6
GTLREF Compatible	Bus Reference Voltage	0.63 V_{CC} –2%	0.63 V_{CC}	0.63 V_{CC} +2%	V	2, 3, 6, 7
R_{TT}	Termination Resistance	45	50	55	Ω	4
R_{TT} Compatible	Termination Resistance	54	60	66	Ω	4, 7
COMP[1:0]	COMP Resistance	50.49	51	51.51	Ω	5
COMP[1:0] Compatible	COMP Resistance	61.3	61.9	62.5	Ω	5, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of V_{CC}.
3. GTLREF should be generated from V_{CC} by a voltage divider of 1% tolerance resistors or 1% tolerance, matched resistors. Refer to the appropriate Platform Design Guide for implementation details.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Refer to processor I/O buffer models for I/V characteristics.
5. COMP resistance must be provided on the system board with 1% tolerance resistors. See the appropriate Platform Design Guide for implementation details.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
7. The specifications are for a platform to be forward compatible with future processors. A compatible platform is one that is designed for some level of compatibility with future processors.

Figure 2-7. Test Circuit

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　　　Intel® Pentium® 4 Processor on 0.13 Micron Process Datasheet
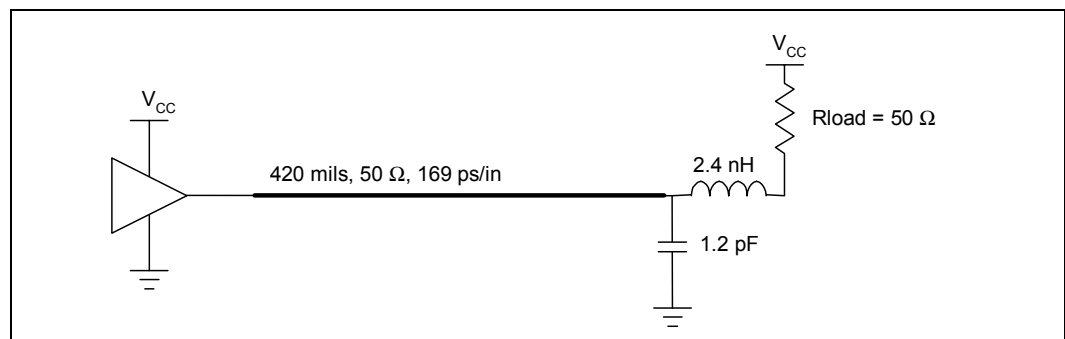
Package Mechanical Specifications 3

The Pentium 4 processor on 0.13 micron process is packaged in a Flip-Chip Pin Grid Array (FC-PGA2) package. Components of the package include an integrated heat spreader (IHS), processor die, and the substrate which is the pin carrier. Mechanical specifications for the processor are given in this section. See Section 1.1. for a terminology listing. The processor socket that accepts the Pentium 4 processor on 0.13 micron process is referred to as a 478-Pin micro PGA (mPGA478B) socket. See the *Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines* for complete details on the mPGA478B socket.

Note: For Figure 3-1 through Figure 3-8, the following notes apply:

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.

2. Figures and drawings labelled as "Reference Dimensions" are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are **not** checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.

3. Drawings are not to scale.

Note: Figure 3-1 is not to scale and is for reference only. The socket and system board are supplied as a reference only.

Figure 3-1. Exploded View of Processor Components on a System Board
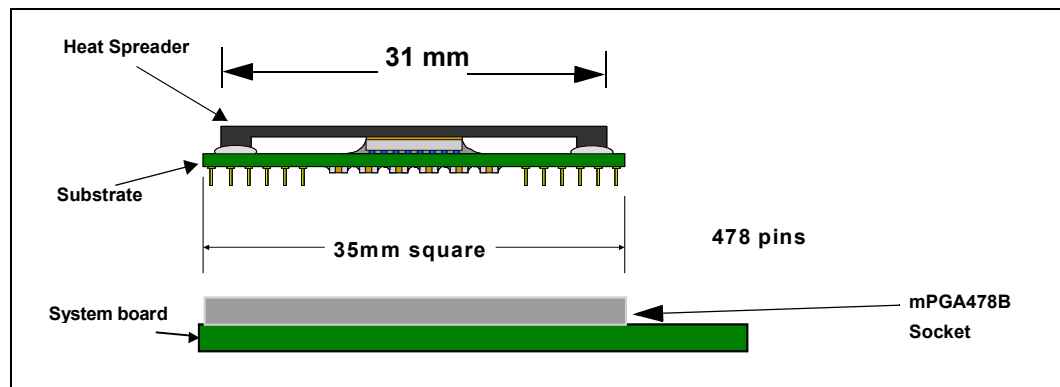
Figure 3-2. Processor Package
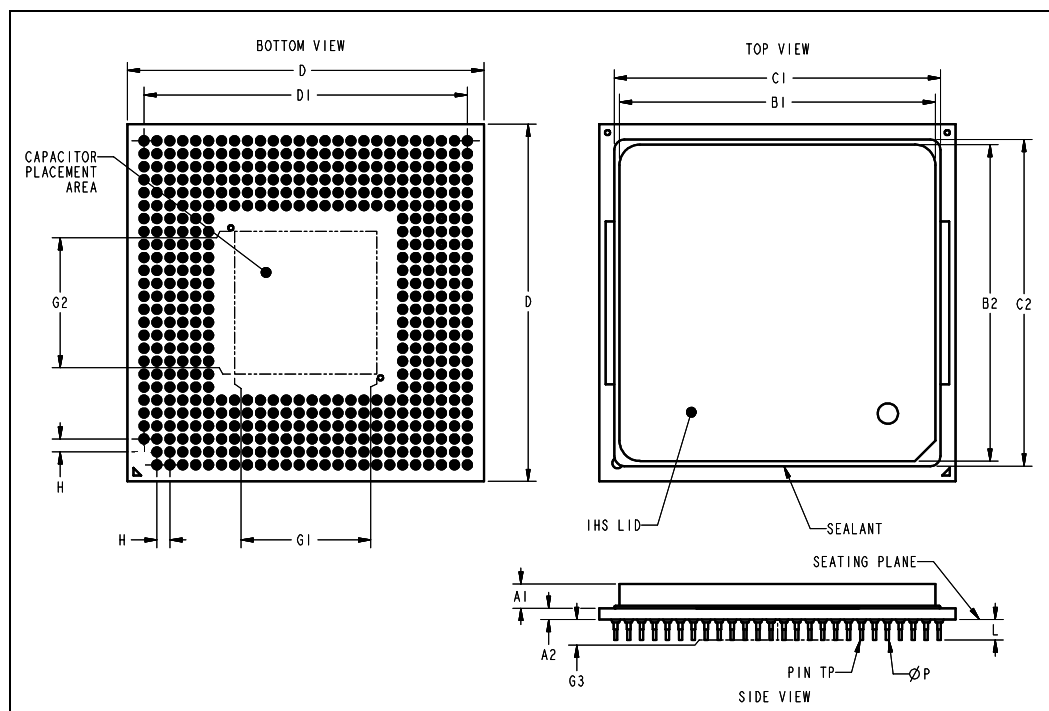
Table 3-1. Description Table for Processor Dimensions

Code Letter	Dimension (mm)			Notes
	Min	Nominal	Max	
A1	2.266	2.378	2.490	Original package (6 layer)
A2	0.980	1.080	1.180	Original package (6 layer)
A1	2.42	2.55	2.67	Alternate equivalent package (8 layer)
A2	1.13	1.20	1.27	Alternate equivalent package (8 layer)
B1	30.800	31.000	31.200	
B2	30.800	31.000	31.200	
C1			33.000	Includes placement tolerance
C2			33.000	Includes placement tolerance
D	34.900	35.000	35.100	
D1	31.500	31.750	32.000	
G1			13.970	Keep-In Zone dimension
G2			13.970	Keep-In Zone dimension
G3			1.250	Keep-In Zone dimension
H		1.270		
L	1.950	2.030	2.110	
ϕP	0.280	0.305	0.330	
PIN TP			0.254	Diametric True Position (Pin-to-Pin)
IHS Flatness			0.05	

Figure 3-3 details the keep-in specification for pin-side components. The Pentium 4 processor on 0.13 micron process may contain pin-side capacitors mounted to the processor package.

Figure 3-5 details the flatness and tilt specifications for the IHS. Tilt is measured with the reference datum set to the bottom of the processor susbstrate.

Figure 3-3. Processor Cross-Section and Keep-In
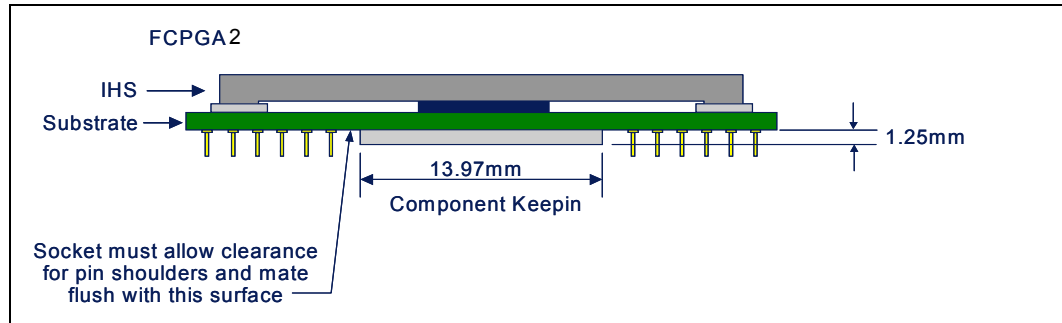
Figure 3-4. Processor Pin Detail
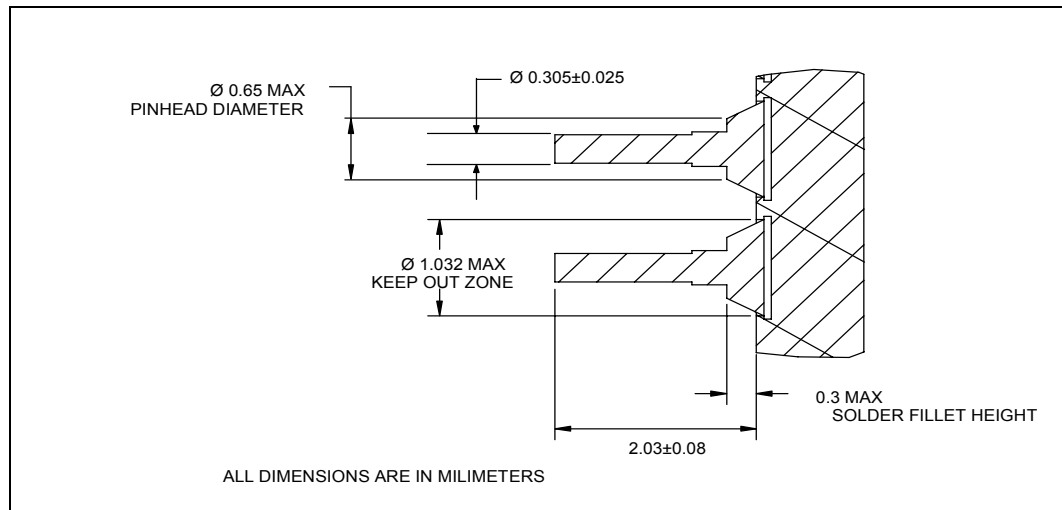
NOTES:
1. Pin plating consists of 0.2 micrometers Au over 2.0 micrometer Ni.
2. 0.254 mm diametric true position, pin-to-pin.

Figure 3-5. IHS Flatness Specification
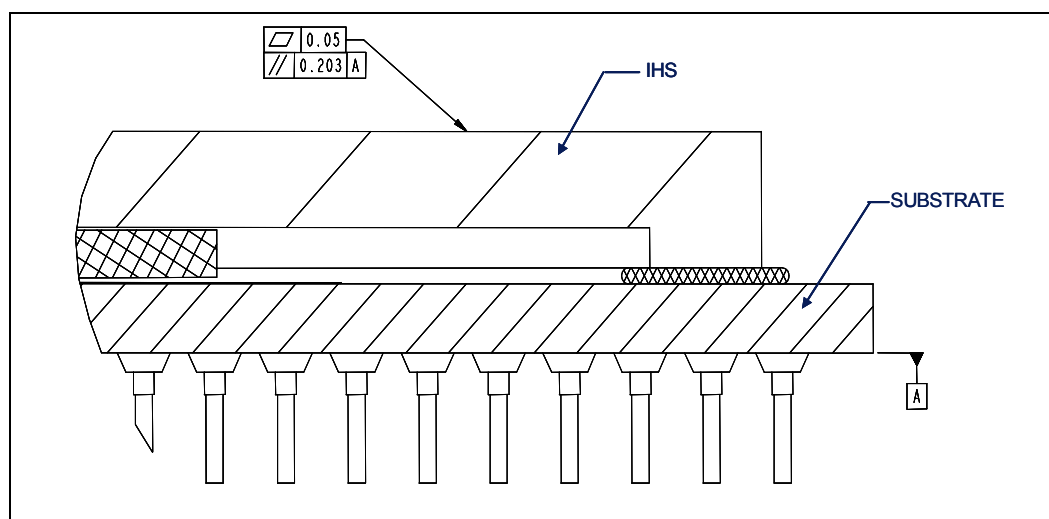
NOTES:
 1. Flatness is specific as overall, not per unit of length.
 2. All Dimensions are in millimeters.

3.1 Package Load Specifications

Table 3-2 provides dynamic and static load specifications for the processor IHS. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heatsink-to-processor thermal interface contact. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.

Table 3-2. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Notes
Static	100	lbf	1, 2
Dynamic	200	lbf	1, 3

NOTES:
 1. This specification applies to a uniform compressive load.
 2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
 3. Dynamic loading specifications are defined assuming a maximum duration of 11 ms and 200 lbf is achieved by superimposing a 100 lbf dynamic load (1 lbm at 50 g) on the static compressive load.

3.2   Processor Insertion Specifications

The Pentium 4 processor on 0.13 micron process can be inserted and removed 15 times from a mPGA478B socket meeting the *Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines* document.

3.3   Processor Mass Specifications

Table 3-3 specifies the processor's mass. This includes all components which make up the entire processor product.

Table 3-3. Processor Mass

Processor	Mass (grams)
Intel® Pentium® 4 processor on 0.13 micron process	19

3.4   Processor Materials

The Pentium 4 processor on 0.13 micron process is assembled from several components. The basic material properties are described in Table 3-4.

Table 3-4. Processor Material Properties

Component	Material
Integrated Heat Spreader	Nickel over copper
Substrate	Fiber-reinforced resin
Substrate pins	Gold over nickel

3.5 Processor Markings

Figure 3-6 and Figure 3-7 detail the processor top-side markings and is provided to aid in the identification of the Pentium 4 processors on 0.13 micron process.

Figure 3-6. Processor Markings (Processors with Fixed VID)
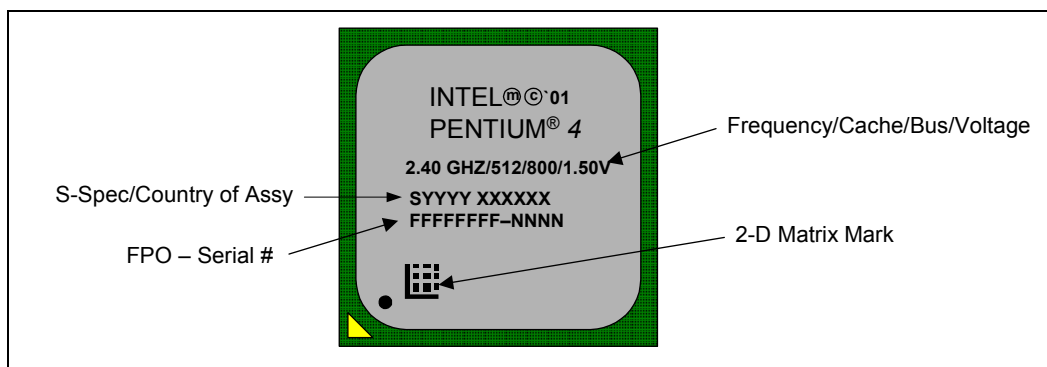
Figure 3-7. Processor Markings (Processors with Multiple VID)
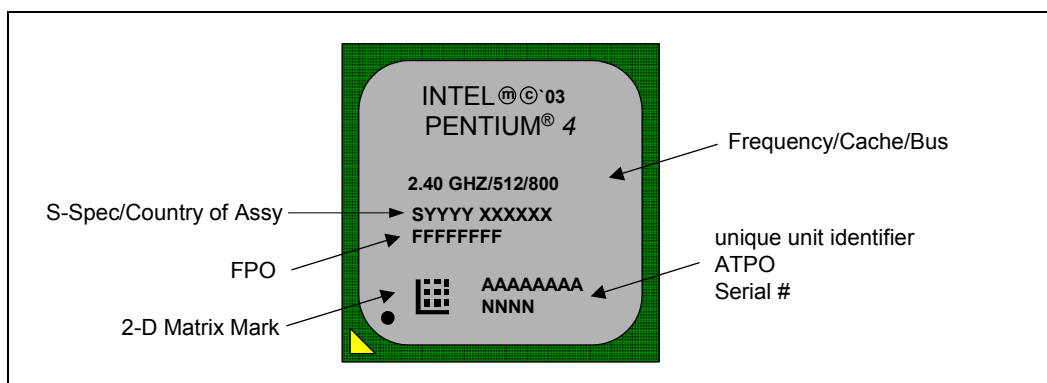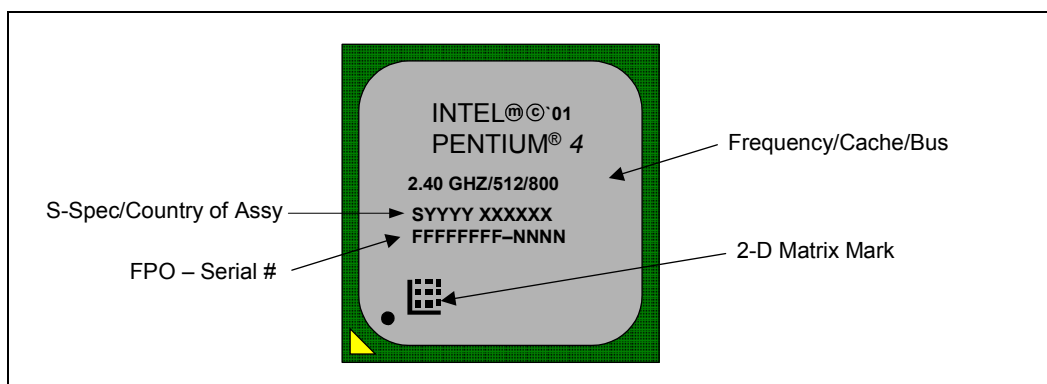
NOTE: Intel will continue to ship old and new marked parts until old mark inventory has been depleted.

Figure 3-8. The Coordinates of the Processor Pins As Viewed from the Top of the Package

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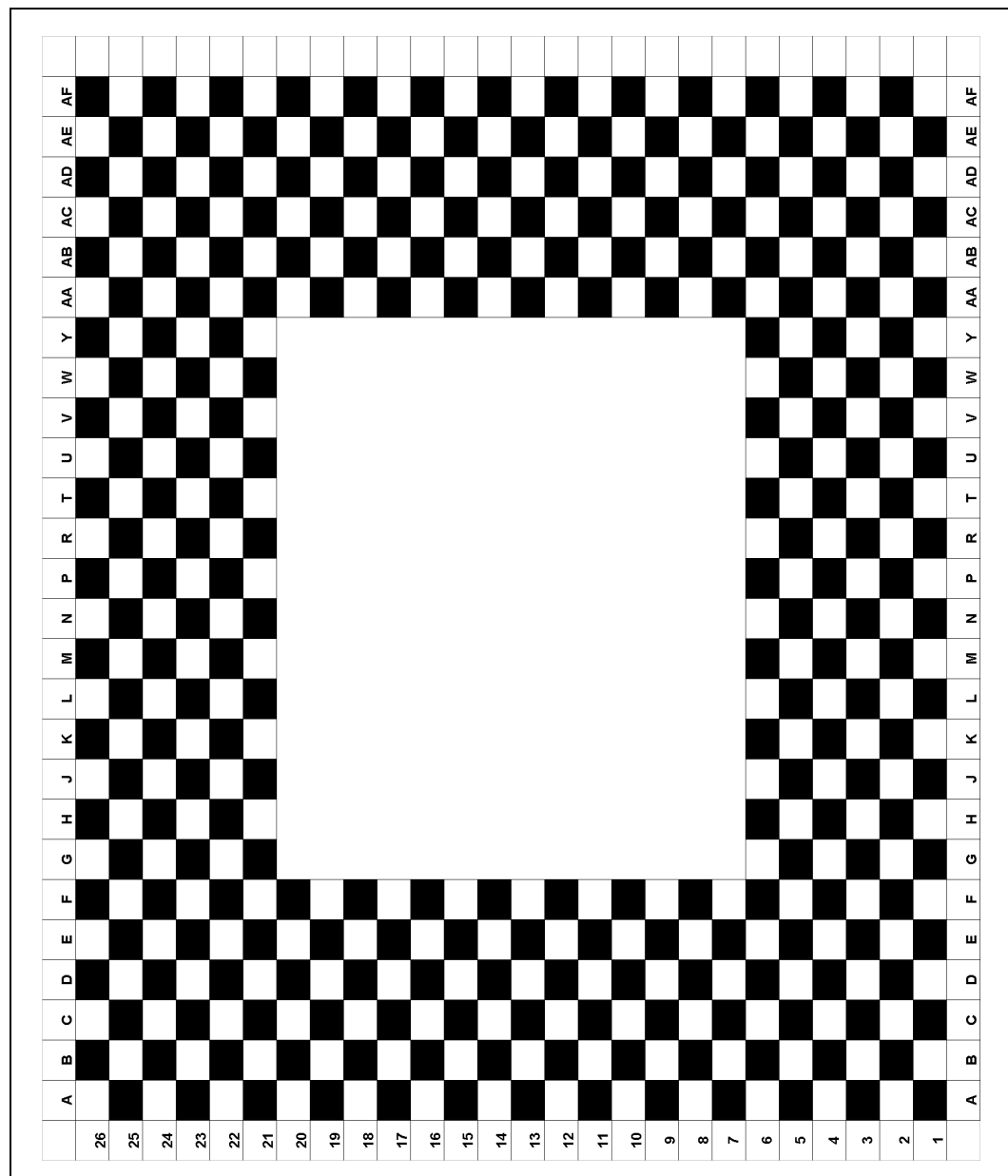
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Pin Lists and Signal Descriptions   **4**

4.1   Processor Pin Assignments

This section contains pin lists for the Pentium 4 processor on 0.13 micron process. Table 4-1 is ordered alphabetically by pin name; Table 4-2 is ordered alphabetically by pin number.

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A3#	K2	Source Synch	Input/Output
A4#	K4	Source Synch	Input/Output
A5#	L6	Source Synch	Input/Output
A6#	K1	Source Synch	Input/Output
A7#	L3	Source Synch	Input/Output
A8#	M6	Source Synch	Input/Output
A9#	L2	Source Synch	Input/Output
A10#	M3	Source Synch	Input/Output
A11#	M4	Source Synch	Input/Output
A12#	N1	Source Synch	Input/Output
A13#	M1	Source Synch	Input/Output
A14#	N2	Source Synch	Input/Output
A15#	N4	Source Synch	Input/Output
A16#	N5	Source Synch	Input/Output
A17#	T1	Source Synch	Input/Output
A18#	R2	Source Synch	Input/Output
A19#	P3	Source Synch	Input/Output
A20#	P4	Source Synch	Input/Output
A21#	R3	Source Synch	Input/Output
A22#	T2	Source Synch	Input/Output
A23#	U1	Source Synch	Input/Output
A24#	P6	Source Synch	Input/Output
A25#	U3	Source Synch	Input/Output
A26#	T4	Source Synch	Input/Output
A27#	V2	Source Synch	Input/Output
A28#	R6	Source Synch	Input/Output
A29#	W1	Source Synch	Input/Output
A30#	T5	Source Synch	Input/Output
A31#	U4	Source Synch	Input/Output
A32#	V3	Source Synch	Input/Output
A33#	W2	Source Synch	Input/Output
A34#	Y1	Source Synch	Input/Output
A35#	AB1	Source Synch	Input/Output
A20M#	C6	Asynch GTL+	Input
ADS#	G1	Common Clock	Input/Output
ADSTB0#	L5	Source Synch	Input/Output
ADSTB1#	R5	Source Synch	Input/Output
AP0#	AC1	Common Clock	Input/Output
AP1#	V5	Common Clock	Input/Output
BCLK0	AF22	Bus Clock	Input
BCLK1	AF23	Bus Clock	Input
BINIT#	AA3	Common Clock	Input/Output
BNR#	G2	Common Clock	Input/Output
BPM0#	AC6	Common Clock	Input/Output

Pin Name	Pin Number	Signal Buffer Type	Direction
BPM1#	AB5	Common Clock	Input/Output
BPM2#	AC4	Common Clock	Input/Output
BPM3#	Y6	Common Clock	Input/Output
BPM4#	AA5	Common Clock	Input/Output
BPM5#	AB4	Common Clock	Input/Output
BPRI#	D2	Common Clock	Input
BR0#	H6	Common Clock	Input/Output
BSEL0	AD6	Power/Other	Output
BSEL1	AD5	Power/Other	Output
COMP0	L24	Power/Other	Input/Output
COMP1	P1	Power/Other	Input/Output
D0#	B21	Source Synch	Input/Output
D1#	B22	Source Synch	Input/Output
D2#	A23	Source Synch	Input/Output
D3#	A25	Source Synch	Input/Output
D4#	C21	Source Synch	Input/Output
D5#	D22	Source Synch	Input/Output
D6#	B24	Source Synch	Input/Output
D7#	C23	Source Synch	Input/Output
D8#	C24	Source Synch	Input/Output
D9#	B25	Source Synch	Input/Output
D10#	G22	Source Synch	Input/Output
D11#	H21	Source Synch	Input/Output
D12#	C26	Source Synch	Input/Output
D13#	D23	Source Synch	Input/Output
D14#	J21	Source Synch	Input/Output
D15#	D25	Source Synch	Input/Output
D16#	H22	Source Synch	Input/Output
D17#	E24	Source Synch	Input/Output
D18#	G23	Source Synch	Input/Output
D19#	F23	Source Synch	Input/Output
D20#	F24	Source Synch	Input/Output
D21#	E25	Source Synch	Input/Output
D22#	F26	Source Synch	Input/Output
D23#	D26	Source Synch	Input/Output
D24#	L21	Source Synch	Input/Output
D25#	G26	Source Synch	Input/Output
D26#	H24	Source Synch	Input/Output
D27#	M21	Source Synch	Input/Output
D28#	L22	Source Synch	Input/Output
D29#	J24	Source Synch	Input/Output
D30#	K23	Source Synch	Input/Output
D31#	H25	Source Synch	Input/Output
D32#	M23	Source Synch	Input/Output

Intel® Pentium® 4 Processor on 0.13 Micron Process Datasheet

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D33#	N22	Source Synch	Input/Output
D34#	P21	Source Synch	Input/Output
D35#	M24	Source Synch	Input/Output
D36#	N23	Source Synch	Input/Output
D37#	M26	Source Synch	Input/Output
D38#	N26	Source Synch	Input/Output
D39#	N25	Source Synch	Input/Output
D40#	R21	Source Synch	Input/Output
D41#	P24	Source Synch	Input/Output
D42#	R25	Source Synch	Input/Output
D43#	R24	Source Synch	Input/Output
D44#	T26	Source Synch	Input/Output
D45#	T25	Source Synch	Input/Output
D46#	T22	Source Synch	Input/Output
D47#	T23	Source Synch	Input/Output
D48#	U26	Source Synch	Input/Output
D49#	U24	Source Synch	Input/Output
D50#	U23	Source Synch	Input/Output
D51#	V25	Source Synch	Input/Output
D52#	U21	Source Synch	Input/Output
D53#	V22	Source Synch	Input/Output
D54#	V24	Source Synch	Input/Output
D55#	W26	Source Synch	Input/Output
D56#	Y26	Source Synch	Input/Output
D57#	W25	Source Synch	Input/Output
D58#	Y23	Source Synch	Input/Output
D59#	Y24	Source Synch	Input/Output
D60#	Y21	Source Synch	Input/Output
D61#	AA25	Source Synch	Input/Output
D62#	AA22	Source Synch	Input/Output
D63#	AA24	Source Synch	Input/Output
DBI0#	E21	Source Synch	Input/Output
DBI1#	G25	Source Synch	Input/Output
DBI2#	P26	Source Synch	Input/Output
DBI3#	V21	Source Synch	Input/Output
DBR#	AE25	Power/Other	Output
DBSY#	H5	Common Clock	Input/Output
DEFER#	E2	Common Clock	Input
DP0#	J26	Common Clock	Input/Output
DP1#	K25	Common Clock	Input/Output
DP2#	K26	Common Clock	Input/Output
DP3#	L25	Common Clock	Input/Output
DRDY#	H2	Common Clock	Input/Output
DSTBN0#	E22	Source Synch	Input/Output

Pin Name	Pin Number	Signal Buffer Type	Direction
DSTBN1#	K22	Source Synch	Input/Output
DSTBN2#	R22	Source Synch	Input/Output
DSTBN3#	W22	Source Synch	Input/Output
DSTBP0#	F21	Source Synch	Input/Output
DSTBP1#	J23	Source Synch	Input/Output
DSTBP2#	P23	Source Synch	Input/Output
DSTBP3#	W23	Source Synch	Input/Output
FERR#	B6	Asynch AGL+	Output
GTLREF	AA21	Power/Other	Input
GTLREF	AA6	Power/Other	Input
GTLREF	F20	Power/Other	Input
GTLREF	F6	Power/Other	Input
HIT#	F3	Common Clock	Input/Output
HITM#	E3	Common Clock	Input/Output
IERR#	AC3	Common Clock	Output
IGNNE#	B2	Asynch GTL+	Input
IMPSEL	AE26	Power/Other	Input
INIT#	W5	Asynch GTL+	Input
ITPCLKOUT0	AA20	Power/Other	Output
ITPCLKOUT1	AB22	Power/Other	Output
ITP_CLK0	AC26	TAP	input
ITP_CLK1	AD26	TAP	input
LINT0	D1	Asynch GTL+	Input
LINT1	E5	Asynch GTL+	Input
LOCK#	G4	Common Clock	Input/Output
MCERR#	V6	Common Clock	Input/Output
PROCHOT#	C3	Asynch GTL+	Input/Output
PWRGOOD	AB23	Power/Other	Input
REQ0#	J1	Source Synch	Input/Output
REQ1#	K5	Source Synch	Input/Output
REQ2#	J4	Source Synch	Input/Output
REQ3#	J3	Source Synch	Input/Output
REQ4#	H3	Source Synch	Input/Output
RESERVED	A22		
RESERVED	A7		
RESERVED	AD2		
RESERVED	AD3		
RESERVED	AE21		
RESERVED	AF3		
RESERVED	AF24		
RESERVED	AF25		
RESET#	AB25	Common Clock	Input
RS0#	F1	Common Clock	Input
RS1#	G5	Common Clock	Input

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
RS2#	F4	Common Clock	Input
RSP#	AB2	Common Clock	Input
SKTOCC#	AF26	Power/Other	Output
SLP#	AB26	Asynch GTL+	Input
SMI#	B5	Asynch GTL+	Input
STPCLK#	Y4	Asynch GTL+	Input
TCK	D4	TAP	Input
TDI	C1	TAP	Input
TDO	D5	TAP	Output
TESTHI0	AD24	Power/Other	Input
TESTHI1	AA2	Power/Other	Input
TESTHI2	AC21	Power/Other	Input
TESTHI3	AC20	Power/Other	Input
TESTHI4	AC24	Power/Other	Input
TESTHI5	AC23	Power/Other	Input
TESTHI8	U6	Power/Other	Input
TESTHI9	W4	Power/Other	Input
TESTHI10	Y3	Power/Other	Input
TESTHI11	A6	Power/Other	Input
TESTHI12	AD25	Power/Other	Input
THERMDA	B3	Power/Other	
THERMDC	C4	Power/Other	
THERMTRIP#	A2	Asynch GTL+	Output
TMS	F7	TAP	Input
TRDY#	J6	Common Clock	Input
TRST#	E6	TAP	Input
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A14	Power/Other	
VCC	A16	Power/Other	
VCC	A18	Power/Other	
VCC	A20	Power/Other	
VCC	A8	Power/Other	
VCC	AA10	Power/Other	
VCC	AA12	Power/Other	
VCC	AA14	Power/Other	
VCC	AA16	Power/Other	
VCC	AA18	Power/Other	
VCC	AA8	Power/Other	
VCC	AB11	Power/Other	
VCC	AB13	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB19	Power/Other	

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC14	Power/Other	
VCC	AC16	Power/Other	
VCC	AC18	Power/Other	
VCC	AC8	Power/Other	
VCC	AD11	Power/Other	
VCC	AD13	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD19	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE16	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AE6	Power/Other	
VCC	AE8	Power/Other	
VCC	AF11	Power/Other	
VCC	AF13	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF19	Power/Other	
VCC	AF2	Power/Other	
VCC	AF21	Power/Other	
VCC	AF5	Power/Other	
VCC	AF7	Power/Other	
VCC	AF9	Power/Other	
VCC	B11	Power/Other	
VCC	B13	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B19	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C14	Power/Other	
VCC	C16	Power/Other	

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AD20	Power/Other	
VCCIOPLL	AE23	Power/Other	
VCC_SENSE	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VID0	AE5	Power/Other	Output
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VSS	D10	Power/Other	
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	
VSS	A3	Power/Other	
VSS	A9	Power/Other	
VSS	AA1	Power/Other	

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AA11	Power/Other	
VSS	AA13	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA19	Power/Other	
VSS	AA23	Power/Other	
VSS	AA26	Power/Other	
VSS	AA4	Power/Other	
VSS	AA7	Power/Other	
VSS	AA9	Power/Other	
VSS	AB10	Power/Other	
VSS	AB12	Power/Other	
VSS	AB14	Power/Other	
VSS	AB16	Power/Other	
VSS	AB18	Power/Other	
VSS	AB20	Power/Other	
VSS	AB21	Power/Other	
VSS	AB24	Power/Other	
VSS	AB3	Power/Other	
VSS	AB6	Power/Other	
VSS	AB8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC13	Power/Other	
VSS	AC15	Power/Other	
VSS	AC17	Power/Other	
VSS	AC19	Power/Other	
VSS	AC2	Power/Other	
VSS	AC22	Power/Other	
VSS	AC25	Power/Other	
VSS	AC5	Power/Other	
VSS	AC7	Power/Other	
VSS	AC9	Power/Other	
VSS	AD1	Power/Other	
VSS	AD10	Power/Other	
VSS	AD12	Power/Other	
VSS	AD14	Power/Other	
VSS	AD16	Power/Other	
VSS	AD18	Power/Other	
VSS	AD21	Power/Other	
VSS	AD23	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE13	Power/Other	

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AE15	Power/Other	
VSS	AE17	Power/Other	
VSS	AE19	Power/Other	
VSS	AE22	Power/Other	
VSS	AE24	Power/Other	
VSS	AE7	Power/Other	
VSS	AE9	Power/Other	
VSS	AF1	Power/Other	
VSS	AF10	Power/Other	
VSS	AF12	Power/Other	
VSS	AF14	Power/Other	
VSS	AF16	Power/Other	
VSS	AF18	Power/Other	
VSS	AF20	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	B10	Power/Other	
VSS	B12	Power/Other	
VSS	B14	Power/Other	
VSS	B16	Power/Other	
VSS	B18	Power/Other	
VSS	B20	Power/Other	
VSS	B23	Power/Other	
VSS	B26	Power/Other	
VSS	B4	Power/Other	
VSS	B8	Power/Other	
VSS	C11	Power/Other	
VSS	C13	Power/Other	
VSS	C15	Power/Other	
VSS	C17	Power/Other	
VSS	C19	Power/Other	
VSS	C2	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	C5	Power/Other	
VSS	C7	Power/Other	
VSS	C9	Power/Other	
VSS	D12	Power/Other	
VSS	D14	Power/Other	
VSS	D16	Power/Other	
VSS	D18	Power/Other	
VSS	D20	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	D3	Power/Other	
VSS	D6	Power/Other	
VSS	D8	Power/Other	
VSS	E1	Power/Other	
VSS	E11	Power/Other	
VSS	E13	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E19	Power/Other	
VSS	E23	Power/Other	
VSS	E26	Power/Other	
VSS	E4	Power/Other	
VSS	E7	Power/Other	
VSS	E9	Power/Other	
VSS	F10	Power/Other	
VSS	F12	Power/Other	
VSS	F14	Power/Other	
VSS	F16	Power/Other	
VSS	F18	Power/Other	
VSS	F2	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	G21	Power/Other	
VSS	G24	Power/Other	
VSS	G3	Power/Other	
VSS	G6	Power/Other	
VSS	H1	Power/Other	
VSS	H23	Power/Other	
VSS	H26	Power/Other	
VSS	H4	Power/Other	
VSS	J2	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	J5	Power/Other	
VSS	K21	Power/Other	
VSS	K24	Power/Other	
VSS	K3	Power/Other	
VSS	K6	Power/Other	
VSS	L1	Power/Other	
VSS	L23	Power/Other	
VSS	L26	Power/Other	
VSS	L4	Power/Other	

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Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	M2	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	M5	Power/Other	
VSS	N21	Power/Other	
VSS	N24	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	P2	Power/Other	
VSS	P22	Power/Other	
VSS	P25	Power/Other	
VSS	P5	Power/Other	
VSS	R1	Power/Other	
VSS	R23	Power/Other	
VSS	R26	Power/Other	
VSS	R4	Power/Other	
VSS	T21	Power/Other	
VSS	T24	Power/Other	
VSS	T3	Power/Other	

Table 4-1. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	T6	Power/Other	
VSS	U2	Power/Other	
VSS	U22	Power/Other	
VSS	U25	Power/Other	
VSS	U5	Power/Other	
VSS	V1	Power/Other	
VSS	V23	Power/Other	
VSS	V26	Power/Other	
VSS	V4	Power/Other	
VSS	W21	Power/Other	
VSS	W24	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	Y2	Power/Other	
VSS	Y22	Power/Other	
VSS	Y25	Power/Other	
VSS	Y5	Power/Other	
VSSA	AD22	Power/Other	
VSS_SENSE	A4	Power/Other	Output

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A2	THERMTRIP#	Asynch GTL+	Output
A3	VSS	Power/Other	
A4	VSS_SENSE	Power/Other	Output
A5	VCC_SENSE	Power/Other	Output
A6	TESTHI11	Power/Other	Input
A7	RESERVED		
A8	VCC	Power/Other	
A9	VSS	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VSS	Power/Other	
A14	VCC	Power/Other	
A15	VSS	Power/Other	
A16	VCC	Power/Other	
A17	VSS	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	VSS	Power/Other	
A22	RESERVED		
A23	D2#	Source Synch	Input/Output
A24	VSS	Power/Other	
A25	D3#	Source Synch	Input/Output
A26	VSS	Power/Other	
AA1	VSS	Power/Other	
AA2	TESTHI1	Power/Other	Input
AA3	BINIT#	Common Clock	Input/Output
AA4	VSS	Power/Other	
AA5	BPM4#	Common Clock	Input/Output
AA6	GTLREF	Power/Other	Input
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA9	VSS	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VSS	Power/Other	
AA14	VCC	Power/Other	
AA15	VSS	Power/Other	
AA16	VCC	Power/Other	
AA17	VSS	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AA20	ITPCLK[0]	Power/Other	Output
AA21	GTLREF	Power/Other	Input
AA22	D62#	Source Synch	Input/Output
AA23	VSS	Power/Other	
AA24	D63#	Source Synch	Input/Output
AA25	D61#	Source Synch	Input/Output
AA26	VSS	Power/Other	
AB1	A35#	Source Synch	Input/Output
AB2	RSP#	Common Clock	Input
AB3	VSS	Power/Other	
AB4	BPM5#	Common Clock	Input/Output
AB5	BPM1#	Common Clock	Input/Output
AB6	VSS	Power/Other	
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VSS	Power/Other	
AB11	VCC	Power/Other	
AB12	VSS	Power/Other	
AB13	VCC	Power/Other	
AB14	VSS	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VSS	Power/Other	
AB19	VCC	Power/Other	
AB20	VSS	Power/Other	
AB21	VSS	Power/Other	
AB22	ITPCLK[1]	Power/Other	Output
AB23	PWRGOOD	Power/Other	Input
AB24	VSS	Power/Other	
AB25	RESET#	Common Clock	Input
AB26	SLP#	Asynch GTL+	Input
AC1	AP#[0]	Common Clock	Input/Output
AC2	VSS	Power/Other	
AC3	IERR#	Common Clock	Output
AC4	BPM2#	Common Clock	Input/Output
AC5	VSS	Power/Other	
AC6	BPM0#	Common Clock	Input/Output
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC9	VSS	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AC12	VCC	Power/Other	
AC13	VSS	Power/Other	
AC14	VCC	Power/Other	
AC15	VSS	Power/Other	
AC16	VCC	Power/Other	
AC17	VSS	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	TESTHI3	Power/Other	Input
AC21	TESTHI2	Power/Other	Input
AC22	VSS	Power/Other	
AC23	TESTHI5	Power/Other	Input
AC24	TESTHI4	Power/Other	Input
AC25	VSS	Power/Other	
AC26	ITP_CLK0	TAP	input
AD1	VSS	Power/Other	
AD2	RESERVED		
AD3	RESERVED		
AD4	VSS	Power/Other	
AD5	BSEL1	Power/Other	Output
AD6	BSEL0	Power/Other	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VSS	Power/Other	
AD11	VCC	Power/Other	
AD12	VSS	Power/Other	
AD13	VCC	Power/Other	
AD14	VSS	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VSS	Power/Other	
AD19	VCC	Power/Other	
AD20	VCCA	Power/Other	
AD21	VSS	Power/Other	
AD22	VSSA	Power/Other	
AD23	VSS	Power/Other	
AD24	TESTHI0	Power/Other	Input
AD25	TESTHI12	Power/Other	Input
AD26	ITP_CLK1	TAP	input
AE1	VID4	Power/Other	Output
AE2	VID3	Power/Other	Output
AE3	VID2	Power/Other	Output

Pin Number	Pin Name	Signal Buffer Type	Direction
AE4	VID1	Power/Other	Output
AE5	VID0	Power/Other	Output
AE6	VCC	Power/Other	
AE7	VSS	Power/Other	
AE8	VCC	Power/Other	
AE9	VSS	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VSS	Power/Other	
AE16	VCC	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	RESERVED		
AE22	VSS	Power/Other	
AE23	VCCIOPLL	Power/Other	
AE24	VSS	Power/Other	
AE25	DBR#	Asynch GTL+	Output
AE26	IMPSEL	Power/Other	Input
AF1	VSS	Power/Other	
AF2	VCC	Power/Other	
AF3	RESERVED		
AF4	VCCVID	Power/Other	Input
AF5	VCC	Power/Other	
AF6	VSS	Power/Other	
AF7	VCC	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VSS	Power/Other	
AF13	VCC	Power/Other	
AF14	VSS	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VSS	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AF22	BCLK[0]	Bus Clock	Input
AF23	BCLK[1]	Bus Clock	Input
AF24	RESERVED		
AF25	RESERVED		
AF26	SKTOCC#	Power/Other	Output
B2	IGNNE#	Asynch GTL+	Input
B3	THERMDA	Power/Other	
B4	VSS	Power/Other	
B5	SMI#	Asynch GTL+	Input
B6	FERR#	Asynch AGL+	Output
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VSS	Power/Other	
B11	VCC	Power/Other	
B12	VSS	Power/Other	
B13	VCC	Power/Other	
B14	VSS	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VSS	Power/Other	
B19	VCC	Power/Other	
B20	VSS	Power/Other	
B21	D0#	Source Synch	Input/Output
B22	D01#	Source Synch	Input/Output
B23	VSS	Power/Other	
B24	D6#	Source Synch	Input/Output
B25	D9#	Source Synch	Input/Output
B26	VSS	Power/Other	
C1	TDI	TAP	Input
C2	VSS	Power/Other	
C3	PROCHOT#	Asynch GTL+	Input/Output
C4	THERMDC	Power/Other	
C5	VSS	Power/Other	
C6	A20M#	Asynch GTL+	Input
C7	VSS	Power/Other	
C8	VCC	Power/Other	
C9	VSS	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VSS	Power/Other	
C14	VCC	Power/Other	

Pin Number	Pin Name	Signal Buffer Type	Direction
C15	VSS	Power/Other	
C16	VCC	Power/Other	
C17	VSS	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	VCC	Power/Other	
C21	D4#	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	D7#	Source Synch	Input/Output
C24	D8#	Source Synch	Input/Output
C25	VSS	Power/Other	
C26	D12#	Source Synch	Input/Output
D1	LINT0	Asynch GTL+	Input
D2	BPRI#	Common Clock	Input
D3	VSS	Power/Other	
D4	TCK	TAP	Input
D5	TDO	TAP	Output
D6	VSS	Power/Other	
D7	VCC	Power/Other	
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VSS	Power/Other	
D11	VCC	Power/Other	
D12	VSS	Power/Other	
D13	VCC	Power/Other	
D14	VSS	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VSS	Power/Other	
D19	VCC	Power/Other	
D20	VSS	Power/Other	
D21	VSS	Power/Other	
D22	D5#	Source Synch	Input/Output
D23	D13#	Source Synch	Input/Output
D24	VSS	Power/Other	
D25	D15#	Source Synch	Input/Output
D26	D23#	Source Synch	Input/Output
E1	VSS	Power/Other	
E2	DEFER#	Common Clock	Input
E3	HITM#	Common Clock	Input/Output
E4	VSS	Power/Other	
E5	LINT1	Asynch GTL+	Input
E6	TRST#	TAP	Input

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
E7	VSS	Power/Other	
E8	VCC	Power/Other	
E9	VSS	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VSS	Power/Other	
E14	VCC	Power/Other	
E15	VSS	Power/Other	
E16	VCC	Power/Other	
E17	VSS	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	DBI0#	Source Synch	Input/Output
E22	DSTBN0#	Source Synch	Input/Output
E23	VSS	Power/Other	
E24	D17#	Source Synch	Input/Output
E25	D21#	Source Synch	Input/Output
E26	VSS	Power/Other	
F1	RS0#	Common Clock	Input
F2	VSS	Power/Other	
F3	HIT#	Common Clock	Input/Output
F4	RS2#	Common Clock	Input
F5	VSS	Power/Other	
F6	GTLREF	Power/Other	Input
F7	TMS	TAP	Input
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VSS	Power/Other	
F11	VCC	Power/Other	
F12	VSS	Power/Other	
F13	VCC	Power/Other	
F14	VSS	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VSS	Power/Other	
F19	VCC	Power/Other	
F20	GTLREF	Power/Other	Input
F21	DSTBP0#	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	D19#	Source Synch	Input/Output
F24	D20#	Source Synch	Input/Output

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
F25	VSS	Power/Other	
F26	D22#	Source Synch	Input/Output
G1	ADS#	Common Clock	Input/Output
G2	BNR#	Common Clock	Input/Output
G3	VSS	Power/Other	
G4	LOCK#	Common Clock	Input/Output
G5	RS1#	Common Clock	Input
G6	VSS	Power/Other	
G21	VSS	Power/Other	
G22	D10#	Source Synch	Input/Output
G23	D18#	Source Synch	Input/Output
G24	VSS	Power/Other	
G25	DBI1#	Source Synch	Input/Output
G26	D25#	Source Synch	Input/Output
H1	VSS	Power/Other	
H2	DRDY#	Common Clock	Input/Output
H3	REQ4#	Source Synch	Input/Output
H4	VSS	Power/Other	
H5	DBSY#	Common Clock	Input/Output
H6	BR0#	Common Clock	Input/Output
H21	D11#	Source Synch	Input/Output
H22	D16#	Source Synch	Input/Output
H23	VSS	Power/Other	
H24	D26#	Source Synch	Input/Output
H25	D31#	Source Synch	Input/Output
H26	VSS	Power/Other	
J1	REQ0#	Source Synch	Input/Output
J2	VSS	Power/Other	
J3	REQ3#	Source Synch	Input/Output
J4	REQ2#	Source Synch	Input/Output
J5	VSS	Power/Other	
J6	TRDY#	Common Clock	Input
J21	D14#	Source Synch	Input/Output
J22	VSS	Power/Other	
J23	DSTBP1#	Source Synch	Input/Output
J24	D29#	Source Synch	Input/Output
J25	VSS	Power/Other	
J26	DP0#	Common Clock	Input/Output
K1	A6#	Source Synch	Input/Output
K2	A3#	Source Synch	Input/Output
K3	VSS	Power/Other	
K4	A4#	Source Synch	Input/Output
K5	REQ1#	Source Synch	Input/Output
K6	VSS	Power/Other	

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
K21	VSS	Power/Other	
K22	DSTBN1#	Source Synch	Input/Output
K23	D30#	Source Synch	Input/Output
K24	VSS	Power/Other	
K25	DP1#	Common Clock	Input/Output
K26	DP2#	Common Clock	Input/Output
L1	VSS	Power/Other	
L2	A9#	Source Synch	Input/Output
L3	A7#	Source Synch	Input/Output
L4	VSS	Power/Other	
L5	ADSTB0#	Source Synch	Input/Output
L6	A5#	Source Synch	Input/Output
L21	D24#	Source Synch	Input/Output
L22	D28#	Source Synch	Input/Output
L23	VSS	Power/Other	
L24	COMP0	Power/Other	Input/Output
L25	DP3#	Common Clock	Input/Output
L26	VSS	Power/Other	
M1	A13#	Source Synch	Input/Output
M2	VSS	Power/Other	
M3	A10#	Source Synch	Input/Output
M4	A11#	Source Synch	Input/Output
M5	VSS	Power/Other	
M6	A8#	Source Synch	Input/Output
M21	D27#	Source Synch	Input/Output
M22	VSS	Power/Other	
M23	D32#	Source Synch	Input/Output
M24	D35#	Source Synch	Input/Output
M25	VSS	Power/Other	
M26	D37#	Source Synch	Input/Output
N1	A12#	Source Synch	Input/Output
N2	A14#	Source Synch	Input/Output
N3	VSS	Power/Other	
N4	A15#	Source Synch	Input/Output
N5	A16#	Source Synch	Input/Output
N6	VSS	Power/Other	
N21	VSS	Power/Other	
N22	D33#	Source Synch	Input/Output
N23	D36#	Source Synch	Input/Output
N24	VSS	Power/Other	
N25	D39#	Source Synch	Input/Output
N26	D38#	Source Synch	Input/Output
P1	COMP1	Power/Other	Input/Output
P2	VSS	Power/Other	

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
P3	A19#	Source Synch	Input/Output
P4	A20#	Source Synch	Input/Output
P5	VSS	Power/Other	
P6	A24#	Source Synch	Input/Output
P21	D34#	Source Synch	Input/Output
P22	VSS	Power/Other	
P23	DSTBP2#	Source Synch	Input/Output
P24	D41#	Source Synch	Input/Output
P25	VSS	Power/Other	
P26	DBI2#	Source Synch	Input/Output
R1	VSS	Power/Other	
R2	A18#	Source Synch	Input/Output
R3	A21#	Source Synch	Input/Output
R4	VSS	Power/Other	
R5	ADSTB1#	Source Synch	Input/Output
R6	A28#	Source Synch	Input/Output
R21	D40#	Source Synch	Input/Output
R22	DSTBN2#	Source Synch	Input/Output
R23	VSS	Power/Other	
R24	D43#	Source Synch	Input/Output
R25	D42#	Source Synch	Input/Output
R26	VSS	Power/Other	
T1	A17#	Source Synch	Input/Output
T2	A22#	Source Synch	Input/Output
T3	VSS	Power/Other	
T4	A26#	Source Synch	Input/Output
T5	A30#	Source Synch	Input/Output
T6	VSS	Power/Other	
T21	VSS	Power/Other	
T22	D46#	Source Synch	Input/Output
T23	D47#	Source Synch	Input/Output
T24	VSS	Power/Other	
T25	D45#	Source Synch	Input/Output
T26	D44#	Source Synch	Input/Output
U1	A23#	Source Synch	Input/Output
U2	VSS	Power/Other	
U3	A25#	Source Synch	Input/Output
U4	A31#	Source Synch	Input/Output
U5	VSS	Power/Other	
U6	TESTHI8	Power/Other	Input
U21	D52#	Source Synch	Input/Output
U22	VSS	Power/Other	
U23	D50#	Source Synch	Input/Output
U24	D49#	Source Synch	Input/Output

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Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
U25	VSS	Power/Other	
U26	D48#	Source Synch	Input/Output
V1	VSS	Power/Other	
V2	A27#	Source Synch	Input/Output
V3	A32#	Source Synch	Input/Output
V4	VSS	Power/Other	
V5	AP1#	Common Clock	Input/Output
V6	MCERR#	Common Clock	Input/Output
V21	DBI3#	Source Synch	Input/Output
V22	D53#	Source Synch	Input/Output
V23	VSS	Power/Other	
V24	D54#	Source Synch	Input/Output
V25	D51#	Source Synch	Input/Output
V26	VSS	Power/Other	
W1	A29#	Source Synch	Input/Output
W2	A33#	Source Synch	Input/Output
W3	VSS	Power/Other	
W4	TESTHI9	Power/Other	Input
W5	INIT#	Asynch GTL+	Input

Table 4-2. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
W6	VSS	Power/Other	
W21	VSS	Power/Other	
W22	DSTBN3#	Source Synch	Input/Output
W23	DSTBP3#	Source Synch	Input/Output
W24	VSS	Power/Other	
W25	D57#	Source Synch	Input/Output
W26	D55#	Source Synch	Input/Output
Y1	A34#	Source Synch	Input/Output
Y2	VSS	Power/Other	
Y3	TESTHI10	Power/Other	Input
Y4	STPCLK#	Asynch GTL+	Input
Y5	VSS	Power/Other	
Y6	BPM3#	Common Clock	Input/Output
Y21	D60#	Source Synch	Input/Output
Y22	VSS	Power/Other	
Y23	D58#	Source Synch	Input/Output
Y24	D59#	Source Synch	Input/Output
Y25	VSS	Power/Other	
Y26	D56#	Source Synch	Input/Output

4.2 Signal Descriptions

Table 4-3. Signal Descriptions (Sheet 1 of 8)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Pentium® 4 processor on 0.13 micron process system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 6.1 for more details.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** **Associated Strobe** REQ[4:0]#, A[16:3]# ADSTB0# A[35:17]# ADSTB1#
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processors on 0.13 micron process system bus agents. The following table defines the coverage model of these signals. **Request Signals** **Subphase 1** **Subphase 2** A[35:24]# AP0# AP1# A[23:3]# AP1# AP0# REQ[4:0]# AP1# AP0#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.

Table 4-3. Signal Descriptions (Sheet 2 of 8)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processors on 0.13 micron process system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Refer to the appropriate Platform Design Guide for more detailed information. These signals do not have on-die termination and must be terminated on the system board.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. This signal does not have on-die termination and must be terminated.
BSEL[1:0]	Input/ Output	BSEL[1:0] (Bus Select) are used to select the processor input clock frequency. Table 2-4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. For more information about these pins, including termination recommendations refer to Section 2.9 and the appropriate platform design guidelines.
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the appropriate Platform Design Guide for details on implementation.

Table 4-3. Signal Descriptions (Sheet 3 of 8)

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#. *Quad-Pumped Signal Groups* | Data Group	DSTBN#/ DSTBP#	DBI#
D[15:0]#	0	0
D[31:16]#	1	1
D[47:32]#	2	2
D[63:48]#	3	3 | Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits within a 16-bit group would have been asserted electrically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group. *DBI[3:0]# Assignment To Data Bus* 	Bus Signal	Data Bus Signals
---	---
DBI3#	D[63:48]#
DBI2#	D[47:32]#
DBI1#	D[31:16]#
DBI0#	D[15:0]#	
DBR#	Output	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.
DBSY#	Input/ Output	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.
DEFER#	Input	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.
DP[3:0]#	Input/ Output	DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor on 0.13 micron process system bus agents.

Table 4-3. Signal Descriptions (Sheet 4 of 8)

Name	Type	Description
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#: **Signals** **Associated Strobe** D[15:0]#, DBI0# DSTBN0# D[31:16]#, DBI1# DSTBN1# D[47:32]#, DBI2# DSTBN2# D[63:48]#, DBI3# DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#: **Signals** **Associated Strobe** D[15:0]#, DBI0# DSTBP0# D[31:16]#, DBI1# DSTBP1# D[47:32]#, DBI2# DSTBP2# D[63:48]#, DBI3# DSTBP3#
FERR#/PBE#	Output	FERR#/PBE# (floating point error/pending break event) is a multiplexed signal which is qualified by STPCLK#. When STPCLK# is not asserted, FERR# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using Microsoft MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. For addition information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to the *IA-32 Intel® Architecture Software Developer's Manual (Vol. 1 - Vol. 3)* and the *Intel ® Processor Identification and the CPUID Instruction* application note.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CC}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the appropriate Platform Design Guide for more information.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination and must be terminated on the system board.

Table 4-3. Signal Descriptions (Sheet 5 of 8)

Name	Type	Description
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
IMPSEL	Input	IMPSEL input will determine whether the processor uses a 50 Ω or 60 Ω buffer. This pin must be tied to GND on 50 Ω platforms and left as NC on 60 Ω platforms.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	ITPCLKOUT[1:0] is an uncompensated differential clock output that is a delayed copy of BCLK[1:0], which is an input to the processor. This clock output can be used as the differential clock into the ITP port that is designed onto the motherboard. If ITPCLKOUT[1:0] outputs are not used, they must be terminated properly. Refer to Section 2.5 for additional details and termination requirements. Refer to the *ITP 700 Debug Port Design Guide* for details on implementing a debug port.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.

Table 4-3. Signal Descriptions (Sheet 6 of 8)

Name	Type	Description
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Intel$^®$ Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. See Section 6.3 for more details. **NOTE:** The PROCHOT# signal functionality has changed from output to input/output on CPUID 0xF27 and beyond.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1. This signal does not have on-die termination and must be terminated on the system board.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.

Table 4-3. Signal Descriptions (Sheet 7 of 8)

Name	Type	Description
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will only recognize the assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	Assertion of STPCLK# (Stop Clock) causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] TESTHI[5:0]	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a V_{CC} power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 6.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 6.3.1.

Table 4-3. Signal Descriptions (Sheet 8 of 8)

Name	Type	Description
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level where permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (V_{CC}) must be removed within 0.5 seconds of the assertion of THERMTRIP#. For processors with CPUID of 0xF24: • Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted. For processors with CPUID of 0xF27 and beyond: • Driving of the THERMTRIP# signal is enabled within 10 μs of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 μs of the assertion of PWRGOOD.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 Ω pull-down resistor.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLLs. Refer to the appropriate Platform Design Guide for complete implementation details.
$V_{CCIOPLL}$	Input	$V_{CCIOPLL}$ provides isolated power for internal processor system bus PLLs. Follow the guidelines for V_{CCA}, and refer to the appropriate Platform Design Guide for complete implementation details.
V_{CC_SENSE}	Output	V_{CC_SENSE} is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure power near the silicon with little noise.
$V_{CC}VID$	Input	Independent 1.2 V supply must be routed to $V_{CC}VID$ pin for the Pentium 4 processor on 0.13 micron process's Voltage Identification circuit.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike previous generations of processors, these are open drain signals that are driven by the Pentium 4 processor on 0.13 micron process and must be pulled up to 3.3 V (max.) with 1 kΩ resistors. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2-2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
V_{SSA}	Input	V_{SSA} is the isolated ground for internal PLLs.
V_{SS_SENSE}	Output	V_{SS_SENSE} is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise

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Thermal Specifications and Design Considerations 5

The Pentium 4 processor on 0.13 micron process uses an Integrated Heat Spreader (IHS) for heatsink attachment that is intended to provide for multiple types of thermal solutions. This chapter provides data necessary for development of a thermal solution. See Figure 5-1 for an enlarged view of an example of the Pentium 4 processor on 0.13 micron process thermal solution. This is for illustration purposes only. For further thermal solution design details, refer to the. *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.

Note: The processor is shipped either by itself or with a heatsink for boxed processors. See Chapter 7 for details on boxed processors.

Figure 5-1. Example Thermal Solution (Not to Scale)
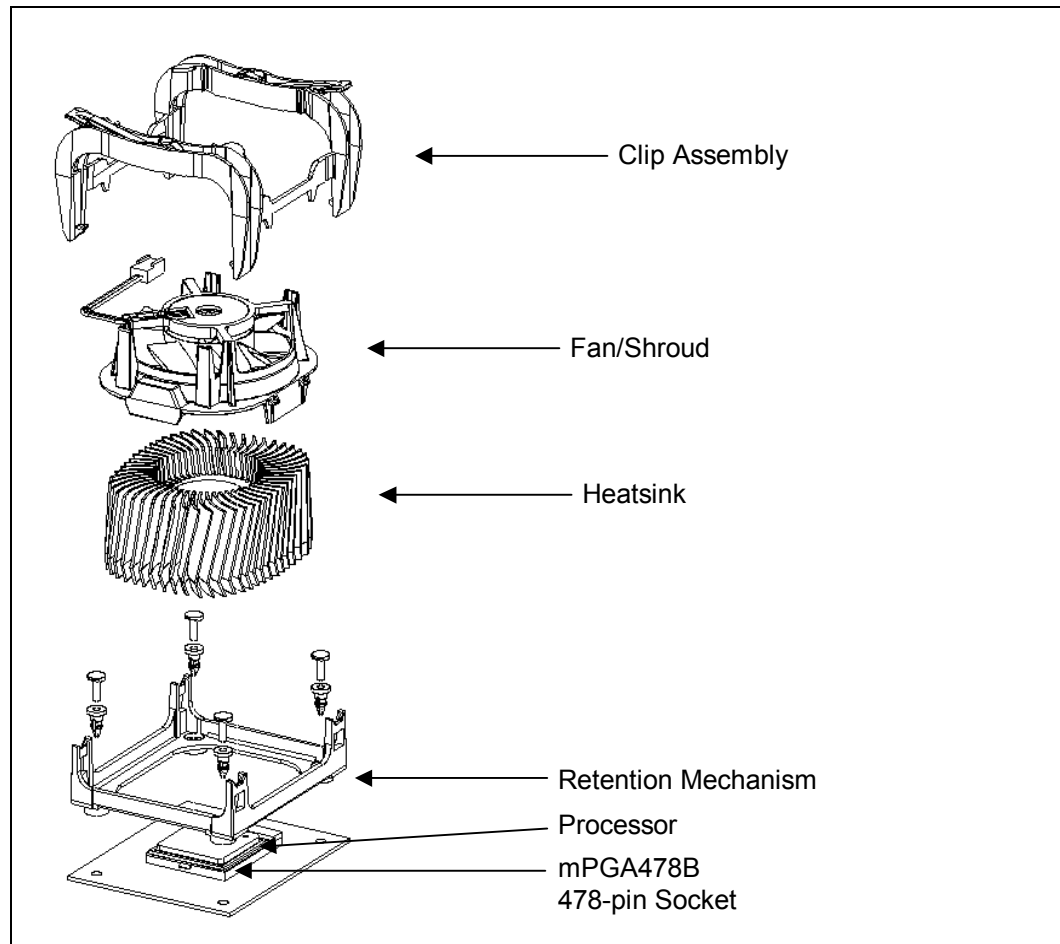
5.1 Processor Thermal Specifications

The Pentium 4 processor on 0.13 micron process requires a thermal solution to maintain temperatures within the operating limits as set forth in Section 5.1.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component-level thermal solutions can include active or passive heatsinks attached to the processor IHS. Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to *Intel*® *Pentium*® *4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.

5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature (T_C) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 5-1. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate processor thermal design guidelines.

The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained periods of time. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 5-1 instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 6.3. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with a lower thermal dissipation is currently planned. **In all cases, the Thermal Monitor feature must be enabled for the processor to remain within specification**.

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Table 5-1. Processor Thermal Design Power

| Front Side Bus Frequency	Processor and Core Frequency	Thermal Design Power[1,2] (W)	Minimum T_C (°C)	Maximum T_C (°C)	Notes[3]
400 MHz	**Processors with VID=1.500 V** 2A GHz 2.20 GHz 2.40 GHz 2.50 GHz	 52.4 55.1 57.8 59.3	 5 5 5 5	 68 69 70 71	
	Processors with VID=1.525 V 2A GHz 2.20 GHz 2.40 GHz 2.50 GHz 2.60 GHz	 54.3 57.1 59.8 61.0 62.6	 5 5 5 5 5	 69 70 71 72 72	
	Processors with multiple VIDs 2A GHz 2.20 GHz 2.40 GHz 2.50 GHz 2.60 GHz	 54.3 57.1 59.8 61.0 62.6	 5 5 5 5 5	 69 70 71 72 72	
533 MHz	**Processors with VID=1.500 V** 2.26 GHz 2.40B GHz 2.53 GHz	 56.0 57.8 59.3	 5 5 5	 70 70 71	
	Processors with VID=1.525 V 2.26 GHz 2.40B GHz 2.53 GHz 2.66 GHz 2.80 GHz	 58.0 59.8 61.5 66.1 68.4	 5 5 5 5 5	 70 71 72 74 75	
	Processors with multiple VIDs 2.26 GHz 2.40B GHz 2.53 GHz 2.66 GHz 2.80 GHz 3.06 GHz	 58.0 59.8 61.5 66.1 68.4 81.8	 5 5 5 5 5 5	 70 71 72 74 75 69	
800 MHz FSB with 512-KB L2 Cache Only	**Processors with multiple VIDs** 2.40C GHz 2.60C GHz 2.80C GHz 3 GHz 3.20C GHz 3.40 GHz	 66.2 69.0 69.7 81.9 82.0 89.0	 5 5 5 5 5 5	 74 75 75 70 70 68	
800 MHz FSB with 2-MB L3 Cache	**Processors with multiple VIDs** 3.20 GHz 3.40 GHz	 92.1 102.9	 5 5	 64 67	

NOTES:
1. These values are specified at V_{CC_MAX} for the processor. Systems must be designed to ensure that the processor is not subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Refer to loadline specifications in Chapter 2.
2. The numbers in this column reflect Intel's recommended design point and are not indicative of the maximum power the processor can dissipate under worst case conditions. For more details, refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.
3. TDP and T_C are specified for highest VID only. Processors will be shipped under multiple VIDs for each frequency; however, the TDP and T_C specifications will be the same as highest VID specified in the table.

5.1.2 Thermal Metrology

5.1.2.1 Processor Case Temperature Measurement

The maximum and minimum case temperature (T_C) for the Pentium 4 processor on 0.13 micron process is specified in Table 5-1. This temperature specification is meant to help ensure proper operation of the processor. Figure 5-2 illustrates where Intel recommends T_C thermal measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Intel® Pentium® Processor 4 with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.

Figure 5-2. Guideline Locations for Case Temperature (T_C) Thermocouple Placement
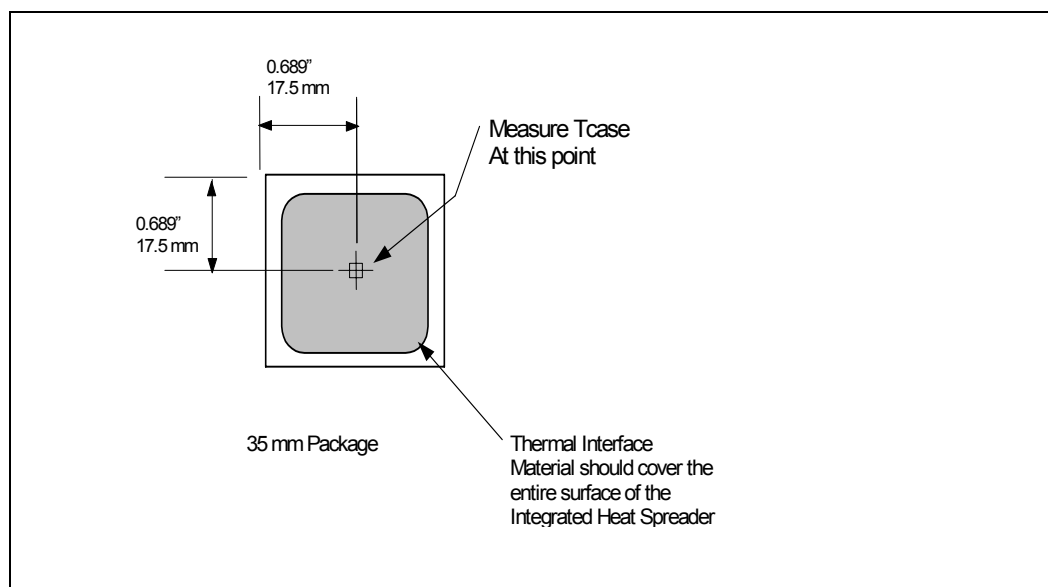
Features 6

6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Pentium 4 processor on 0.13 micron process samples hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 6-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a "warm" reset and a "power-on" reset.

Table 6-1. Power-On Configuration Option Pins

Configuration Option	Pin[1]
Output tristate	SMI#
Execute BIST	INIT#
In Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Disable Hyper-Threading Technology	A31#
Symmetric agent arbitration ID	BR0#

NOTE:
 1. Asserting this signal during RESET# will select the corresponding option.

6.2 Clock Control and Low Power States

The use of AutoHALT, Stop-Grant, and Sleep states is allowed in Pentium 4 processor on 0.13 micron process-based systems to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 6-1 for a visual representation of the processor low power states.

6.2.1 Normal State—State 1

This is the normal operating state for the processor.

## 6.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process bus snoops and interrupts.

Figure 6-1. Stop Clock State Machine
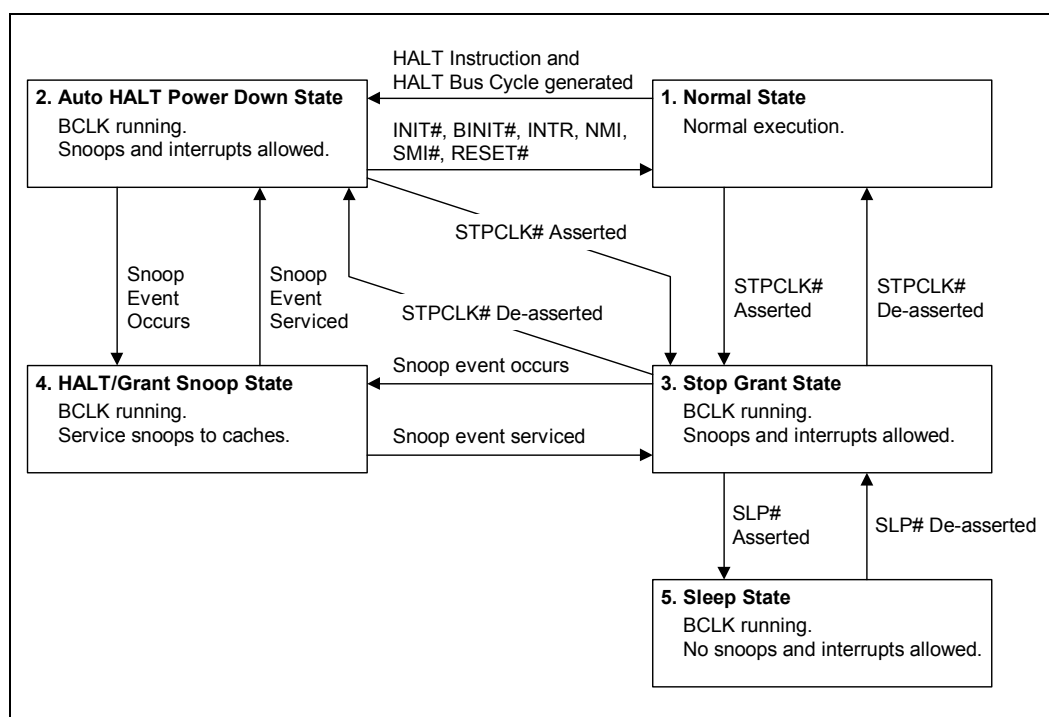
6.2.3   Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 6.2.4). A transition to the Sleep state (see Section 6.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the system bus and it will latch interrupts delivered on the system bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

6.2.4   HALT/Grant Snoop State—State 4

The processor will respond to snoop or interrupt transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or other agent on the system bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

6.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can be entered only from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should be asserted only when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification, and may result in unapproved operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state and is held active as specified in the RESET# pin specification, the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure that the processor correctly executes the Reset sequence.

Once in the Sleep state, the SLP# pin must be de-asserted if another asynchronous system bus event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

6.3 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. The Thermal Monitor feature must be enabled for the processor to be operating within specifications. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 µs when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may

cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines* for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Thermal Monitor Control Register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed. However, in On-Demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used at the same time Automatic mode is enabled. However, if the system tries to enable the TCC via On-Demand mode at the same time automatic mode is enabled AND a high temperature condition exists, the duty cycle of the automatic mode will override the duty cycle selected by the On-Demand mode.

An external signal, PROCHOT# (processor hot), is asserted when the processor detects that its temperature is at the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active. The temperature at which the thermal control circuit activates is not user configurable and is not software visible.

Besides the thermal sensor and TCC, the Thermal Monitor feature also includes one ACPI register, performance monitoring logic, bits in three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Thermal Monitor feature. Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

If automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling of the automatic or On-Demand modes, in the event of a catastrophic cooling failure the processor automatically shuts down when the silicon has reached a temperature of approximately 135 °C. At this point the system bus signal THERMTRIP# goes active and stays active until RESET# has been initiated. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (V_{CC}) must be removed within 0.5 seconds.

6.3.1   Thermal Diode

The Pentium 4 processor on 0.13 micron process incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. Table 6-2 and Table 6-3 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 6-2. Thermal Diode Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
I_{FW}	Forward Bias Current	5		300	µA	1
n	Diode Ideality Factor	1.0011	1.0021	1.0030		2,3,4
R_T	Series Resistance		3.64		Ω	2,3,4,5

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 75 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   $$I_{FW}=I_s *(e^{(qV_D/nkT)} -1)$$
   Where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the diode junction temperature. R_T as defined includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
   $$T_{error} = [R_T*(N-1)*I_{FWmin}]/[(nk/q)*ln N]$$
   Where T_{error} = sensor temperature error, N = sensor current ration, k = Boltzmann Constant, q = electronic charge.

Table 6-3. Thermal Diode Interface

| Pin Name	Pin Number	Pin Description
THERMDA	B3	diode anode
THERMDC	C4	diode cathode

Boxed Processor Specifications   **7**

7.1   Introduction

The Pentium 4 processor on 0.13 micron process will also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Pentium 4 processor on 0.13 micron process will be supplied with a cooling solution. This chapter documents motherboard and system requirements for the cooling solution that will be supplied with the boxed Pentium 4 processor on 0.13 micron process This chapter is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 7-1 shows a mechanical representation of a boxed Pentium 4 processor on 0.13 micron process.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis. Refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines* for further guidance.

Figure 7-1. Mechanical Representation of the Boxed Processor
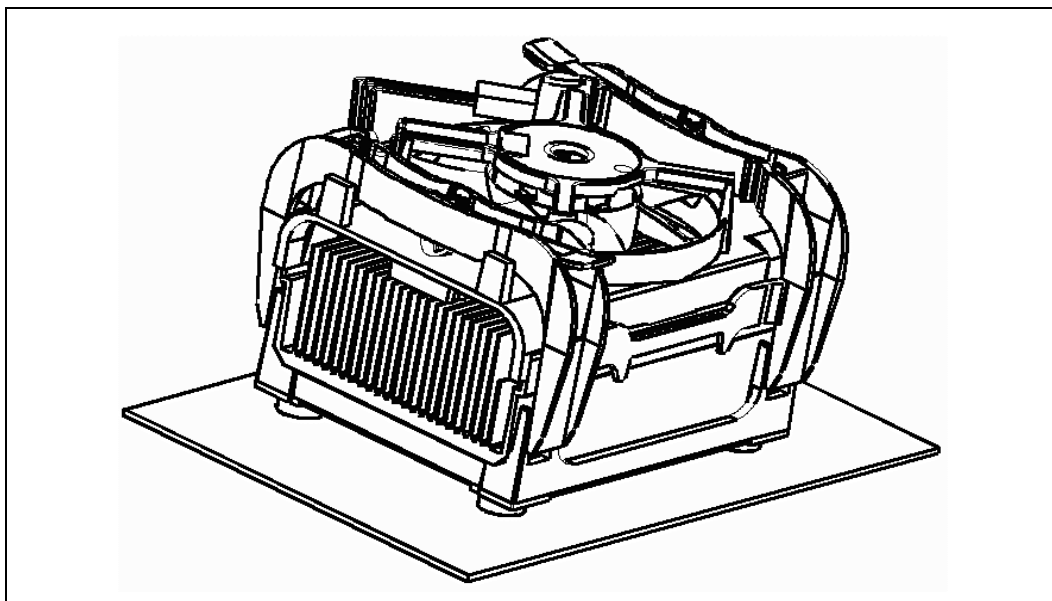
NOTE: The airflow is into the center and out of the sides of the fan heatsink.

7.2 Mechanical Specifications

7.2.1 Boxed Processor Cooling Solution Dimensions

This section describes the mechanical specifications of the boxed Pentium 4 processor on 0.13 micron process. The boxed processor will be shipped with an unattached fan heatsink. Figure 7-1 shows a mechanical representation of the boxed Pentium 4 processor on 0.13 micron process.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 7-2 (Side Views), and Figure 7-3 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new motherboard and system designs. Airspace requirements are shown in Figure 7-6 and Figure 7-7. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

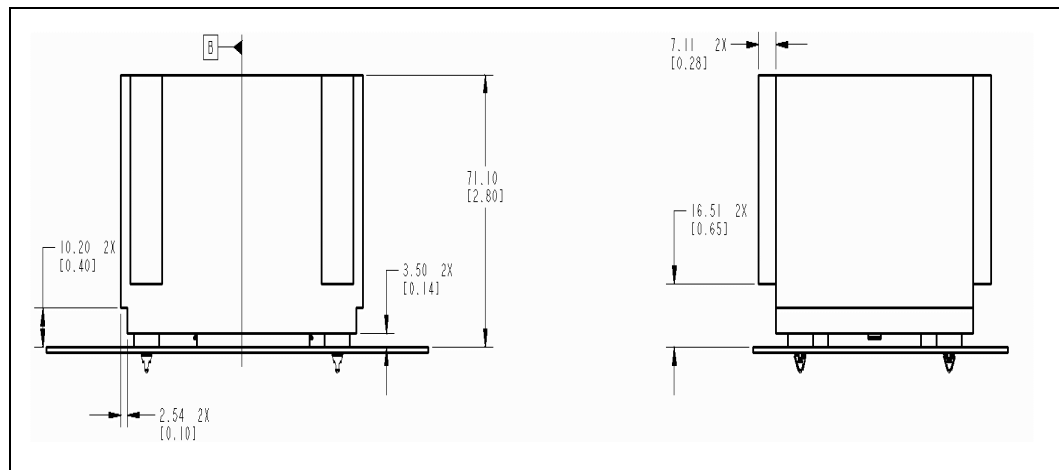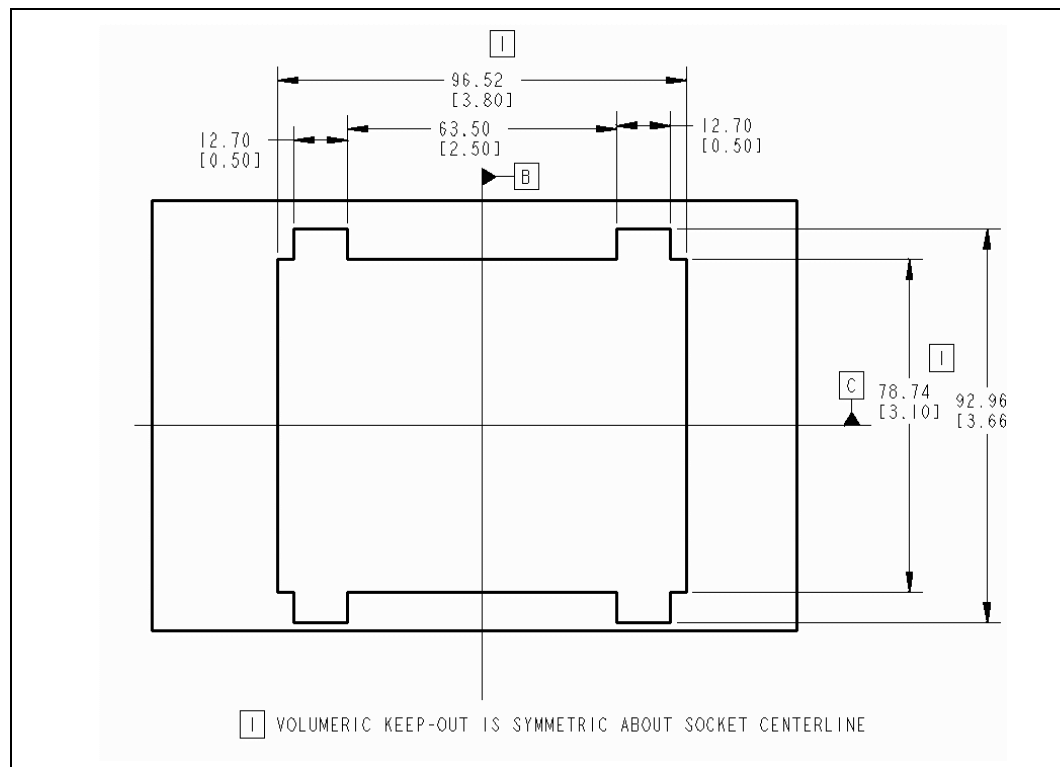**Figure 7-2. Side View Space Requirements for the Boxed Processor**

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Figure 7-3. Top View Space Requirements for the Boxed Processor

7.2.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. See Chapter 5 and the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines* for details on the processor weight and heatsink requirements.

7.2.3 Boxed Processor Retention Mechanism and Heatsink Assembly

The boxed processor thermal solution requires a processor retention mechanism and a heatsink attach clip assembly to secure the processor and fan heatsink in the baseboard socket. The boxed processor will not ship with retention mechanisms but will ship with the heatsink attach clip assembly. Motherboards designed for use by system integrators should include the retention mechanism that supports the boxed Pentium 4 processor on 0.13 micron process. Motherboard documentation should include appropriate retention mechanism installation instructions.

Note: The processor retention mechanism based on the Intel reference design should be used to ensure compatibility with the heatsink attach clip assembly and the boxed processor thermal solution. The heatsink attach clip assembly is latched to the retention tab features at each corner of the retention mechanism.

The target load applied by the clips to the processor heat spreader for Intel's reference design is 75 ± 15 lbf (maximum load is constrained by the package load capability). It is normal to observe a bow or bend in the board due to this compressive load on the processor package and the socket. The level of bow or bend depends on the motherboard material properties and component layout. Any additional board stiffening devices such as plates are not necessary and should not be used along with the reference mechanical components and boxed processor. Using such devices increase the compressive load on the processor package and socket, likely beyond the maximum load that is specified for those components. Refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines* for details on the Intel reference design.

7.3 Electrical Requirements

7.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 7-4. Motherboards must provide a matched power header to support the boxed processor. Table 7-1 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides V_{OH} to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

Note: The motherboard must supply a constant +12 V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 7-5 shows the location of the fan power connector relative to the processor socket. The motherboard power header should be positioned within 4.33 inches from the center of the processor socket.

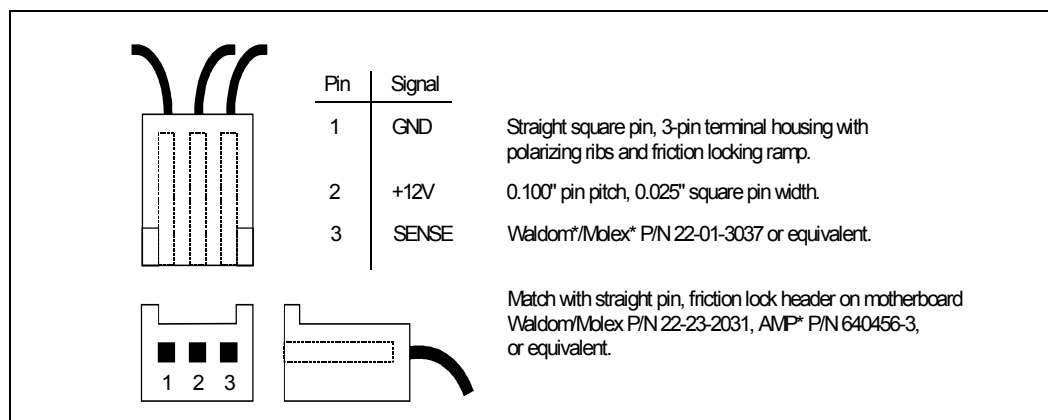**Figure 7-4. Boxed Processor Fan Heatsink Power Cable Connector Description**

Pin	Signal	
1	GND	Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.
2	+12V	0.100" pin pitch, 0.025" square pin width.
3	SENSE	Waldom*/Molex* P/N 22-01-3037 or equivalent.

Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP* P/N 640456-3, or equivalent.

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Table 7-1. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12 V: 12 Volt fan power supply	10.2	12	13.8	V	
IC: Fan current draw			740	mA	
SENSE: SENSE frequency		2		pulses per fan revolution	1

NOTE:
1. Motherboard should pull this pin up to V_{CC} with a resistor.

Figure 7-5. MotherBoard Power Header Placement Relative to Processor Socket
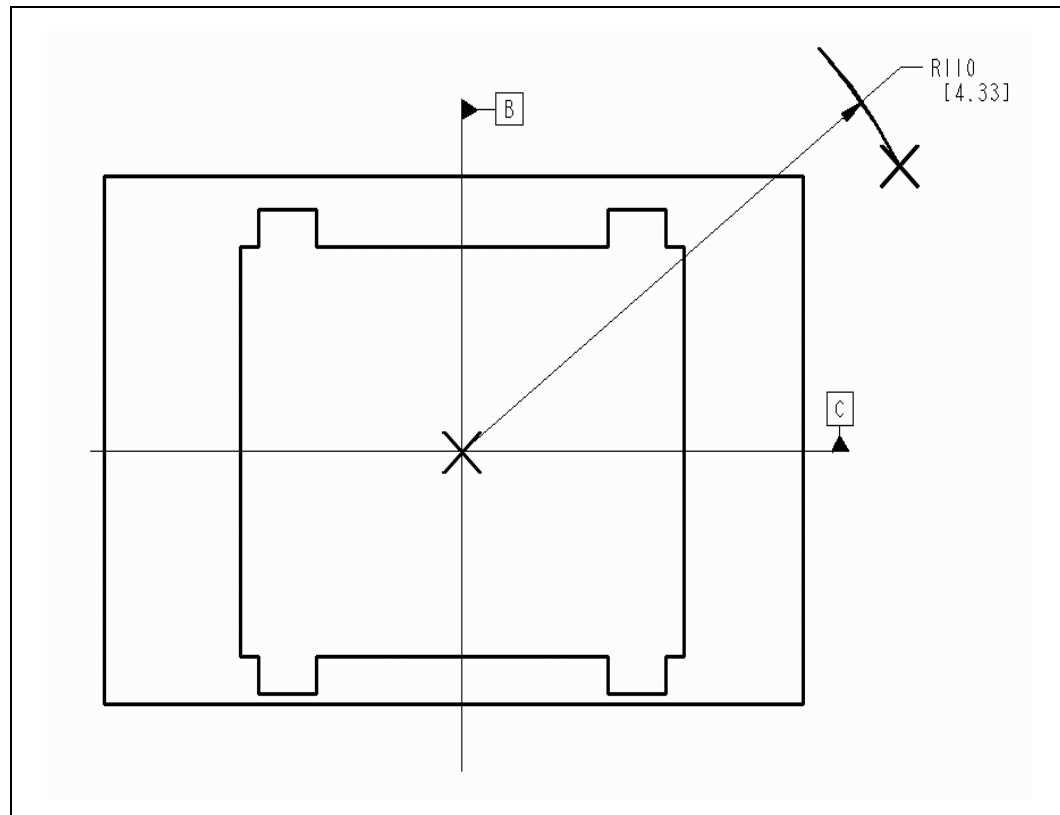
7.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

7.4.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and is ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 5. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 5-1) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink be unimpeded. Airflow is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 7-6 and Figure 7-7 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 40 °C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

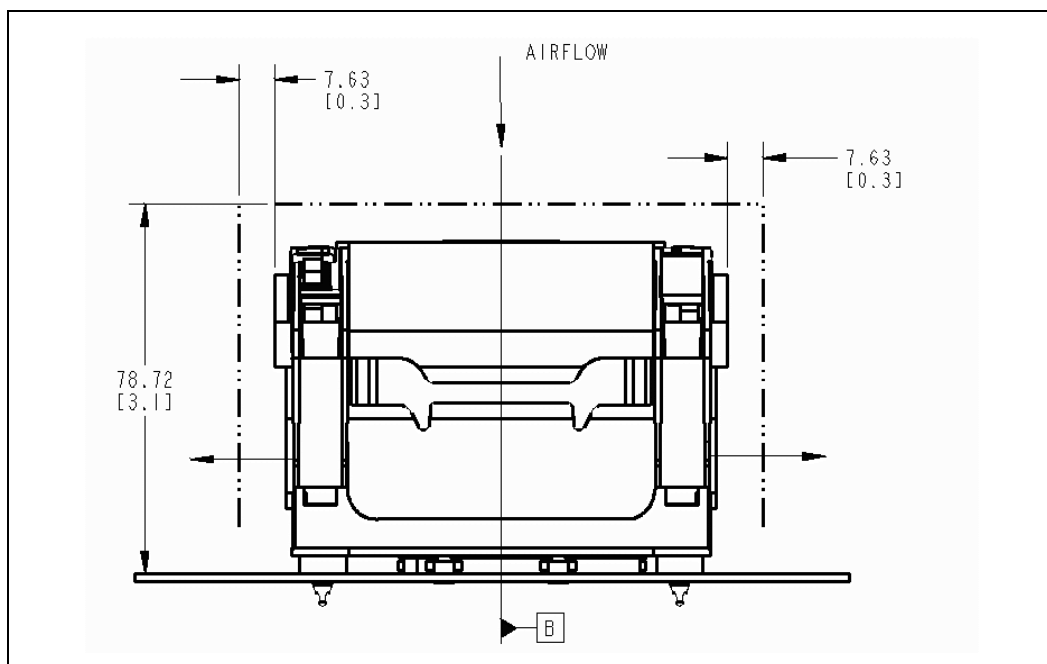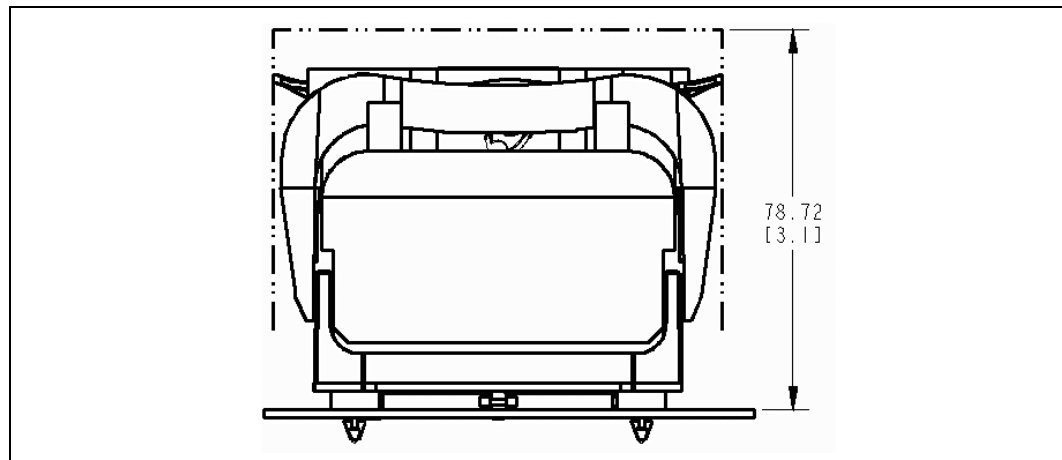**Figure 7-6. Boxed Processor Fan Heatsink Airspace Keep-Out Requirements (Side 1 View)**

Figure 7-7. Boxed Processor Fan Heatsink Airspace Keep-Out Requirements (Side 2 View)

7.4.2   Variable Speed Fan

The boxed processor fan will operate at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed and noise level, while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains below the lower set point. These set points, represented in Figure 7-8 and Table 7-2, can vary by a few degrees from fan heatsink to fan heatsink. The internal chassis temperature should be kept below 38 ºC. Meeting the processor's temperature specification (see Chapter 5) is the responsibility of the system integrator.
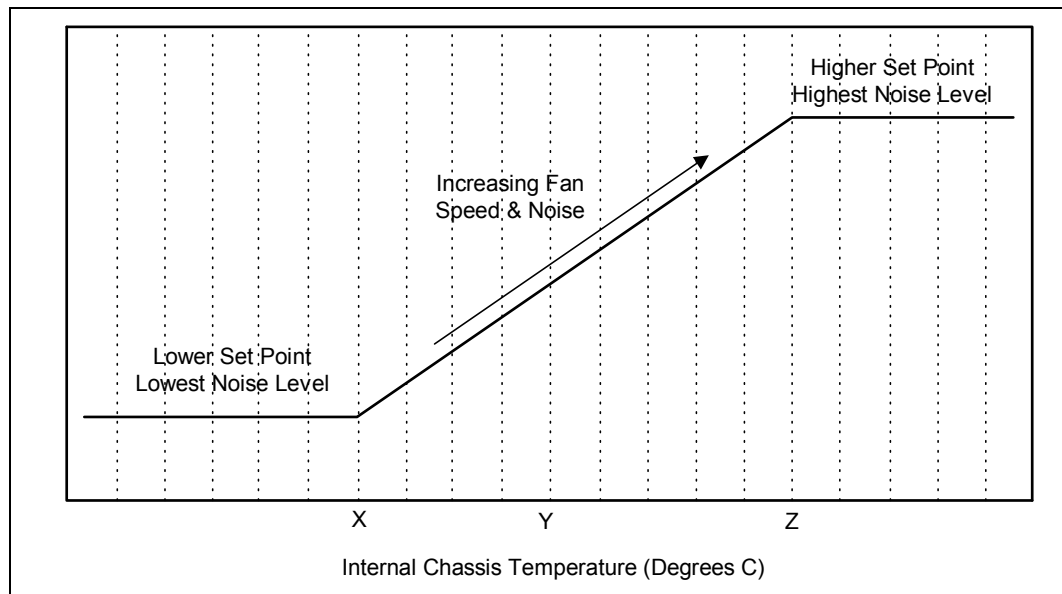
Figure 7-8. Boxed Processor Fan Heatsink Set Points

Table 7-2. Boxed Processor Fan Heatsink Set Points

Boxed Processor Fan Heatsink Set Point (°C)	Boxed Processor Fan Speed	Notes
Boxed Intel® Pentium® 4 Processors 2.80 GHz (and below)		
X ≤ 33	When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.	1
Y = 40	When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.	
Z ≥ 43	When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.	1
Boxed Intel® Pentium® 4 Processors 3 GHz (and above)		
X ≤ 32	When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.	1
Y = 38	When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.	
Z ≥ 40	When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.	1

NOTE:

1. Set point variance is approximately ± 1 °C from fan heatsink to fan heatsink.

Debug Tools Specifications 8

Refer to the *ITP 700 Debug Port Design Guide* and the appropriate platform design guidelines for more detailed information regarding debug tools specifications (such as integration details).

8.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Pentium 4 processors on 0.13 micron process systems. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Pentium 4 processor on 0.13 micron process systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor on 0.13 micron process system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Pentium 4 processor on 0.13 micron process heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.