Data Sheet | November 16, 2004 | FN4631.5

PCI Hot Plug Controller

The HIP1011A is the second PCI Hot Plug Voltage bus control IC from Intersil. A drop-in alternative to the widely used HIP1011, the HIP1011A has the same form, fit and function but additionally features an adjustable latch-off time of the MOSFET switches and fault reporting.

Like the HIP1011, the HIP1011A creates a small and simple yet complete power control solution with discrete power MOSFETs and a few passive components. Four independent supplies are controlled, +5V, +3.3, +12V, and -12V. The +12V and -12V switches are integrated. For the +5V and +3.3V supplies, overcurrent (OC) protection is provided by sensing the voltage across external current-sense resistors. For the +12V and -12V supplies OC protection is provided internally. In addition, an on-chip reference is used to monitor the +5V, +3.3V and +12V outputs for undervoltage (UV) conditions. The PWRON input controls the state of the switches. During an OC condition on any output, or a UV condition on the +5V, +3.3V or +12V outputs, a LOW (0V) is asserted on the FLTN output and all MOSFETs are latched-off. The time to FLTN signal going LOW and MOSFET latch-off is determined by a single capacitor from the FLTN pin to ground. This added feature allows the system OS to complete housekeeping activities in preparation for an unplanned shut down of the affected card. The FLTN latch is cleared when the PWRON input is toggled low again. During initial power-up of the main VCC supply (+12V), the PWRON input is inhibited from turning on the switches, and the latch is held in the Reset state until the VCC input is greater than 10V.

User programmability of the overcurrent threshold, fault reporting response time, latch-off response time and turn-on slew rate is provided. A resistor connected to the OCSET pin programs the OC threshold. A capacitor may be added to the FLTN pin to adjust both the delay time to reporting a fault and the latch-off of the supplies after an OC or UV event. Capacitors connected to the gate pins set the turn-on rate. In addition the HIP1011A has also been enhanced to tolerate spurious system noise.

Features

- Adjustable Delay Time for Turn-Off and Fault Reporting
- Controls All PCI Supplies: +5V, +3.3V, +12V, -12V
- Internal MOSFET Switches for +12V and -12V Outputs
- μP Interface for On/Off Control and Fault Reporting
- Adjustable Overcurrent Protection for All Supplies
- Provides Fault Isolation
- Adjustable Turn-On Slew Rate
- Minimum Parts Count Solution
- No Charge Pump
- Pb-Free Available (RoHS Compliant)

Applications

- PCI Hot Plug
- CompactPCI

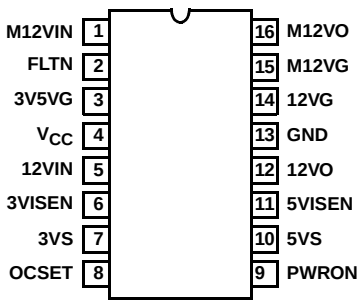
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
HIP1011ACB	0 to 70	16 Ld SOIC	M16.15
HIP1011ACBZA (See Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
HIP1011ACB-T	0 to 70	Tape and Reel	
HIP1011ACBZA-T (See Note)	0 to 70	Tape and Reel (Pb-free)	

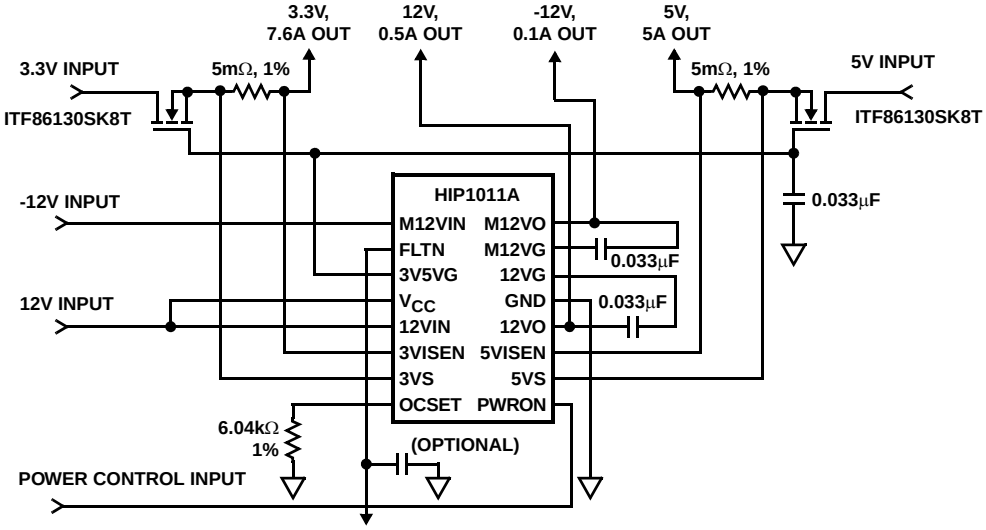
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Pinout

HIP1011A
(SOIC)
TOP VIEW

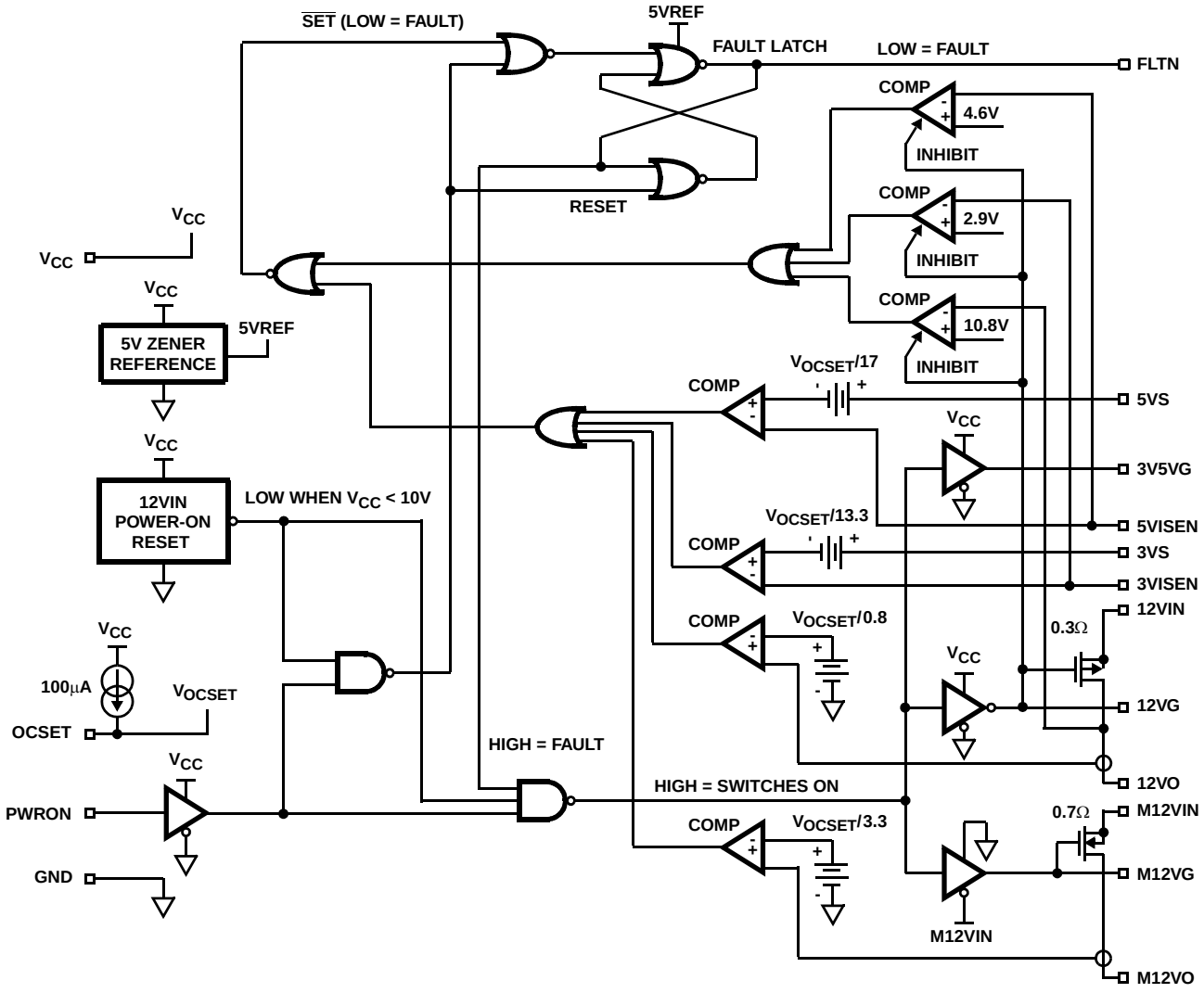


Typical Application



NOTE: All capacitors are ±10%.

Simplified Schematic



Pin Descriptions

PIN NO.	DESIGNATOR	FUNCTION	DESCRIPTION
1	M12VIN	-12V Input	-12V Supply Input. Also provides power to the -12V overcurrent circuitry.
2	FLTN	Fault Output	5V CMOS Fault Output; LOW = FAULT. A capacitor may be placed from this pin to ground to provide delay time to fault notification and power supply latch-off.
3	3V5VG	3.3V/5V Gate Output	Drive the gates of the 3.3V and 5V MOSFETs. Connect a capacitor to ground to set the start-up ramp. During turn on, this capacitor is charged with a 25µA current source.
4	VCC	12V V_{CC} Input	Connect to unswitched 12V supply.
5	12VIN	12V Input	Switched 12V supply input.
6	3VISEN	3.3V Current Sense	Connect to the load side of the current sense resistor in series with source of external 3.3V MOSFET.
7	3VS	3.3V Source	Connect to source of 3.3V MOSFET. This connection along with pin 6 (3VISEN) senses the voltage drop across the sense resistor.
8	OCSET	Overcurrent Set	Connect a resistor from this pin to ground to set the overcurrent trip point of all four switches. All four over current trips can be programmed by changing the value of this resistor. The default (6.04kΩ, 1%) is compatible with the maximum allowable currents as outlined in the PCI specification.
9	PWRON	Power On Control	Controls all four switches. High to turn switches ON, Low to turn them OFF.
10	5VS	5V Source	Connect to source of 5V MOSFET switch. This connection along with pin 11 (5VISEN) senses the voltage drop across the sense resistor.
11	5VISEN	5V Current Sense	Connect to the load side of the current sense resistor in series with source of external 5V MOSFET.
12	12VO	Switched 12V Output	Switched 12V output.
13	GND	Ground	Connect to common of power supplies.
14	12VG	Gate of Internal PMOS	Connect a capacitor between 12VG and 12VO to set the start up ramp for the +12V supply. This capacitor is charged with a 25µA current source during start-up. The UV circuitry is enabled after the voltage on 12VG is less than 400mV. Therefore, if the capacitor on the pin 3 (3V5VG) is more than 25% larger than the capacitor on pin 14 (12VG) a false UV may be detected during start up.
15	M12VG	Gate of Internal NMOS	Connect a capacitor between M12VG and M12VO to set the start up ramp for the M12V supply. This capacitor is charged with 25µA during start up.
16	M12VO	Switched -12V Output	Switched 12V Output.

Absolute Maximum Ratings

V_{CC}, 12VIN . . . . . -0.5V to +14.0V
12VO . . . . . -0.5V to V_{12VIN} +0.5V
12VO, 12VG, 3V5VG . . . . . -0.5V to V_{CC} +0.5V
M12VIN . . . . . -15.0V to +0.5V
M12VO, M12VG . . . . . V_{M12VIN}-0.5V to +0.5V
3VISEN, 5VISEN . . . . . -0.5V to the Lesser of V_{CC} or +7.0V
Voltage, Any Other Pin . . . . . -0.5V to +7.0V
12VO Output Current 3A
M12VO Output Current 0.8A
ESD Classification . . . . . .4KeV (HBM)

Operating Conditions

VCC Supply Voltage Range . . . . . .+10.8V to +13.2V
±12V, 5V and 3.3V Input Supply Tolerances . . . . . .±10%
12VO Output Current . . . . . .0 to +0.5A
M12VO Output Current . . . . . .0 to +0.1A
Temperature Range (T_A) . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	105

Maximum Junction Temperature . . . . . .125^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . .300^oC
(SOIC - Lead Tips Only)

Die Characteristics

Number of Transistors 290

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief 379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal 5.0V and 3.3V Input Supply Voltages,
V_{CC} = 12VIN = 12V, M12VIN = -12V, $T_A = T_J$ = 0 to 70^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V/3.3V SUPPLY CONTROL						
5V Overcurrent Threshold	I_{OC5V}	See Typical Application Diagram	-	7.1	-	A
5V Overcurrent Threshold Voltage	V_{OC5V_1}	V_{OCSET} = 0.6V	30	36	42	mV
5V Overcurrent Threshold Voltage	V_{OC5V_2}	V_{OCSET} = 1.2V	66	72	79	mV
5V Undervoltage Trip Threshold	V_{5VUV}		4.42	4.65	4.75	V
5V Undervoltage Fault Response Time	t_{5VUV}		-	150	350	ns
5V Turn-On Time (PWRON High to 5VOUT = 4.75V)	t_{ON5V}	C_{3V5VG} = 0.022µF, C_{5VOUT} = 2000µF, R_L = 1Ω	-	6.5	-	ms
5VS Input Bias Current	IB_{5VS}	PWRON = High	-40	-26	-20	µA
5VISEN Input Bias Current	IB_{5VISEN}	PWRON = High	-160	-140	-110	µA
3V Overcurrent Threshold	I_{OC3V}	See Typical Application Diagram	-	9.0	-	A
3V Overcurrent Threshold Voltage	V_{OC3V_1}	V_{OCSET} = 0.6V	42	49	56	mV
3V Overcurrent Threshold Voltage	V_{OC3V_2}	V_{OCSET} = 1.2V	88	95	102	mV
3V Undervoltage Trip Threshold	V_{3VUV}		2.74	2.86	2.97	V
3V Undervoltage Fault Response Time	t_{3VUV}		-	150	350	ns
3V Turn-On Time (PWRON High to 3VOUT = 3.00V)	t_{ON3V}	C_{3V5VG} = 0.022µF, C_{3VOUT} = 2000µF, R_L = 0.43Ω	-	6.5	-	ms
3VS Input Bias Current	IB_{3VS}	PWRON = High	-40	-26	-20	µA
3VISEN Input Bias Current	IB_{3VISEN}	PWRON = High	-160	-140	-110	µA
3V5VG Vout Low	Vout_lo_35VG	PWRON = Low, FLTN = Low	-	0.1	0.4	V
3V5VG Vout High	Vout_hi_35VG	PWRON = High, FLTN = High	10.5	11.1	-	V
Gate Output Charge Current	IC_{3V5VG}	PWRON = High, V_{3V5VG} = 2V	22.5	25.0	27.5	µA

Electrical Specifications Nominal 5.0V and 3.3V Input Supply Voltages, V_{CC} = 12VIN = 12V, M12VIN = -12V, $T_A = T_J$ = 0 to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Turn-On Time (PWRON High to 3V5VG = 11V)	t_{ON3V5V}	C_{3V5VG} = 0.1µF	-	280	500	µs
Gate Turn-Off Time	$t_{OFF3V5V}$	C_{3V5VG} = 0.1µF, 3V5VG from 9.5V to 1V	-	13	17	µs
Gate Turn-Off Time		C_{3V5VG} = 0.022µF, 3V5VG Falling 90% to 10%	-	2	-	µs
+12V SUPPLY CONTROL						
On Resistance of Internal PMOS	$r_{DS(ON)12}$	PWRON = High, I_D = 0.5A, $T_A = T_J$ = 25°C	0.18	0.3	0.35	Ω
Overcurrent Threshold	I_{OC12V_1}	V_{OCSET} = 0.6V	0.6	0.75	0.9	A
Overcurrent Threshold	I_{OC12V_2}	V_{OCSET} = 1.2V	1.25	1.50	1.8	A
12V Undervoltage Trip Threshold	V_{12VUV}		10.5	10.8	11.15	V
Undervoltage Fault Response Time	t_{12VUV}		-	150	-	ns
Gate Charge Current	IC_{12VG}	PWRON = High, V_{12VG} = 3V	23.5	25.0	28.5	µA
Turn-On Time (PWRON High to 12VG = 1V)	t_{ON12V}	C_{12VG} = 0.022µF	-	16	20	ms
Turn-Off Time	t_{OFF12V}	C_{12VG} = 0.1µF, 12VG	-	9	12	µs
Turn-Off Time		C_{12VG} = 0.022µF, 12VG Rising 10% - 90%	-	3	-	µs
-12V SUPPLY CONTROL						
On Resistance of Internal NMOS	$r_{DS(ON)M12}$	PWRON = High, I_D = 0.1A, $T_A = T_J$ = 25°C	0.5	0.7	0.9	Ω
Overcurrent Threshold	I_{OC12V_1}	V_{OCSET} = 0.6V	0.15	0.18	0.25	A
Overcurrent Threshold	I_{OC12V_2}	V_{OCSET} = 1.2V	0.30	0.37	0.50	A
Gate Output Charge Current	IC_{M12VG}	PWRON = High, V_{3VG} = -4V	22.5	25	27.5	µA
Turn-On Time (PWRON High to M12VG = -1V)	t_{ONM12V}	C_{M12VG} = 0.022µF	-	160	300	µs
Turn-On Time (PWRON High to M12VO = -10.8V)	t_{ONM12V}	C_{M12VG} = 0.022µF, C_{M12VO} = 50µF, R_L = 120Ω	-	16	-	ms
Turn-Off Time	$t_{OFFM12V}$	C_{M12VG} = 0.1µF, M12VG	-	18	23	µs
Turn-Off Time		C_{M12VG} = 0.022µF, M12VG Falling 90% to 10%	-	3	-	µs
M12VIN Input Bias Current	IB_{M12VIN}	PWRON = High	-	2	2.6	mA
CONTROL I/O PINS						
Supply Current	I_{VCC}		4	5	5.8	mA
OCSET Current	I_{OCSET}		95	100	105	µA
Overcurrent to Fault Response Time	t_{OC}	FLTN Cap = 100pF	-	500	960	ns
Overcurrent to Fault Response Time		FLTN Cap = 1000pF	-	2200	-	ns
Overcurrent to Fault Response Time		FLTN Cap = 10µF	-	30	-	µs
PWRON Threshold Voltage	$V_{THPWRON}$		0.8	1.6	2.1	V
FLTN Output Low Voltage	$V_{FLTN,OL}$	I_{FLTN} = 2mA	-	0.6	0.9	V
FLTN Output High Voltage	$V_{FLTN,OH}$	I_{FLTN} = 0 to -4mA	3.9	4.3	4.9	V
FLTN Output Latch Threshold	$V_{FLTN,TH}$		1.45	1.8	2.25	V
12V Power On Reset Threshold	$V_{POR,TH}$	V_{CC} Voltage Falling	9.4	10	10.6	V

Typical Performance Curves

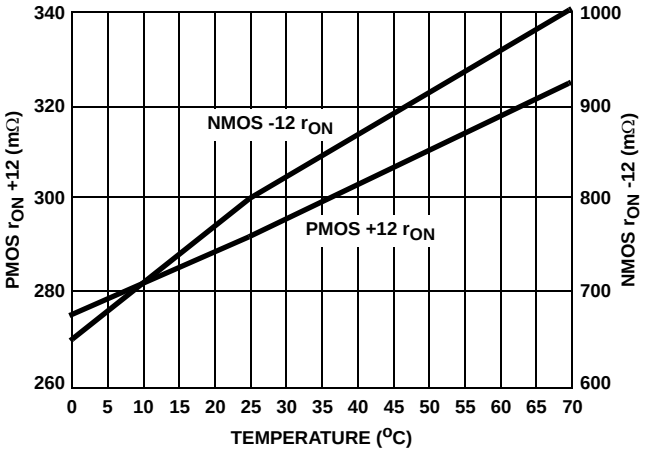


FIGURE 1. r_{ON} vs TEMPERATURE

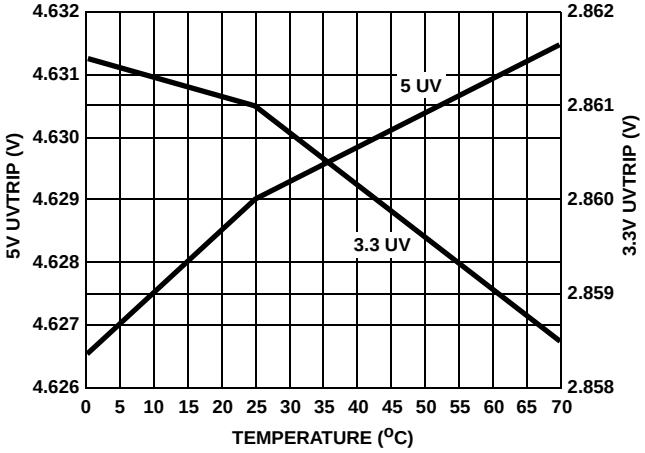


FIGURE 2. UV TRIP vs TEMPERATURE

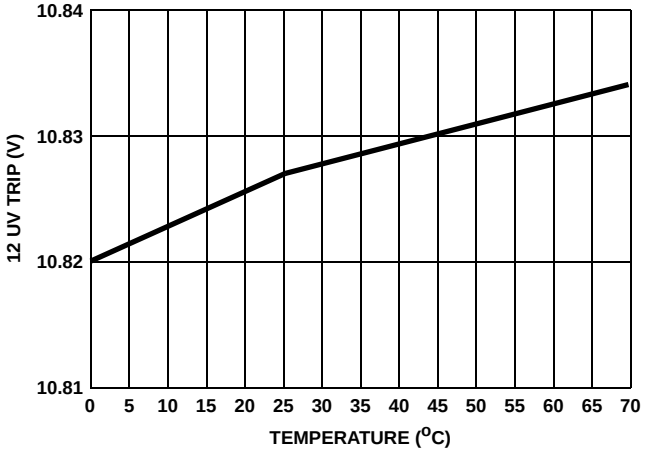


FIGURE 3. 12 UV TRIP vs TEMPERATURE

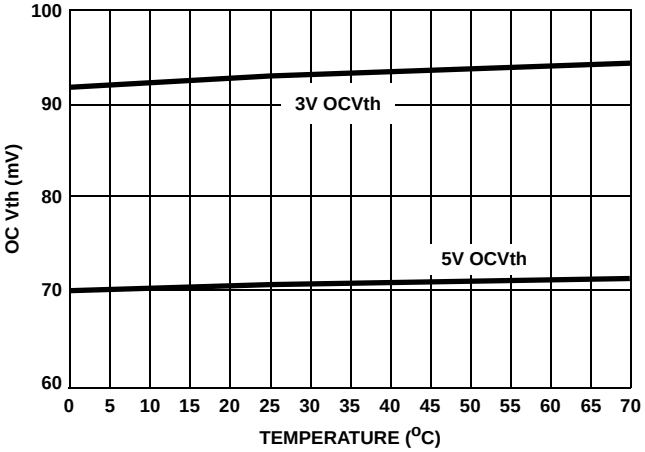


FIGURE 4. OC Vth vs TEMPERATURE (VR_{OCSET} = 1.21V)

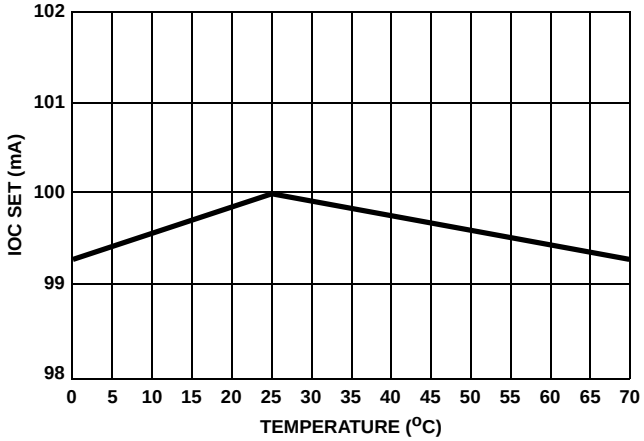


FIGURE 5. OCSET I vs TEMPERATURE

Typical Performance Curves (Continued)

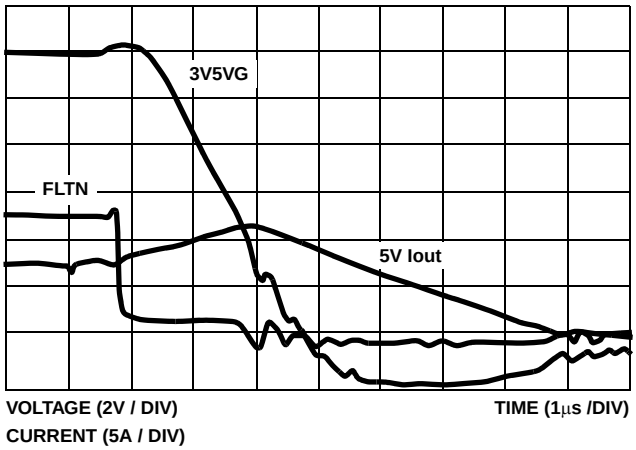


FIGURE 6. FLTN, 3V5VG RESPONSE TO OC, FLTN = 100pF

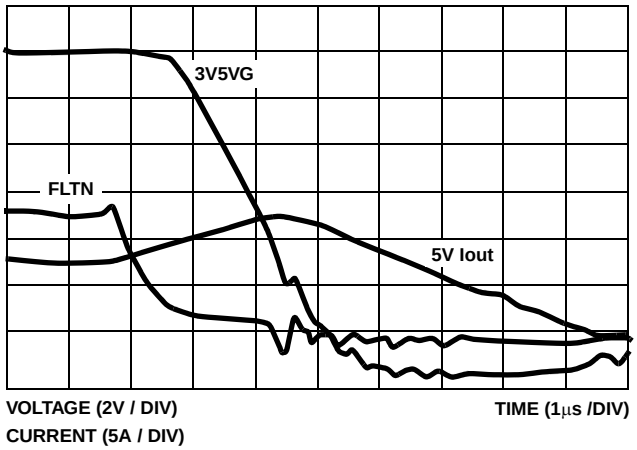


FIGURE 7. FLTN, 3V5VG RESPONSE TO OC, FLTN CAP = 0.001µF

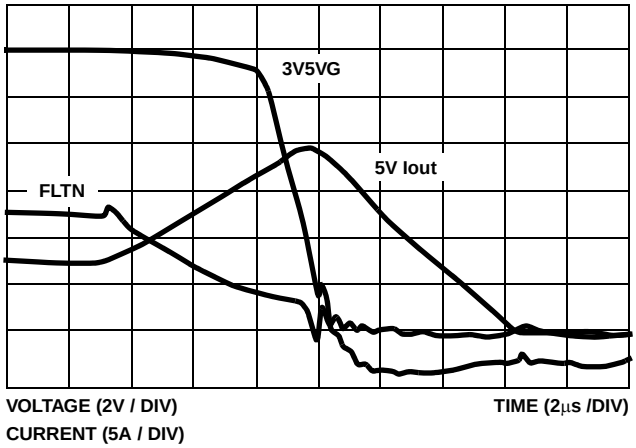


FIGURE 8. FLTN, 3V5VG RESPONSE TO OC, FLTN CAP = 0.01µF

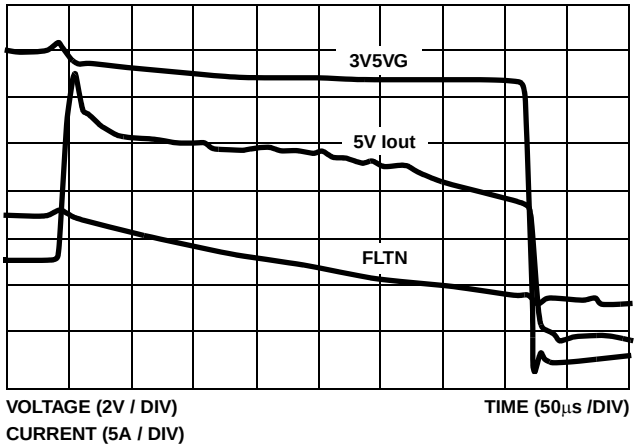


FIGURE 9. FLTN, 3V5VG RESPONSE TO OC, FLTN CAP = 1µF

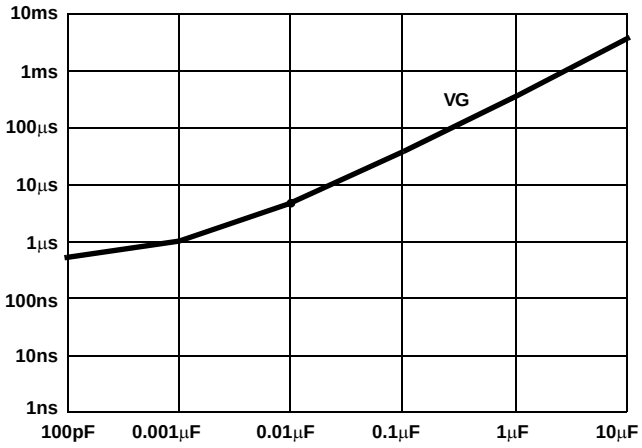


FIGURE 10. RESPONSE TIME vs FLTN CAP

HIP1011A PCI Hot Plug Controller

Key Feature Description and Operation

A drop-in alternative to the widely used HIP1011, the HIP1011A additionally features an adjustable delay time to fault reporting and latch-off of the MOSFET switches. During an over current condition (OC) on any output, or an under voltage (UV) condition on the +5V, +3.3V or +12V outputs, a LOW (0V) is presented on the FLTN output and all MOSFETs are latched-off. A programmable delay time from an OC or UV event to the FLTN signal going LOW and MOSFET latch-off can be designed into the system by a single capacitor from the FLTN pin to ground. The addition of an increasingly larger capacitor value on the FLTN pin increases the time from the OC or UV occurrence to the start of the FLTN high to low transition. The capacitor also slows the falling ramp thus delaying reaching the FLTN latch threshold of ~2.4V. Once the FLTN latch voltage threshold is reached the HIP1011A then simultaneously shuts down all four supplies. This added feature enables the HIP1011A to ignore both transient UV and OC events to the extent of a single capacitor value in the system design. This feature also may allow the system OS to complete housekeeping activities in preparation for a possible unplanned shutdown of the affected card by receiving an early warning signal from the HIP1011A.

Customizing and Optimizing Circuit Performance and Functionality

HOW ADJUSTABLE IS THE FAULT REPORTING DELAY AND TIME TO POWER SUPPLY LATCH-OFF?

Figure 12 illustrates the relationship between the FLTN signal and the gate drive outputs. Duration **a**, indicates the time between FLTN starting to transition from High to Low, (indicating a fault has occurred) and the start of the gate drive outputs latching off. The latch-off is initiated by the falling FLTN signal reaching the output latch threshold voltage, $V_{FLTN, TH}$. Table 1 illustrates the effect of the FLTN capacitor on the response time.

TABLE 1. RESPONSE TIME TABLE

	0.001µF	0.1µF	10µF
3V5VG Response **a**	0.85µs	37µs	3.8ms

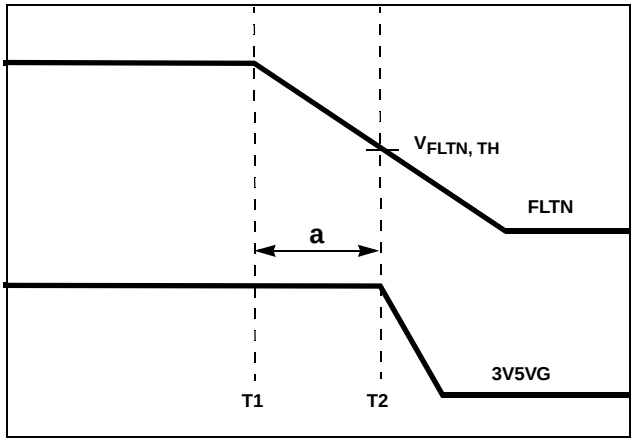
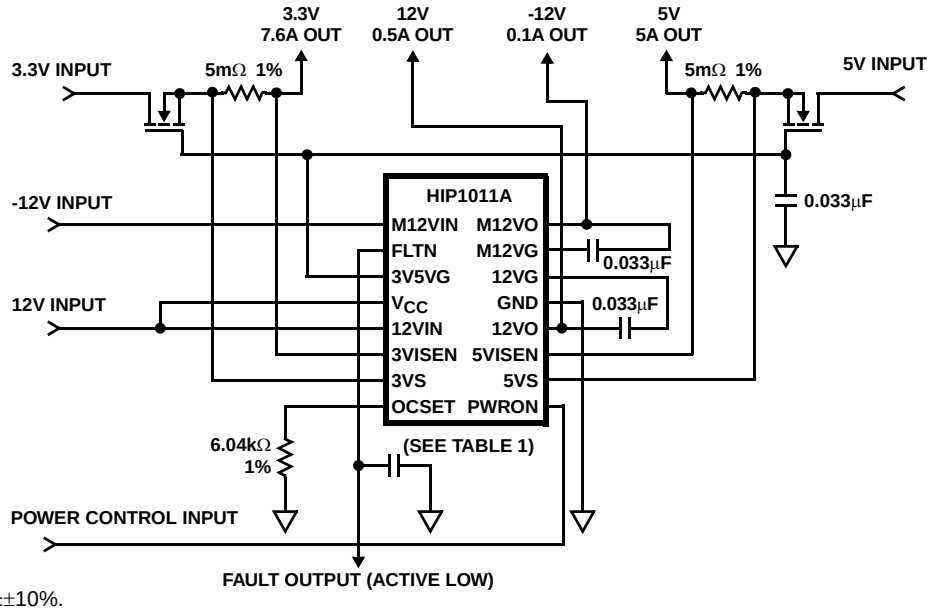


FIGURE 12. TIMING DIAGRAM

CAN THE HIP1011A BE USED ON A CompactPCI BOARD?

Yes, the HIP1011A can be used on a CompactPCI card application. See Technical Brief TB358.



NOTE:

3. All capacitors are ±±10%.

FIGURE 11. HIP1011A TYPICAL APPLICATION

ARE THERE PCB LAYOUT DESIGN BEST PRACTICES TO FOLLOW? WHAT ARE THEY?

As with most innovative ICs performing critical tasks there are crucial PCB layout best practices to follow for optimal performance. PCB traces that connect each end of the current sense resistors to the HIP1011A must not carry any load current. This can be accomplished by two dedicated PCB traces directly from the sense resistor to the HIP1011A, see examples of correct and incorrect layouts in Figure 13.

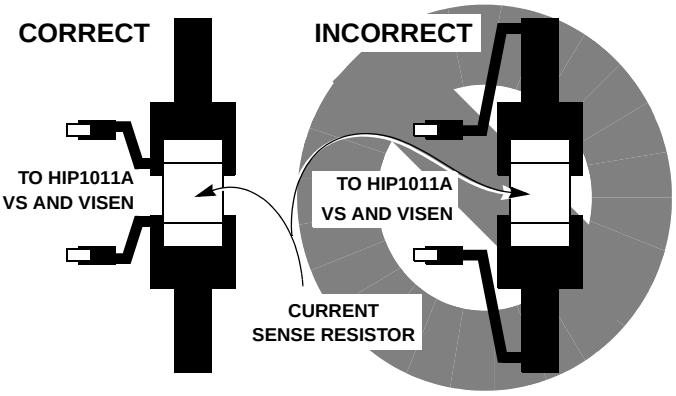


FIGURE 13. SENSE RESISTOR LAYOUT

Typical Applications: HIP1011A PCI Hot Plug Controller

Introduction to HIP1011A and PCI Hot Plug Evaluation Board

The HIP1011A is compatible with the PCI Hot Plug specification as it is derived from the widely used HIP1011. This device facilitates “HOT PLUGGING”, the removal or insertion of PCI compliant cards without the need to power down the server voltage bus. The HIP1011A controls all four, -12V, +12V, +3.3V, +5V supplies found in PCI applications, monitoring and protecting all against over current (OC) and the +12V, +3.3V, +5V for under voltage (UV) conditions. Reference the PCI Hot Plug specification available from www.pcisig.com.

Figure 14 illustrates the PCB pattern for implementation of the HIP1011A with 4 power MOSFETs. Additional components for optimizing performance in particular applications, ambient electrical noise levels or desired features will be necessary. The ease of implementation of the HIP1011A and MOSFETs is complemented by the small PCB foot print necessary, since both are available in 0.150 inch SOICs. The typical application requires only 1.1 square inches of PCB board space.

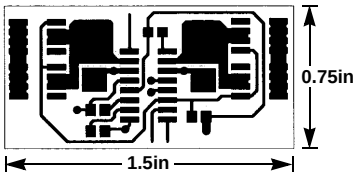


FIGURE 14. LAYOUT PLOT, ACTUAL SIZE (0.75in x 1.5in)

IS THERE A HIP1011A PCI HOT PLUG EVALUATION BOARD AVAILABLE?

There is an evaluation board available through your local Intersil sales office. The HIP1011AEVAL1 board (Figure 15) is a simple board designed to demonstrate and evaluate the HIP1011A using an external PWRON signal simulating a PCI Hot Plug environment. The HIP1011AEVAL1 board comes in 2 parts, the mother board with the HIP1011A, MOSFETs with external components and a load board simulating a ‘typical’ PCI load with adequate space for modifying the existing load or to add an electronic load. Even with a number of available test points the HIP1011A implementation space is still very efficient. In addition, the demo board offers adequate space to evaluate the application note discussions found in AN9737.

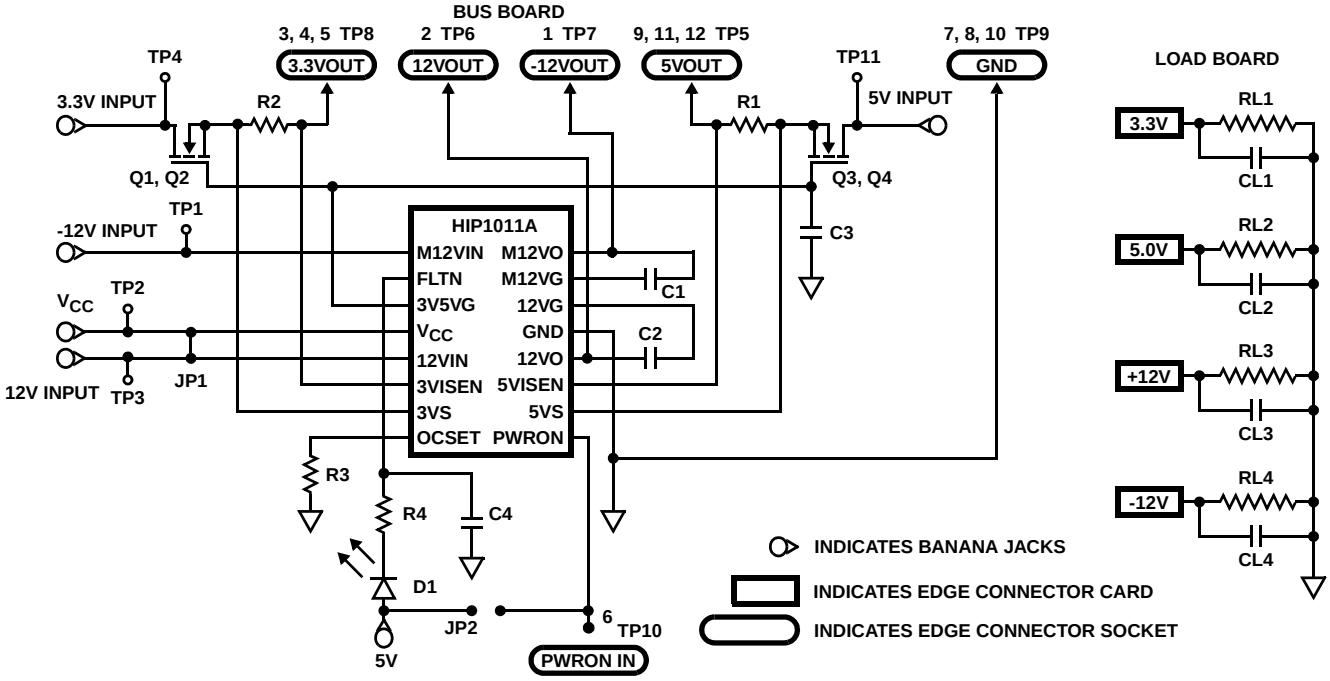


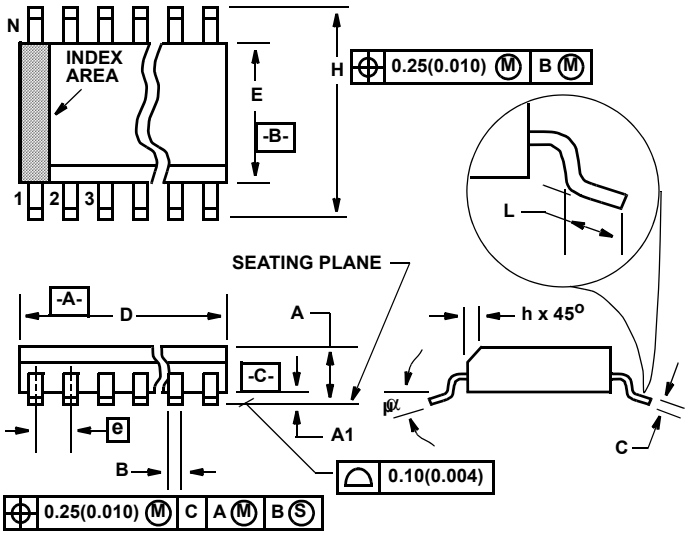
FIGURE 15. HIP1011AEVAL1

Table 2 details the BOM for the HIP1011AEVAL1 board.

TABLE 2.

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
U1	HIP1011ACB PCI Hot Plug Controller	Intersil Corporation, HIP1011ACB PCI Hot Plug Controller
Q1, Q2, Q3, Q4	RF1K49211	Intersil Corporation, RF1K49211 7A, 12V, 20mΩ, Logic Level N-Channel MOSFET
R1, R2	R_{SENSE} for 3.3V and 5V Supplies	Dale, WSL-2512 10mΩ Metal Strip Resistor
C1, C2, C3	Gate Timing Capacitors	0.033µF 805 Chip Capacitor
R3	Over Current Set Resistor	12.1kΩ 805 Chip Resistor
C4	Fault Stability Capacitor	100pF 805 Chip Cap
Conn. 1	Connector for Load Card	Sullins EZM06DRXH
R4	LED Series Resistor	4.7kΩ 805 Chip Resistor
D1	Fault Indicating LED	Red LED
JP1	V_{CC} to Switched or Unswitched 12V Supply	0.01” Spaced Pins for Jumper Block
JP2	PWRON to 5V	0.01” Spaced Pins for Jumper Block
RL1	3.3V Load Board Resistor	1.1Ω, 10W
RL2	5.0V Load Board Resistor	2.5Ω, 10W
RL3	+12V Load Board Resistor	47Ω, 5W
RL4	-12V Load Board Resistor	240Ω, 2W
CL1, CL2	+3.3V and +5.0V Load Board Capacitor	2200µF
CL3, CL4	+12V and -12V Load Board Capacitor	100µF

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 02/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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HIP1011ACBZA HIP1011ACBZA-T