Data Sheet | May 6, 2010 | FN6294.3

100V, 2A Peak, High Frequency Half-Bridge Drivers

The ISL2100A, ISL2101A are 100V, high frequency, half-bridge N-channel power MOSFET driver ICs. They are based on the popular HIP2100, HIP2101 half-bridge drivers, but offer several performance improvements. The ISL2100A has additional input hysteresis for superior operation in noisy environments and the inputs of the ISL2101A, like those of the ISL2100A, can now safely swing to the V_{DD} supply rail. Finally, both parts are available in a very compact 9 Ld DFN package to minimize the required PCB footprint

Ordering Information

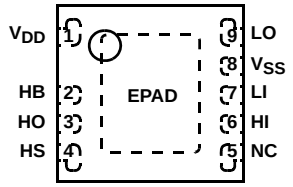
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL2100AAR3Z*	00AZ	-40 to +125	9 Ld 3x3 DFN	L9.3x3
ISL2101AAR3Z*	01AZ	-40 to +125	9 Ld 3x3 DFN	L9.3x3
ISL2100AABZ*	001ABZ	-40 to +125	8 Ld SOIC	M18.15
ISL2101AABZ*	01ABZ	-40 to +125	8 Ld SOIC	M18.15

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

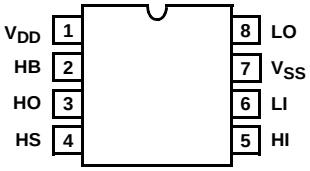
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL2100A, ISL2101A
(9 LD DFN)
TOP VIEW



ISL2100A, ISL2101A
(8 LD SOIC)
TOP VIEW



NOTE: EPAD = Exposed PAD.

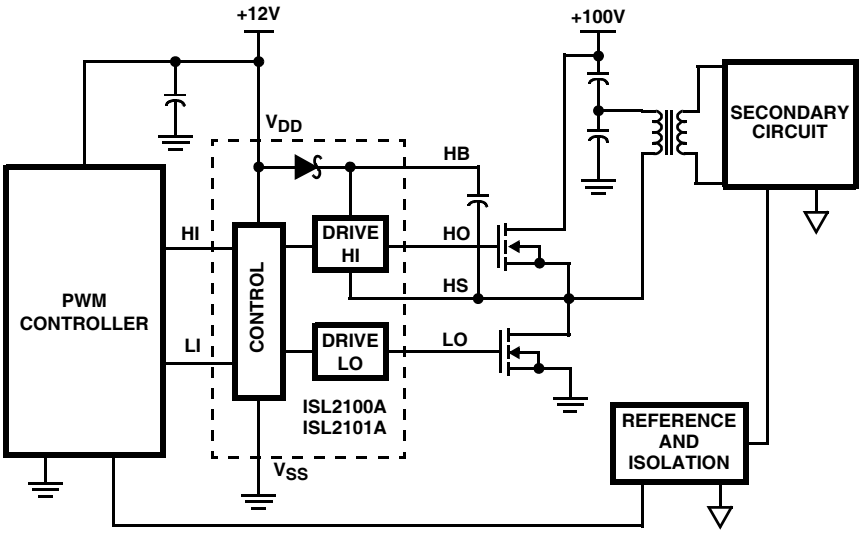
Features

- Drives N-Channel MOSFET Half-Bridge
- Space-Saving DFN Package
- DFN Package Compliant with 100V Conductor Spacing Guidelines per IPC-2221
- Pb-Free (RoHS compliant)
- Bootstrap Supply Max Voltage to 114VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times for Multi-MHz Circuits
- Drives 1nF Load with Typical Rise/Fall Times of 10ns
- CMOS Compatible Input Thresholds (ISL2100A)
- 3.3V/TTL Compatible Input Thresholds (ISL2101A)
- Independent Inputs Provide Flexibility
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Voltage Range (9V to 14V)
- Supply Undervoltage Protection
- 2.5Ω Typical Output Pull-Up/Pull-Down Resistance

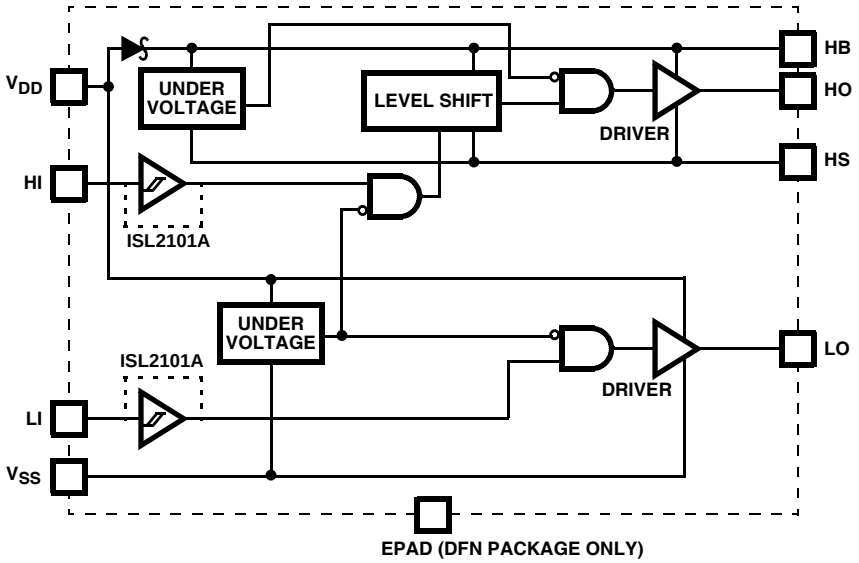
Applications

- Telecom Half-Bridge Converters
- Telecom Full-Bridge Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- Class-D Audio Amplifiers

Application Block Diagram



Functional Block Diagram



*EPAD = EXPOSED PAD. THE EPAD IS ELECTRICALLY ISOLATED FROM ALL OTHER PINS. FOR BEST THERMAL PERFORMANCE CONNECT THE EPAD TO THE PCB POWER GROUND PLANE.

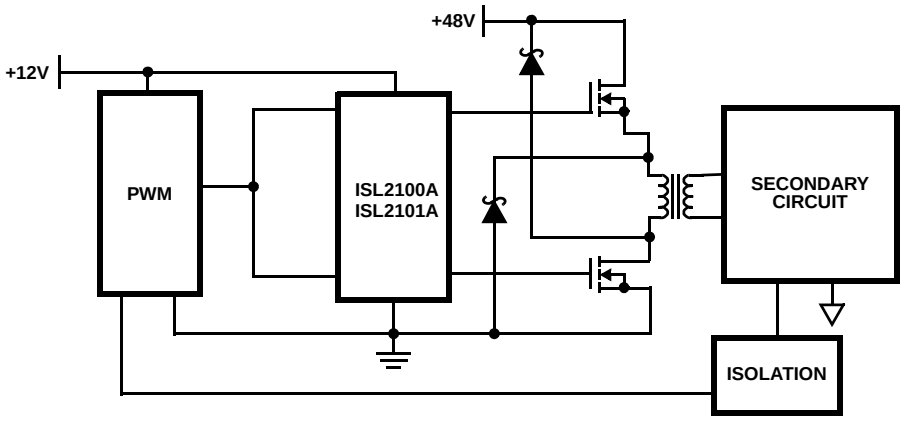


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

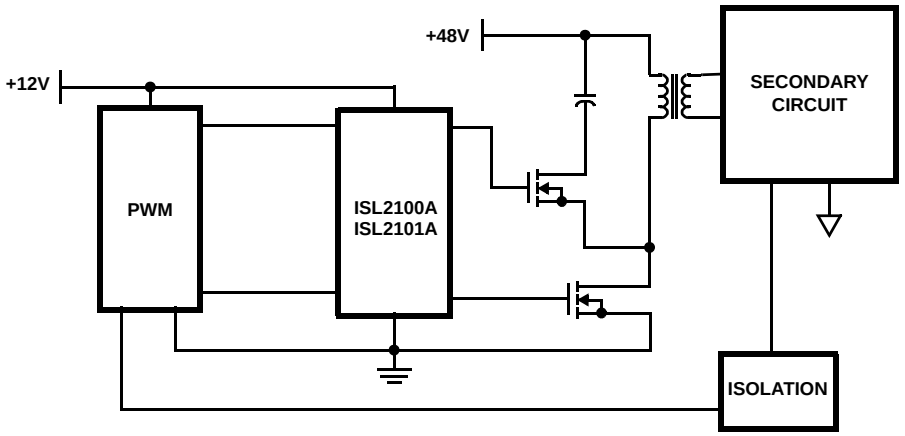


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE-CLAMP

Absolute Maximum Ratings

Supply Voltage, V_{DD}, V_{HB} - V_{HS} (Notes 1, 2) . . . . . -0.3V to 18V
LI and HI Voltages (Note 2) . . . . . -0.3V to V_{DD} + 0.3V
Voltage on LO (Note 2) . . . . . -0.3V to V_{DD} + 0.3V
Voltage on HO (Note 2) . . . . . V_{HS} - 0.3V to V_{HB} + 0.3V
Voltage on HS (Continuous) (Note 2) . . . . . -1V to 110V
Voltage on HB (Note 2) 118V
Average Current in V_{DD} to HB Diode 100mA

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . 9V to 14V
Voltage on HS . . . . . -1V to 100V
Voltage on HS . . . . . (Repetitive Transient) -5V to 105V
Voltage on HB . . V_{HS} + 8V to V_{HS} + 14V and V_{DD} - 1V to V_{DD} + 100V
HS Slew Rate. . . . . <50V/ns

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN (Notes 3, 4)	47	3.5
SOIC (Note 3)	120	N/A

Max Power Dissipation at +25°C in Free Air (DFN, Note 3) . . . 2.27W
Storage Temperature Range . . . . . -65°C to +150°C
For Recommended soldering conditions see Tech Brief TB389.
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. The ISL2100A-ISL2101A are capable of derated operation at supply voltages exceeding 14V. Figure 22 shows the high-side voltage derating curve for this mode of operation.
2. All voltages referenced to V_{SS} unless otherwise specified.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.
4. For θ_{JC}, the “case temp” is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379 for details.

Electrical Specifications

V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS								
V_{DD} Quiescent Current	I_{DD}	ISL2100A; LI = HI = 0V	-	0.1	0.25	-	0.3	mA
V_{DD} Quiescent Current	I_{DD}	ISL2101A; LI = HI = 0V	-	0.3	0.45	-	0.55	mA
V_{DD} Operating Current	I_{DDO}	ISL2100A; f = 500kHz	-	1.6	2.2	-	2.7	mA
V_{DD} Operating Current	I_{DDO}	ISL2101A; f = 500kHz	-	1.9	2.5	-	3	mA
Total HB Quiescent Current	I_{HB}	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	I_{HBO}	f = 500kHz	-	2.0	2.5	-	3	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	LI = HI = 0V; V_{HB} = V_{HS} = 114V	-	0.05	1	-	10	µA
HB to V_{SS} Current, Operating	I_{HBSO}	f = 500kHz; V_{HB} = V_{HS} = 114V	-	0.9	-	-	-	mA
INPUT PINS								
Low Level Input Voltage Threshold	V_{IL}	ISL2100A	3.7	4.4	-	2.7	-	V
Low Level Input Voltage Threshold	V_{IL}	ISL2101A	1.4	1.8	-	1.2	-	V
High Level Input Voltage Threshold	V_{IH}	ISL2100A	-	6.6	7.4	-	8.4	V
High Level Input Voltage Threshold	V_{IH}	ISL2101A	-	1.8	2.2	-	2.4	V
Input Voltage Hysteresis	V_{IHYS}	ISL2100A	-	2.2	-	-	-	V
Input Pull-down Resistance	R_I		-	210	-	100	500	kΩ
UNDERVOLTAGE PROTECTION								
V_{DD} Rising Threshold	V_{DDR}		6.8	7.3	7.8	6.5	8.1	V
V_{DD} Threshold Hysteresis	V_{DDH}		-	0.6	-	-	-	V
HB Rising Threshold	V_{HBR}		6.2	6.9	7.5	5.9	7.8	V

Electrical Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
HB Threshold Hysteresis	V_{HBH}		-	0.6	-	-	-	V
BOOTSTRAP DIODE								
Low Current Forward Voltage	V_{DL}	I_{VDD-HB} = 100µA	-	0.5	0.6	-	0.7	V
High Current Forward Voltage	V_{DH}	I_{VDD-HB} = 100mA	-	0.7	0.9	-	1	V
Dynamic Resistance	R_D	I_{VDD-HB} = 100mA	-	0.8	1	-	1.5	Ω
LO GATE DRIVER								
Low Level Output Voltage	V_{OLL}	I_{LO} = 100mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHL}	I_{LO} = -100mA, $V_{OHL} = V_{DD} - V_{LO}$	-	0.25	0.3	-	0.4	V
Peak Pull-Up Current	I_{OHL}	V_{LO} = 0V	-	2	-	-	-	A
Peak Pull-Down Current	I_{OLL}	V_{LO} = 12V	-	2	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V_{OLH}	I_{HO} = 100mA	-	0.25	0.3	-	0.4	V
High Level Output Voltage	V_{OHH}	I_{HO} = -100mA, $V_{OHH} = V_{HB} - V_{HO}$	-	0.25	0.3	-	0.4	V
Peak Pull-Up Current	I_{OHH}	V_{HO} = 0V	-	2	-	-	-	A
Peak Pull-Down Current	I_{OLH}	V_{HO} = 12V	-	2	-	-	-	A

Electrical Specifications Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	34	50	-	60	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	31	50	-	60	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	39	50	-	60	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	39	50	-	60	ns
Delay Matching: Upper Turn-Off to Lower Turn-On	t_{MON}		1	8	-	-	16	ns
Delay Matching: Lower Turn-Off to Upper Turn-On	t_{MOFF}		1	6	-	-	16	ns
Either Output Rise/Fall Time (10% to 90%/90% to 10%)	t_{RC}, t_{FC}	C_L = 1nF	-	10	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V/9V to 3V)	t_R, t_F	C_L = 0.1µF	-	0.5	0.6	-	0.8	us
Minimum Input Pulse Width that Changes the Output	t_{PW}		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

Pin Descriptions

SYMBOL	DESCRIPTION
V_{DD}	Positive supply to lower gate driver. Bypass this pin to V_{SS}.
HB	High-side bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
HO	High-side output. Connect to gate of high-side power MOSFET.
HS	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	High-side input.
LI	Low-side input.
V_{SS}	Chip negative supply, which will generally be ground.
LO	Low-side output. Connect to gate of low-side power MOSFET.
EPAD	Exposed pad. Connect to ground or float. The EPAD is electrically isolated from all other pins.

Timing Diagrams

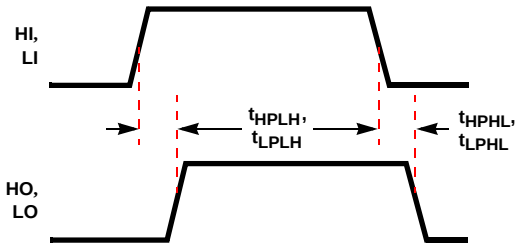


FIGURE 3. PROPAGATION DELAYS

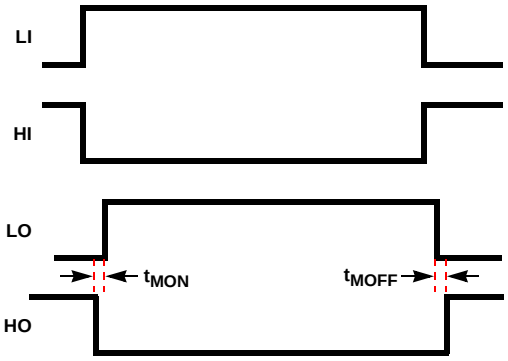


FIGURE 4. DELAY MATCHING

Typical Performance Curves

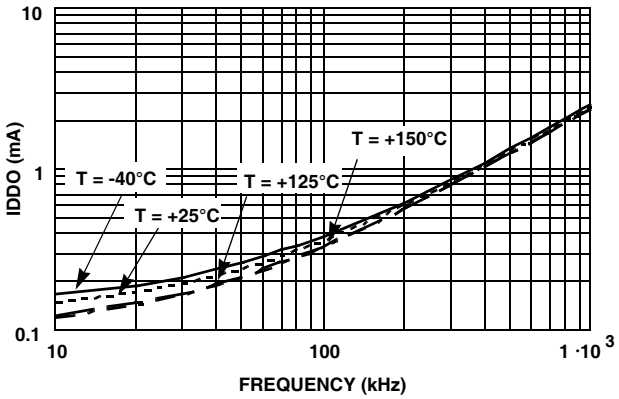


FIGURE 5. ISL2100A IDD OPERATING CURRENT vs FREQUENCY

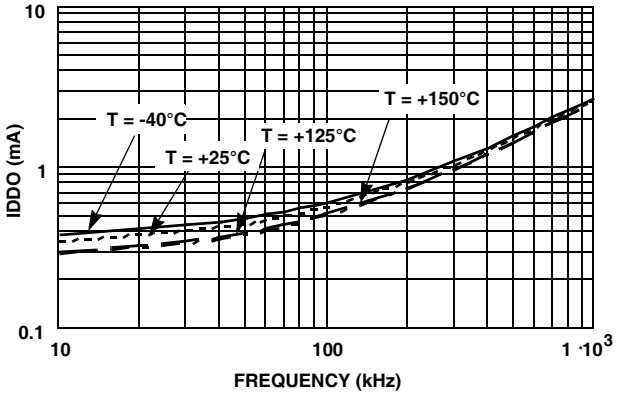


FIGURE 6. ISL2101A IDD OPERATING CURRENT vs FREQUENCY

Typical Performance Curves (Continued)

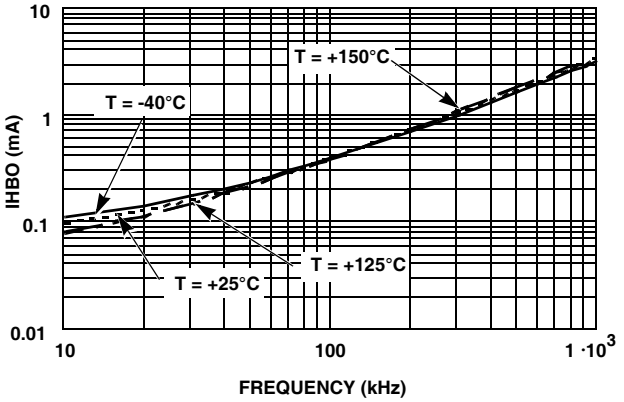


FIGURE 7. IHB OPERATING CURRENT vs FREQUENCY

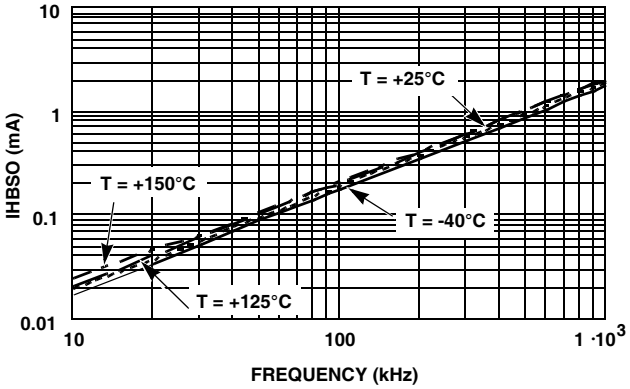


FIGURE 8. IHBS OPERATING CURRENT vs FREQUENCY

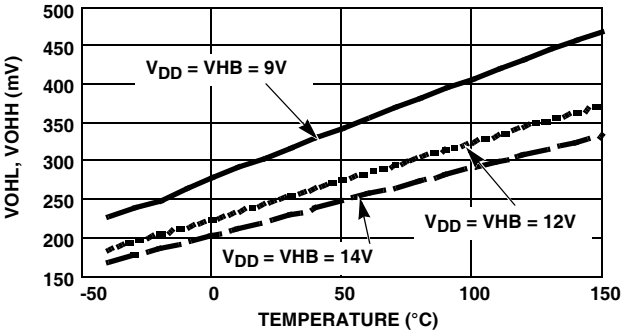


FIGURE 9. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

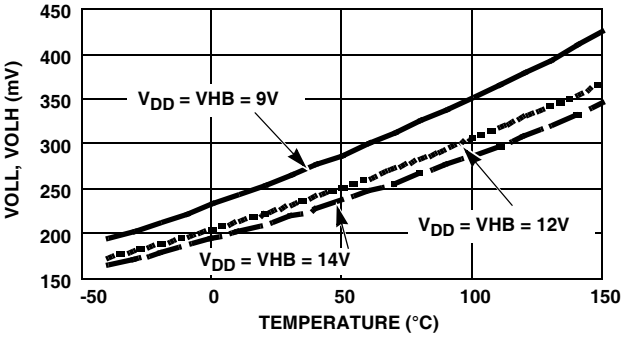


FIGURE 10. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

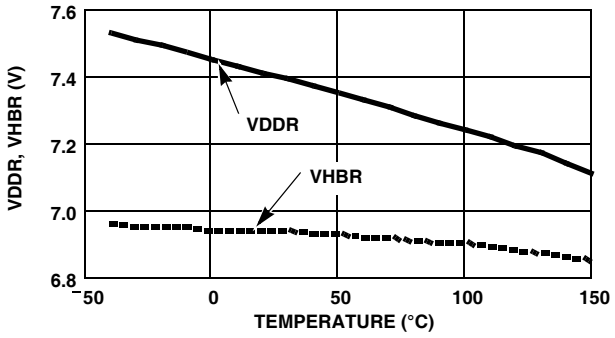


FIGURE 11. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

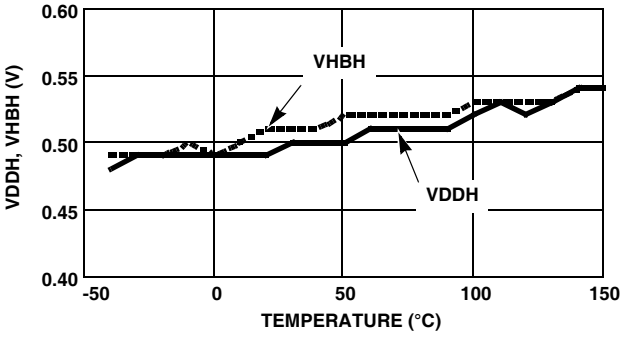


FIGURE 12. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

Typical Performance Curves (Continued)

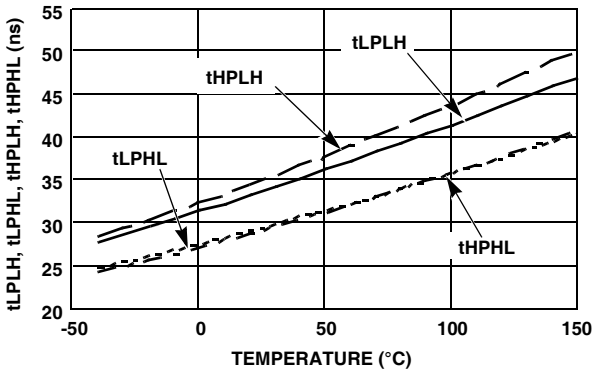


FIGURE 13. ISL2100A PROPAGATION DELAYS vs TEMPERATURE

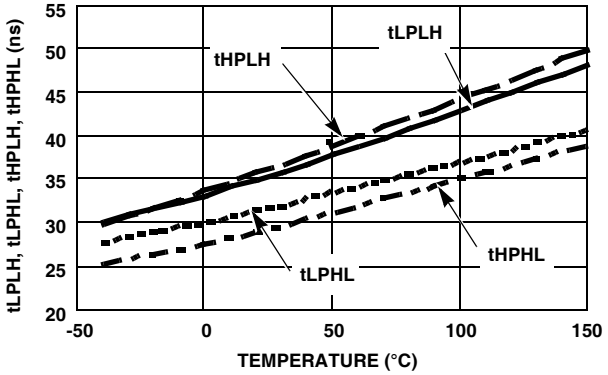


FIGURE 14. ISL2101A PROPAGATION DELAYS vs TEMPERATURE

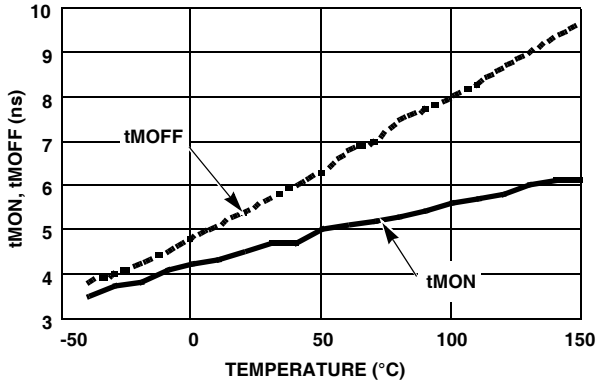


FIGURE 15. ISL2100A DELAY MATCHING vs TEMPERATURE

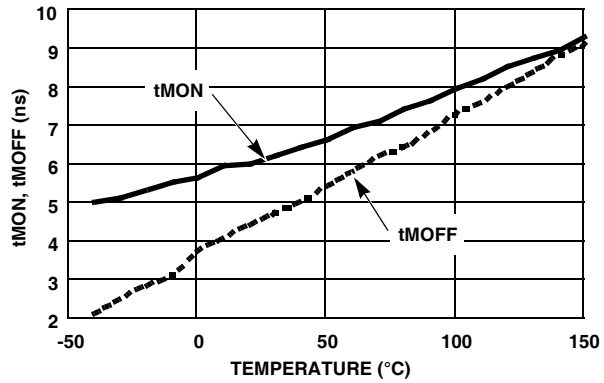


FIGURE 16. ISL2101A DELAY MATCHING vs TEMPERATURE

FIGURE 17. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

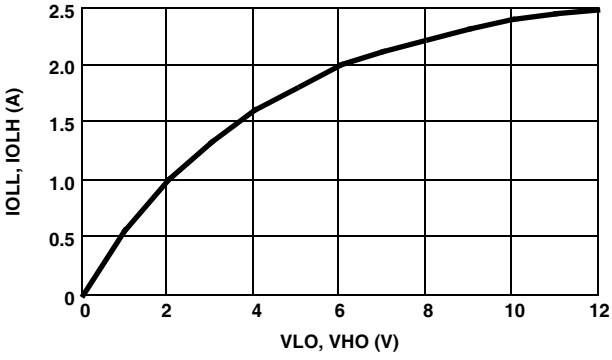


FIGURE 18. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

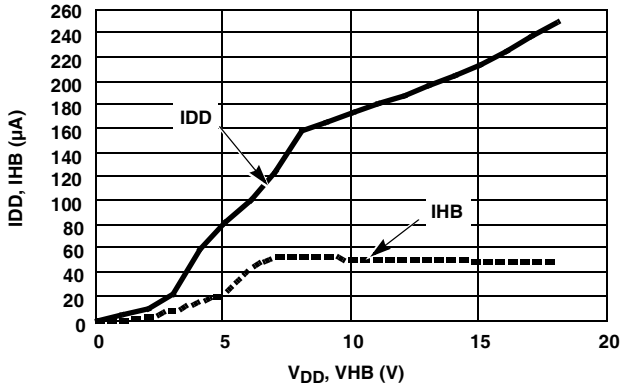


FIGURE 19. ISL2100A QUIESCENT CURRENT vs VOLTAGE

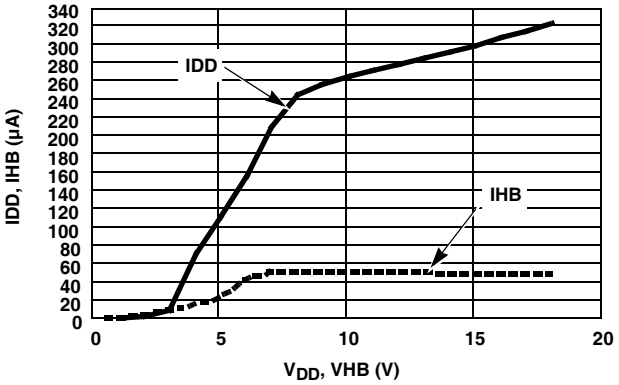


FIGURE 20. ISL2101A QUIESCENT CURRENT vs VOLTAGE

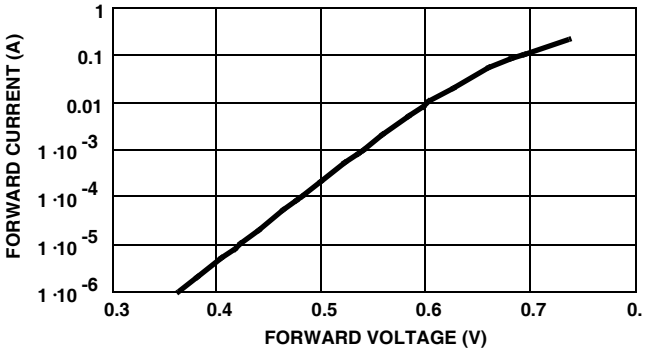


FIGURE 21. BOOTSTRAP DIODE I-V CHARACTERISTICS

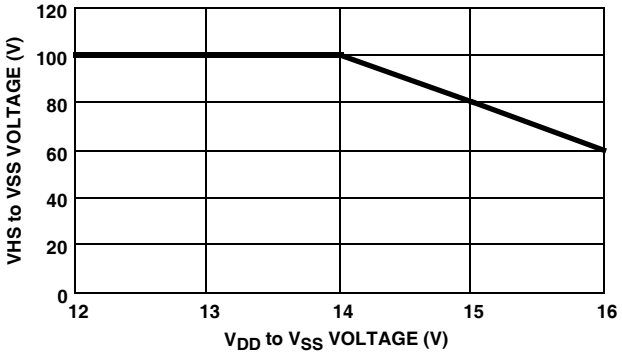
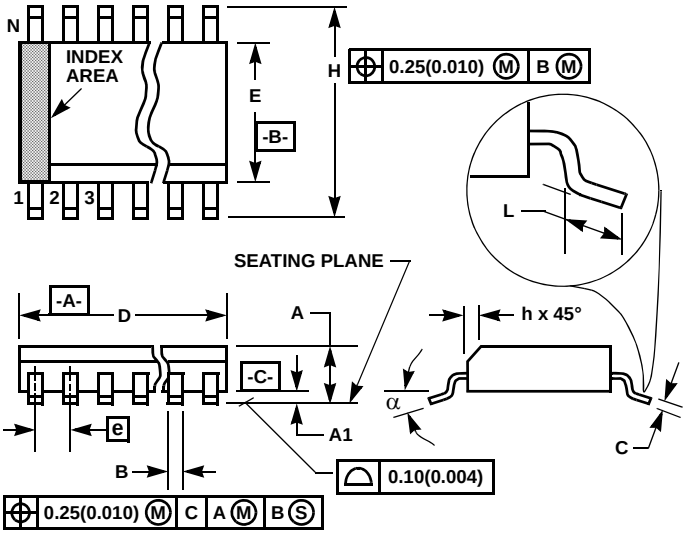


FIGURE 22. VHS VOLTAGE vs V_{DD} VOLTAGE

Small Outline Plastic Packages (SOIC)



NOTES:

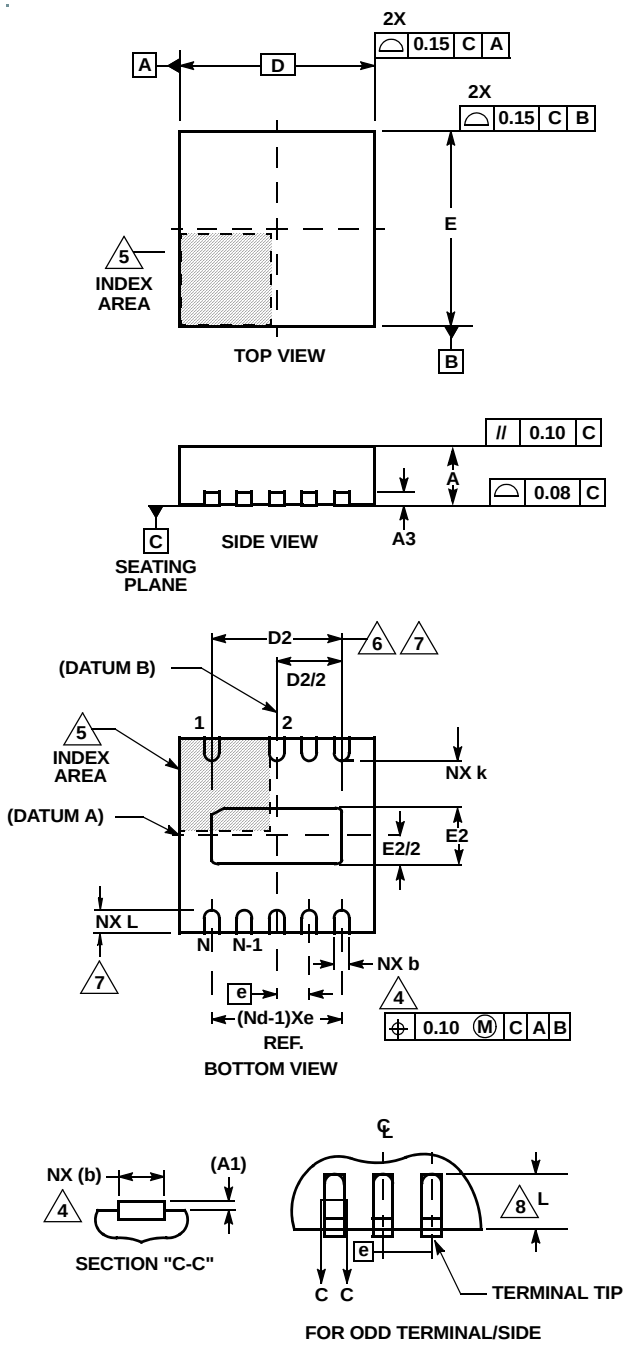
5. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
6. Dimensioning and tolerancing per ANSI Y14.5M-1982.
7. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
8. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
9. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
10. “L” is the length of terminal for soldering to a substrate.
11. “N” is the number of terminal positions.
12. Terminal numbers are shown for reference only.
13. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
14. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

Dual Flat No-Lead Plastic Package (DFN)



L9.3x3

9 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	4, 7
D		3.00 BSC		-
D2	1.85	2.00	2.10	6, 7
E		3.00 BSC		-
E2	0.80	0.95	1.05	6, 7
e		0.50 BSC		-
k	0.60	-	-	-
L	0.25	0.35	0.45	7
N		9		2

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. All dimensions are in millimeters. Angles are in degrees.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
7. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
8. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

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