ISL25700

Programmable Temperature Controlled MOSFET Driver

FN6885
Rev 1.00
July 23, 2014

The Temperature Controlled MOSFET Driver is a highly integrated solution that combines a MOSFET driver with overcurrent protection and two 8-bit resolution DACs on a monolithic CMOS integrated circuit (IC).

The ISL25700 sets up and monitors temperature at the point of interest, compares it with the user programmable setpoint, and adjusts the output until the set temperature is reached. An external power MOSFET, a heater, an NTC thermistor and the ISL25700 are parts of the temperature control loop.

It also features programmable overcurrent protection of the MOSFET. The current protection automatically adjusts the output voltage in order to keep MOSFET power under user defined limits. The protection settings always override the temperature settings that cause violation of the current limit.

There is an additional 8-bit General Purpose DAC that is available for application specific use.

The ISL25700 can be used in a variety of applications where constant temperature is a key parameter.

Applications

- Oven Controlled Applications with Micro Temperature Chamber in:
  - Basestations
  - Spectrometers
  - Precision Meters
  - Precision Generators

Features

- User-programmable setpoint via I^2C serial interface
- Setpoint temperature range from +40°C to +110°C
- Operational temperature range from -40°C to +125°C
- 3°C initial setpoint accuracy
- Coarse and fine tuning setpoint control
  - +15°C coarse adjustment
  - +0.1°C fine adjustment
- ±0.5°C long-term drift error
- Programmable current protection of external MOSFET
- 5-bit Selectable Gain Control
- Wide Power Supply Range: 3V to 15V
- Works with 20kΩ to 200kΩ External NTC Thermistor
- General Purpose 8-bit DAC - 0.4% Output Resolution
- High Reliability
  - Endurance: 10,000 Data Changes per Bit per Register
  - Register Data Retention: 10 years @ T ≤ +125°C
- 10 Lead µTQFN 2.1mmx1.6mm Package
- Pb-free (RoHS Compliant)

Related Literature

- AN1825, “Overcoming the Minimum V_{DD} Ramp Rate Limitation of the ISL25700”

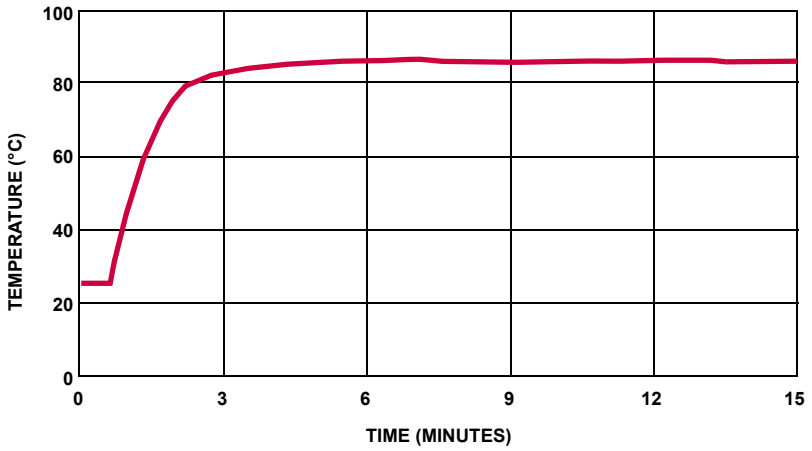
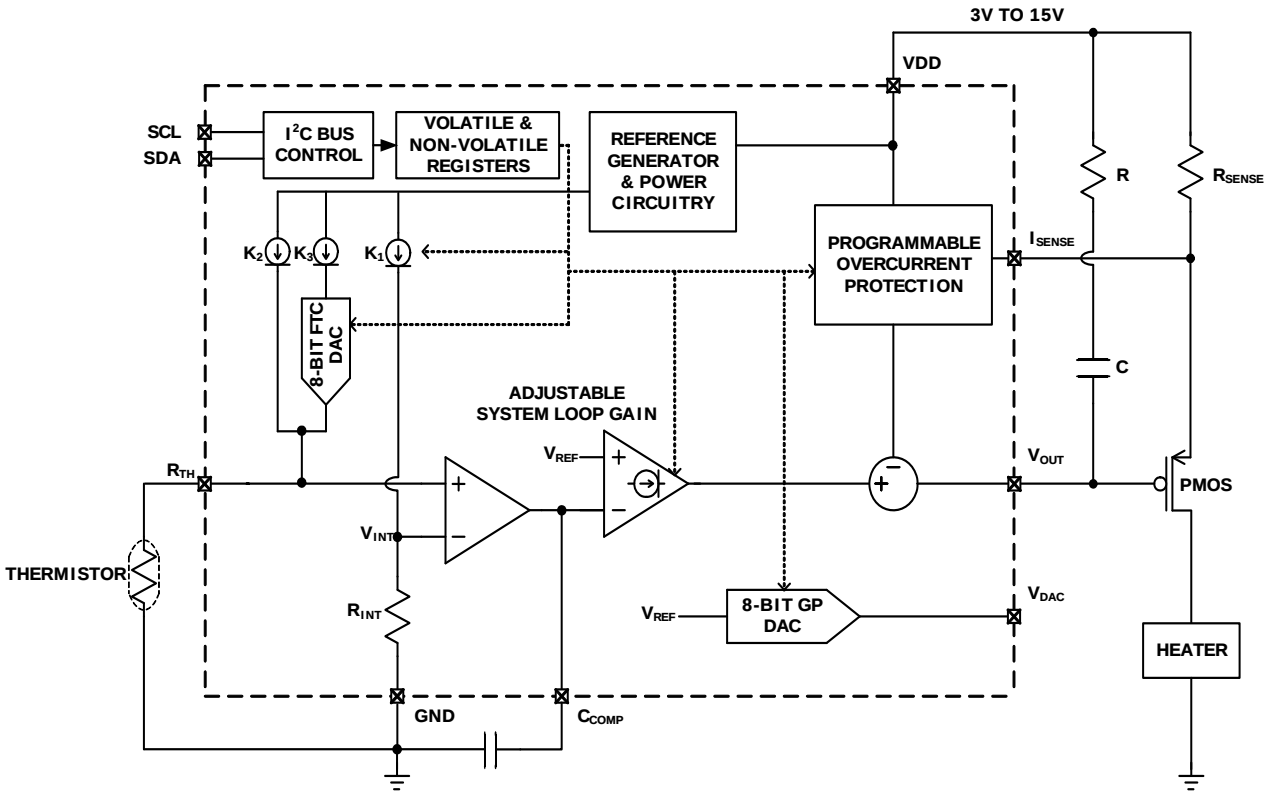


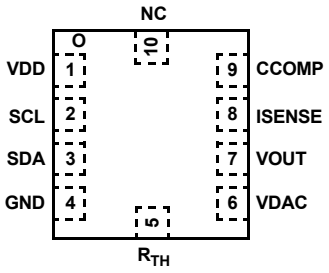
FIGURE 1. TYPICAL TEMPERATURE SETTLING TIME

Block Diagram/Application Circuit



Pin Configuration

ISL25700
(10 LD µTQFN)
TOP VIEW



Pin Descriptions

µTQFN PIN	SYMBOL	DESCRIPTION
1	VDD	Power supply. This pins supplies the power necessary to operate the chip.
2	SCL	I^2C interface input clock. This input is the serial clock of the I^2C serial interface. SCL requires an external pull-up resistor. It has an internal pull-down resistor of ~3MΩ to prevent a floating input if the pin will be left unconnected.
3	SDA	Open Drain Serial Data Input/Output for the I^2C interface. The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock. The SDA pin requires an external pull-up resistor. It has an internal pull-down resistor of ~3MΩ to prevent a floating input if the pin will be left unconnected.
4	GND	Ground. Bias and reference ground of the chip.
5	R_{TH}	External NTC thermistor. An external NTC thermistor makes one shoulder of the Wheatstone bridge and must be connected between the R_{TH} pin and GND.
6	VDAC	DAC Output. This is the output of the precision 8-bit DAC. Default DAC output is in the range of 0V to 2V. The DAC output range can be extended with a gain of 2 by setting the DAC Gain bit.
7	VOUT	Output voltage that controls an external P-MOSFET. This pin drives an external P-MOSFET proportional to unbalanced condition of the Wheatstone bridge.
8	ISENSE	Current Sense input. This pin monitors voltage drop over an external current sense resistor RSENSE. Power dissipation of the P-MOSFET will be limited when ISENSE exceeds the voltage drop limit set in the Current Sense Register.
9	CCOMP	Compensation capacitor. A compensation ceramic capacitor must be added between CCOMP and GND to increase chip stability. This capacitor provides a negative feedback for the operational amplifier and its value can be from 30pF to 1000pF.
10	NC	Not internally connected.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	UNITS PER REEL	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL25700FRUZ-T	GT	3000	-40 to +125	10 Ld 2.1x1.6 µTQFN	L10.2.1x1.6A
ISL25700FRUZ-TK	GT	1000	-40 to +125	10 Ld 2.1x1.6 µTQFN	L10.2.1x1.6A
ISL25700FRUZ-T7A	GT	250	-40 to +125	10 Ld 2.1x1.6 µTQFN	L10.2.1x1.6A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL25700. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Voltage at any Digital Interface Pin
with respect to GND . . . . . -0.3V to 6V
V_{DD} . . . . . -0.3V to +16.5V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 5kV
Machine Model (Tested per JESD22-A115B) 200V
Latchup . . . . . Class II, Level A at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN Package (Note 4, 5)	135	75

Storage Temperature . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Full-range Industrial) . . . . . -40°C to +125°C
V_{DD} . . . . . 3V to 15V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Analog Specifications

Over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 13)	TYP (Note 6)	MAX (Note 13)	UNITS
T_{SET}	Temperature Set Point	T_{SET} must be above ambient	MIN		40		°C
			MAX		110		°C
	Temperature Set Point Accuracy	3 sigma standard deviation			±3		°C
T_{SET_COARSE}	Coarse Adjustment of Set Point	R_{TH} = 100k @ +25°C, $B_{25/85}$ = 4100k (Note 14)			15		°C
T_{SET_FINE}	Fine Adjustment of Set Point				0.1		°C
$T_{SET\_FINE\_INL}$ (Note 9)	Fine Control Integral Non-linearity			**-2.5**	±0.9	**+2.5**	LSB (Note 7)
$T_{SET\_FINE\_DNL}$ (Note 8)	Fine Control Differential Non-linearity			**-2**	±0.5	**+2**	LSB (Note 7)
T_{DRIFT}	Long-term Drift of Set Point	1000h, Reg.1 = x2h, Reg.2 = 80h, Reg.3 = 90h			±0.5		°C
I_{TH}	Thermistor Current Range			**25**	40	**55**	µA
R_{TH}	NTC Thermistor Range	Resistance @ +25°C		20	100	200	kΩ
V_{OUT}	External P-MOSFET Gate Voltage	I_{OUT} = 0µA		**0.25**		**V_{DD}**	V
	V_{OUT} Swing @ Fixed V_{DD}	I_{OUT} = 0µA	MIN		V_{DD} - 2.5		V
I_{OUT}	Output Current					7	µA
V_{SENSE}	Overcurrent Protection Set Point	$V_{SENSE} = I_{SENSE} \times R_{SENSE}$; see Table 3			200 to 1750		mV
GENERAL PURPOSE DAC (MEASUREMENTS BETWEEN GND AND VDAC)							
$V_{DAC\ MAX}$	Maximum DAC Output	Using internal V_{REF}, $V_{DD} \leq$ 5V, No load, Gain = 1			2	**2.5**	V
		V_{DD} > 5V, No load, Gain = 2			4	**5.0**	V
INL (Note 9)	Integral Non-Linearity	No load		**-1**	±0.4	**+1**	LSB (Note 7)
DNL (Note 8)	Differential Non-linearity	No load		**-0.75**	±0.3	**+0.75**	LSB (Note 7)

Analog Specifications

Over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 6)	MAX (Note 13)	UNITS
V_{DAC_OFFSET}	Offset	DAC register set to 0, No load	**0**	0.2	**1**	LSB (Note 7)
R_{OUT}	DAC Output Impedance			350		Ω
PSRR	Power Supply Rejection Ratio	DAC at middle scale, frequency from 0Hz to 25kHz		-85		dB
TC_V (Notes 10, 11)	Temperature Coefficient	DAC register set between 20 hex and FF hex		±45		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 6)	MAX (Note 13)	UNITS
I_{DD1}	V_{DD} Supply Current (Non-Volatile Write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Write States) I_{PMOS} = 0mA, DAC unload			**4**	mA
I_{DD2}	V_{DD} Supply Current (Volatile Write/read)	I_{PMOS} = 0mA, DAC unload			**2.8**	mA
I_{LkgDig}	Leakage Current, at SDA and SCL Pins	Voltage at pin from GND to VCC	**-3**		**3**	µA
t_{DAC} (Note 11)	DAC Settling Time	From bus STOP condition to V_{DAC} change			**3**	µs
V_{POR}	Power-On Recall Voltage	Minimum V_{DD} at which memory recall occurs		2.5	**2.9**	V
V_{DD} Ramp	V_{DD} Ramp Rate	@ any level from 0V to 15V	**0.2**		**50**	V/ms
t_D (Note 11)	Power-Up Delay	V_{DD} above V_{POR}, to DAC Register recall completed, and I^2C Interface in standby state			**1**	ms
EEPROM SPECIFICATIONS						
	EEPROM Endurance		**10,000**			Cycles
	EEPROM Retention	Temperature ≤ +55°C	50			Years
		Temperature ≤ +125°C	10			Years
SERIAL INTERFACE SPECIFICATIONS						
V_{I2C}	I^2C Bus Voltage	$V_{I2C} \leq V_{DD}$	**2.7**		**5.5**	V
V_{IL}	SDA, and SCL Input Buffer LOW Voltage	V_{I2C} from 2.7V to 5.5V			**0.8**	V
V_{IH}	SDA, and SCL Input Buffer HIGH Voltage	V_{I2C} from 2.7V to 5.5V	**1.4**			V
Hysteresis (Note 11)	SDA and SCL Input Buffer Hysteresis		**0.05*V_{I2C}**			V
V_{OL} (Note 11)	SDA Output Buffer LOW Voltage, Sinking 4mA		**0**		**0.4**	V
Cpin (Note 11)	SDA, and SCL Pin Capacitance				**10**	pF
f_{SCL}	SCL Frequency				**400**	kHz
t_{IN} (Note 11)	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			**50**	ns
t_{AA} (Note 11)	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{I2C}, until SDA exits the 30% to 70% of V_{I2C} window			**900**	ns

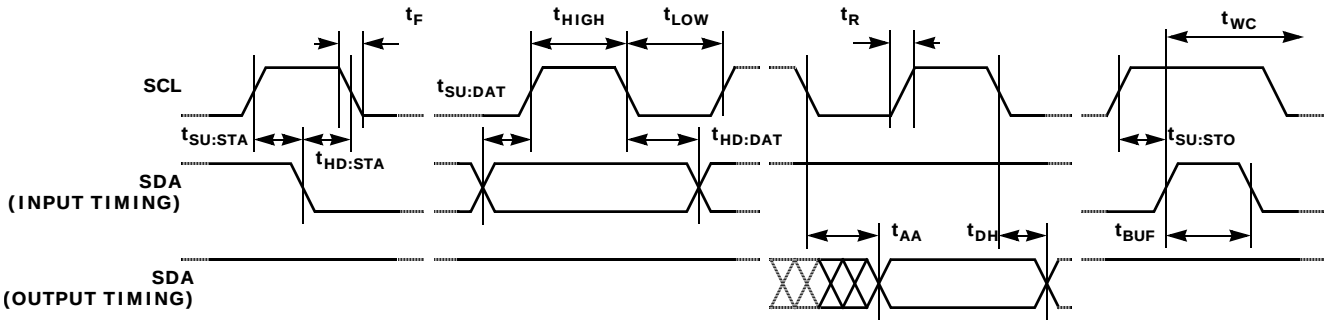
Operating Specifications Over the recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 13)	TYP (Note 6)	MAX (Note 13)	UNITS
t_{BUF} (Note 11)	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{I2C} during a STOP condition, to SDA crossing 70% of V_{I2C} during the following START condition	**1300**			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{I2C} crossing	**1300**			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{I2C} crossing	**600**			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{I2C}	**600**			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{I2C} to SCL falling edge crossing 70% of V_{I2C}	**600**			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{I2C} window, to SCL rising edge crossing 30% of V_{I2C}	**100**			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 70% of V_{I2C} to SDA entering the 30% to 70% of V_{I2C} window	**0**			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{I2C}, to SDA rising edge crossing 30% of V_{I2C}	**600**			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{I2C}, until SDA enters the 30% to 70% of V_{I2C} window	**0**			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{I2C}	**20 + 0.1 * Cb**		**250**	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{I2C}	**20 + 0.1 * Cb**		**250**	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	**10**		**400**	pF
Rpu (Note 11)	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	**1**			kΩ
t_{WC} (Notes 11, 12)	Non-Volatile Write Cycle Time			15	**20**	ms

NOTES:

6. Typical values are for T_A = +25°C and 12V supply voltage.
7. LSB: $[VDAC_{255} - VDAC_0]/255$. $VDAC_{255}$ and $VDAC_0$ are the DAC output voltage when DAC register set to FF hex and 00 hex respectively.
8. DNL = $[VDAC_i - VDAC_{i-1}]$/LSB-1, for i = 1 to 255. i is the DAC register setting.
9. INL = $[VDAC_i - (i \bullet LSB + VDAC_0)]$/LSB for i = 1 to 255.
10. $$TC_V = \frac{VDAC_i(T) - VDAC_i(40°C)}{VDAC_i(40°C)} \times \frac{10^6}{(T-40)°C}$$ for i = 1 to 255 decimal, T = -40°C to +125°C, referenced to 40°C.
11. Limits established by characterization and are not production tested.
12. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle. The Busy Polling method can be used to determine the end of the non-volatile write cycle.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. $B_{25/85}$ is a thermistor material specific constant; represents the slope of the Resistance vs. Temperature curve.

SDA vs SCL Timing



Typical Performance Curves

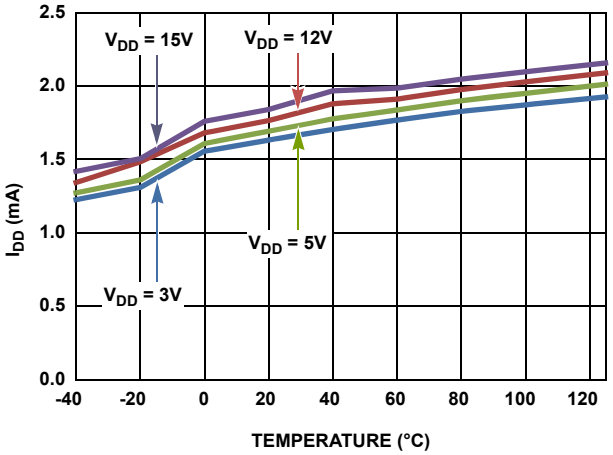


FIGURE 2. SUPPLY CURRENT I_{DD} vs V_{DD}

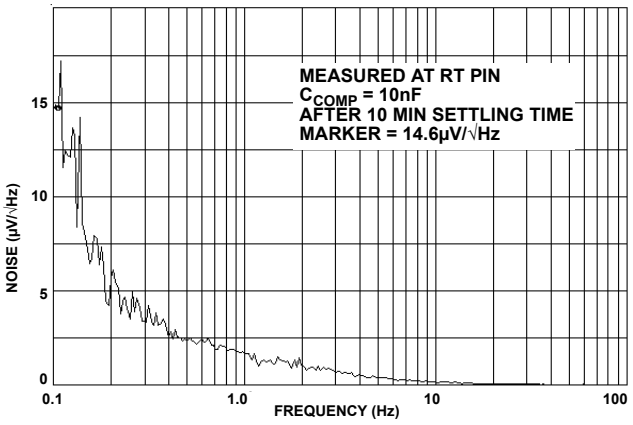


FIGURE 3. NOISE LEVEL AT R_{TH} INPUT IN CLOSE LOOP APPLICATION 2µV/√Hz @ 1Hz

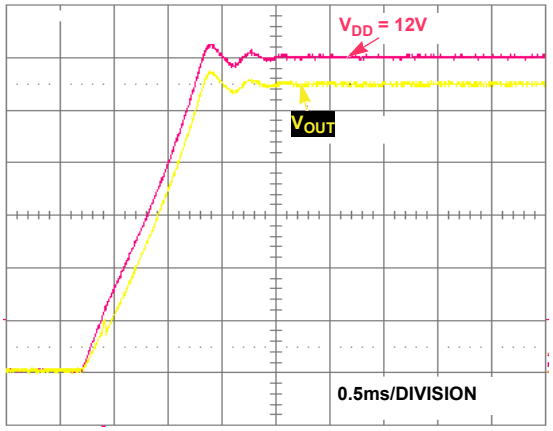


FIGURE 4. V_{OUT} POWER-UP DELAY

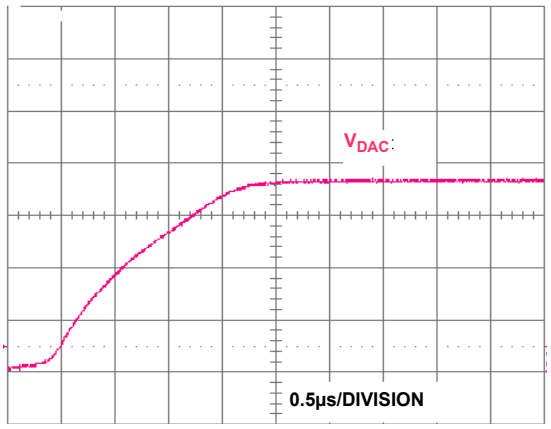


FIGURE 5. GP DAC SETTLING TIME (FULL SCALE, GAIN = 2)

Typical Performance Curves (Continued)

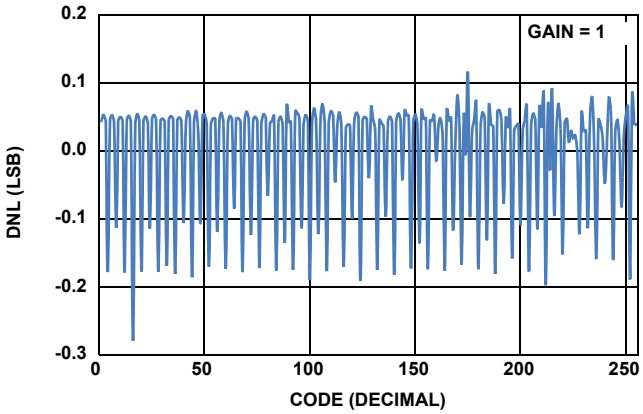


FIGURE 6. GP DAC DNL vs CODE V_{DD} = 3V

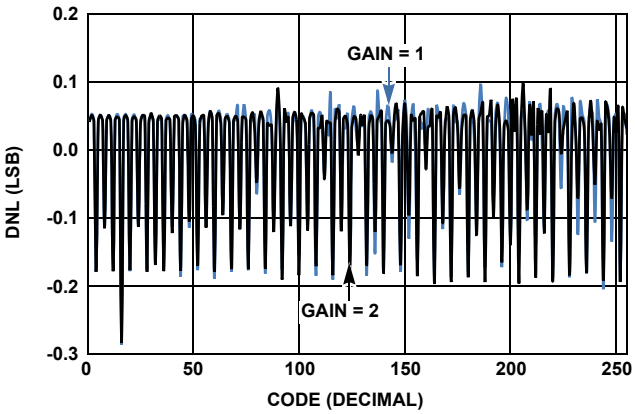


FIGURE 7. GP DAC DNL vs CODE V_{DD} = 5V

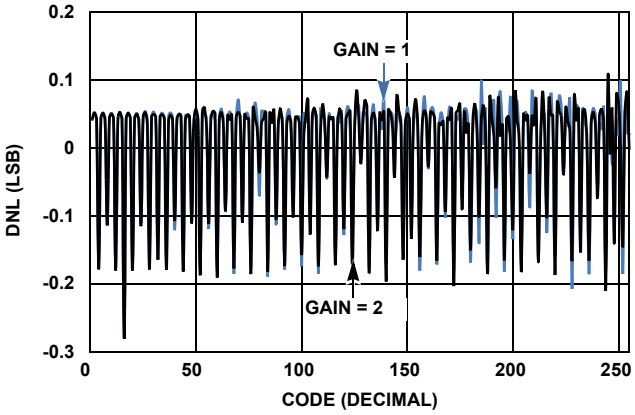


FIGURE 8. GP DAC DNL vs CODE V_{DD} = 15V

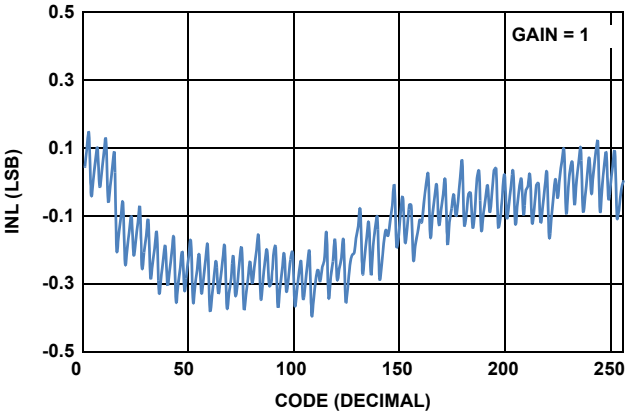


FIGURE 9. GP DAC INL vs CODE V_{DD} = 3V

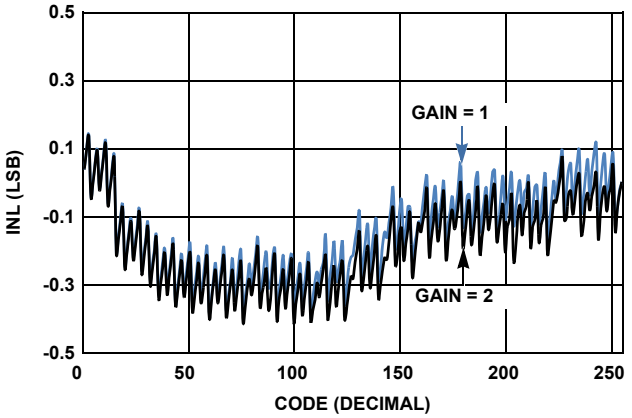


FIGURE 10. GP DAC INL vs CODE V_{DD} = 5V

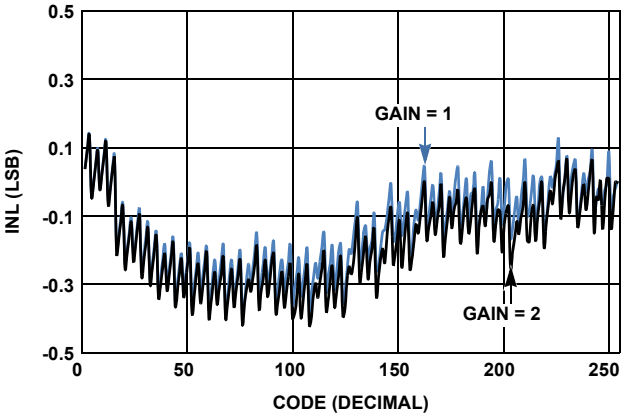


FIGURE 11. GP DAC INL vs CODE V_{DD} = 15V

Typical Performance Curves (Continued)

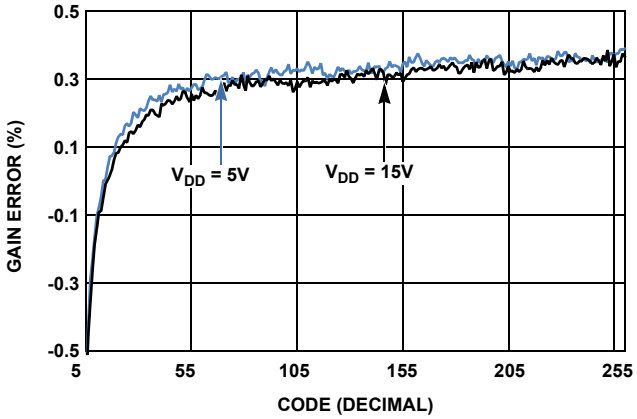


FIGURE 12. GP DAC GAIN ERROR

Principles of Operation

The ISL25700 allows for precisely controlling the temperature of an external object and/or power dissipation of the external P-MOSFET. The temperature control is done by continuously sensing resistance of the NTC thermistor, and adjusting the current flow through the P-MOSFET (temperature controlling element).

ISL25700 drives the P-MOSFET proportionally inverted to the difference between the object temperature and target temperature set point (T_{SET}), set by the user through the I^2C serial interface. Temperature is sensed by the external NTC thermistor and converted to a driving voltage by the Wheatstone bridge and its amplifier. One leg of the current-mode Wheatstone bridge contains an external NTC thermistor with the programmable 8-bit FTC DAC and another leg contains the selectable current source k1 that feeds an internal resistor R_{INT}.

The 8-bit FTC DAC allows fine-tuning the T_{SET} with resolution better than +0.1°C within a +15°C coarse temperature range window. The T_{SET} temperature is set through the Temperature Coarse Range Control Register, Reg.01h[2:0], and the Fine Temperature Control Register, Reg.02h[7:0]; refer to "ISL25700 MEMORY MAP" on page 11. A +15°C temperature coarse range window can be centered on T_{SET} point based on the thermistor's parameters, such as resistance, R/T curve type, tolerance and NTC slope and by adjusting a current ratio flowing through the legs of the Wheatstone bridge. Note that the T_{SET} target temperature should be higher than the anticipated maximum ambient temperature for the application.

There are total of 32 system gain settings available in the Gain Control Register, Reg.03h[4:0], with 0.35dB resolution per step. The gain control allows to prevent the thermal system from oscillation by adjusting the total system gain remotely, without use of external components.

The internal current sensing circuitry provides the ability to control and adjust the power dissipated in the P-MOSFET through the Current Sense Register, Reg.01h[7:3]. This function allows for adjusting the initial turn on heating curve and protects from over-heating of the P-MOSFET. An external current sensing resistor R_{SENSE}, serial with the P-MOSFET, is required. A current limit can be selected for the chosen R_{SENSE}. It should have an effective voltage drop from 200mV to 1750mV and be inside the safe operating area of the MOSFET.

A General Purpose 8-bit DAC, GP DAC provides a programmable voltage output V_{DAC} through the General Purpose DAC Register, Reg.04h[7:0]. The output swing of General Purpose DAC can be set through the Gain Control bit in Reg.03h[6] or totally disabled by resetting the DAC Enable Bit in Reg.03h[7].

Memory Map

The are two types of memory banks in the chip; volatile (RAM) and non-volatile (EEPROM). Volatile registers from address 00h to 07h are identical to non-volatile registers in terms of the register's name and bit definitions. All the data is recalled from non-volatile registers and maintained in the volatile registers at power-up. It is possible to do independent write/read to the volatile and non-volatile banks after power-up by setting $\overline{NV}$ bit in the Control/Status Register, Reg.08h[7]. Note that the data written to the non-volatile registers will be automatically written to corresponding volatile registers, however no direct reading from non-volatile registers is possible. All the readings are from corresponding volatile registers.

The Memory Map of the chip is in Table 1.

TABLE 1. ISL25700 MEMORY MAP

REGISTER NAME	REGISTER ADDRESS	BIT MAP								DEFAULT SETTINGS
		7	6	5	4	3	2	1	0	
Device ID (Read Only)	00h	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	00h
Current Sense/ Coarse Temperature Control	01h	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	CTC[2]	CTC[1]	CTC[0]	03h
Fine Temperature Control	02h	FTC[7]	FTC[6]	FTC[5]	FTC[4]	FTC[3]	FTC[2]	FTC[1]	FTC[0]	80h
Gain Control (DAC Enable/ DAC Gain/System Loop Gain)	03h	DAC Enable	DAC Gain	NA	SLG[4]	SLG[3]	SLG[2]	SLG[1]	SLG[0]	90h
General Purpose DAC	04h	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]	80h
General Purpose Register 1	05h	GP1[7]	GP1[6]	GP1[5]	GP1[4]	GP1[3]	GP1[2]	GP1[1]	GP1[0]	00h
General Purpose Register 2	06h	GP2[7]	GP2[6]	GP2[5]	GP2[4]	GP2[3]	GP2[2]	GP2[1]	GP2[0]	00h
R_{INT} Absolute Error (Read Only)	07h	sign bit	ERR[6]	ERR[5]	ERR[4]	ERR[3]	ERR[2]	ERR[1]	ERR[0]	XX
Control/Status Register (Volatile Only)	08h	$\overline{NV}$	NA	NA	NA	NA	NA	NA	BUSY	00h

Device ID Register (Reg.00h)

This is a read only register. It contains device ID code 00h.

Coarse Temperature Control (Reg.01h [2:0])

These 3 bits allow one to choose one of the seven coarse windows for the temperature set point. The default set point is about +59°C for the 100k R_{TH} thermistor with a temperature coefficient of -4.25%/°C at +25°C, i.e. Reg.01h[2:0] = 011b. The temperature set point can be changed to any other set point within an operational range from +40°C to +110°C, or use another type of thermistor, including different resistance value or R/T curve type (NTC slope), and then center the +15°C coarse range temperature window on that new setting based on the ratio of R_{INT}/R_{TH} according to Equation 1:

$$\frac{R_{INT}(T)}{R_{TH}(setpoint)} = \frac{K2 + K3 \times \frac{Code}{255}}{K1} \quad \text{(EQ. 1)}$$

where:

R_{INT} - is an internal 9kΩ resistor, forming another leg of the Wheatstone Bridge;

k1, k2 and k3 - are coefficients representing the ratio of the current flowing through the legs of the Wheatstone Bridge;

Code - is the decimal code in the Fine Temperature Control register 02h.

The value of internal resistor R_{INT} can vary from part to part and depends on the package temperature. The actual R_{INT} at temperature T can be calculated using Equation 2:

$$R_{INT}(T) = R_{INT}(25)x[1 + \alpha(T-25) + \beta(T-25)^2] \quad \text{(EQ. 2)}$$

where:
$R_{INT}(25)$ = 9000 + R_{INT} abs. error x 15 - is internal resistor value at +25°C in Ohms;
R_{INT} abs. error - is a signed integer value of absolute error stored in Reg.07h[7:0] converted to a decimal number; bit [7] represents a sign bit, 0 for "+" and 1 for "-";
$\alpha = -1337 \times 10^{-6}$ - 1st order temperature coefficient, ppm/°C;
$\beta = 5 \times 10^{-6}$ - 2nd order temperature coefficient, ppm/°C^2;
T - temperature in Celsius.

The k1, k2 and k3 coefficients and the thermistor value range for each Coarse Temperature setting in Reg.01h[2:0] should be taken according to Table 2.

TABLE 2. COARSE TEMPERATURE RANGE

Register 01h[2:0]	k1	k2	k3	THERMISTOR RESISTANCE RANGE AT SET POINT (kΩ)
000	Do not use			
001	3	3	2	5.4 to 9.0
010	4	3	2	7.2 to 12.0
100	5	3	2	9.0 to 15.0
011	7	3	2	12.6 to 21.0
101	8	3	2	14.4 to 24.0
110	9	3	2	16.2 to 27.0
111	12	3	2	21.6 to 36.0

Current Sense Threshold (Reg.01h [7:3])

This register sets the current limit trip point. When the voltage applied to the I_{SENSE} pin falls below the programmed voltage threshold, V_{OUT} goes high, thus forming a negative feedback loop proportional to I_{SENSE} x R_{SENSE}.

The value for this register should be taken according to Table 3.

TABLE 3. CURRENT SENSE THRESHOLD

Register 01h[7:3] Value	SENSE RESISTOR VOLTAGE DROP THRESHOLD V_{DD} - (I_{SENSE} X R_{SENSE})	TYPICAL ERROR (%)	
		V_{DD} = 3V	V_{DD} = 15V
00000	V_{DD} - 200mV	±5	+20
00001	V_{DD} - 250mV	±5	+20
00010	V_{DD} - 300mV	±5	+20
00011	V_{DD} - 350mV	±5	+20
00100	V_{DD} - 400mV	±5	+20
00101	V_{DD} - 450mV	±5	+20
00110	V_{DD} - 500mV	±5	+20
00111	V_{DD} - 550mV	±5	+20
01000	V_{DD} - 600mV	±5	+20
01001	V_{DD} - 650mV	±5	+20
01010	V_{DD} - 700mV	±5	+20
01011	V_{DD} - 750mV	±5	+20
01100	V_{DD} - 800mV	±5	+20
01101	V_{DD} - 850mV	±5	+20
01110	V_{DD} - 900mV	±5	+20
01111	V_{DD} - 950mV	±5	+20
10000	V_{DD} - 1000mV	±5	+20
10001	V_{DD} - 1050mV	±5	+20
10010	V_{DD} - 1100mV	±5	+20
10011	V_{DD} - 1150mV	±5	+20
10100	V_{DD} - 1200mV	±5	+20
10101	V_{DD} - 1250mV	±5	+20
10110	V_{DD} - 1300mV	±5	+20
10111	V_{DD} - 1350mV	±5	+20
11000	V_{DD} - 1400mV	±5	+20
11001	V_{DD} - 1450mV	±5	+20
11010	V_{DD} - 1500mV	±5	+20
11011	V_{DD} - 1550mV	±5	+20
11100	V_{DD} - 1600mV	±5	+20
11101	V_{DD} - 1650mV	±5	+20
11110	V_{DD} - 1700mV	±5	+20
11111	V_{DD} - 1750mV	±5	+20

Fine Temperature Control Register (Reg.02h [7:0])

This register allows fine tuning to the final temperature T_{SET} within the predetermined range set in Reg.01h[2:0] by choosing appropriate code for the 8-bit FTC DAC. The final temperature can be adjusted with approximately +0.07°C increment/decrement resolution per step.

System Loop Gain (Reg.03h [4:0])

This 5 bits allow one to adjust a total system loop gain in ±0.35dB per step, according to Table 4.

The default system loop gain depends on the MOSFET type, thermal conductivity and level of insulation from the ambient temperature.

TABLE 4. SYSTEM LOOP GAIN ADJUSTMENT

Reg.03h[4:0]	LOOP GAIN ADJUSTMENT (dB)
00000	-5.60
00001	-5.25
00010	-4.90
00011	-4.55
00100	-4.20
00101	-3.85
00110	-3.50
00111	-3.15
01000	-2.80
01001	-2.45
01010	-2.10
01011	-1.75
01100	-1.40
01101	-1.05
01110	-0.70
01111	-0.35
10000	Initial Gain (default)
10001	0.35
10010	0.70
10011	1.05
10100	1.40
10101	1.75
10110	2.10
10111	2.45
11000	2.80
11001	3.15
11010	3.50
11011	3.85
11100	4.20
11101	4.55
11110	4.90
11111	5.25

DAC Enable and Gain Control (Reg.03h [7:6])

When the DAC Enable bit, Reg.03h[7], is 0, the DAC output is disabled, regardless of Reg.04h settings. When DAC Enable bit is 1, the DAC output depends on the settings of the DAC Gain bit Reg.03[6] and Reg.04h[7:0].

When the DAC Gain bit, Reg.03h[6], is 0, the DAC output range is from 0V to 2V, i.e. Gain = 1. When the DAC Gain bit is 1, the DAC output range is from 0V to 4V, i.e. Gain = 2.

General Purpose DAC Register (Reg.04h [7:0])

This 8-bit register writes directly to the GP DAC to set the output voltage. The default setting of this register is 80h. The DAC output depends on the Gain setting in Reg.03h[6].

General Purpose Registers (Reg.05h and Reg.06h)

These 8-bit General Purpose non-volatile and volatile registers can be used for application specific purposes. For example, they can be used to store calibration data or other valuable system information.

R_{INT} Absolute Error Register (Reg.07h [7:0])

This register contains the difference between the nominal value and the real value of the internal resistor R_{INT}. The nominal value of this resistor is 9k and the voltage drop on this resistor represents the temperature setpoint. The LSB weight of the R_{INT} absolute error is 15Ω. Refer to Equation 2 for calculation of R_{INT}.

Control/Status Register (Reg.08h [7:0])

The setting of the $\overline{NV}$ bit, Reg.08h[7], determines if data is to be read or written to the non-volatile and/or volatile memory. When this bit is 0, all operation will be targeted to non-volatile memory, and the data will be copied to volatile memory simultaneously. When this bit is 1, all operation will be targeted to the volatile memory only. The default setting of the $\overline{NV}$ bit is 0.

The Busy bit, Reg.08h[0], is a read only bit. When “1” is read from this bit, it indicates that the non-volatile cycle is in progress. Reading from this bit eliminates getting a NACK if the host attempts to write to the non-volatile memory before the previous data is stored.

I^2C Serial Interface

The ISL25700 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL25700 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 13). On power-up of the ISL25700, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL25700 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 13). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 13). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes, only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 14).

The ISL25700 responds with an ACK after recognition of a START condition, followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL25700 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101000 in seven MSBs. The LSB is the Read/$\overline{Write}$ bit. Its value is “1” for a Read operation and “0” for a Write operation (see Table 5).

TABLE 5. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	R/$\overline{W}$
(MSB)							(LSB)

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL25700 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL25700 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL25700 enters its standby state (see Figure 14).

The byte at address 08h determines if the Data Byte is to be written to volatile and/or non-volatile memory (see “Memory Map” on page 10). A 20ms delay is required between two consecutive writes to the non-volatile registers.

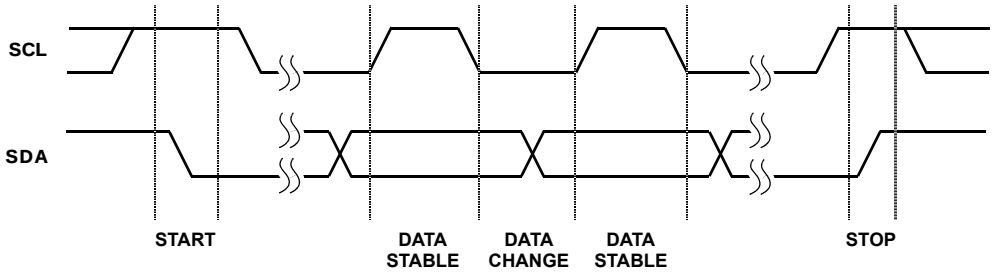


FIGURE 13. VALID DATA CHANGES, START, AND STOP CONDITIONS

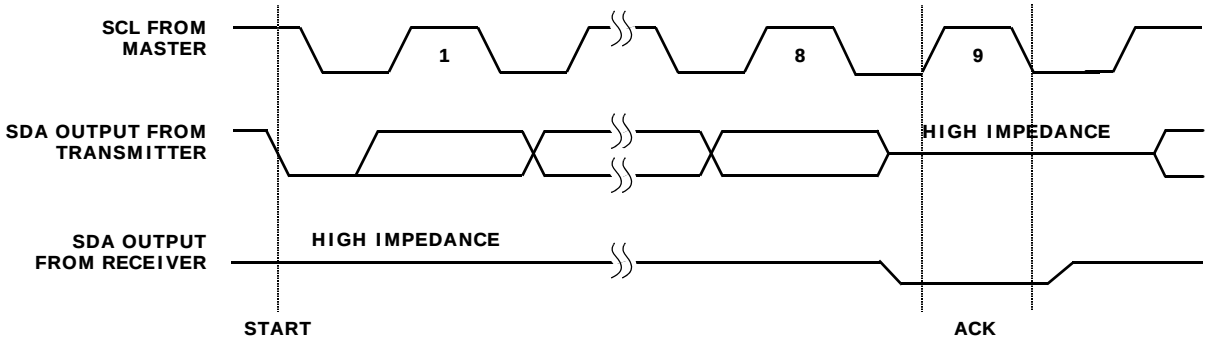


FIGURE 14. ACKNOWLEDGE RESPONSE FROM RECEIVER

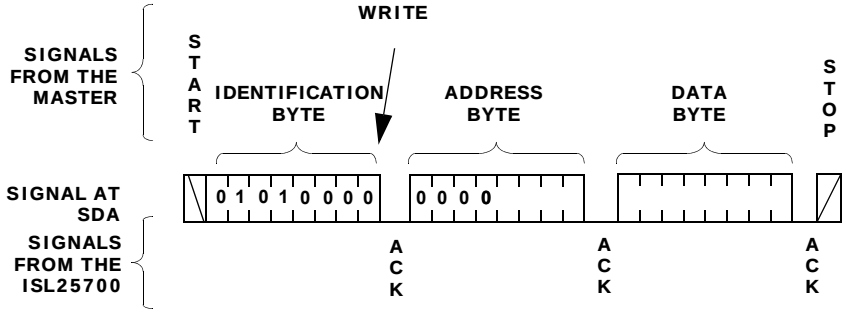


FIGURE 15. BYTE WRITE SEQUENCE

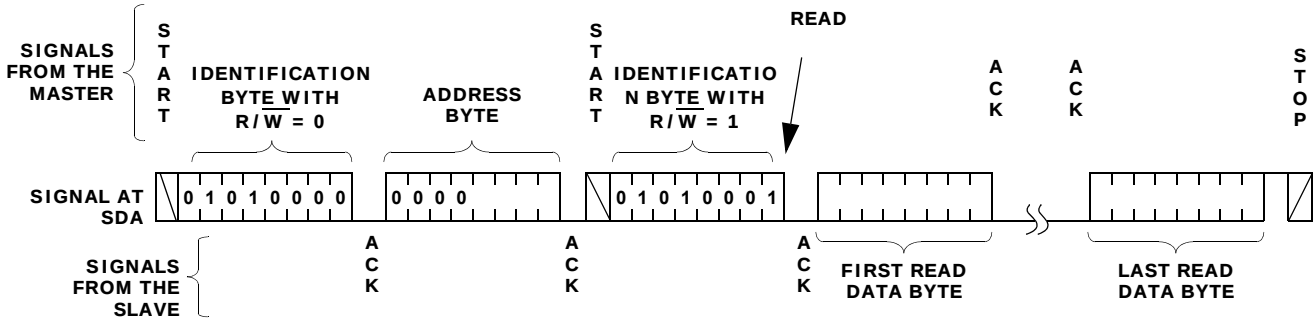


FIGURE 16. READ SEQUENCE

Polling Method

It is possible to check if the non-volatile memory write cycle is finished or is in progress by polling (reading) the BUSY bit in Control/Status Register, Reg.08h[0] (see “Control/Status Register (Reg.08h [7:0])” on page 13). The non-volatile write cycle is in progress when the BUSY bit is 1. No other write attempt is allowed when the BUSY bit is 1. The non-volatile write cycle is finished when the BUSY bit is 0.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 16). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL25700 responds with an ACK. Then the ISL25700 then transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (see Figure 16).

The byte at address 08h determines if the Data Bytes being read are from volatile or non-volatile memory (see “Memory Map” on page 10).

Application Information

In order to get the correct temperature setting, it is very important to chose an appropriate thermistor and calibrate the complete system. The following sequence describes the thermistor selection and calibration procedure.

1. Select a thermistor type and get the RT curve from manufacturer.
2. Find out a thermistor resistance at the desired temperature and select the coarse temperature range from Table 2. The thermistor value at set point should be in the middle of the coarse range. Note, the coarse ranges overlap.
3. Set the Current Sense limit in Reg.01h[7:3] and System Loop Gain in Reg. 03h[4:0] as high as possible to enable fast settling yet prevent thermal oscillation.
4. Perform system calibration and fine tuning using an external temperature sensor.

Thermistor Selection

Chose the thermistor whose resistance at the desired temperature set point T_{SET} will be within the range specified in Table 2. The R/T characteristics of the thermistor are usually provided by the manufacturer as a table or as a curve.

For example, you are going to stabilize the temperature at T_{SET} = +91.5°C. You decided to use a 100k NTC thermistor from Vishay, NTCS0805E3104FXT. The resistance at +91.5°C will be 8109.12Ω, according to the manufacturer data provided online at http://www.vishay.com/doc?29100. This resistance fits in the coarse temperature range settings of 001b or 002b, as per Table 2.

Current Sense Resistor and MOSFET Selection

The current sense resistor should be selected with consideration of system maximum power consumption, maximum current, and minimum resolution. It is recommended to select a current sense resistor in the range from 0.1Ω to 10Ω. The 0.1Ω resistor allows sensing and will limit the maximum current from 2A to 17.5A, while a 10Ω resistor allows selecting a current limit from 20mA to 175mA. The type and size of current sense resistor should have an appropriate power rating.

The ISL25700 will work only with the P-type of power MOSFETs or Darlington pair. Since the driving capability is limited, it is not recommended to drive a bipolar transistor. The power MOSFET can be used as a heater inside a micro temperature chamber.

System Loop Gain Setting

Assemble the application circuit including ISL25700, the power MOSFET, heating element and thermistor. The System Loop Gain allows controlling thermal stability of the feedback system. In other words, current through the power MOSFET should settle fast and without oscillation when setpoint changes from one temperature to another. Settling time of the current can be monitored by oscilloscope with the current probe.

Another way to determine system stability is to obtain a phase margin of the system by analyzing Bode plots. Bode plots of the gain and phase margins can be obtained by disconnecting the thermistor from R_{TH} - breaking the loop, and connecting a low frequency signal analyzer between the R_{TH} pin and the thermistor. That will allow analysis of the system transfer function vs. frequency. Note the thermistor has to be biased with 30µA DC current from an external supply. The signal analyzer sweeps the frequency at input node (R_{TH}) and measures the phase change of the output node (thermistor). As a rule of thumb, phase margin should be at least 45° when the system gain reaches 0dB.

It is not recommended to change the system loop gain when it is determined.

Calibration Procedure

Power-up the circuit and program Reg.01h[2:0] = 001b of ISL25700. Use an externally calibrated temperature sensor to measure the temperature of the thermistor. When the thermistor temperature is stabilized, it can be adjusted to the desired point by changing the Fine Temperature Control settings in Reg.02h[7:0] until the external thermometer indicates +91.5°C (for this example).

The decimal FTC code can be calculated by solving for Equations 1 and 2 as follows:

$$Code = \frac{K1 \times R_{INT}(T) - K2 \times R_{TH}(T)}{K3 \times R_{TH}(T)} \times 255 \quad \text{(EQ. 3)}$$

Note, the final application system temperature depends on the allowed power consumption and the level of insulation from the ambient temperature.

Two different calibration point settings can be stored in General Purpose non-volatile registers. More calibrated temperature points can be stored and used as a look-up table in an external memory.

Placement and Layout Consideration

It is recommended to place the ISL25700 and thermistor as close as possible to each other, inside the insulated area to achieve higher accuracy and keep the ground trace between the thermistor and the device as short as possible. The device ground pin and the system ground should be connected at a single point, known as the “single point ground”, preventing picking up the common ground noise into the R_{TH} feedback pin.

The ISL25700 also can be placed outside of the insulated area and far away from the thermistor, but the setpoint accuracy will decrease, due to the wide ambient temperature range. It is recommended to use a look-up table based on Equation 2 to compensate for the setpoint shift.

Put a 1µF capacitor in parallel with 0.1µF decoupling capacitor close to the VDD pin.

It is recommended to have a pull-up resistor of 500k or higher, or a high-pass RC filter, as shown in the “Block Diagram/Application Circuit” on page 2, to the gate of a P-MOSFET in order to prevent a high current spike through the MOSFET at power-up. The time constant of the high-pass filter should be in the range of 1µs to 20µs.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 23, 2014	FN6885.1	Added Related Literature on page 1. Operating Specification table on “Voltage at pin from GND to VCC” on page 6: Changed the value for Min from -2 to -3 and Max from 2 to 3.
September 3, 2010	FN6885.0	Initial release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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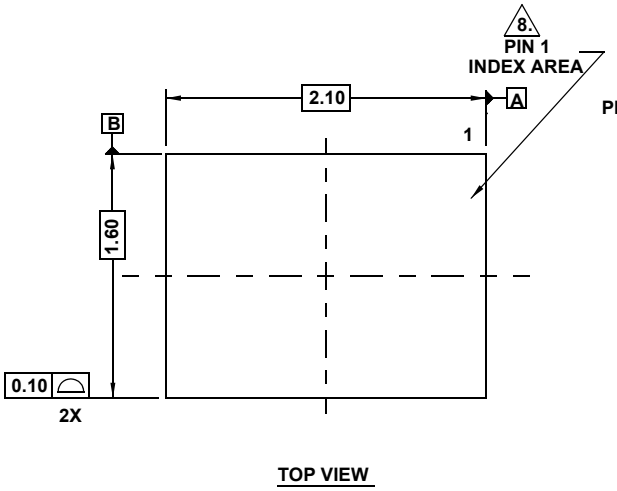
Package Outline Drawing

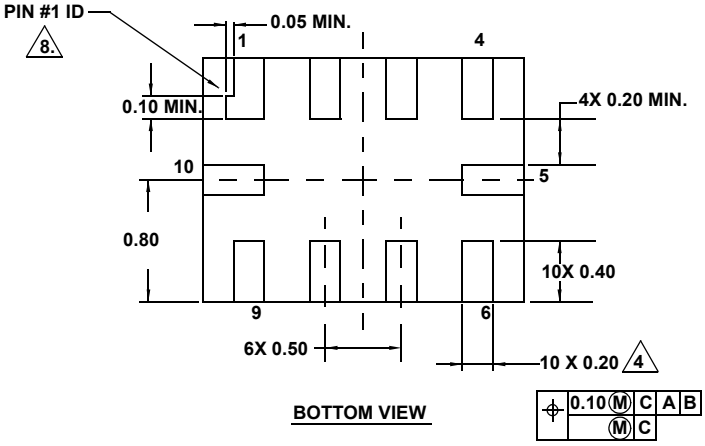
L10.2.1x1.6A

10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

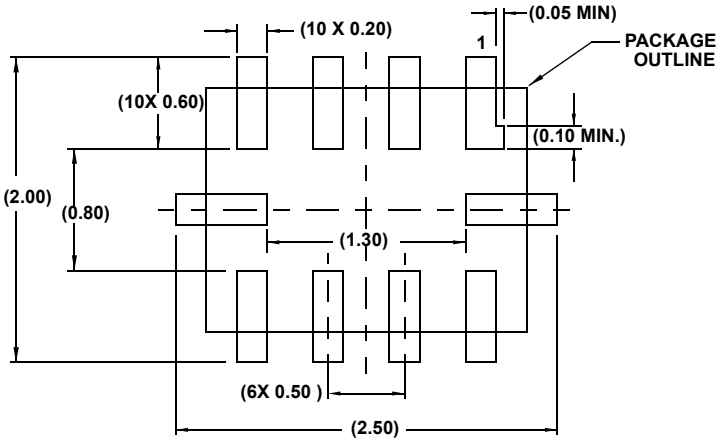
Rev 5, 3/10



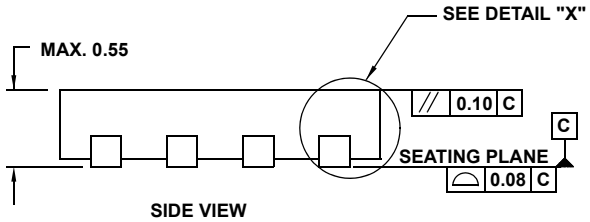
TOP VIEW



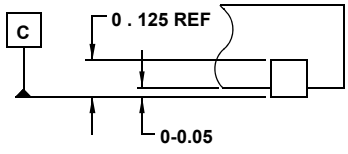
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters. Angles are in degrees. Dimensions in ( ) for Reference Only.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Maximum package warpage is 0.05mm.
6. Maximum allowable burrs is 0.076mm in all directions.
7. Same as JEDEC MO-255UABD except:
   No lead-pull-back, MIN. Package thickness = 0.45 not 0.50mm
   Lead Length dim. = 0.45mm max. not 0.42mm.
8. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.