60mW, Capfree, Stereo Headphone Amplifier

The ISL99202 is a stereo, capfree headphone amplifier. The wide operating voltage of 2.4V to 5.5V makes it versatile enough to be used in mobile battery powered applications powered by 2 AA or Single cell Li-Ion batteries as well as 3.3/5V power supply available notebook computers.

The ISL99202 has robust RF immunity, which makes it ideally suited for today's mobile applications.

It has audiophile quality SNR and THD specifications and Click/Pop suppression.

The ISL99202 comes with Comprehensive Protection features, which include undervoltage and short-circuit protection and thermal shutdown.

The ISL99202 lowest power consumption in the industry is achieved by low I_{qq} and current shutdown.

The product is available in 12 Ld TQFN.

Features

- Supports 16W to 600W speaker impedance
- Ground referenced: No output coupling capacitors
- Audiophile quality sound THD of 0.01%, SNR of 102dB
- PSRR < -90dB, no need for LDO
- Wide operating voltage of 2.4V to 5.5V
- < 3mA quiescent current and 0.1µA shutdown current
- State of the art pop and click suppression
- Pb-Free (RoHS Compliant)

Applications

- Mobile phones
- MP3 players

Ordering Information

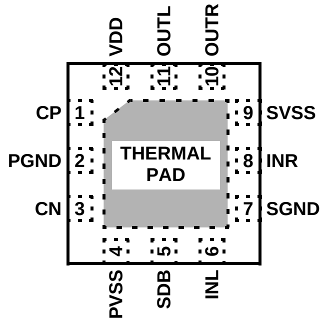
PART NUMBER	PART MARKING	GAIN SETTING (dB)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL99202IRTAZ (Notes 1, 2)	202A	-1.5V/V	-40 to +85	12 Ld 3x3 TQFN	L12.3x3Z
ISL99202IRTAZ-T (Notes 1, 2)	202A	-1.5V/V	-40 to +85	12 Ld 3x3 TQFN	L12.3x3Z
ISL99202IRTAZ-TK (Notes 1, 2)	202A	-1.5V/V	-40 to +85	12 Ld 3x3 TQFN	L12.3x3Z
ISL99202IRTAEVZ	Evaluation Board				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-20.

Pinouts

ISL99202
(12 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	CP	Charge pump positive terminal
2	PGND	Charge pump Ground
3	CN	Charge pump negative terminal
4	PVSS	Charge pump output
5	SDB	Active low shutdown input
6	INL	Left channel input
7	SGND	Analog ground
8	INR	Right channel input
9	SVSS	Amplifier negative supply
10	OUTR	Right channel output
11	OUTL	Left channel output
12	VDD	Positive power supply

NOTE: Exposed Pad is connected to PGND and SGND

Absolute Maximum Ratings (Reference to GND)

Supply Voltage. . . . . -0.3V to 6V
INR, INL, CP, SDB . . . . -0.3V to V_{DD} + 0.3V
ESD Rating
Human Body Model
All pins 2kV
OUTL, OUTR 8kV
Machine Model. 200V

Operating Conditions

Ambient Temperature Range. . . . .-40°C to +85°C
Maximum Supply Voltage (VDD Pin) 5.5V
Operating Supply Voltage (VDD Pin) . . . . 2.4V to 5V

Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TQFN Package	54	8

Maximum Junction Temperature (Plastic Package) -65°C to +150°C
Maximum Storage Temperature Range . . . .-65°C to +150°C
Dissipation Ratings
Derating Factor
12 LD 3x3 TQFN . . . . .14.7mW/°C
Power Rating T_A
12 Ld 3x3 TQFN
+25°C 1.84W
+70°C 1.12W
+85°C 0.96W
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For theta θ_{JC} the "case temp." location is the center of the exposed metal pad on the package underside.

Electrical Specifications
Typical Values are Tested at V_{DD} = 5V, T_A = +25°C and R_L = 32Ω.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
OUTPUT POWER						
Output Power	P_{OUT}	R_L = 32Ω, THD = 1%	30	63		mW
		R_L = 16Ω		70		mW
Total Harmonic Distortion + Ratio	THD+N	R_L = 1kΩ, V_{OUT} = 1.5V_{RMS}, f = 1kHz		0.003		%
		R_L = 32Ω, P_{OUT} = 50mW, f = 1kHz		0.01		%
		R_L = 16Ω, P_{OUT} = 35mW, f = 1kHz		0.02		%
PROTECTION						
Thermal Shutdown	OTP			160		°C
Thermal Shutdown Hysteresis				15		°C
Overcurrent Protection	OCP			200		mA
Undervoltage Shutdown					2.4	V
LOGIC INPUTS (SDB)						
Input Voltage High	V_{INH}		1.4			V
Input Voltage Low	V_{INL}				0.9	V
POWER SUPPLY						
Supply Voltage Range	V_{DD}		2.4		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.0V at 217Hz		96		dB
		V_{DD} = 2.5V to 5.0V at 1kHz		88		dB
		V_{DD} = 2.5V to 5.0V at 20kHz		76		dB
Quiescent Current	I_{qq}	V_{DD} = 5.0V		3	4.6	mA
Shutdown Current	I_{SDB}	SDB = GND, V_{DD} = 5.0V		0.1	1.1	µA

Electrical Specifications

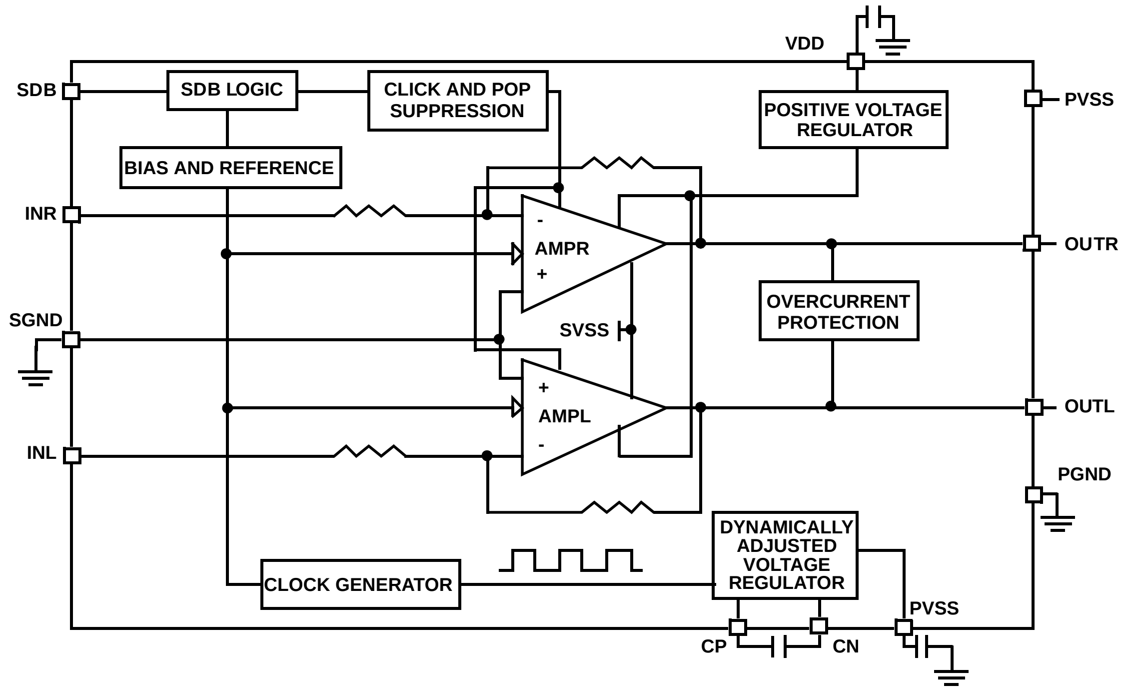
Typical Values are Tested at V_{DD} = 5V, T_A = +25°C and R_L = 32Ω. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNITS
GAIN CONTROL						
Voltage Gain	A_V		-1.55	-1.50	-1.45	V/V
Ch to Ch Gain Tracking				±0.15		%
Total Harmonic Distortion + Ratio	THD+N	R_L = 1kΩ, V_{OUT} = 1.5V_{RMS}, f = 1kHz		0.005		%
		R_L = 32Ω, P_{OUT} = 50mW, f = 1kHz		0.01		%
		R_L = 16Ω, P_{OUT} = 35mW, f = 1kHz		0.04		%
NOISE PERFORMANCE						
Signal to Noise Ratio	SNR	R_L = 1kΩ, V_{OUT} = 1.5V_{RMS}, BW = 22Hz to 20kHz		102		dB
		R_L = 1kΩ, V_{OUT} = 1.5V_{RMS}, BW = 22Hz to 20kHz, A-weighted		105		dB
		R_L = 32Ω, P_{OUT} = 35mW, BW = 22Hz to 20kHz		100		dB
		R_L = 32Ω, P_{OUT} = 35mW, BW = 22Hz to 20kHz, A-weighted		113		dB
Slew Rate	SR			0.5		VµS
Capacitve Drive	C_L			100		pF
Crosstalk	xtalk	R_L = 16Ω, P_{OUT} = 15mW, f = 10kHz		-76		dB
Charge Pump Oscillation Frequency	f_{soc}		400	500	600	kHz
Click and Pop Level	K_{CP}	R_L = 32Ω, Peak voltage, Awtg. 32 sam/sec		-67		dB
V_{DD} = 3.0V						
Power Supply Rejection Ratio	PSRR	217Hz		96		dB
		1kHz		88		dB
		20kHz		76		dB
Quiescent Current	I_{qq}			2.4	3.6	mA
Shutdown Current	I_{SDB}	SDB = GND		0.1	1.1	µA
Output Offset Voltage	VOS		-1	0.05	1	mV
Output Power at 32Ω Load		R_L = 32Ω, THD = 1%		54		mW
Output Power at 16Ω Load		R_L = 16Ω, THD = 1%		56		mW
Total Harmonic Distortion + Noise Ratio	THD+N	R_L = 1kΩ, V_{OUT} = 1.5V_{RMS}, f = 1kHz		0.005		%
		R_L = 32Ω, P_{OUT} = 50mW, f = 1kHz		0.01		%
		R_L = 16Ω, P_{OUT} = 35mW, f = 1kHz		0.02		%

NOTE:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Block Diagram



Typical Performance Curves

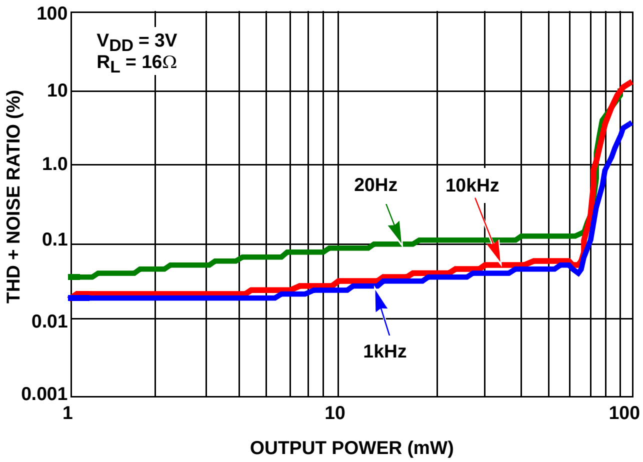


FIGURE 1. TOTAL HARMONIC DISTORTION + NOISE RATIO vs OUTPUT POWER

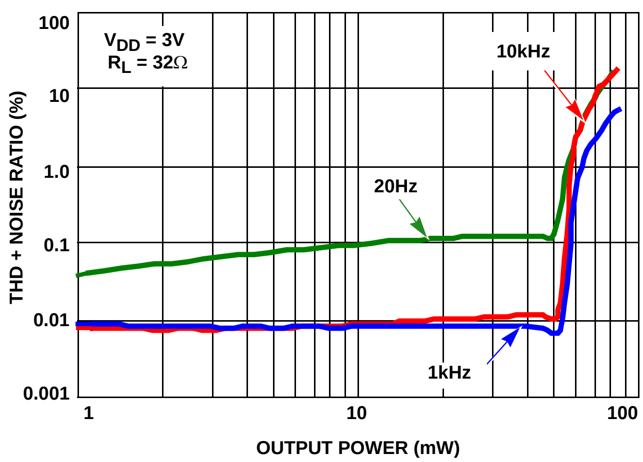


FIGURE 2. TOTAL HARMONIC DISTORTION + NOISE RATIO vs OUTPUT POWER

Typical Performance Curves (Continued)

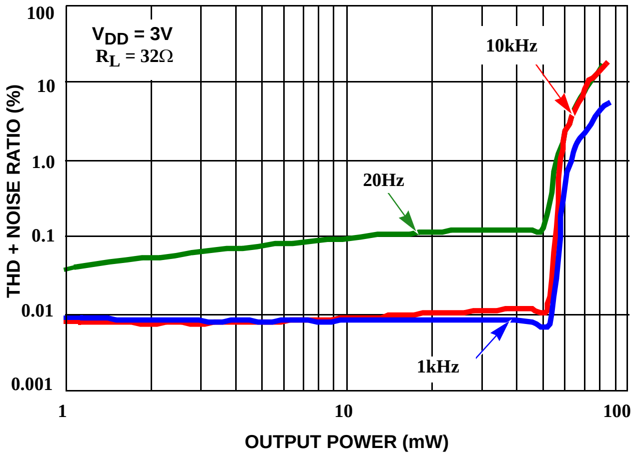


FIGURE 3. TOTAL HARMONIC DISTORTION + NOISE RATIO vs OUTPUT POWER

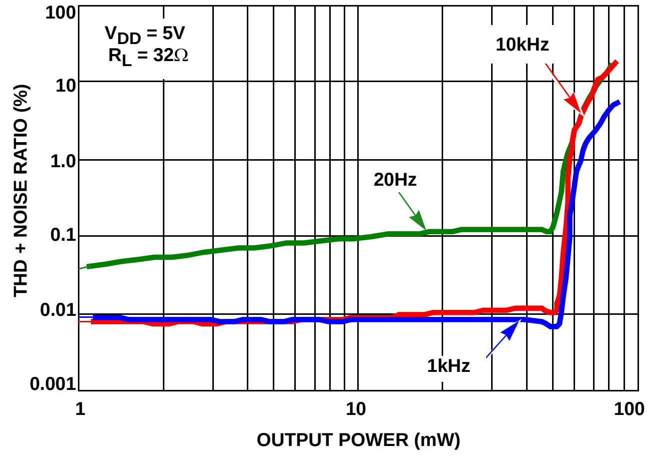


FIGURE 4. TOTAL HARMONIC DISTORTION + NOISE RATIO vs OUTPUT POWER

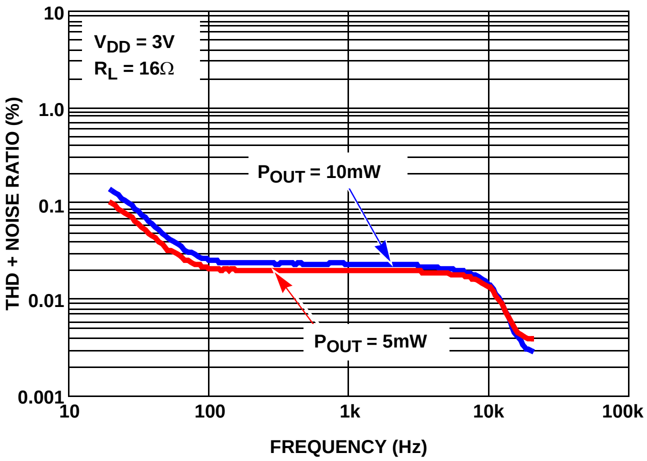


FIGURE 5. TOTAL HARMONIC DISTORTION + NOISE RATIO vs FREQUENCY

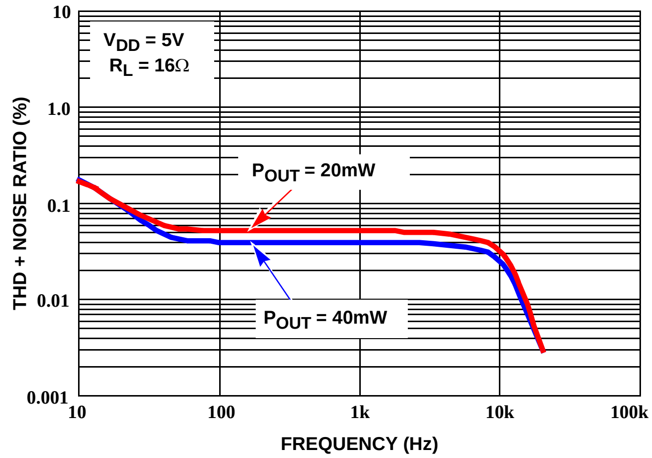


FIGURE 6. TOTAL HARMONIC DISTORTION + NOISE RATIO vs FREQUENCY

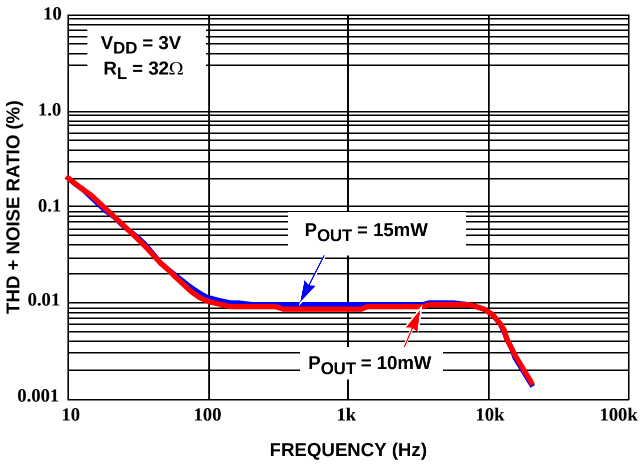


FIGURE 7. TOTAL HARMONIC DISTORTION + NOISE RATIO vs FREQUENCY

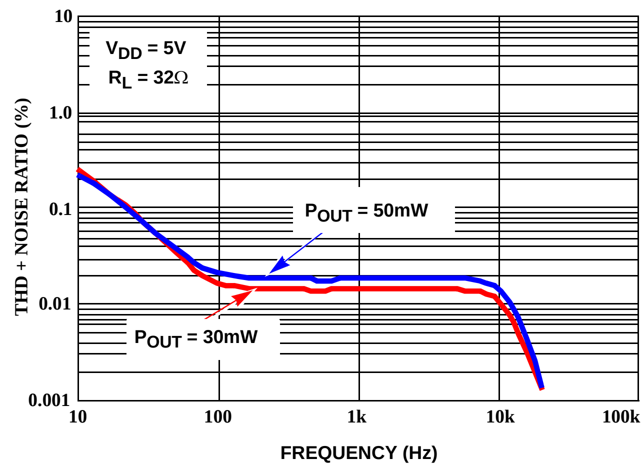


FIGURE 8. TOTAL HARMONIC DISTORTION + NOISE RATIO vs FREQUENCY

Typical Performance Curves (Continued)

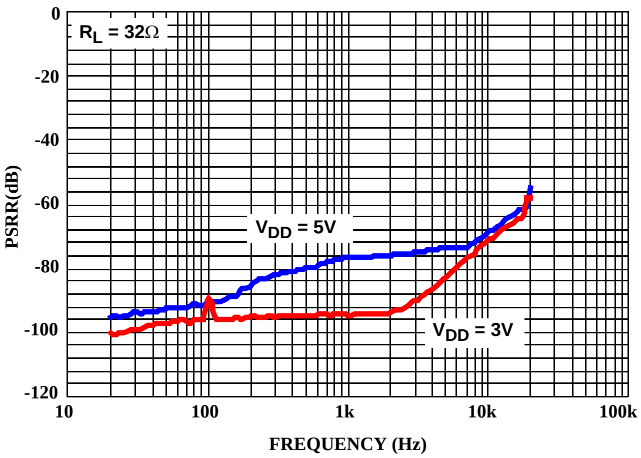


FIGURE 9. POWER SUPPLY REJECTION RATIO vs FREQUENCY

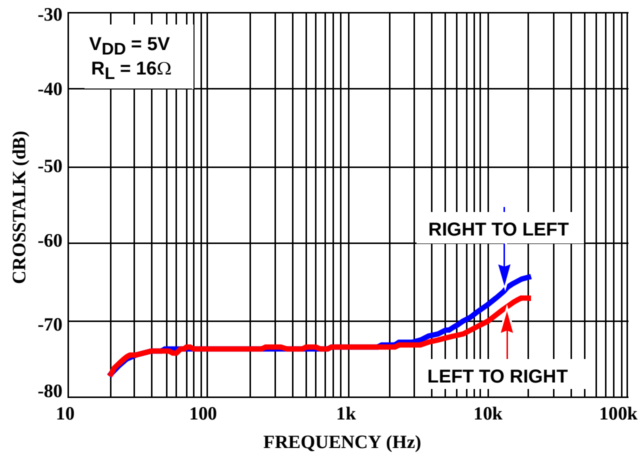


FIGURE 10. CROSSTALK vs FREQUENCY

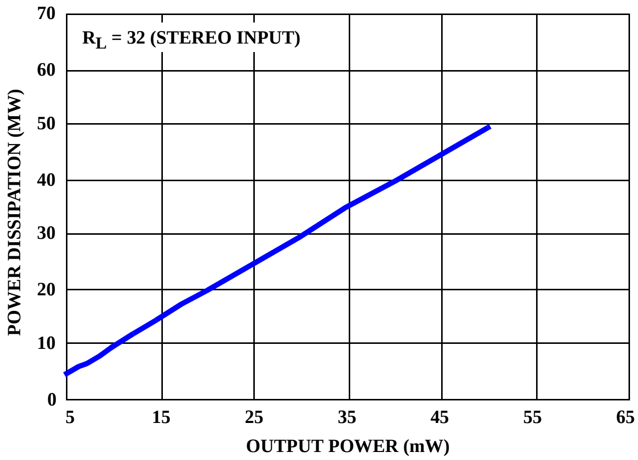


FIGURE 11. POWER DISSIPATION vs OUTPUT POWER

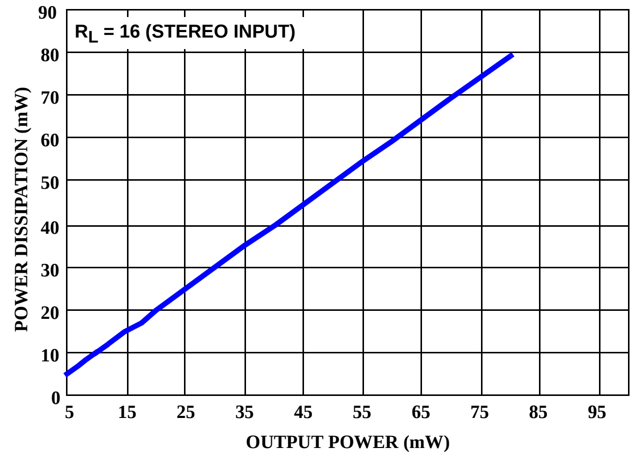


FIGURE 12. POWER DISSIPATION vs OUTPUT POWER

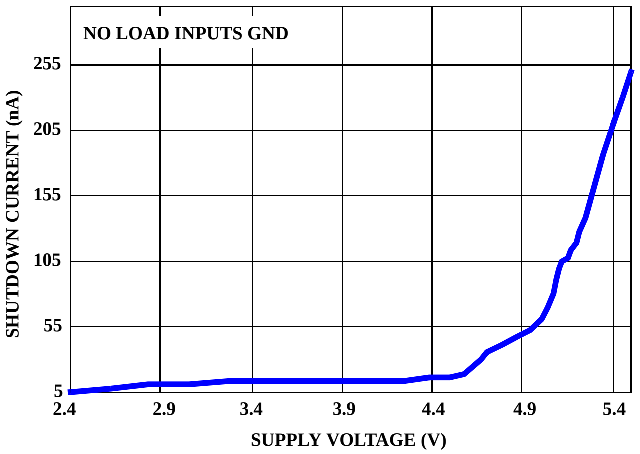


FIGURE 13. SHUTDOWN CURRENT vs SUPPLY VOLTAGE

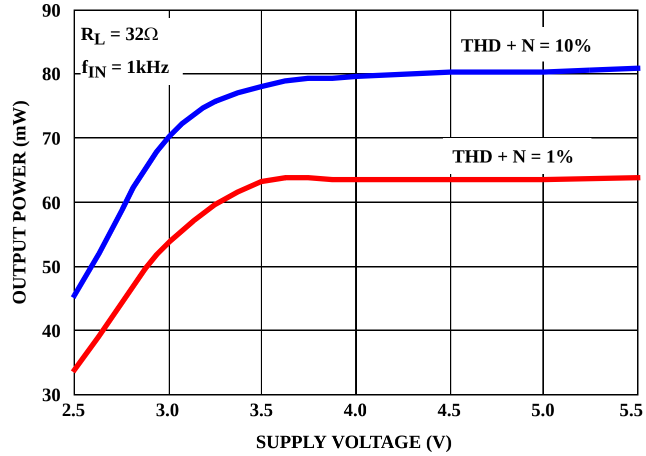


FIGURE 14. OUTPUT POWER vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

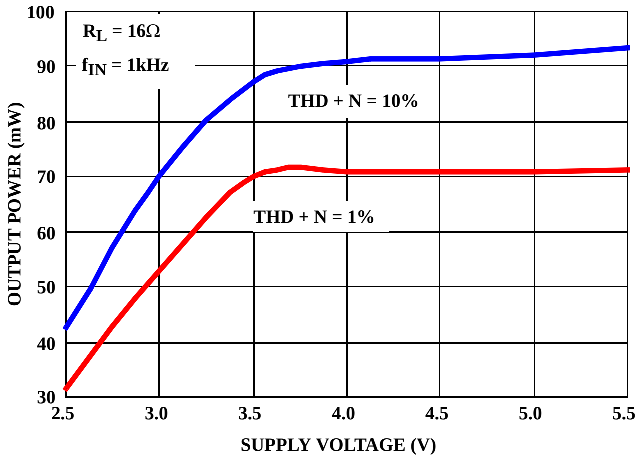


FIGURE 15. OUTPUT POWER vs SUPPLY VOLTAGE

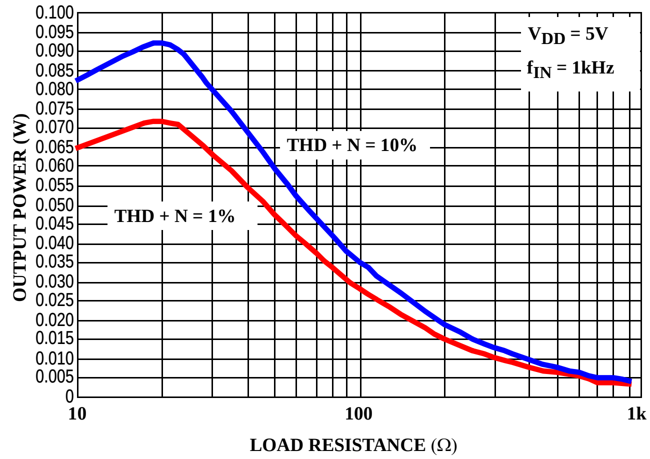


FIGURE 16. OUTPUT POWER vs LOAD RESISTANCE

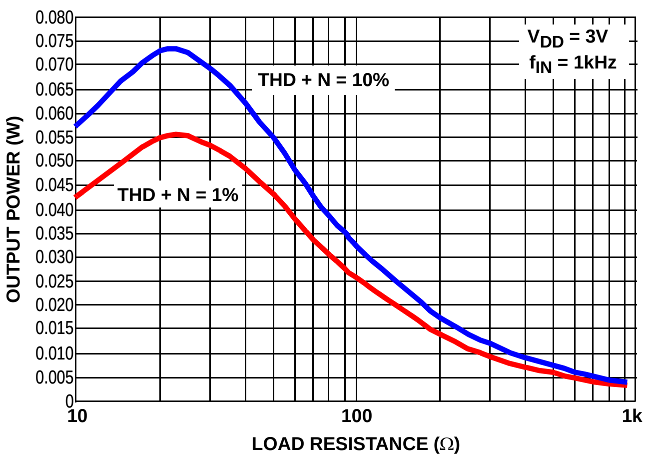


FIGURE 17. OUTPUT POWER vs. LOAD RESISTANCE

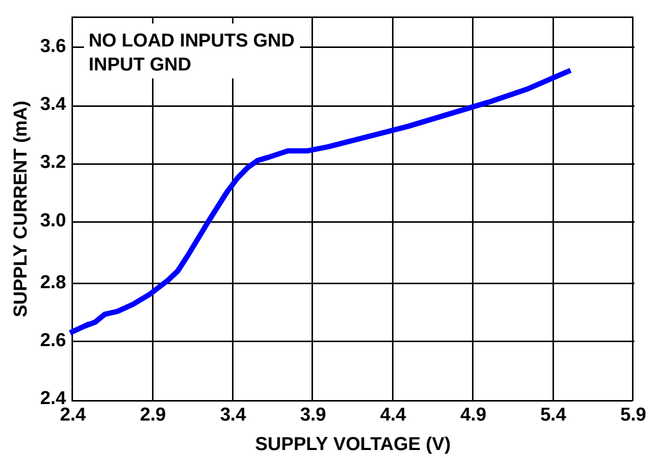


FIGURE 18. SUPPLY CURRENT vs. SUPPLY VOLTAGE

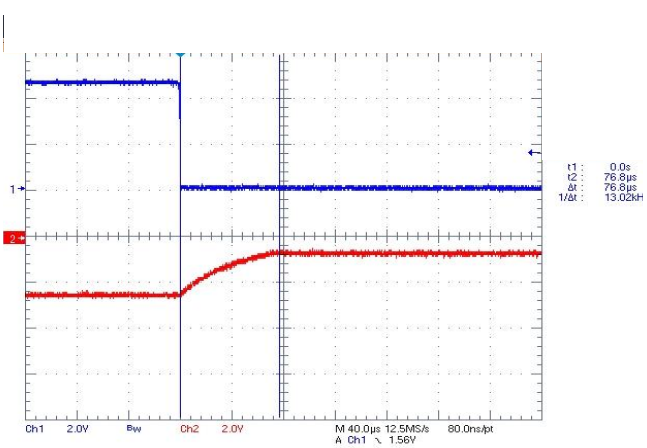


FIGURE 19. CHARGE PUMP RESPONSE FOR SDB GOING HIGH

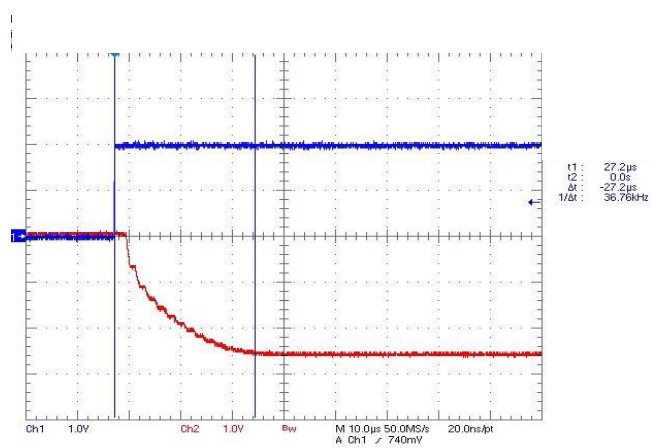
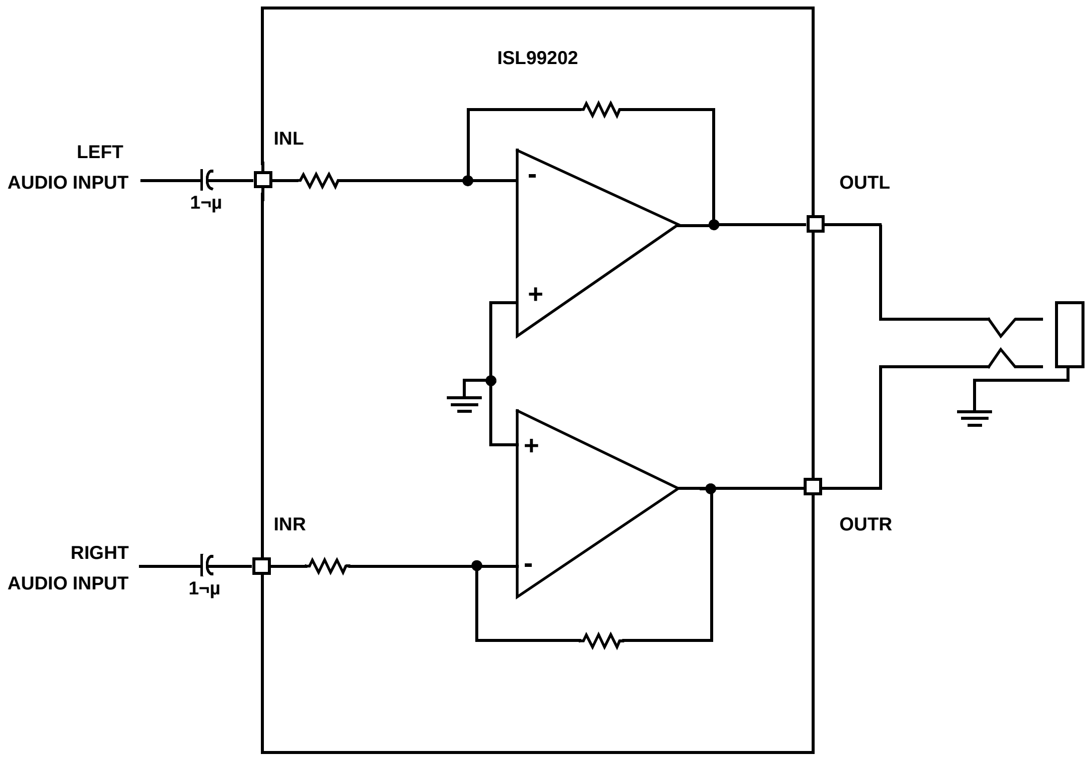


FIGURE 20. CHARGE PUMP RESPONSE FOR SDB GOING LOW

Typical Application Circuit



Detailed Description

The ISL99202 incorporates a novel proprietary architecture to eliminate the large output capacitors associated with single supply headphone amplifiers. Traditional charge pump based architectures that eliminated the output capacitors required additional power to operate the charge pump, which made them ill-suited for portable battery powered applications. The ISL99202 architecture eliminates the need for large output capacitors while consuming industry's lowest quiescent and shutdown currents.

Capfree Architecture

At the core of the Capfree architecture is a dynamically adjusted negative voltage regulator. By continuously monitoring the output power requirements, it adjusts the energy delivery circuitry. The feedback system ensures that overhead power required to deliver audio at the headphone speaker is always optimized for lower power dissipation.

Integrated LDO

A high precision LDO integrated into the power path of the amplifier accounts for a 92dB PSRR. This eliminates the need for a dedicated LDO used in some systems resulting in BOM/cost savings.

Offset Cancellation Circuitry

The DC offset is a very important parameter. It is a principal contributor to Click and Pop. In the cast Capfree architecture, the DC offset can also be a source of DC current in quiescent state. The ISL99202 is tested and trimmed to have very low offset voltages (typically 50µV).

RF Immunity

Most portable applications for ISL99202 are subject to RF radiation from a myriad of sources, like Wi-Fi networks or cellular phone networks. Though these signals are not in the audio band, they can interfere with the audio signals through complex non-linear mechanisms, aliasing or demodulations to create audio band noise. The ISL99202 architecture prevents this coupling into audio band to achieve superior audio performance.

Protection Circuitry

The ISL99202 has comprehensive protection circuitry, which protects the part due to undervoltage, over-temperature and overcurrent. There is hysteresis built into over-temperature and undervoltage, while the overcurrent is designed to limit the output current in case of accidental short circuit or low impedance headphone load connection.

References

Intersil Technical Brief 389: “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”
http://www.intersil.com/data/tb/tb389.pdf

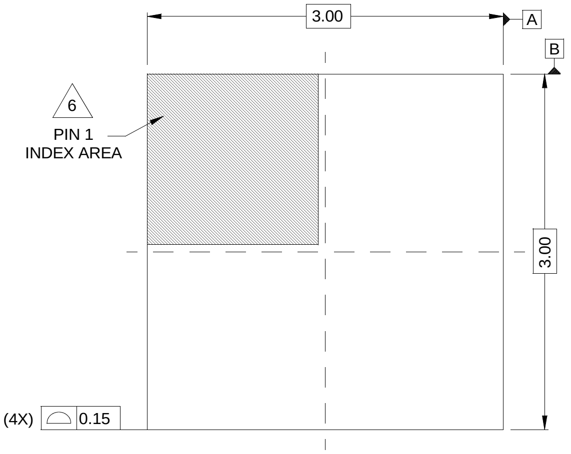
Package Outline Drawing

L12.3x3Z

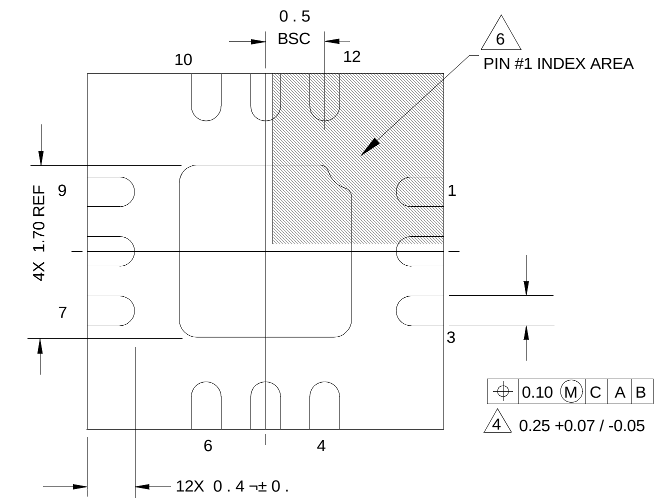
12 LEAD THIN QUAD FLAT NO LEAD PLASTIC PACKAGE

FOR ISL99202 USE ONLY WITH REDUCED e-PAD SIZE TO 1.4mm ON LAND PATTERN

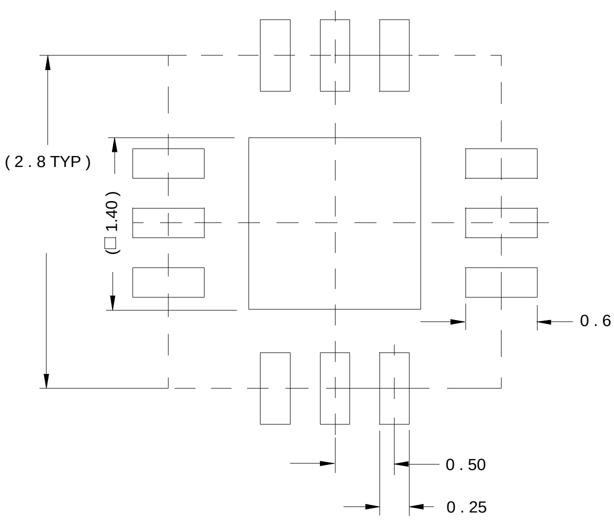
Rev 0, 10/08



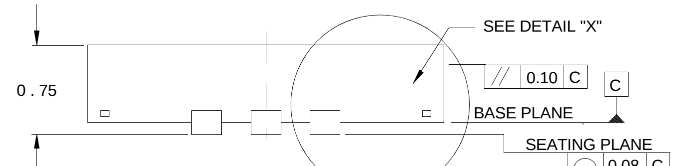
TOP VIEW



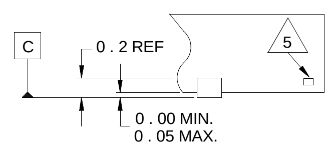
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to JEDEC STD MO-229.
3. Unless otherwise specified, tolerance : Decimal ¬± 0.0
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.32mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.