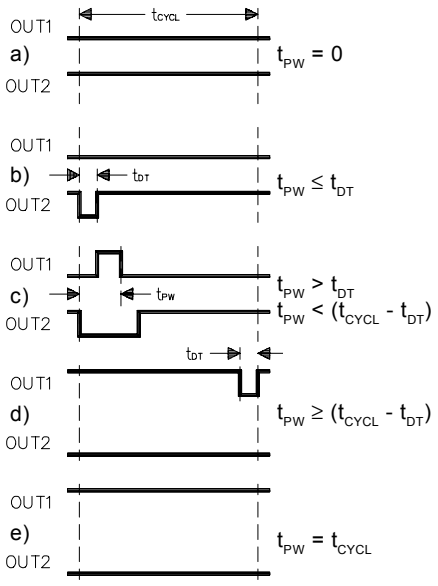

Fig. 6 Effect of Nonzero Dead-time on PWM Waveform

on-time of an output is less than one dead-time period, the output will not turn on. This is shown in Fig. 6b and 6d. Therefore, the commanded duty cycle and the actual duty cycle may differ slightly, especially at extreme duty cycle values.

Additionally, the dead-time can have an effect on the voltage applied to the load by the switching power bridge; the exact effect is a function of the direction of the current in the bridge and the architecture of the bridge. One should try and choose the smallest dead-time that works with the given switch configuration.

Fig. 6.a and 6c illustrate the two duty cycle extremes, 0 % and 100 %. In these two instances there will never be a dead-time period, regardless of the value programmed in the dead-time register, because neither output ever turns off. Fig. 6b and 6d have only one dead-time period inserted in each PWM cycle. In Fig. 6b the desired ontime of OUT1 is less than the one dead-time period, therefore OUT1 can never turn on. The same is true for OUT2 in Fig. 6d. Fig. 6c is the normal situation, where both outputs turn on and off during one PWM cycle and, as a result, two dead-time periods are inserted.

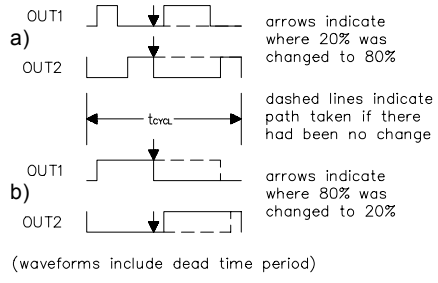

Fig. 7 Effect of Changing the Duty Cycle during a PWM Cycle

Response to a Change in the Pulse Width Number

One can change the Pulse Width number at any time. It is not necessary to synchronize writes to the Pulse Width latch with the CLK or the PWM cycle period. The IXDP610 responds to the new Pulse Width number three clock cycles after the Pulse Width latch is loaded (1 CLK cycle after $\overline{WR}$ goes high). Thus, OUT1 and OUT2 will immediately reflect the new Pulse Width number. The IXDP610 does not wait until the next PWM cycle to implement a change in the Pulse Width number. (See Fig. 7)

The resulting duty cycle is somewhere between the old and the new duty cycle. The exact value of the resulting duty cycle depends on when the Width Latch is loaded (1 CLK cycle after $\overline{WR}$ goes high). Thus, OUT1 and OUT2 will immediately reflect the new Pulse Width number. The IXDP610 does not wait until the next PWM cycle to implement a change in the Pulse Width number.

Fig. 7a shows what happens when the Pulse Width number is changed from 20 % to 80 % near the middle of the PWM cycle. Fig. 7b shows the reverse situation.

The resulting duty cycle is somewhere between the old and the new duty cycle. The exact value of the resulting duty cycle depends when the Width latch is loaded (1 CLK cycle after $\overline{WR}$ goes high). Thus, OUT1 and OUT2 will immediately reflect the new Pulse Width number. The IXDP610 does not wait until the next PWM cycle to implement a change in the Pulse Width number.