

LTM9001 16-Bit IF/Baseband Receiver Subsystem

DESCRIPTION

Demonstration circuit 1241 is an evaluation board featuring Linear Technology Corporation's LTM9001 16-bit Receiver Subsystem. DC1241 demonstrates good circuit layout techniques and recommended external circuitry for optimal system performance.

DC1241 comes with Linear Technology's 16-bit LTM9001 amplifier/ADC subsystem installed. The board includes a wideband input transformer (for evaluation with a single-ended RF signal generator) and output LVDS buffers. **The LTM9001 is also capable of generat**-

ing CMOS outputs – for evaluation of the part with CMOS outputs, obtain DC1250. DC1241 plugs into the DC890 Data Acquisition demo board and the output can be easily analyzed with Linear Technology's PScope data processing software, which is available for no charge on our website at http://www.linear.com.

Design files for this circuit board are available. Call the LTC factory.

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QUICK START PROCEDURE

Validating the performance of the LTM9001 is simple with DC1241, and requires only an input source, a clock source, a computer, and a lab power supply. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

- Connect the power supply as shown in Figure 1. There are on-board low-noise voltage regulators that provide the three supply voltages for the LTM9001. The entire board and all components share a common ground. The power supply should still be a lownoise lab power supply capable of supplying at least 1 Amp.
- 2. Provide an encode clock to the ADC via SMA connector J3. Use a low-phase-noise clock source such as a filtered RF signal generator or a high-quality clock oscillator. Obtain DC1216 for a low-phasenoise ADC clock source that can plug directly into DC1241.

NOTE. Similar to having a noisy input, a high-jitter (phase noise) encode clock will degrade the signal-to-noise ratio (SNR) of the system.

Table 1: DC1241 Connectors and Jumpers

REFERENCE	FUNCTION
J1 (AIN-)	Differential Board Input. Normally not con-
	nected. See text for differential-input evalua-

	tion methods.
J2 (AIN+)	Board Signal Input. Impedance-matched to
	50 Ω for use with lab signal generators.
J3 (ENC)	Board Clock Input. Impedance-matched to
	50Ω . Drive with a low-phase-noise clock oscil-
	lator or filtered sine wave signal source.
E3 (EXT REF)	Reference input to adjust the full-scale range of
	the LTM9001. Connects to the SENSE pin; by
	default, tied to VDD for internal reference.
E4 (VS)	DC Supply input (3.8 to 6VDC).
E5 (GND)	DC ground.
JP1 (AMP_EN)	Enables the LTM9001 amplifier. Default is EN.
JP2 (PGA_GAIN)	Selects the input range of LTM9001. Default is
	LOW (low PGA gain, larger input range)
JP3 (RAND)	Output Randomizer. NORM is default.
JP4 (ADC_SHDN)	Enables the LTM9001 ADC. Default is NORM.
JP5 (DITH)	ADC Internal Dither. Default is OFF.

- **3.** Apply an input signal to the board. DC1241 allows great flexibility in applying input signals (see the section on Applying Input Signals). For best results, use a low distortion, low noise signal generator with sufficient filtering to avoid degrading the performance of the amplifier and ADC.
- **4.** Observe the ADC output with demo circuit DC890, a USB cable, a Windows computer, and Linear Technology's Pscope data processing software. Note that



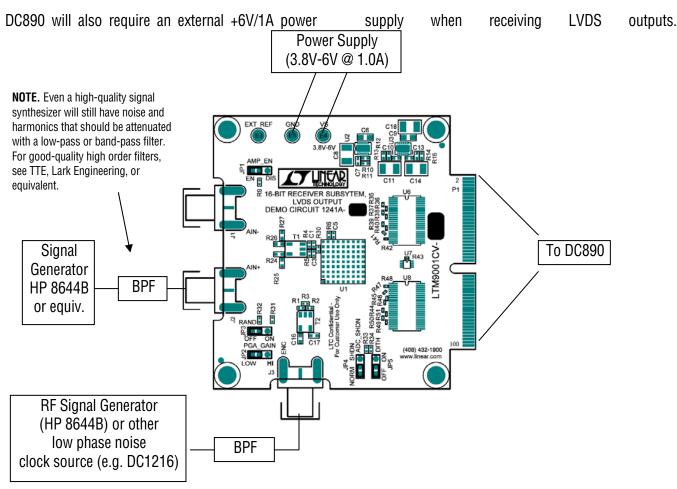


Figure 1. Proper Evaluation Equipment Setup

ADDITIONAL INFORMATION

Although the DC1241 demo board is ready to use on delivery, it has additional flexibility built in for various types of input networks. Below is some information about configuring DC1241 to meet the specific needs of your evaluation.

APPLYING INPUT SIGNALS

The input network consists of various components designed to allow either single-ended or differential inputs, AC-coupled or DC-coupled. Table 2 shows some possible input configurations, and which components to install. LTM9001 is designed for excellent performance with both single-ended and differential input drive, with little difference in distortion performance. When using DC-coupled inputs, the inputs to DC1241 need to be level-shifted to within the input common-mode limits in the datasheet.

Table 2: DC1241 Input Configuration Guide

CONFIGURATION	COMPONENTS NECESSARY
Single-Ended Input	No change. Transformer T1 acts as a balun for
AC-Coupled	differential drive.
(Default Setup)	
Single-Ended Input	Remove T1, replace with 0Ω jumpers. May need
No Transformer	to install impedance-matching resistor at
AC-Coupled	R30 or R4/R5.
Single-Ended Input	Same as above. Change C1 and C3 to 0Ω jump-
No Transformer	ers. Inputs must be within the common-
DC-Coupled	mode voltage limits of LTM9001.
Differential Inputs	Remove R27 and install R26. T1 and C1/C3 can
	be replaced with 0Ω for DC coupling.



NOTE. When driving the ADC driver with a direct DC-coupled path, increased input bias currents may occur due to the amplifier's input impedance. See the LTM9001 datasheet for more details.

OTHER BOARD CIRCUITRY

Logic gate U9, installed on the back of DC1241, enables the LVDS output buffers when DC1241 is plugged into DC890, which pulls its input high. Device U5 is an EEPROM device that is used by the PScope software to identify the board and apply the correct settings for the data collection.

USING PSCOPE SOFTWARE

PScope, downloadable from Linear Technology's website http://www.linear.com/, processes data from the DC890

FastDAACS board and displays FFT and signal analysis information on the computer screen.

The on-board EEPROM U5 should enable automatic board detection and auto-configuration of the software, but if the user wishes to change the settings, they can easily do so.

From the Configure menu in the toolbar, uncheck "Autodetect Device". The default settings for DC1241A are shown in Figure 2. The LTM9001 also has an output randomizer, which the user needs to select if it is enabled on the board. The software will automatically unrandomize the output by performing an exclusive-OR with each bit and the LSB.

ADC Configuration	
Read Demo Board	🗹 Config Manually
DemoBd DC1241B-A	LTC9001-AA
Bits 16	1 Channs
Alignment 16	🔽 Bipolar
FPGA Ld LVDS	Positive-Edge Clk
Cancel	Apply

Figure 2. Entering the correct device information for your ADC. Select the correct parameters for the DC1241. Under normal conditions, PSCOPE should automatically recognize the board and adjust the software settings accordingly.



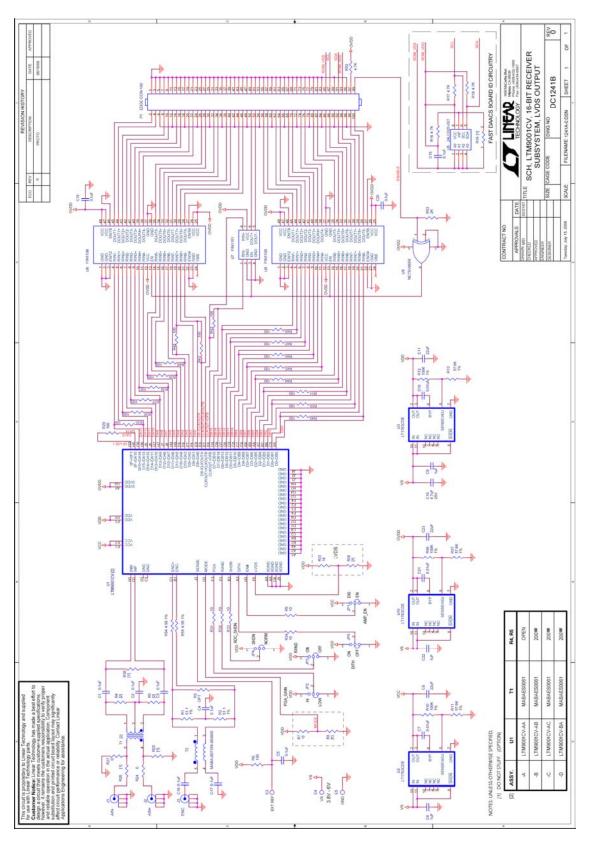


Figure 3. Schematic

