19-2761; Rev 0; 1/03

EVALUATION KIT AVAILABLE

Ultra-High-Efficiency White LED Drivers

General Description

The MAX1984/MAX1985/MAX1986 are white light-emitting diode (LED) drivers that use individual regulators to control the current of up to eight LEDs. A high-efficiency step-up regulator generates just enough voltage to keep all the current regulators in regulation. A versatile dimming interface accommodates analog, digitally adjusted pulse-width modulation (DPWM), or parallel control.

The individual current regulators allow good current matching between LEDs. Open or shorted LEDs cannot affect the performance of other LEDs.

The step-up regulator achieves high efficiency by using synchronous rectification. The internal N-channel switch and P-channel synchronous rectifier eliminate the need for external MOSFETs and diodes. The 1MHz switching frequency allows the use of low-profile inductors and ceramic capacitors.

The brightness can be easily adjusted using a multimode dimming interface, which allows brightness control through a DPWM signal, a 2- or 3-bit parallel control interface, or an analog signal. The DPWM signal can be connected directly to the control pin without the need for an external RC filter if its frequency is 10kHz or above.

The MAX1984 drives up to eight LEDs, the MAX1985 drives up to six LEDs, and the MAX1986 drives up to four LEDs. Each device has an LED select pin (SEL) that allows one subset, the other subset, or all LEDs to be illuminated. All three devices are available in a 4mm × 4mm thin QFN package.

Applications

PDAs and Hand-Held PCs

Cellular Phones

Digital Cameras

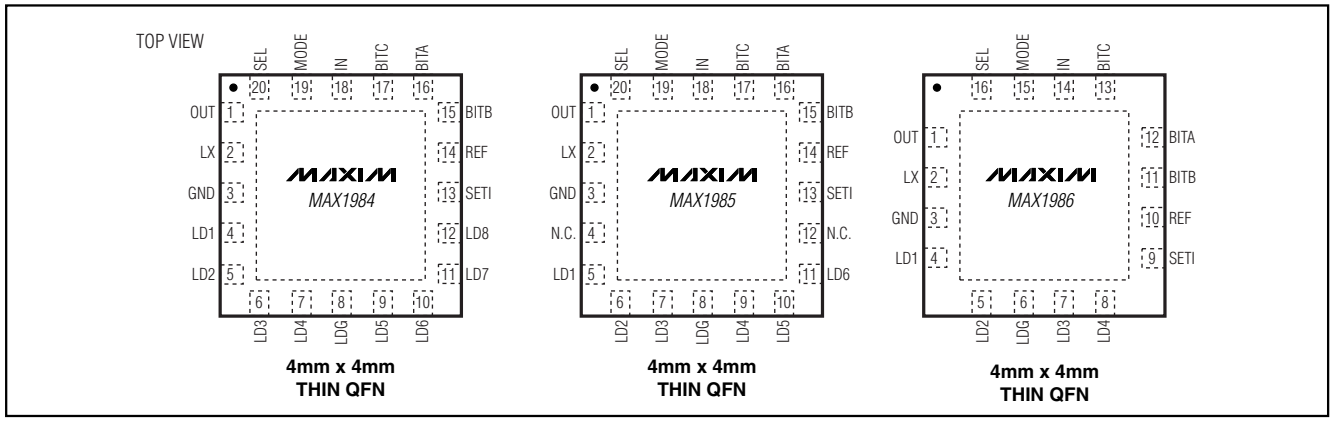
Features

- **Synchronous Step-Up Regulator**
  - **Achieves >95% Efficiency**
  - **Internal Switch and Synchronous Rectifier Eliminates External MOSFETs and Diodes**
  - **1MHz Fixed Frequency Minimizes Component Sizes**
- **Up to 90% Total LED Efficiency**
- **Accurate LED Current Matching (8% max)**
- **Adjustable Maximum LED Current**
- **Multimode Dimming Control**
  - **Digital Pulse-Width Modulation Control**
  - **2-Bit Parallel Control**
  - **3-Bit Parallel Control**
  - **Analog Control**
- **Selectively Enable LEDs**
- **Open-LED Detection**
- **Unique 0.5mA LED Test Mode**
- **2.7V to 5.5V Input Supply Range**
- **Small 4mm x 4mm 20-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	NO. OF LEDs
MAX1984ETP	-40°C to +85°C	20 Thin QFN	8
MAX1985ETP	-40°C to +85°C	20 Thin QFN	6
MAX1986ETE	-40°C to +85°C	16 Thin QFN	4

Pin Configurations



Ultra-High-Efficiency White LED Drivers

ABSOLUTE MAXIMUM RATINGS

OUT, IN, BITA, BITB, BITC, LD1, LD2, LD3, LD4, LD5, LD6, LD7, LD8 to GND .....-0.3V to +6V
LDG to GND.....±0.3V
LX to GND .....-0.3V to (V_{OUT} + 0.3V)
SETI, REF, MODE, SEL to GND.....-0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 16.9mW/°C above +70°C) ...1349mW
20-Pin Thin QFN (derate 16.9mW/°C above +70°C) ...1349mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1; V_{IN} = 3.3V, SETI = BITA = BITB = BITC = SEL = IN, MODE = GND, C_{OUT} = 4.7µF, C_{REF} = 0.22µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Supply Range		2.7		5.5	V
IN Undervoltage Lockout Threshold	50mV typical hysteresis	2.2	2.4	2.6	V
IN Quiescent Current	BITA = BITB = BITC = IN, LD1 to LD8 = GND		400	600	µA
IN Shutdown Current	BITA = BITB = BITC = GND		0.1	1	µA
REF Output Voltage	I_{REF} = 0	1.230	1.250	1.270	V
REF Line Regulation	2.7V < V_{IN} < 5.5V		0.2	5	mV
REF Load Regulation	-1µA < I_{REF} < +50µA		5	15	mV
Oscillator Frequency		0.8	1	1.2	MHz
Oscillator Maximum Duty Cycle			85		%
OUT Overvoltage Protection (OVP) Threshold	V_{LD1} to V_{LD8} = 50mV, OUT rising, 100mV typical hysteresis	5.1	5.3	5.5	V
INTERNAL MOSFET SWITCHES					
N-Channel MOSFET On-Resistance	I_{LX} = 200mA		0.4	0.8	Ω
N-Channel MOSFET Leakage Current	V_{LX} = 5.5V, BITA = BITB = BITC = GND		0.1	1	µA
P-Channel MOSFET On-Resistance	I_{LX} = 200mA		0.5	1	Ω
P-Channel MOSFET Leakage Current	LX = GND, V_{OUT} = 5.5V, BITA = BITB = BITC = GND		0.1	1	µA
N-Channel MOSFET Current Limit	MAX1984	0.50	0.65	0.81	A
	MAX1985	0.40	0.52	0.65	
	MAX1986	0.30	0.39	0.52	
CONTROL INPUTS					
BITA, BITB, BITC Input Logic Low Level	2.7V < V_{IN} < 5.5V			0.4	V
BITA, BITB, BITC Input Logic High Level	2.7V < V_{IN} < 5.5V	1.6			V
MODE Input Logic Low Level	2.7V < V_{IN} < 5.5V			0.4	V
MODE Input Logic High Level	2.7V < V_{IN} < 5.5V	V_{IN} - 0.4			V
MODE, BITA, BITB, BITC Input Bias Current	2.7V < V_{IN} < 5.5V		0.01	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1; V_{IN} = 3.3V, SETI = BITA = BITB = BITC = SEL = IN, MODE = GND, C_{OUT} = 4.7µF, C_{REF} = 0.22µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SEL Input Logic Low Level	2.7V < V_{IN} < 5.5V			0.4	V
SEL Input Logic Midlevel	2.7V < V_{IN} < 5.5V	0.50		1.85	V
SEL Input Logic High Level	2.7V < V_{IN} < 5.5V	2.05			V
SEL Input Bias Current	SEL = GND, current out of the pin			5	µA
	SEL = IN, current into the pin			10	
FULL-SCALE LED CURRENT ADJUSTMENT					
LD1 to LD8 Output Current	$V_{LD\_}$ = 80mV, SETI = BITA = BITB = BITC = IN	16.5	18	19.5	mA
	$V_{LD\_}$ = 80mV, R_{SETI} = 278kΩ ±0.1%, BITA = BITB = BITC = IN	22.5	25	27.5	
	$V_{LD\_}$ = 80mV, R_{SETI} = 1.8MΩ ±0.1%, BITA = BITB = BITC = IN	12.5	14	15.5	
	$V_{LD\_}$ = 80mV, R_{SETI} = 597kΩ ±0.1%, BITA = BITB = BITC = IN	16.5	18	19.5	
	V_{LD1} = 1V, R_{SETI} = 10kΩ, BITA = BITB = BITC = IN		26		
	SETI = GND	0.42	0.50	0.60	
LD1 to LD8 Regulation Voltage	SETI = IN, I_{LX} = 120mA (MAX1984), 110mA (MAX1985), 98mA (MAX1986)	80	100	120	mV
SETI High-Level Threshold (18mA LED Default Current)	2.7V < V_{IN} < 5.5V	V_{IN} - 0.4			V
SETI Low-Level Threshold (0.5mA LED Default Current)	2.7V < V_{IN} < 5.5V	50		125	mV
SETI Output Current	SETI = GND	40	70	100	µA
OUTPUT CURRENT SOURCE					
LD1 to LD8 On-Resistance	$V_{LD\_}$ = 50mV, V_{OUT} = 3.5V		3	4	Ω
LD1 to LD8 Current-Source Compliance	BITA = BITB = BITC = IN, 80mV < $V_{LD\_}$ < 1V (Note 1)		0.3	5	%
LD1 to LD8 Leakage Current	BITA = BITB = BITC = GND		0.01	1	µA
DIGITAL BRIGHTNESS CONTROL					
2-Bit Control DAC LSB	MODE = SETI = BITB = IN, BITA = BITC = GND (Note 2)	26	33	39	%
3-Bit Control DAC LSB	SETI = BITC = IN, MODE = BITA = BITB = GND (Note 2)	7	14	21	%
DPWM BRIGHTNESS CONTROL					
DPWM Input Supply Range	MODE = BITC = IN	2.3		5.5	V
DPWM Shutdown Duty Cycle	BITC = GND	3	5	7	%

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1; V_{IN} = 3.3V, SETI = BITA = BITB = BITC = SEL = IN, MODE = GND, C_{OUT} = 4.7µF, C_{REF} = 0.22µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Supply Range		2.7		5.5	V
IN Undervoltage Lockout Threshold	50mV typical hysteresis	2.2		2.6	V
IN Quiescent Current	BITA = BITB = BITC = IN, LD1 to LD8 = GND			600	µA
REF Output Voltage	I_{REF} = 0	1.230		1.270	V
REF Line Regulation	2.7V < V_{IN} < 5.5V			5	mV
REF Load Regulation	-1µA < I_{REF} < +50µA			15	mV
Oscillator Frequency		0.8		1.2	MHz
OUT Overvoltage Protection Threshold	V_{LD1} to V_{LD8} = 50mV, OUT rising, 100mV typical hysteresis	5.1		5.5	V
INTERNAL MOSFET SWITCHES					
N-Channel MOSFET On-Resistance	I_{LX} = 200mA			0.8	Ω
P-Channel MOSFET On-Resistance	I_{LX} = 200mA			1.0	Ω
N-Channel MOSFET Current Limit	MAX1984	0.50		0.81	A
	MAX1985	0.40		0.65	
	MAX1986	0.30		0.52	
CONTROL INPUTS					
BITA, BITB, BITC Input Logic Low Level	2.7V < V_{IN} < 5.5V			0.4	V
BITA, BITB, BITC Input Logic High Level	2.7V < V_{IN} < 5.5V	1.6			V
MODE Input Logic Low Level	2.7V < V_{IN} < 5.5V			0.4	V
MODE Input Logic High Level	2.7V < V_{IN} < 5.5V	V_{IN} - 0.4			V
SEL Input Logic Low Level	2.7V < V_{IN} < 5.5V			0.4	V
SEL Input Logic Midlevel	2.7V < V_{IN} < 5.5V	0.50		1.85	V
SEL Input Logic High Level	2.7V < V_{IN} < 5.5V	2.05			V
FULL-SCALE LED CURRENT ADJUSTMENT					
LD1 to LD8 Output Current	$V_{LD\_}$ = 80mV, SETI = BITA = BITB = BITC = IN	16		20	mA
	$V_{LD\_}$ = 80mV, R_{SETI} = 278kΩ ±1%, BITA = BITB = BITC = IN	22		28	
	$V_{LD\_}$ = 80mV, R_{SETI} = 1.8MΩ ±1%, BITA = BITB = BITC = IN	11.5		16.0	
	$V_{LD\_}$ = 80mV, R_{SETI} = 697kΩ ±1%, BITA = BITB = BITC = IN	15.5		20.0	
	SETI = GND	0.42		0.60	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1; V_{IN} = 3.3V, SETI = BITA = BITB = BITC = SEL = IN, MODE = GND, C_{OUT} = 4.7µF, C_{REF} = 0.22µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LD1 to LD8 Regulation Voltage	SETI = IN, I_{LX} = 120mA (MAX1984), 110mA (MAX1985), 98mA (MAX1986)	80		120	mV
SETI High-Level Threshold (18mA LED Default Current)	2.7V < V_{IN} < 5.5V	V_{IN} - 0.4			V
SETI Low-Level Threshold (0.5mA LED Default Current)	2.7V < V_{IN} < 5.5V	50		125	mV
SETI Output Current	SETI = GND	40		100	µA
OUTPUT CURRENT SOURCE					
LD1 to LD8 On-Resistance	$I_{LD\_}$ = 25mA, V_{OUT} = 3.5V			4	Ω
LD1 to LD8 Current-Source Compliance	BITA = BITB = BITC = IN, 80mV < $V_{LD\_}$ < 1V (Note 1)			8	%
DIGITAL BRIGHTNESS CONTROL					
2-Bit Control DAC LSB	MODE = SETI = BITB = IN, BITA = BITC = GND	26		39	%
3-Bit Control DAC LSB	SETI = BITC = IN, MODE = BITA = BITB = GND (Note 2)	7		21	%
DPWM BRIGHTNESS CONTROL					
DPWM Input Supply Range	MODE = BITC = IN	2.3		5.5	V
DPWM Shutdown Duty Cycle	BITC = GND	3		7	%

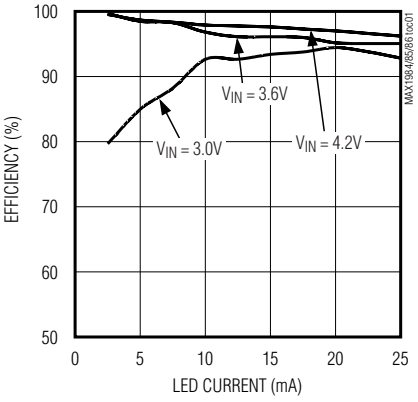
Note 1: Current variation is caused by the current source voltage changes.
Note 2: Measurement is with respect to 100% of the programmed LED output current.
Note 3: Specifications to -40°C are guaranteed by design, not production tested.

Ultra-High-Efficiency White LED Drivers

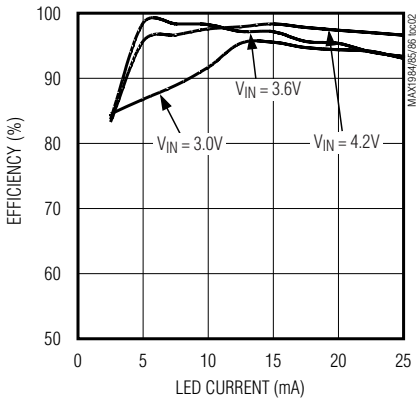
Typical Operating Characteristics

(Circuit of Figure 1; V_{IN} = 3.3V, SETI = IN, MODE = IN, T_A = +25°C, unless otherwise noted.)

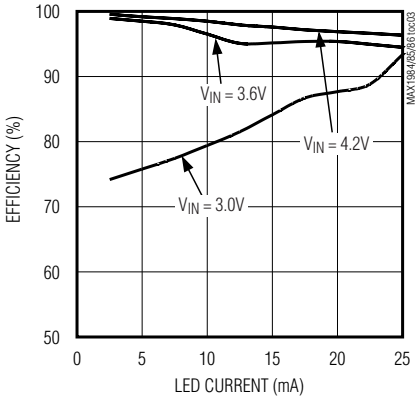
STEP-UP REGULATOR EFFICIENCY vs. LED CURRENT (8 LEDs)



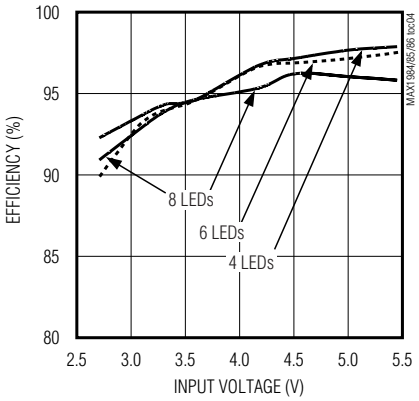
STEP-UP REGULATOR EFFICIENCY vs. LED CURRENT (6 LEDs)



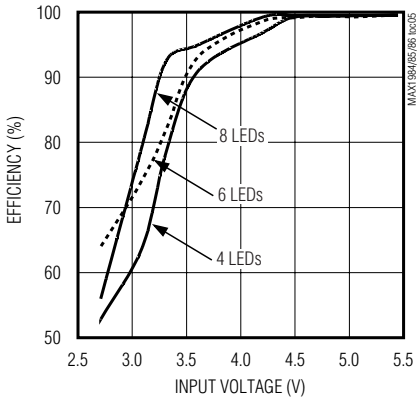
STEP-UP REGULATOR EFFICIENCY vs. LED CURRENT (4 LEDs)



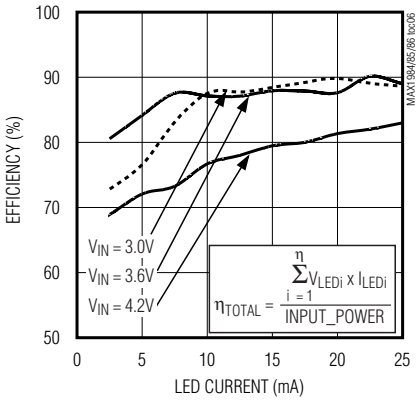
STEP-UP REGULATOR EFFICIENCY vs. INPUT VOLTAGE (25mA LED CURRENT)



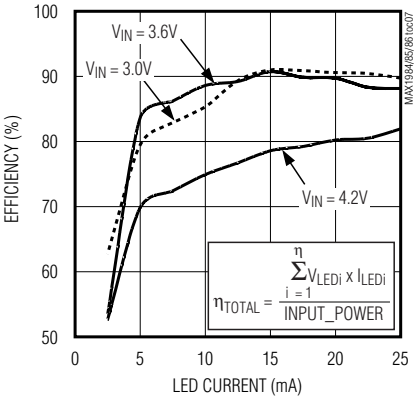
STEP-UP REGULATOR EFFICIENCY vs. INPUT VOLTAGE (4mA LED CURRENT)



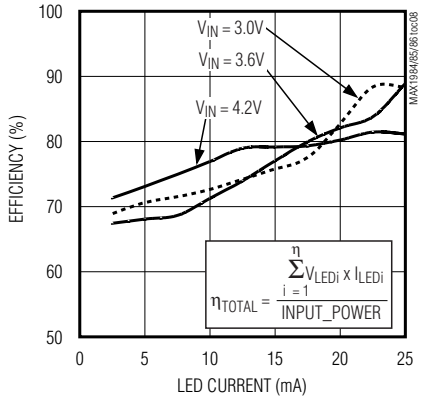
TOTAL EFFICIENCY vs. LED CURRENT (8 LEDs)



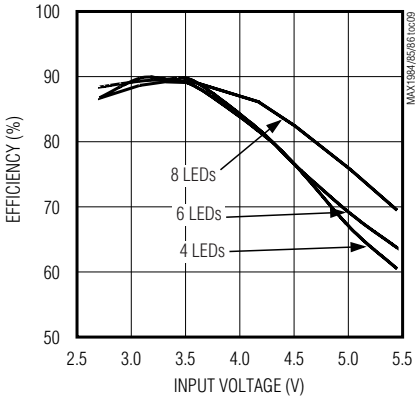
TOTAL EFFICIENCY vs. LED CURRENT (6 LEDs)



TOTAL EFFICIENCY vs. LED CURRENT (4 LEDs)



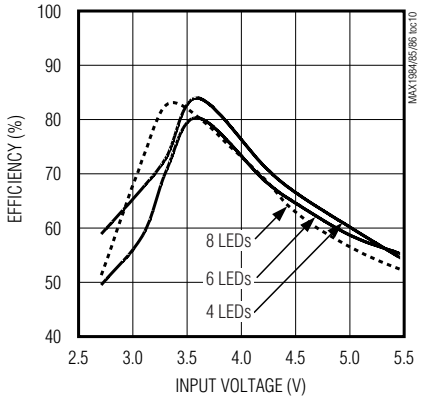
TOTAL EFFICIENCY vs. INPUT VOLTAGE (25mA LED CURRENT)



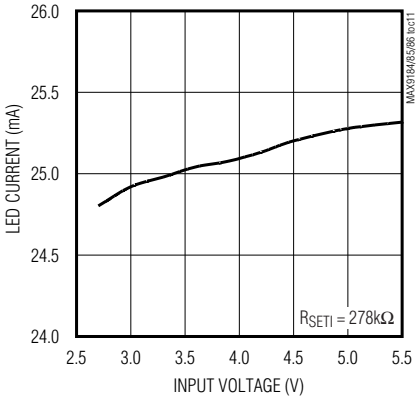
Typical Operating Characteristics (continued)

(Circuit of Figure 1; V_{IN} = 3.3V, SETI = IN, MODE = IN, T_A = +25°C, unless otherwise noted.)

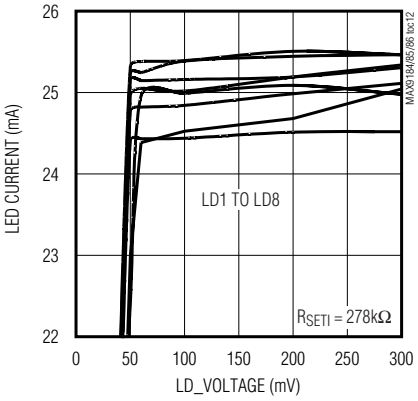
TOTAL EFFICIENCY vs. INPUT VOLTAGE (4mA LED CURRENT)



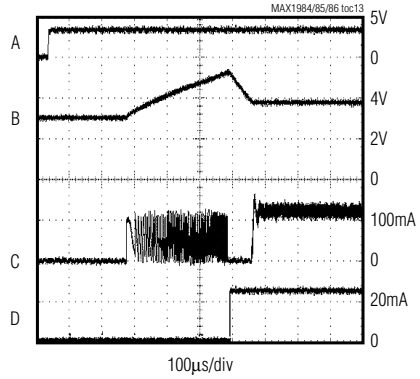
LED CURRENT vs. INPUT VOLTAGE



LED CURRENT MATCHING

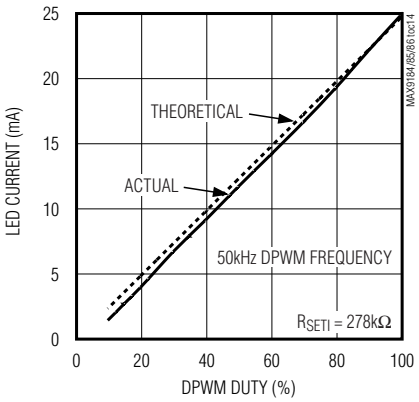


STARTUP WAVEFORMS

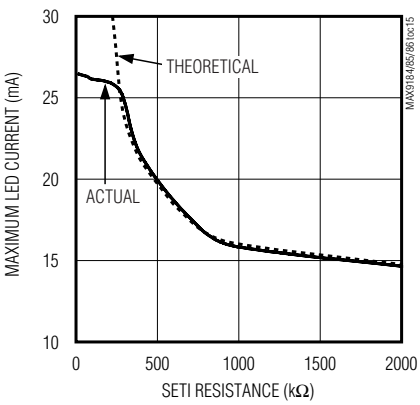


A: BITA VOLTAGE, 5V/div
B: OUT VOLTAGE, 2V/div
C: INDUCTOR CURRENT, 100mA/div
D: LD_ CURRENT, 20mA/div

LED CURRENT vs. DPWM DUTY



MAXIMUM LED CURRENT vs. SETI RESISTANCE



Ultra-High-Efficiency White LED Drivers

Pin Description

PIN			NAME	FUNCTION
MAX1984	MAX1985	MAX1986		
1	1	1	OUT	Step-Up Regulator Output. Bypass OUT to GND with a 4.7µF capacitor.
2	2	2	LX	Inductor Connection. LX is connected to the drains of the internal N-channel and P-channel MOSFETs.
3	3	3	GND	Ground
—	4, 12	—	N.C.	No Connection. Not internally connected.
4	5	4	LD1	LED1 Cathode Connection. LD1 is the open-drain output of an internal current regulator for controlling the current through LED1. It is able to sink up to 25mA. If not used, connect LD1 to GND.
5	6	5	LD2	LED2 Cathode Connection. LD2 is the open-drain output of an internal current regulator for controlling the current through LED2. It is able to sink up to 25mA. If not used, connect LD2 to GND.
6	7	7	LD3	LED3 Cathode Connection. LD3 is the open-drain output of an internal current regulator for controlling the current through LED3. It is able to sink up to 25mA. If not used, connect LD5 to GND.
7	9	8	LD4	LED4 Cathode Connection. LD4 is the open-drain output of an internal current regulator for controlling the current through LED4. It is able to sink up to 25mA. If not used, connect LD4 to GND.
8	8	6	LDG	Common Ground Connection for Internal Current Regulators. Connect LDG to GND.
9	10	—	LD5	LED5 Cathode Connection. LD5 is the open-drain output of an internal current regulator for controlling the current through LED5. It is able to sink up to 25mA. If not used, connect LD5 to GND.
10	11	—	LD6	LED6 Cathode Connection. LD6 is the open-drain output of an internal current regulator for controlling the current through LED6. It is able to sink up to 25mA. If not used, connect LD6 to GND.
11	—	—	LD7	LED7 Cathode Connection. LD7 is the open-drain output of an internal current regulator for controlling the current through LED7. It is able to sink up to 25mA. If not used, connect LD7 to GND.
12	—	—	LD8	LED8 Cathode Connection. LD8 is the open-drain output of an internal current regulator for controlling the current through LED8. It is able to sink up to 25mA. If not used, connect LD8 to GND.
13	13	9	SETI	Maximum LED Current Set Input. SETI sets the maximum current through each LED. Connect SETI to IN for a default maximum current of 18mA; connect SETI to GND for the 0.5mA LED test mode. Connect a resistor from SETI to GND to adjust the maximum current between 12mA to 25mA (see the *Setting the Maximum LED Current* section).
14	14	10	REF	1.25V Reference Output. Bypass REF to GND with a minimum 0.22µF ceramic capacitor.
15	15	11	BITB	Brightness Control Input (Multimode): DPWM Mode: Leave unconnected for greater than 50kHz operation. Add a capacitor from BITB to ground for lower frequency operation. Analog Mode: Analog control signal input. 2- or 3-Bit Parallel Mode: Digital input. Least significant bit (LSB) for 2-bit mode.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1984	MAX1985	MAX1986		
16	16	12	BITA	Brightness Control Input (Multimode): DPWM Mode: DPWM control signal input. Analog Mode: Connect to IN. 2- or 3-Bit Parallel Mode: Digital input. Most significant bit (MSB).
17	17	13	BITC	Brightness Control Input: DPWM Mode: Connect to IN. Analog Mode: Connect to IN. 2-Bit Parallel Mode: Connect to GND. 3-Bit Parallel Mode: Digital input (LSB).
18	18	14	IN	Input Supply. IN provides power to the internal control circuitry and MOSFET drivers. Bypass IN to GND with a minimum 0.1µF ceramic capacitor.
19	19	15	MODE	Brightness Control Mode Selection Input. Connect MODE and BITC to IN for DPWM control. Connect MODE, BITA, and BITC to IN for analog control. For 2-bit parallel control, connect MODE to IN and BITC to ground. For 3-bit parallel control, connect MODE to GND.
20	20	16	SEL	LED Selection Input. Connect SEL to IN to turn on all LEDs. Connect SEL to ground to turn on only LED1–LED5 (MAX1984), LED1–LED4 (MAX1985), or LED1 to LED3 (MAX1986). Leave SEL unconnected or force to $V_{IN}/2$ to turn on only LED6 to LED8 (MAX1984), LED3–LED6 (MAX1985), or LED4 (MAX1986).

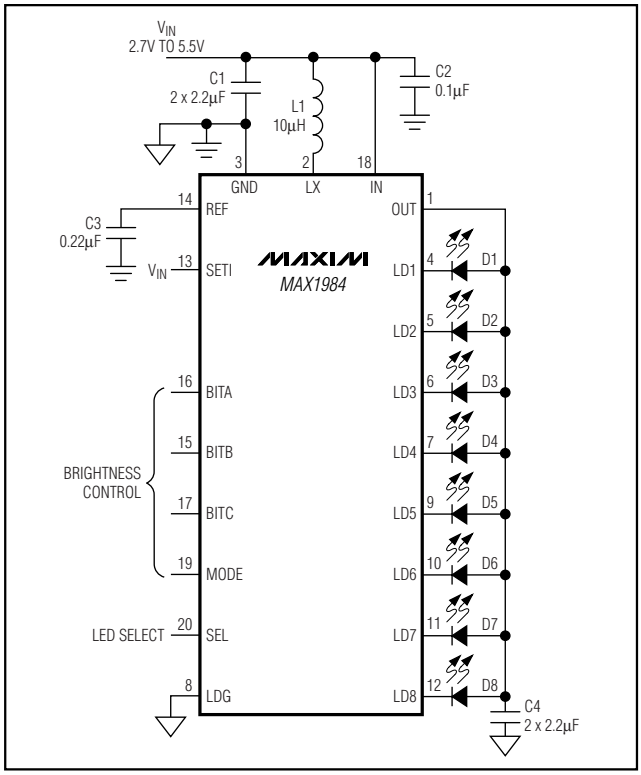


Figure 1. Standard Application Circuit of the MAX1984

Ultra-High-Efficiency White LED Drivers

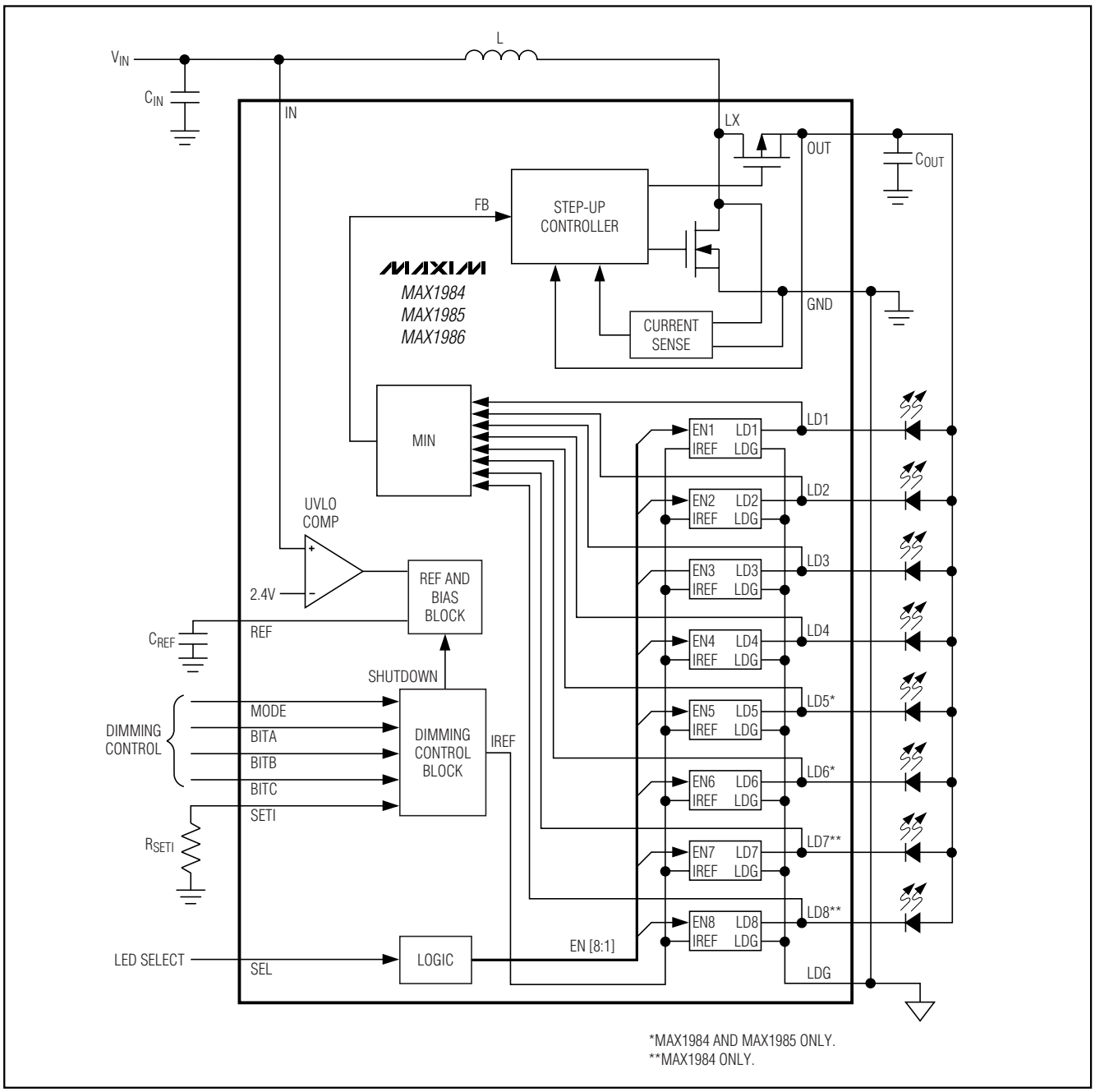


Figure 2. System Functional Diagram

Standard Application Circuits

The standard application circuit of the MAX1984 drives eight white LEDs (Figure 1). The standard application circuit of the MAX1985 drives six white LEDs (Figure 6). The standard application circuit of the MAX1986 drives four white LEDs (Figure 7). The input voltage range is from 2.7V to 5.5V. Table 1 lists the recommended component options and Table 2 lists the component suppliers.

Detailed Description

The MAX1984/MAX1985/MAX1986 are white LED drivers that use individual regulators to control the current of up to eight LEDs. A high-efficiency step-up regulator generates just enough voltage to keep all the current regulators in regulation. A versatile dimming interface accommodates analog, DPWM, or parallel control.

LED Current Regulators

Good LED current matching is achieved using individual current regulators for each LED (Figure 3). The regulator is an analog gain block with an open-drain N-channel MOSFET output stage and can sink up to 25mA LED current. The LED current is sensed using an internal 1Ω resistor connected between the source of the MOSFET and ground. The regulator controls the output current by comparing the voltage across the current-sense resistor with a reference voltage (IREF) set by the dimming control circuitry.

Startup and Feedback

The step-up converter is regulated at a voltage just high enough to power the LEDs. Since the forward voltage is different for each LED, the LED with the largest forward voltage sets the regulation voltage. Each current regulator's voltage drop (from LD_ to LDG) is monitored and the lowest voltage drop is used as the step-up regulator's feedback.

At startup, it is important to ensure the output voltage rises high enough to forward bias all LEDs and allow their current regulators to detect their presence. Therefore, before the current regulators are enabled the step-up regulator output is made to rise up to the OUT OVP threshold (5.3V, typ). Then, the step-up regulator stops switching and each current regulator output is tested

Table 1. Component List

DESIGNATION	DESCRIPTION		
	MAX1984	MAX1985	MAX1986
C1, C4	2 x 2.2µF, 6.3V X5R ceramic capacitors (0603) Taiyo Yuden JMK107BJ225MA TDK C1608X5ROJ225K	2 x 2.2µF, 6.3V X5R ceramic capacitors (0603) Taiyo Yuden JMK107BJ225MA TDK C1608X5ROJ225K	2.2µF, 6.3V X5R ceramic capacitors (0603) Taiyo Yuden JMK107BJ225MA TDK C1608X5ROJ225K
D1–D4, D5*, D6*, D7**, D8**	Surface-mount white LEDs Nichia NSCW215T		
L1	10µH, 1A inductor Sumida CLS5D11HP-100NC	15µH, 0.85A inductor Sumida CLS5D11HP-150NC	22µH, 0.65A inductor Sumida CLS5D11HP-220NC

**MAX1984 and MAX1985 only.*
***MAX1984 only.*

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Nichia	717-285-2323	717-285-9378	www.nichia.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
Taiyo Yuden	800-348-2496	847-925-0899	www.t-yuden.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com

Ultra-High-Efficiency White LED Drivers

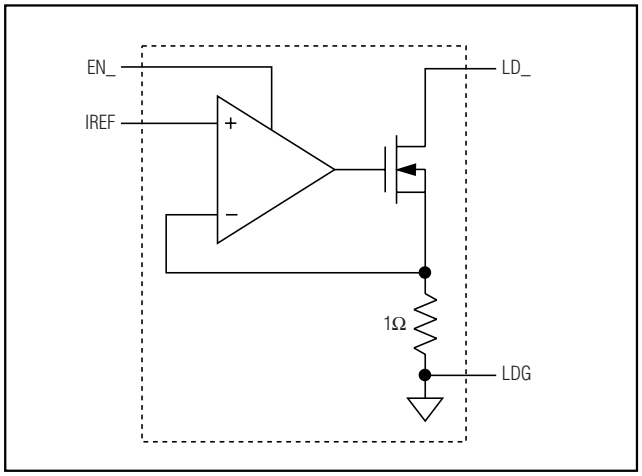


Figure 3. Current Regulator Functional Diagram

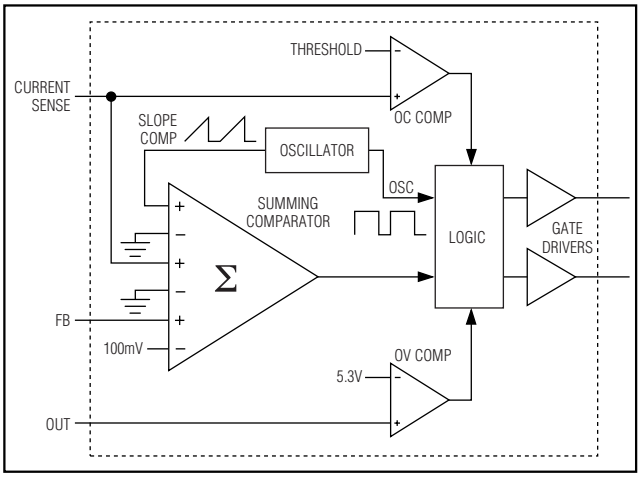


Figure 4. Step-Up Regulator Functional Diagram

for an LED's presence. The current regulators are enabled and any regulator with an output voltage less than 45mV is detected and is ignored, preventing outputs left open or shorted to ground from dominating the step-up regulation loop. Outputs shorted to IN, OUT, or any voltage above 45mV resemble valid LEDs and are regulated at the current set point.

As the LEDs draw current, the step-up regulator's output voltage gradually falls and the voltage drop across each of the current regulators reduces. Eventually, the voltage drop across whichever current regulator drives the LED with the highest forward voltage reaches the step-up regulator's threshold (100mV, typ) and step-up switching starts again (see the Startup Waveform in the *Typical Operating Characteristics*).

Step-Up Regulator

The step-up regulator employs a fixed-frequency current-mode control method to generate the bias voltage for the white LEDs. The regulator takes the minimum value of all the LD_ pin voltages as the feedback signal to ensure that the output voltage is high enough to drive all the LEDs. The heart of the controller is a multi-input, open-loop comparator that sums three signals: the feedback error signal with respect to the 100mV reference, the current-sense signal, and the slope compensation ramp (Figure 4).

In normal operation, the controller starts a new cycle by turning on the N-channel MOSFET and turning off the P-channel MOSFET on the rising edge of the internal oscillator if all of the following three conditions are satisfied: the summing comparator output is low, the switch current does not exceed the overcurrent threshold, and the output voltage does not exceed the overvoltage threshold. The controller turns off the N-channel MOSFET and turns on the P-channel MOSFET when one of the following three conditions occurs: the summing comparator output becomes high, the switch current exceeds the overcurrent threshold, or the falling edge of the oscillator occurs.

Both the N-channel MOSFET and the P-channel MOSFET turn off if the output voltage exceeds the overvoltage rising threshold. Both switches stay off until all of the following three conditions are satisfied: the output voltage is below the overvoltage falling threshold, the summing comparator output is low, and the next rising edge of the oscillator occurs.

Brightness Control Interface

The light intensity of the white LEDs can be easily adjusted from 15% to 100% of the full-scale LED current chosen by SETI. The MAX1984/MAX1985/MAX1986 support DPWM control, analog control, and 2-bit or 3-bit parallel control.

DPWM Control

To use the DPWM control mode, connect MODE and BITC to IN, leave BITB unconnected, and connect the DPWM signal to BITA. The LED current is given by the following equation:

$$I_{LED} = D \times I_{LED(FS)}$$

where $I_{LED(FS)}$ is the full-scale LED current set by SETI, and D is the duty cycle of the DPWM signal. The average voltage of the DPWM signal is obtained through an internal RC filter (Figure 5). The 0.1ms filter time constant allows the use of DPWM frequencies from 10kHz to 2MHz. If lower frequencies are preferred, an external

capacitor can be connected from BITB to ground to increase the total time constant. Use the following equation to calculate the total time constant:

$$\tau = 0.2M\Omega \times C_{EXT} + 0.098ms$$

where C_{EXT} is the external capacitance.

The recommended DPWM duty-factor range is from 20% to 100% for DPWM frequencies between 20kHz and 2MHz, using the internal 0.1ms filter. For lower DPWM operating frequencies, use C_{EXT} and ensure the voltage on C_{EXT} (BITB), including ripple, remains above $DF_{MIN} \times 0.75 \times V_{REF}$, where DF_{MIN} is the minimum reliable DPWM duty factor of 15%.

In DPWM mode, the MAX1984/MAX1985/MAX1986 enter shutdown mode when the DPWM duty cycle is below 5% (typ) and BITC is a logical low level.

Analog Control

To use the analog control mode, connect MODE, BITA, and BITC to IN. Connect BITB to a DC voltage that sets the LED current. The operational range for the analog control is from 140mV (15%) to 0.75 × V_{REF} (100%). The LED current is given by the following equation:

$$I_{LED} = \left(K1 + K2 \times \frac{V_{BITB}}{0.75 \times V_{REF}} \right) \times I_{LED(FS)}$$

where K1 = 0.0465, K2 = 0.953, V_{BITB} is the voltage at the BITB pin, V_{REF} is the 1.25V internal reference voltage, and $I_{LED(FS)}$ is the full-scale LED current set by SETI.

In analog mode, the MAX1984/MAX1985/MAX1986 enter shutdown mode when both V_{BITA} and V_{BITB} are logic low.

Parallel Control

The MAX1984/MAX1985/MAX1986 also support 2-bit or 3-bit parallel control. To use the 3-bit parallel control mode, connect MODE to ground. BITA is the most significant bit and BITC is the least significant bit. To use the 2-bit parallel control, connect MODE to IN and BITC to ground. BITA is the most significant bit and BITB is the least significant bit. In parallel mode, the MAX1984/MAX1985/MAX1986 enter shutdown mode when BITA, BITB, and BITC are logic low. Tables 3 and 4 are the truth tables.

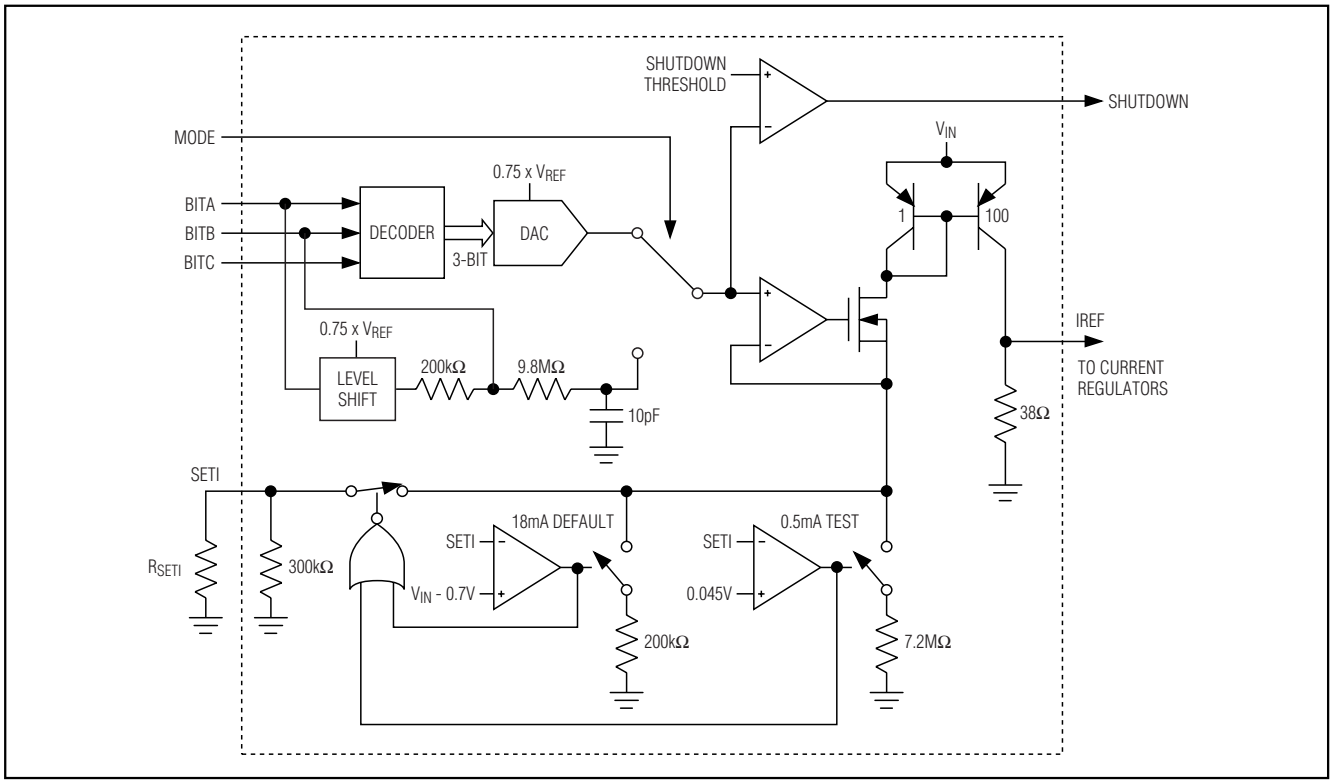


Figure 5. Brightness Control Equivalent Functional Diagram

Ultra-High-Efficiency White LED Drivers

LED Selection

The MAX1984/MAX1985/MAX1986 provide a control input (SEL) to selectively turn on one subset, the other subset, or all of the LEDs. SEL is a three-level logic input that can be connected to logic low, logic high, or left unconnected. Table 5 is the truth table.

LED Test Mode

Connecting SETI to ground enables the LED test mode. In this mode, the LED current is set to 0.5mA and DC-to-DC switching is inhibited. OUT is powered from IN through an internal silicon diode.

Forcing 0.5mA through the LED is a simple way to determine whether the diode has suffered any ESD damage. LEDs that do not light in this mode usually have suffered ESD or other damage. The dimming control inputs are ignored in the test mode.

Table 3. 3-Bit Parallel Control Truth Table

BITA	BITB	BITC	BRIGHTNESS (%)	COMMENTS
0	0	0	0	Shutdown
0	0	1	14.3	Minimum current
0	1	0	26.6	—
0	1	1	42.9	—
1	0	0	57.1	—
1	0	1	71.4	—
1	1	0	85.7	—
1	1	1	100	Full-scale current set by SETI

Table 4. 2-Bit Parallel Control Truth Table

BITA	BITB	BITC	BRIGHTNESS (%)	COMMENTS
0	0	0	0	Shutdown
0	1	0	33.3	Minimum current
1	0	0	66.7	—
1	1	0	100	Full-scale current set by SETI

Table 5. SEL Control Truth Table

SEL	MAX1984	MAX1985	MAX1986
Low (V_{SEL} < 0.4V)	LED1 to LED5 ON	LED1 to LED4 ON	LED1 to LED3 ON
Mid (SEL unconnected or 0.5V < V_{SEL} < 1.8V)	LED6 to LED8 ON	LED5 to LED6 ON	LED4 ON
High (V_{SEL} > 2.05V)	All LEDs ON		

Shutdown

As soon as the input voltage rises above the UVLO threshold and the internal reference is ready, the step-up regulator starts unless the device is in shutdown. If a 2-bit or 3-bit parallel control is used, the MAX1984/MAX1985/MAX1986 enter shutdown mode when BITA, BITB, and BITC are logic low. The parts come out of shutdown if at least 1 bit is logic high. If DPWM control is used, the parts enter shutdown mode when the duty cycle of BITA is less than 5% (typ) and BITC is logic low. If analog control is used, the parts enter shutdown when the voltages on both BITA and BITB are logic low.

Overvoltage Protection

Output OVP prevents the internal switches from being damaged if all LEDs are open. If the output voltage rises above OUT OVP rising threshold, the MAX1984/MAX1985/MAX1986 turn off the step-up regulator. Once the output voltage falls below OVP falling threshold, the step-up regulator turns on again.

Applications Information

Inductor Selection

The MAX1984/MAX1985/MAX1986's 1MHz switching frequency allows the use of low-profile surface-mount inductors. The MAX1984 works well with a 10µH inductor, the MAX1985 works well with a 15µH inductor, and the MAX1986 works well with a 22µH inductor. The inductor saturation current rating should be higher than the N-channel switch current limit. For high efficiency, choose an inductor made of high-frequency core material to reduce core losses. Using a shielded inductor reduces radiated EMI.

Output Capacitor Selection

The output capacitor affects the circuit's stability and output-voltage ripple. The MAX1984 works well with a 4.7µF ceramic output capacitor, the MAX1985 works well with a 3.3µF ceramic output capacitor, and the MAX1986 works well with a 2.2µF ceramic output capacitor. Always use capacitors with working voltage ratings higher than the output OVP rising threshold (5.5V max).

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input supply and reduces noise injection into all devices running from that supply. The input voltage source impedance determines the required size of the input capacitor. The standard application circuits (Figures 1, 6, and 7) use an input capacitor equal to the output capacitor to accommodate the high impedance seen in a typical lab environment. Actual applications usually have much lower source impedance since the step-up regulator typically runs directly from a low-impedance battery. Often, the input capacitor can be reduced by 50% or more of the output capacitor value.

To prevent noise from coupling into the device, connect an additional 0.1µF ceramic capacitor from the IN pin to the GND pin. Place that capacitor within 5mm of the pins.

Setting the Maximum LED Current

The full-scale current through each LED can be set using SETI. When SETI is connected to IN, the full-scale LED current is set to the default value of 18mA. When SETI is connected to GND, the LED current is set to 0.5mA LED test mode. If SETI is connected with a resistor to GND, the full-scale LED current can be adjusted from 14mA to 25mA:

$$I_{LED(FS)} = 12mA + K \times \frac{0.75 \times V_{REF}}{R_{SETI}}$$

where K = 3851, and V_{REF} is the internal reference voltage.

PC Board Layout and Grounding

Careful PC board layout is very important for proper operation. Use the following guidelines for good PC board layout:

1) Minimize the area of high-current loops by placing the input capacitors, inductor, and output capacitors less than 0.2in (5mm) from the LX and GND pins. Connect these components with wide traces. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
2) Create islands for the analog ground and power ground. The analog ground island includes the exposed backside pad of the device, the REF bypass capacitor ground, and the SETI resistor ground. The power ground island includes the GND pin, the common ground for the current regulators (LDG), and the step-up regulator's input/output capacitor grounds. The analog ground and power ground islands are connected together at only one location using a short trace between the GND pin and the exposed backside pad underneath the device.
3) Maximize the width of the power ground traces to improve efficiency, and reduce output-voltage ripple and noise spikes.
4) Place the IN pin and REF pin bypass capacitors within 5mm to the device.
5) Minimize the size of LX node while keeping it wide and short to reduce radiated EMI.

Refer to the MAX1985 evaluation kit for an example of proper board layout.

Chip Information

TRANSISTOR COUNT: 3016

Ultra-High-Efficiency White LED Drivers

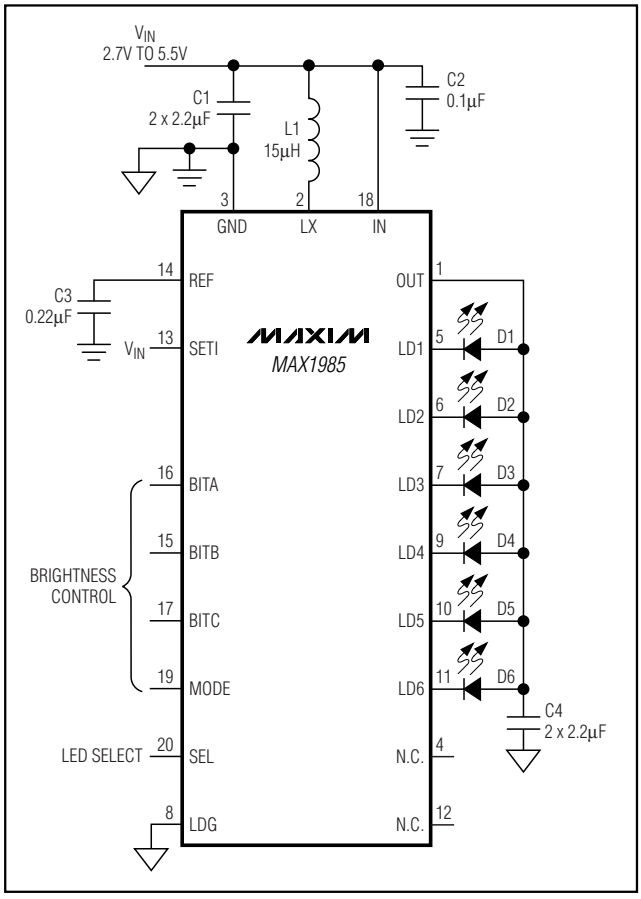


Figure 6. Standard Application Circuit of the MAX1985

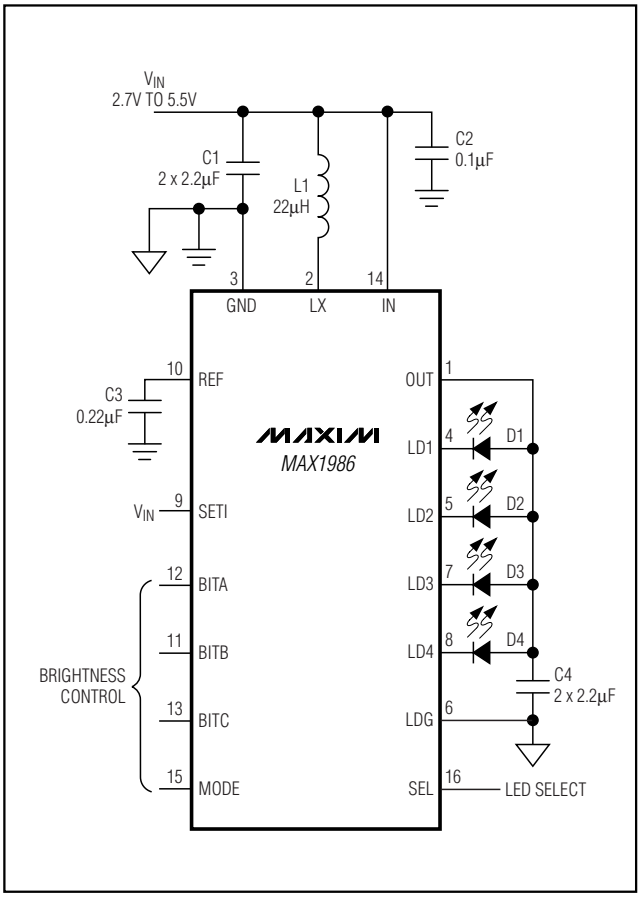
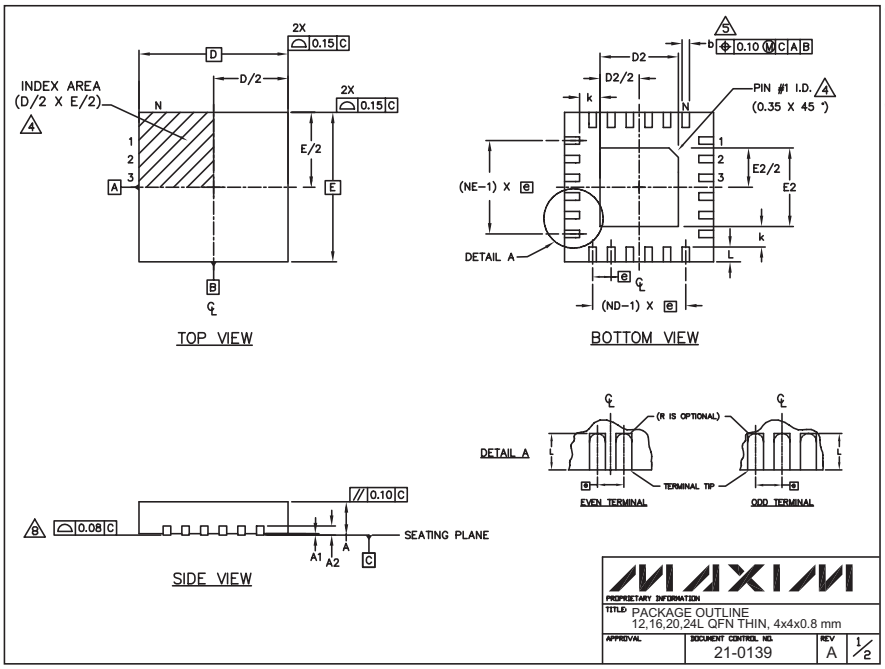


Figure 7. Standard Application Circuit of the MAX1986

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0139
REV
A
2/2

Mouser Electronics

Authorized Distributor

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