MAQ4123/MAQ4124/MAQ4125

Automotive AEC-Q100 Qualified Dual 3A Peak Low-Side MOSFET Driver

Bipolar/CMOS/DMOS Process

General Description

The MAQ4123/MAQ4124/MAQ4125 are a family of dual 3A buffer/MOSFET drivers intended for driving power MOSFETs, IGBTs and other heavy loads (capacitive, resistive or inductive) which require low-impedance, high peak currents and fast switching times. They are available in inverting, non-inverting and complementary configurations.

The MAQ4123/MAQ4124/MAQ4125 operate from a 4.5V to 20V supply, feature an output resistance of 2.3Ω, sink or source 3A of peak current, and switch an 1800pF capacitive load in 10ns with typical propagation delay times of 50ns.

The MAQ4123/MAQ4124/MAQ4125 feature TTL or CMOS compatible inputs with 400mV of hysteresis to provide noise immunity. The inputs can withstand negative voltage swings of 5V and are latch-up protected to withstand 200mA of reverse current.

The MAQ4123/MAQ4124/MAQ4125 are rated for the –40°C to +125°C operating temperature range, have been AEC-Q100 qualified for automotive applications, and are available in the ePad SOIC-8 package for improved power dissipation and thermal performance required by automotive applications.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

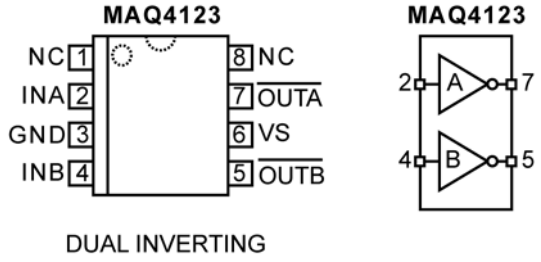
Features

- Automotive AEC-Q100 Qualified
- High ±3A peak output current
- Wide 4.5V to 20V supply voltage range
- Low 2.3Ω output resistance
- Matched rise and fall times
- Fast 10ns rise/fall times with 1800pF capacitive load
- Low propagation delay time of 50ns (typical)
- TTL/CMOS logic inputs independent of supply voltage
- Latch-up protected to 200mA reverse current
- Logic input withstands swing to –5V
- Low equivalent 6pF input capacitance
- Output voltage swings within 25mV of ground or VS
- Low supply current
  - 2.0mA with logic-1 input (maximum over temperature)
  - 300µA with logic-0 input (maximum over temperature)
- '426/7/8-, '1426/7/8-, '4426/7/8 industry standard pin out
- Inverting, non-inverting, and differential configurations
- –40°C to +125°C temperature range
- Exposed backside pad (ePad) packaging for improved power dissipation

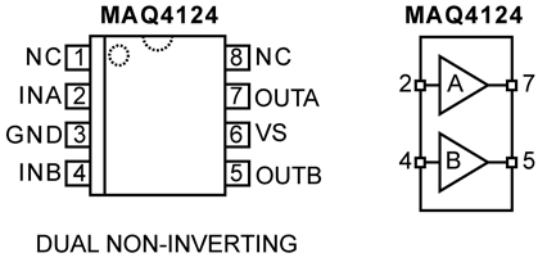
Ordering Information

Part Number	Configuration	Junction Temperature Range	Lead Finish	Package
MAQ4123YME	Dual Inverting	–40°C to +125°C	Pb-Free	ePad 8-Pin SOIC
MAQ4124YME	Dual Non-Inverting	–40°C to +125°C	Pb-Free	ePad 8-Pin SOIC
MAQ4125YME	Inverting + Non-Inverting	–40°C to +125°C	Pb-Free	ePad 8-Pin SOIC

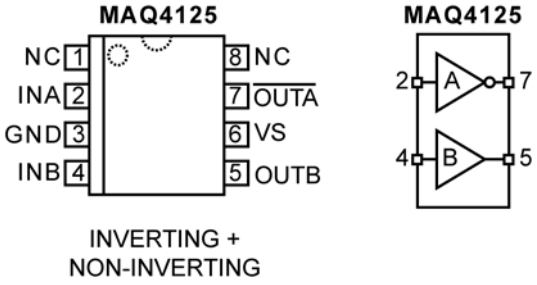
Pin Configuration



ePad SOIC-8 (ME)



ePad SOIC (ME)

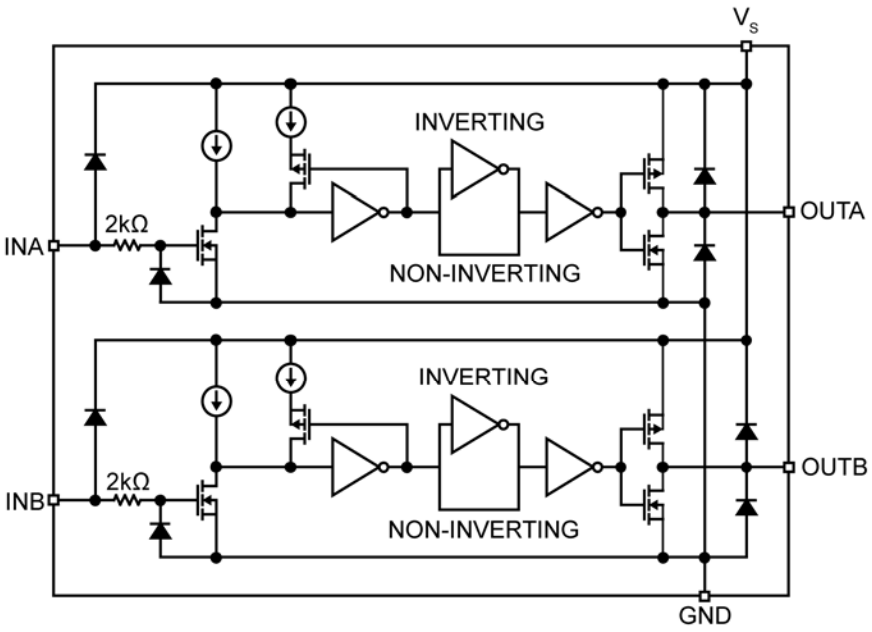


ePad SOIC-8 (ME)

Pin Description

Pin Number	Pin Name	Pin Function
1	NC	Not connected (may be left floating).
2	INA	Input. Control input for the OUTA driver.
3	GND	Ground. Return for both output drive sections and ground reference for both input signals.
4	INB	Input. Control input for the OUTB driver.
5	OUTB	Output Drive. OUTB high-current drive pin.
6	VS	Supply. +4.5V to +20V. Provides power to both driver outputs and internal control circuitry.
7	OUTA	Output Drive. OUTA high-current driver pin.
8	NC	Not connected (may be left floating).
ePad	EP	Exposed Pad (ePad). Must make a full connection to the GND plane to maximize thermal performance of the package.

Functional Diagram



INTEGRATED COMPONENT COUNT:

- 4 RESISTORS
- 4 CAPACITORS
- 52 TRANSISTORS

Absolute Maximum Ratings[1]

Supply Voltage (V_S)..... +24V
Input Voltage (V_{IN})..... V_S + 0.3V to GND – 5V
Maximum Junction Temperature (T_J)..... 150°C
Storage Temperature (Ts).....–65°C to 150°C
Lead Temperature (soldering, 10s)..... 260°C
ESD HBM Rating[3].....2kV
ESD MM Rating[3].....200V

Operating Ratings[2]

Supply Voltage (V_S)..... +4.5V to +20V
Junction Temperature (T_J) .....–40°C to +125°C
Package Thermal Resistance
ePad SOIC-8 (θ_{JA}) .....41°C/W
ePad SOIC-8(θ_{JC})……..……14.7°C/W

Electrical Characteristics[4]

4.5V ≤ V_S ≤ 20V; T_A = +25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Input voltage slew rate >2.5V/µs.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Input						
V_{IH}	Logic 1 Input Voltage		**2.4**	1.6		V
V_{IL}	Logic 0 Input Voltage			1.45	**0.8**	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	–1 **–10**		1 **10**	µA
Output						
V_{OH}	High Output Voltage	I_{OUT} = 100µA	**V_S – 0.025**			V
V_{OL}	Low Output Voltage	I_{OUT} = –100µA			**0.025**	V
R_O	Output Resistance HI State	I_{OUT} = 10mA, V_S = 20V		2.3	5	Ω
		I_{OUT} = 10mA, V_S = 20V			**8**	
	Output Resistance LO State	I_{OUT} = 10mA, V_S = 20V		2.2	5	Ω
		I_{OUT} = 10mA, V_S = 20V			**8**	
I_{PK}	Peak Output Current			3		A
I	Latch-Up Protection Withstand Reverse Current			>200		mA
Switching Time						
t_R	Rise Time	Test figure 1, C_L = 1800pF, V_S = 20V		11	35 **60**	ns
t_F	Fall Time	Test figure 1, C_L = 1800pF, V_S = 20V		11	35 **60**	ns
t_{D1}	Delay Time	Test figure 1, C_L = 1800pF, V_S = 20V		40	75 **100**	ns
t_{D2}	Delay Time	Test figure 1, C_L = 1800pF, V_S = 20V		60	75 **100**	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3.0V (both inputs)		0.75	1.5 **2.0**	mA
I_S	Power Supply Current	V_{IN} = 0.0V (both inputs)		0.05	0.25 **0.30**	mA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.

Test Circuit

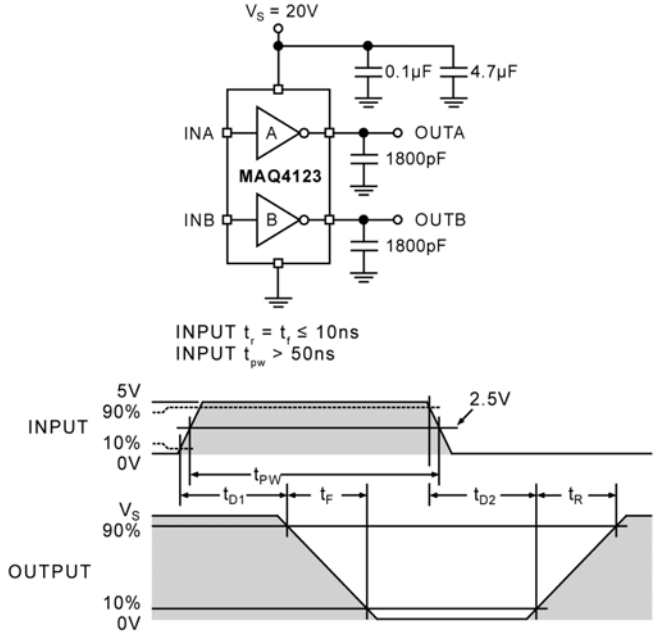


Figure 1a. Inverting Driver Switching Time

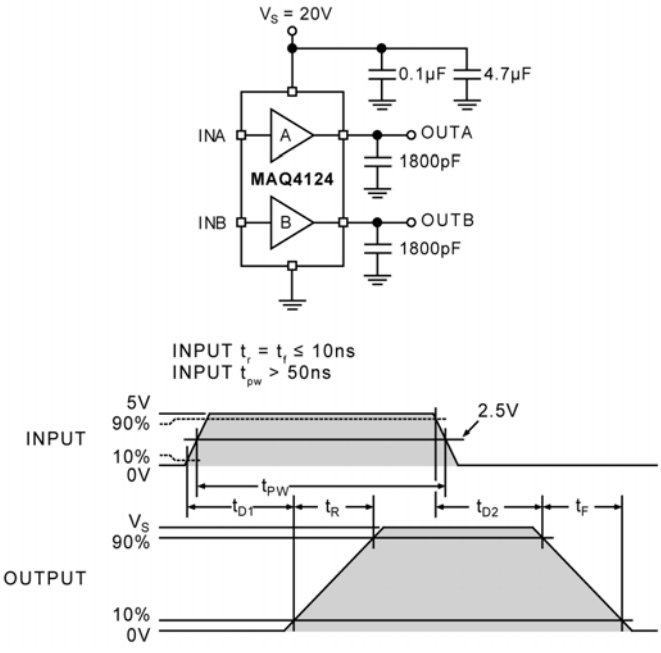
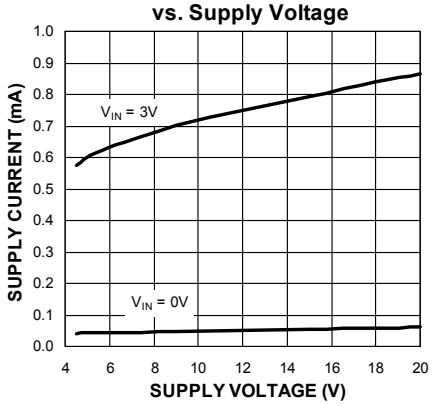


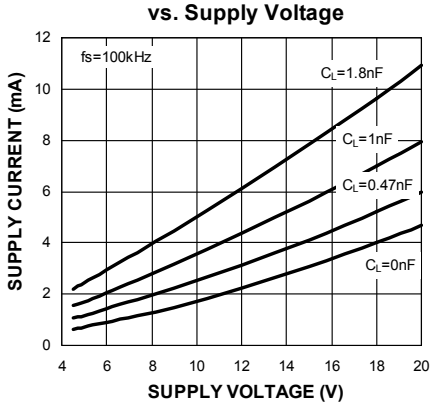
Figure 1b. Non-Inverting Driver Switching Time

Typical Characteristics

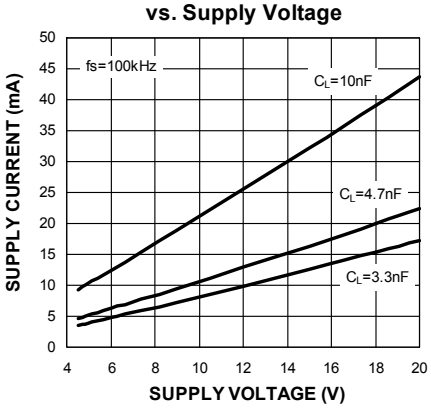
Supply Current (I_S) vs. Supply Voltage



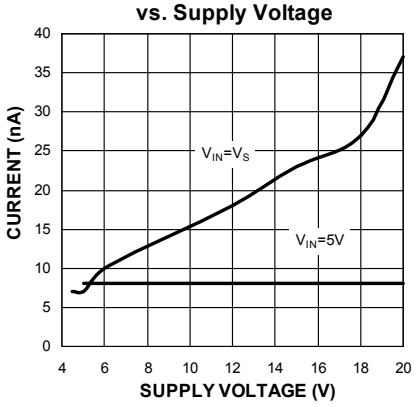
Supply Current (I_S) vs. Supply Voltage



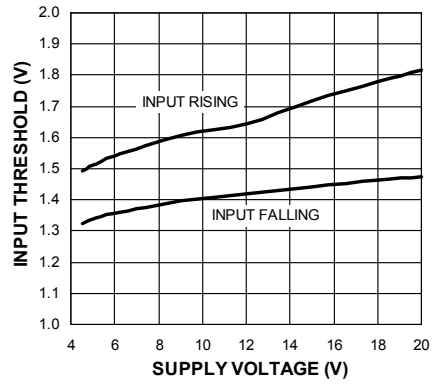
Supply Current (I_S) vs. Supply Voltage



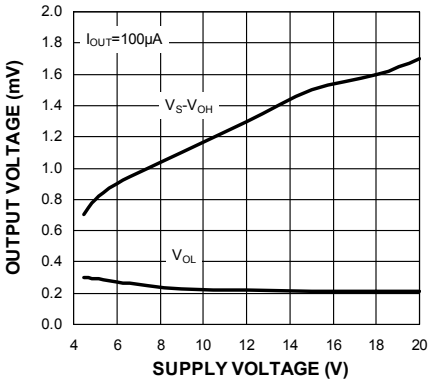
Input Pin Current (I_{IN}) vs. Supply Voltage



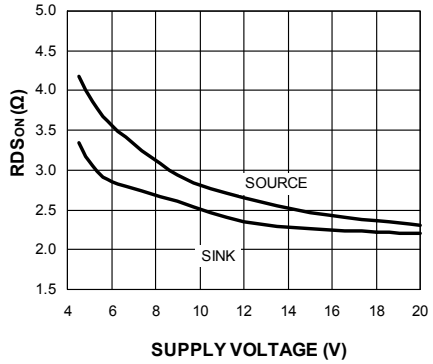
Input Pin Threshold Voltage vs. Supply Voltage



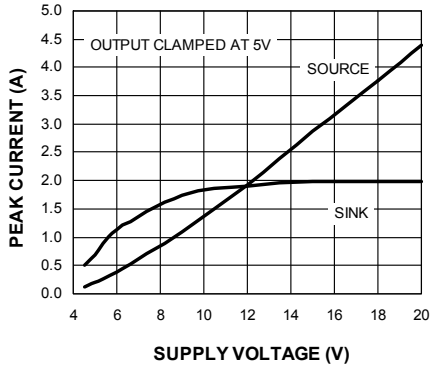
Output Voltage vs. Supply Voltage



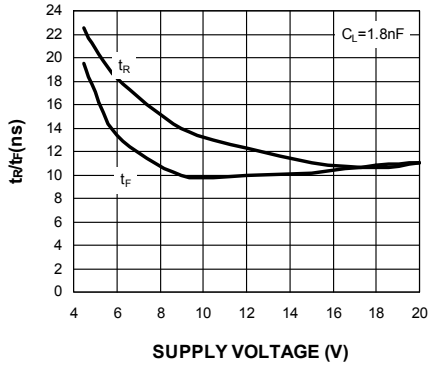
Output Resistance vs. Supply Voltage



Peak Output Current vs. Supply Voltage

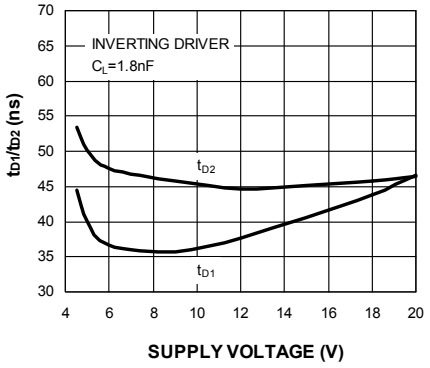


Output Rise/Fall Time vs. Supply Voltage

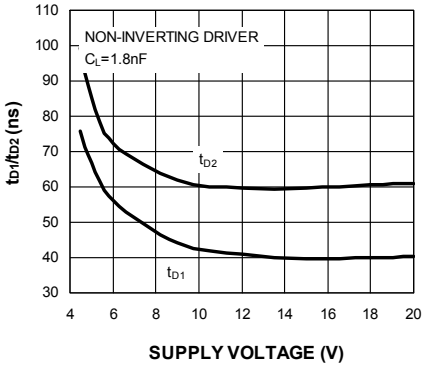


Typical Characteristics (Continued)

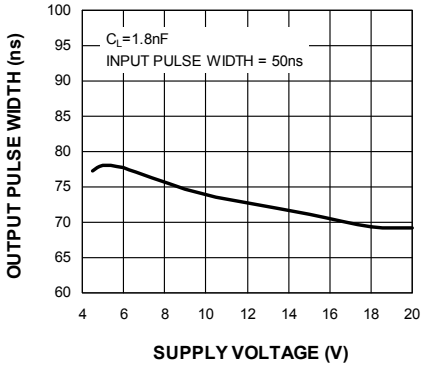
Propagation Delay Time vs. Supply Voltage



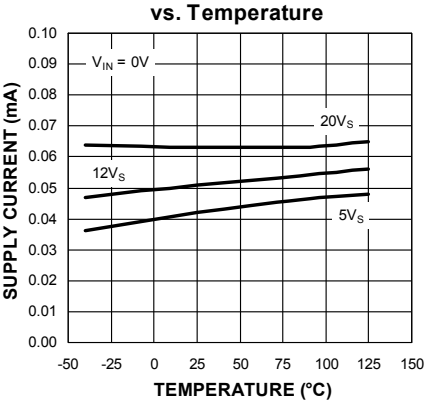
Propagation Delay Time vs. Supply Voltage



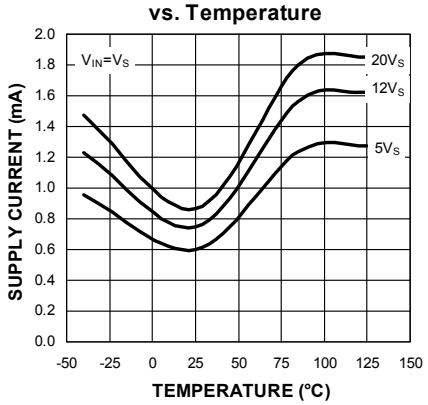
Pulse Stretching vs. Supply Voltage



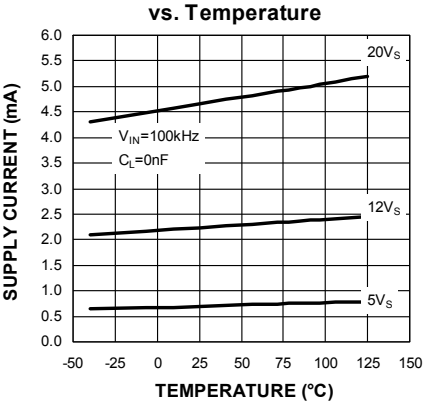
Supply Current (I_S) vs. Temperature



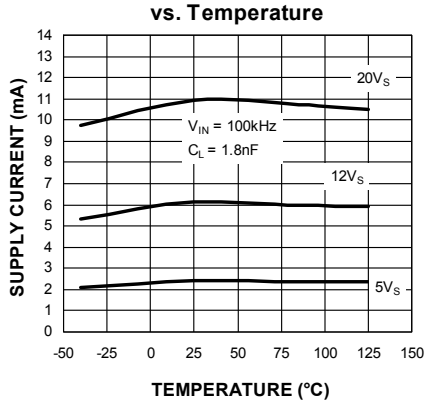
Supply Current (I_S) vs. Temperature



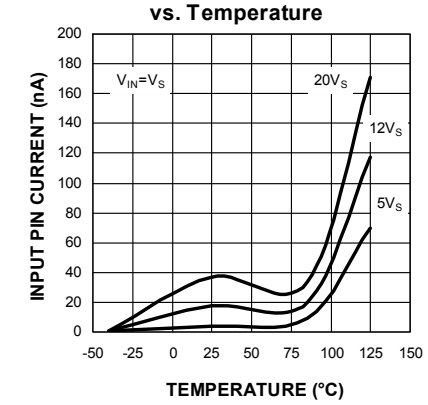
Supply Current (I_S) vs. Temperature



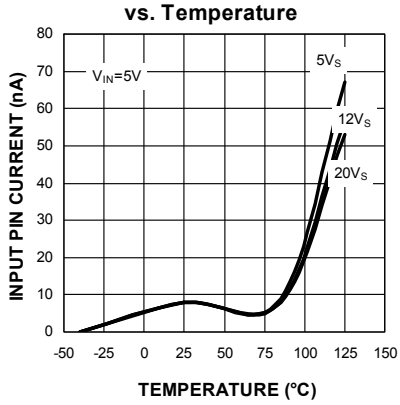
Supply Current (I_S) vs. Temperature



Input Pin Current (I_{IN}) vs. Temperature

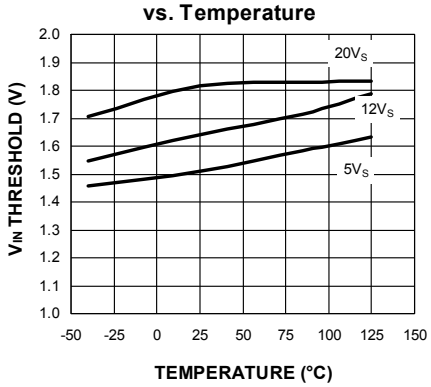


Input Pin Current (I_{IN}) vs. Temperature

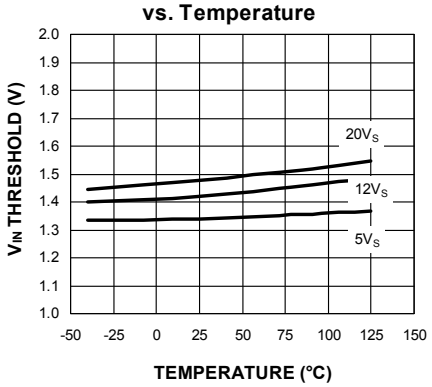


Typical Characteristics (Continued)

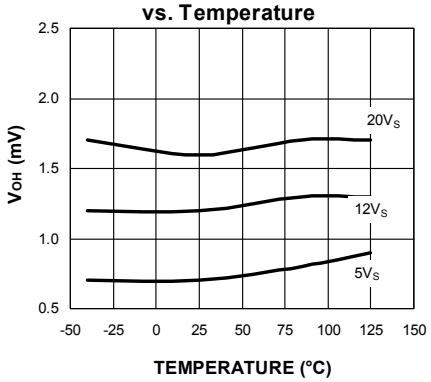
Input Pin Rising Threshold vs. Temperature



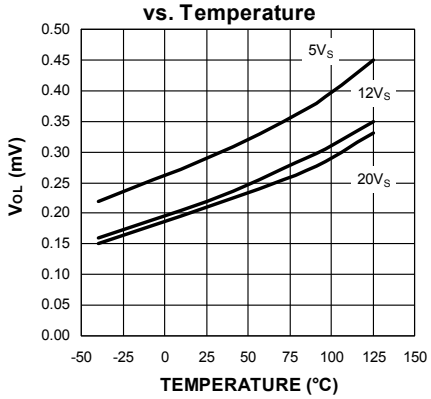
Input Pin Falling Threshold vs. Temperature



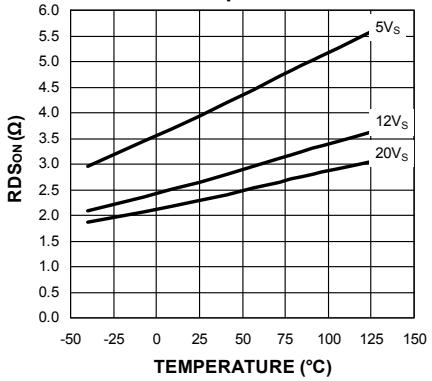
V_{OH} vs. Temperature



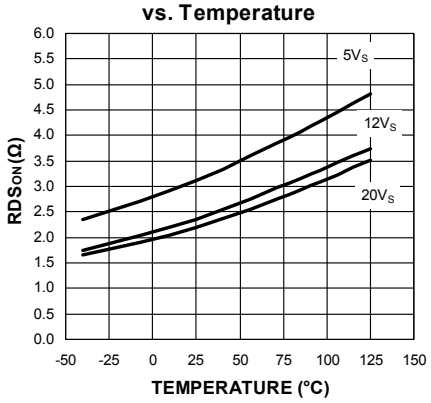
V_{OL} vs. Temperature



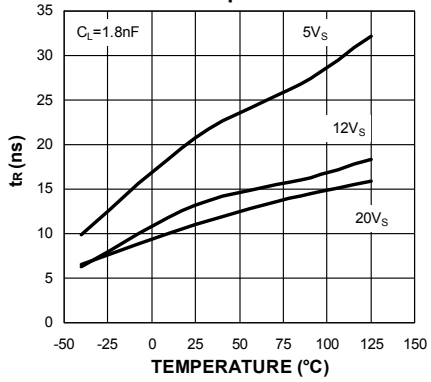
Output Source Resistance vs. Temperature



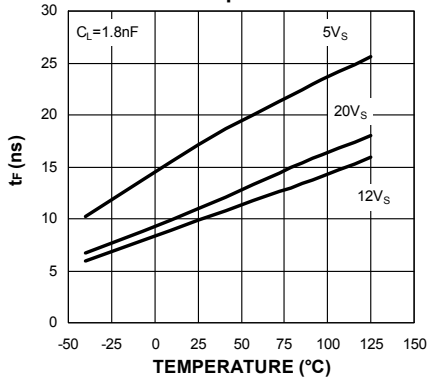
Output Sink Resistance vs. Temperature



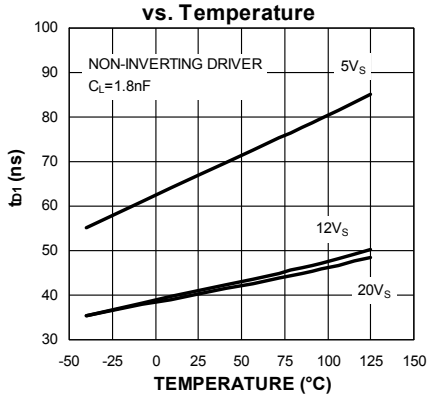
Output Rise Time vs. Temperature



Output Fall Time vs. Temperature

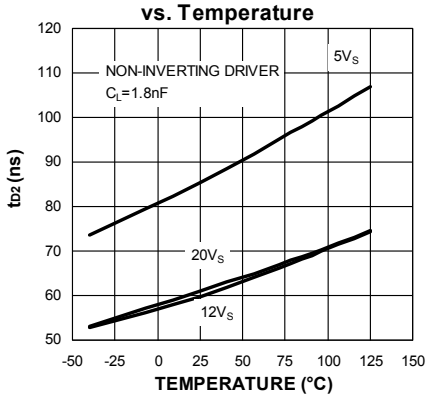


Output t_{D1} Time vs. Temperature

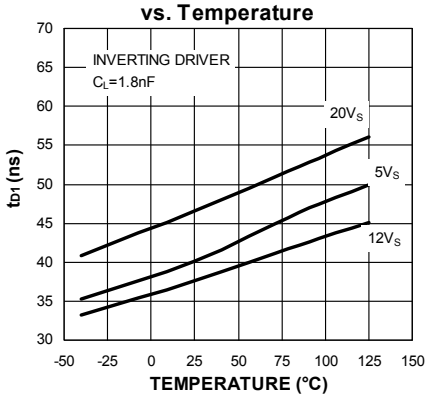


Typical Characteristics (Continued)

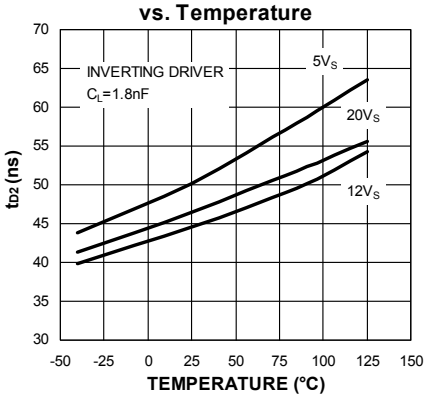
Output t_{D2} Time vs. Temperature



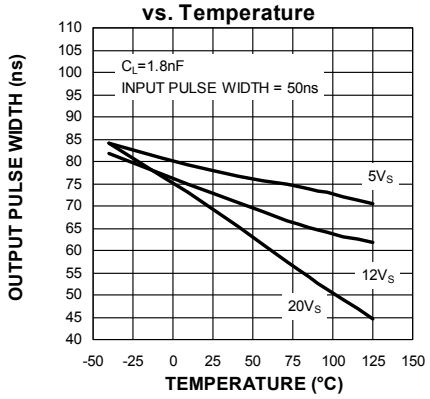
Output t_{D1} Time vs. Temperature



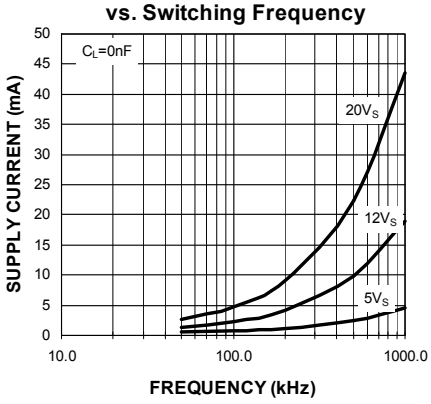
Output t_{D2} Time vs. Temperature



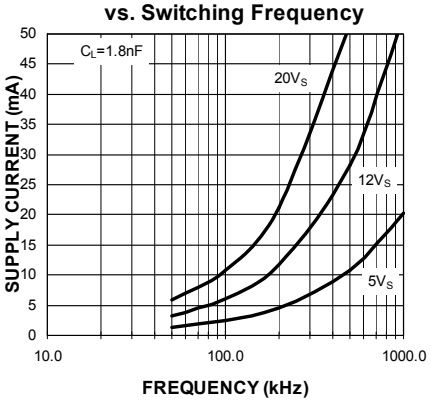
Pulse Stretching (V_{OUT1}) vs. Temperature



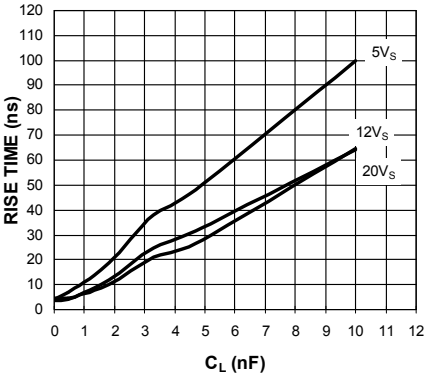
Supply Current (I_S) vs. Switching Frequency



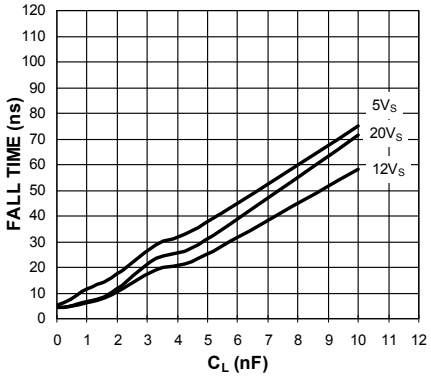
Supply Current (I_S) vs. Switching Frequency



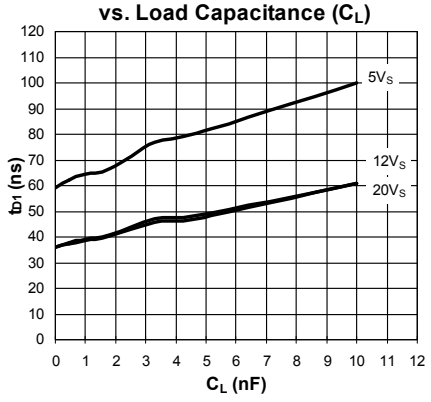
Output Rise Time vs. Load Capacitance (C_L)



Output Fall Time vs. Load Capacitance (C_L)

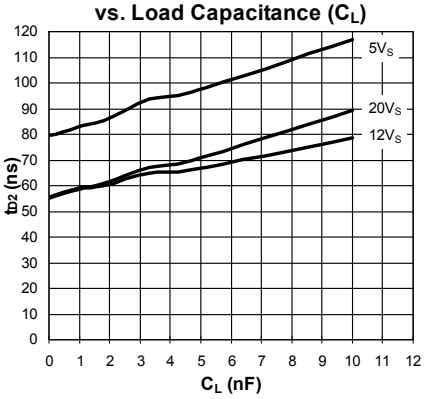


t_{D1} Delay vs. Load Capacitance (C_L)

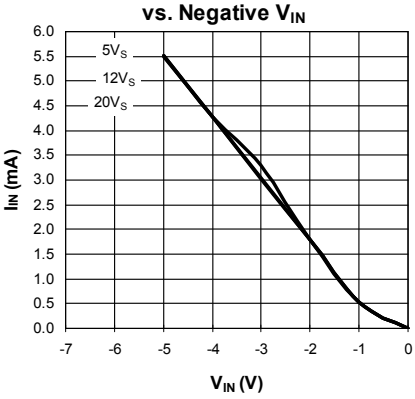


Typical Characteristics (Continued)

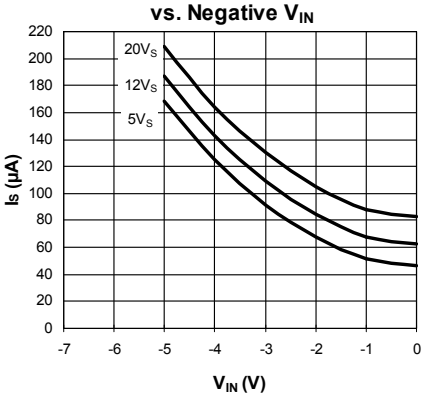
t_{D2} Delay vs. Load Capacitance (C_L)



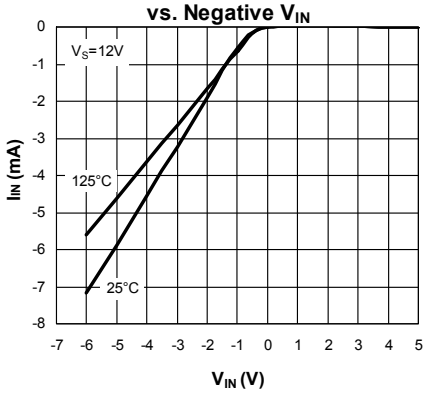
Input Pin Current (I_{IN}) vs. Negative V_{IN}



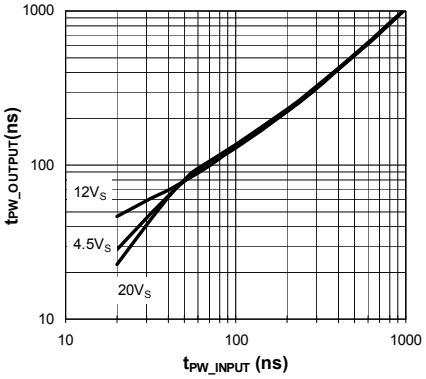
Supply Current (I_S) vs. Negative V_{IN}



Negative I_{IN} vs. Negative V_{IN}



Input Pulse Width vs. Output Pulse Width



Application Information

The MAQ4123/24/25 drivers have been specifically constructed to operate reliably under any practical circumstances, the following details of usage provide for better operation of the device.

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000pF from 0 to 15 volts in 20ns requires a constant current of 1.5A. In practice, the charging current is not constant, and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply, as seen by the driver, must have very low impedance.

As a practical matter, this means the power supply bus decoupling capacitance must be much larger than the driver output load capacitance to achieve optimum driving speed. Additionally, the bypassing capacitors must have very low internal inductance and resistance at all frequencies of interest. High quality X5R or X7R ceramic capacitors meet these requirements. Two capacitors may be used to meet the decoupling requirements. A larger ceramic capacitor in the 1µF to 4.7µF range and a 0.1µF capacitor may be used, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what the designer is trying to accomplish. For optimum results, the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large Δ I) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. Good bypassing practice is essential to proper operation of high speed driver ICs.

Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load on. Eventually (except in rare circumstances) it is also necessary to turn the load OFF. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

The ePad package has an exposed pad under the package. It's important for good thermal performance that this pad is connected to a ground plane.

Best practice for a ground path is a well laid out ground plane. However, this is not always practical, though a poorly-laid out ground plane can be worse than none. Attention to the paths taken by return currents, even in a ground plane, is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it, is most sensitive to resistance or inductance, and ground current from the load is what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: the inductance of a 2cm long land, 1.59mm (0.062") wide on a PCB with no ground plane is approximately 45nH. Assuming a di/dt of 0.3A/ns (which will allow a current of 3A to flow after 10ns, and is thus slightly slow for these purposes) a voltage of 13.5V will develop along this land in response to our postulated Δi. For a 1cm land, (approximately 15nH) 4.5V is developed. Either way, users employing TTL-level input signals to the driver will find that the response of a driver that has been seriously degraded by a common ground path for input to and output from the driver of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59mm (0.062") land of 2oz. Copper carrying 3A will be about 4mV/cm (10mV/in) at DC, and the resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver's input voltage (in order to turn the driver's load off) is countered by the voltage developed on the common ground path as the driver attempts to do what it was supposed to. It takes very little common ground path, under these circumstances, to alter circuit operation drastically.

Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a wider variety of connectors. The second wire of the twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this will not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e., minimize sharp bends, or narrowing in the land, as these will cause ringing. For a rough estimate, on a 1.59mm (0.062") thick G-10 PCB a pair of opposing lands each 2.36mm (0.093") wide translates to a characteristic impedance of about 50Ω; half that width suffices on a 0.787mm (0.031") thick board. For accurate impedance matching with a MAQ4123/24/25 driver, on a 1.59mm (0.062") board a land width of 42.75mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is obviously impractical under most circumstances. Generally the tradeoff point between lands and wires comes when lands narrower than 3.18mm (0.125") would be required on a 1.59mm (0.062") board.

To obtain minimum delay between the driver and the load, it is considered best to locate the driver as close as possible to the load (using adequate bypassing). Using matching transformers at both ends of a piece of coax, or several matched lengths of coax between the driver and the load, works in theory, but is not optimum.

Driving at Controlled Rates

Occasionally, there are situations where a controlled rise or fall time (which may be considerably longer than the normal rise or fall time of the driver's output) is desired for a load. In such cases, it is still prudent to employ best possible practice in terms of bypassing, grounding and PCB layout, and then reduce the switching speed of the load (NOT the driver) by adding a non-inductive series resistor of appropriate value between the output of the driver and the load. For situations where only the rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the Schmitt-trigger action of the driver's input it is not possible to slow the rate of rise (or fall) of the driver's input signal to achieve slowing of the output.

Input Stage

The input stage of the MAQ4123/24/25 consists of a single-MOSFET Class A stage with an input capacitance of ~6pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a current source. Thus, the quiescent current drawn by the driver varies, depending upon the logic state of the input.

Following the input stage, there is a buffer stage which provides hysteresis for the input. This prevents oscillations when slowly-changing input signals are used or when noise is present on the input. Input voltage switching threshold is approximately 1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The input protection circuitry of the MAQ4123/24/25, in addition to providing ESD protection, also works to prevent latch-up or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled OFF and ON. The MAQ4123/24/25 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC.

Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the drivers. TD2, for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that line spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cxxx have outputs which can only source or sink a few milliamps of current. Even shorting the output of the device to ground or VCC may not damage the device. CMOS drivers, on the other hand, are intended to source or sink several Amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain.

The Supply Current vs. Frequency and Supply Current vs. Load characteristic curves furnished with this data sheet aid in estimating power dissipation in the driver. Operating frequency, power supply voltage, and load all affect power dissipation.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin ePad SOIC package, from the datasheet, is 41°C/W. In a 25°C ambient, then, using a maximum junction temperature of 125°C, this package will dissipate 2.4W.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending upon whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load

R_O = the output resistance of the driver when the output is high, at the power supply voltage used (see characteristic curves)

D = fraction of time the load is conducting (duty cycle)

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = f\ C\ (V_S)^2$$

where:

f = Operating Frequency

C = Load Capacitance

V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending upon how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

$$P_{L2} = I V_D (1 – D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L:

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends upon whether the input is high or low. A low input will result in a maximum supply current of ≤0.3mA (per driver); logic high will result in a maximum supply current of ≤1mA (per driver). Quiescent power can therefore be found from:

$$P_Q = V_S [D I_H + (1 – D) I_L]$$

where:

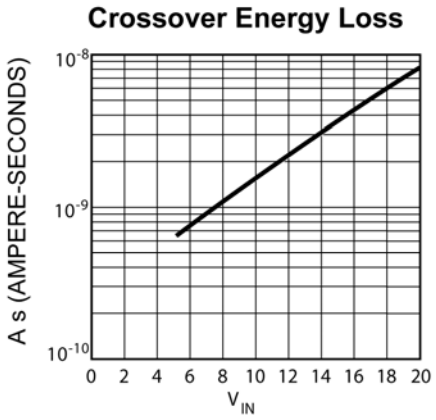
I_H = quiescent current with input high
I_L = quiescent current with input low
D = fraction of time input is high (duty cycle)
V_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = f V_S (A \times s)$$

where (A × s) is a time-current factor derived from Figure 2.



NOTE: THE VALUES ON THIS GRAPH REPRESENT THE LOSS SEEN BY BOTH DRIVERS IN A PACKAGE DURING ONE COMPLETE CYCLE. FOR A SINGLE DRIVER DIVIDE THE STATED VALUES BY 2. FOR A SINGLE TRANSITION OF A SINGLE DRIVER, DIVIDE THE STATED VALUE BY 4.

Figure 2. Crossover Energy Loss

Total power (P_D) then, as previously described is just:

$$P_D = P_L + P_Q + P_T$$

Examples show the relative magnitude for each term:

EXAMPLE 1: A MAQ4123 operating on a 12V supply driving two capacitive loads of 3000pF each, operating at 250kHz, with a duty cycle of 50%, in a maximum ambient of 60°C.

First calculate capacitive load power loss:

$$P_L = f \times C \times (V_S)^2$$

$$P_L = 250{,}000 \times (3 \times 10^{-9} + 3 \times 10^{-9}) \times 12^2$$
$$= 0.216W$$

Then transition power loss:

$$P_T = f \times V_S \times (A \times s) = 250{,}000 \times 12 \times 2.2 \times 10^{-9}$$
$$= 0.007W$$

Then quiescent power loss:

$$P_Q = V_S \times [D \times I_H + (1 - D) \times I_L]$$
$$= 12 \times [(0.5 \times 0.002) + (0.5 \times 0.0003)]$$
$$= 0.014W$$

Total power dissipation, then, is:

$$P_D = 0.216 + 0.007 + 0.014$$
$$= 0.237W$$

Given that the ePad SOIC package has a θ_{JA} of 41°C/W, this will result in the junction running at:

0.237W x 41°C/W = 10°C above ambient, which, given a maximum ambient temperature of 60°C, will result in a maximum junction temperature of 70°C.

EXAMPLE 2: A MAQ4124 operating on a 15V input, with one driver switching a 50Ω resistive load at 1MHz at a 67% duty cycle. The other driver is not switching and its input is grounded. The maximum ambient temperature is 40°C:

$$P_L = I^2 \times R_O \times D$$

First, I_O must be determined:

$$I_O = V_S / (R_O + R_{LOAD})$$

Given R_O from the characteristic curves then,

$$I_O = 15 / (3.3 + 50)$$
$$I_O = 0.281A$$

and:

$$P_L = (0.281)^2 \times 3.3 \times 0.67$$
$$= 0.175W$$

$$P_T = f \times V_S \times (A \times s)/2$$
(because only one side is operating)
$$= (1{,}000{,}000 \times 15 \times 3.3 \times 10^{-9}) / 2$$
$$= 0.025 W$$

and:

$$P_Q = 15 \times [(0.67 \times 0.001) + (0.33 \times 0.00015) + (1 \times 0.00015)] = 0.013W$$

then:

$$P_D = 0.175 + 0.025 + 0.013$$
$$= 0.213W$$

For θ_{JA}= 41°C/W, the junction temperature at 40°C ambient is:

$$(0.213W \times 41°C/W) + 40°C = 49°C$$

The actual junction temperature will be somewhat lower than calculated because the maximum $R_{DS(on)}$ value used was taken at a T_J of 125°C and the $R_{DS(on)}$ at T_J = 52.8°C lower.

Definitions

C_L = Load capacitance in farads.

D = Duty cycle expressed as the fraction of time the input to the driver is high.

f = Operating frequency of the driver in Hz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in watts.

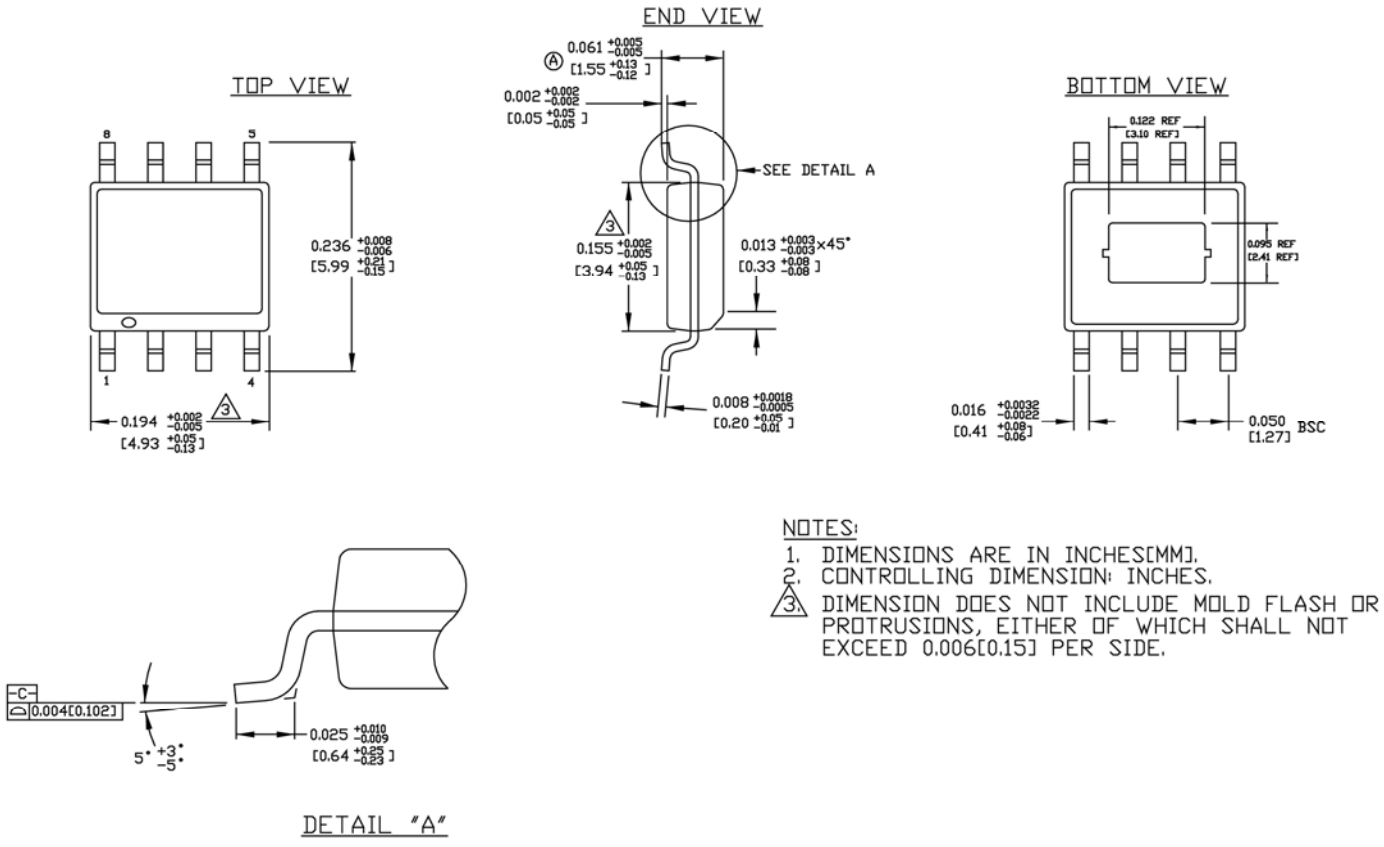
P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts.

NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in the graph on the following page in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency) to find watts.

R_O = Output resistance of a driver in Ωs.

V_S = Power supply voltage to the IC in volts.

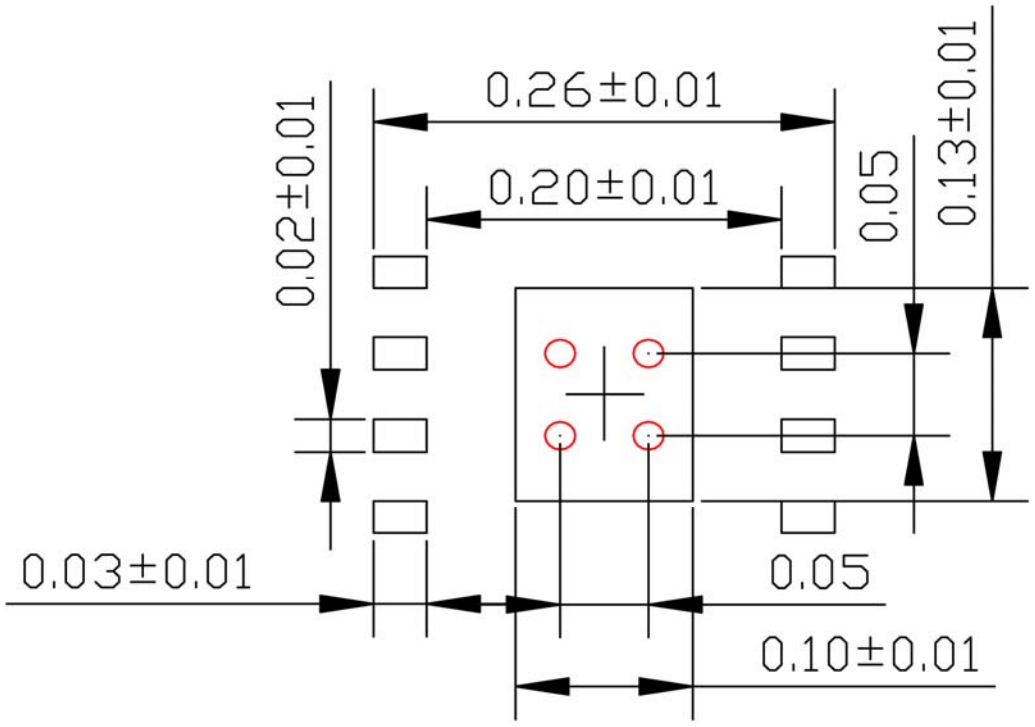
Package Information



8-Pin ePad SOIC (ME)

Recommended Landing Pattern

LP # SOICNEP-8LD-LP-1
All units are in inches
Tolerance ± 0.05 if not noted



8-Pin ePad SOIC (ME)

Red circle indicates Thermal Via. Size should be .015 – 0.17 inches in diameter and it should be connected to GND plane for maximum thermal performance.

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