UHF ASK/FSK Receiver

Description

The T5743N is a multi-chip PLL receiver device supplied in an SO20 package. It has been especially developed for the demands of RF low-cost data transmission systems with data rates from 1 kBaud to 10 kBaud in Manchester or Bi-phase code. The receiver is well suited to operate with Atmels PLL RF transmitter U2741B. Its main applications are in the areas of telemetering, security technology and keyless-entry systems. It can be used in the frequency receiving range of f_0 = 300 MHz to 450 MHz for ASK or FSK data transmission. All the statements made below refer to 433.92 MHz and 315 MHz applications.

Features

- 5 V to 20 V automotive compatible data interface
- Data clock available for Manchester- and Bi-phase-coded signals
- IC condition indicator, sleep or active mode
- Minimal external circuitry requirements, no RF components on the PC board except matching to the receiver antenna
- High sensitivity, especially at low data rates
- Sensitivity reduction possible even while receiving
- Fully integrated VCO
- Low power consumption due to configurable self polling with a programmable timeframe check
- SO20 package
- Supply voltage 4.5 V to 5.5 V, operating temperature range –40°C to 105°C
- Single-ended RF input for easy adaptation to λ/4 antenna or printed antenna on PCB
- Low-cost solution due to high integration level
- ESD protection according to MIL-STD. 883 (4KV HBM)
- High image frequency suppression due to 1 MHz IF in conjunction with a SAW front-end filter. Up to 40 dB is thereby achievable with state-of-the-art SAWs.
- Communication to µC possible via a single, bi-directional data line
- Power management (polling) is also possible by means of a separate pin via the µC
- Programmable digital noise suppresion
- Receiving bandwidth B_{IF} = 600 kHz

System Block Diagram

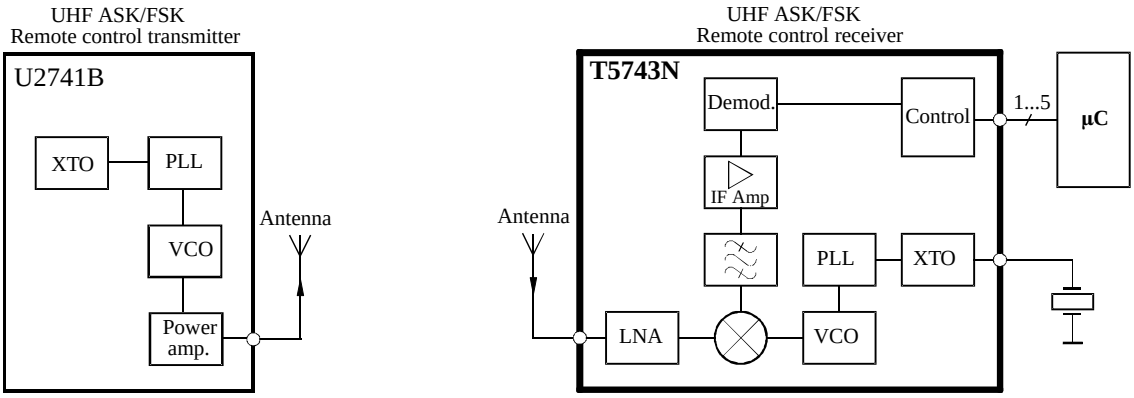


Figure 1. System block diagram

Ordering Information

Extended Type Number	Package	Remarks
T5743N-TG	SO20	Tube
T5743N-TGQ	SO20	Taped and reeled

Pin Description

Pin	Symbol	Function
1	SENS	Sensitivity-control resistor
2	IC_ ACTIVE	IC condition indicator Low = sleep mode High = active mode
3	CDEM	Lower cut-off frequency data filter
4	AVCC	Analog power supply
5	TEST	Test pin, during operation at GND
6	AGND	Analog ground
7	MIXVCC	Power supply mixer
8	LNAGND	High-frequency ground LNA and mixer
9	LNA_IN	RF input
10	n.c.	Not connected
11	LFVCC	Power supply VCO
12	LF	Loop filter
13	LFGND	Ground VCO
14	XTO	Crystal oscillator
15	DVCC	Digital power supply
16	MODE	Selecting 433.92 MHz /315 MHz Low: f_{XT0} = 4.90625 MHz (USA) High: f_{XT0} = 6.76438 MHz (Europe)
17	DATA_ CLK	Bit clock of data stream
18	DGND	Digital ground
19	POLL-ING/_ON	Selects polling or rceiving mode Low: receiving mode High: polling mode
20	DATA	Data output / configuration input

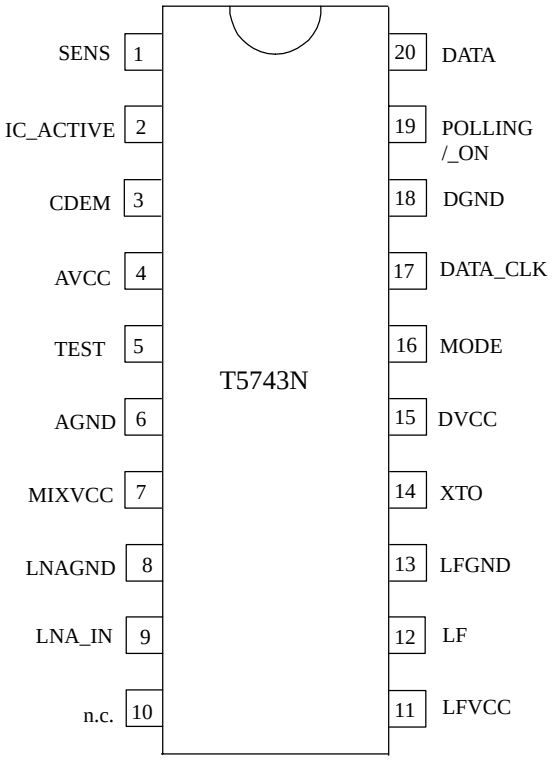


Figure 2. Pinning SO20

Block Diagram

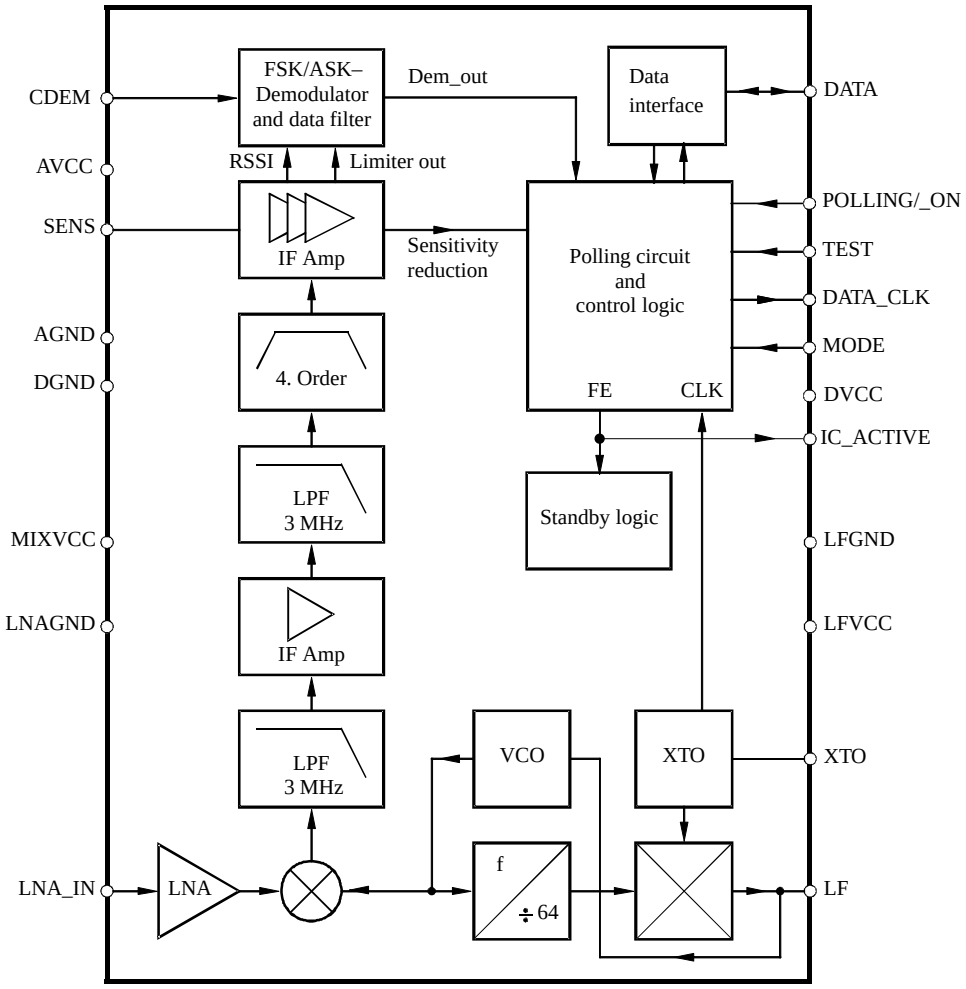


Figure 3. Block diagram

RF Front End

The RF front end of the receiver is a heterodyne configuration that converts the input signal into a 1-MHz IF signal. According to figure 3, the front end consists of an LNA (low noise amplifier), LO (local oscillator), a mixer and an RF amplifier.

The LO generates the carrier frequency for the mixer via a PLL synthesizer. The XTO (crystal oscillator) generates the reference frequency f_{XTO}. The VCO (voltage-controlled oscillator) generates the drive voltage frequency f_{LO} for the mixer. f_{LO} is dependent on the voltage at Pin LF. f_{LO} is divided by factor 64. The divided frequency is compared to f_{XTO} by the phase frequency detector. The current output of the phase frequency detector is connected to a passive loop filter and thereby generates the control voltage V_{LF} for the VCO. By means of that configuration V_{LF} is controlled in a way that $f_{LO}/64$ is equal to f_{XTO}. If f_{LO} is determined, f_{XTO} can be calculated using the following formula: $f_{XTO} = f_{LO}/64$

The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal. According to figure 4, the crystal should be connected to GND via a capacitor CL. The value of that capacitor is recommended by the crystal supplier. The value of CL should be optimized for the individual board layout to achieve the exact value of f_{XTO} and hereby of f_{LO}. When designing the system in terms of receiving bandwidth, the accuracy of the crystal and the XTO must be considered.

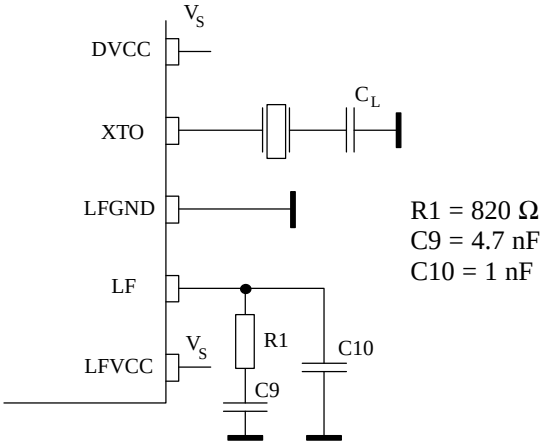


Figure 4. PLL peripherals

The passive loop filter connected to Pin LF is designed for a loop bandwidth of BLoop = 100 kHz. This value for BLoop exhibits the best possible noise performance of the LO. Figure 4 shows the appropriate loop filter components to achieve the desired loop bandwidth. If the filter components are changed for any reason please notify that the maximum capacitive load at Pin LF is limited. If the capacitive load is exceeded, a bit check may no longer be possible since f_{LO} cannot settle in time before the bit check starts to evaluate the incoming data stream. Self polling does therefore also not work in that case.

f_{LO} is determined by the RF input frequency f_{RF} and the IF frequency f_{IF} using the following formula:

$$f_{LO} = f_{RF} - f_{IF}$$

To determine f_{LO}, the construction of the IF filter must be considered at this point. The nominal IF frequency is f_{IF} = 1 MHz. To achieve a good accuracy of the filter's corner frequencies, the filter is tuned by the crystal frequency f_{XTO}. This means that there is a fixed relation between f_{IF} and f_{LO}. This relation is dependent on the logic level at Pin MODE.

This is described by the following formulas:

$$\text{MODE} = 0\ (\text{USA}): \quad f_{IF} = \frac{f_{LO}}{314}$$

$$\text{MODE} = 1\ (\text{Europe}): \quad f_{IF} = \frac{f_{LO}}{432.92}$$

The relation is designed to achieve the nominal IF frequency of f_{IF} = 1 MHz for most applications. For applications where f_{RF} = 315 MHz, MODE must be set to '0'. In the case of f_{RF} = 433.92 MHz, MODE must be set to '1'. For other RF frequencies, f_{IF} is not equal to 1 MHz. f_{IF} is then dependent on the logical level at Pin MODE and on f_{RF}. Table 1 summarizes the different conditions.

The RF input either from an antenna or from a generator must be transformed to the RF input Pin LNA_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances also influence the input matching. The RF receiver T5743N exhibits its highest sensitivity at the best signal-to-noise ratio in the LNA. Hence, noise matching is the best choice for designing the transformation network.

A good practice when designing the network is to start with power matching. From that starting point, the values of the components can be varied to some extent to achieve the best sensitivity.

If a SAW is implemented into the input network a mirror frequency suppression of ΔP_{Ref} = 40 dB can be achieved. There are SAWs available that exhibit a notch at Δf = 2 MHz. These SAWs work best for an intermediate frequency of f_{IF} = 1 MHz. The selectivity of the receiver is also improved by using a SAW. In typical automotive applications, a SAW is used.

Figure 5 shows a typical input matching network, for f_{RF} = 315 MHz and f_{RF} = 433.92 MHz using a SAW. Figure 6 illustrates an according input matching to 50 Ω without a SAW. The input matching networks shown in figure 6 are the reference networks for the parameters given in the electrical characteristics.

Table 1 Calculation of LO and IF frequency

Conditions	Local Oscillator Frequency	Intermediate Frequency
f_{RF} = 315 MHz, MODE = 0	f_{LO} = 314 MHz	f_{IF} = 1 MHz
f_{RF} = 433.92 MHz, MODE = 1	f_{LO} = 432.92 MHz	f_{IF} = 1 MHz
300 MHz < f_{RF} < 365 MHz, MODE = 0	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{314}}$	$f_{IF} = \frac{f_{LO}}{314}$
365 MHz < f_{RF} < 450 MHz, MODE = 1	$f_{LO} = \frac{f_{RF}}{1 + \frac{1}{432.92}}$	$f_{IF} = \frac{f_{LO}}{432.92}$

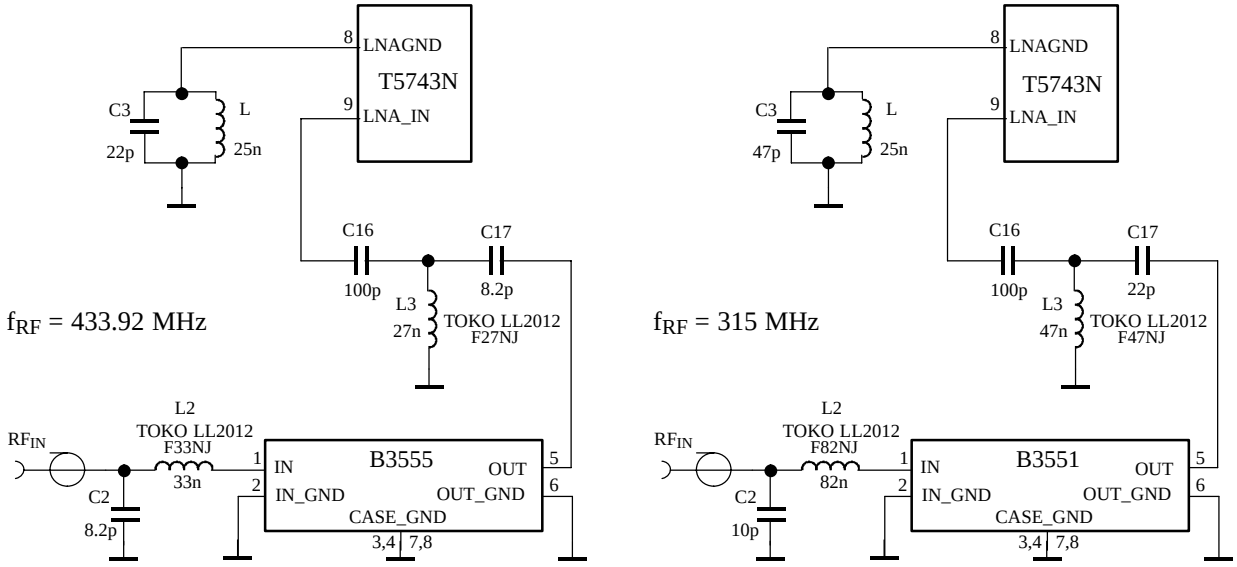


Figure 5. Input matching network with SAW filter

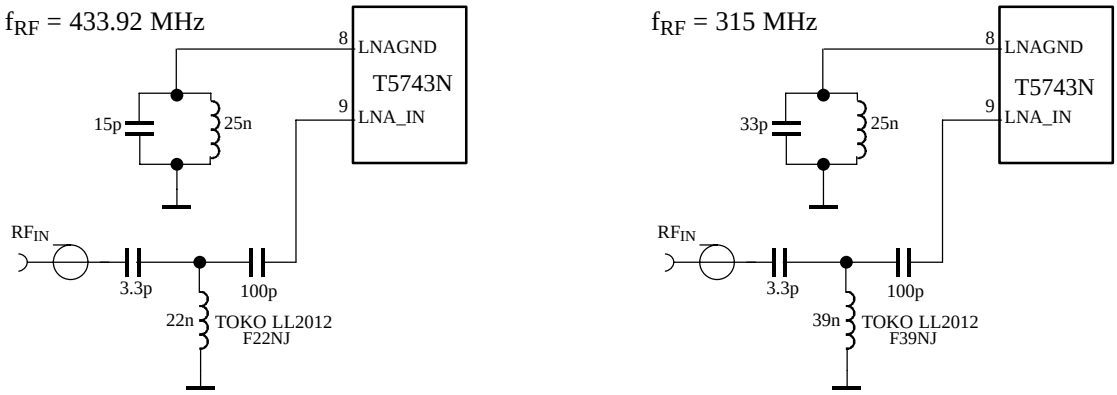


Figure 6. Input matching network without SAW filter

Please notify that for all coupling conditions (see figures 5 and 6), the bond wire inductivity of the LNA ground is compensated. C3 forms a series resonance circuit together with the bond wire. L = 25 nH is a feed inductor to establish a DC path. Its value is not critical but must be large enough not to detune the series resonance circuit. For cost reduction this inductor can be easily printed on the PCB. This configuration improves the sensitivity of the receiver by about 1 dB to 2 dB.

Analog Signal Processing

IF Amplifier

The signals coming from the RF front end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is f_{IF} = 1 MHz for applications where f_{RF} = 315 MHz or f_{RF} = 433.92 MHz is used. For other RF input frequencies refer to table 1 to determine the center frequency.

The receiver T5743N employs an IF bandwidth of B_{IF} = 600 kHz and can be used together with the U2741B in FSK and ASK mode.

RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is DR_{RSSI} = 60 dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is about 60 dB higher compared to the RF input signal at full sensitivity.

In FSK mode the S/N ratio is not affected by the dynamic range of the RSSI amplifier.

The output voltage of the RSSI amplifier is internally compared to a threshold voltage V_{Th_red}. V_{Th_red} is determined by the value of the external resistor R_{Sens}. R_{Sens} is connected between Pin SENS and GND or V_S. The output of the comparator is fed into the digital control logic. By this means it is possible to operate the receiver at a lower sensitivity.

If R_{Sens} is connected to GND, the receiver operates at full sensitivity.

If R_{Sens} is connected to V_S, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of R_{Sens}, the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in figure 6 and exhibits the best possible sensitivity.

R_{Sens} can be connected to V_S or GND via a µC. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at Pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to figure 7 is issued at Pin DATA to indicate that the receiver is still active (see also figure 34).

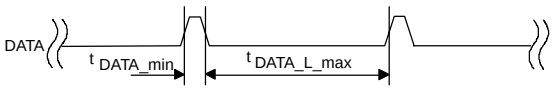


Figure 7. Steady L state limited DATA output pattern

FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via the bit ASK/_FSK in the OPMODE register. Logic ‘L’ sets the demodulator to FSK, applying ‘H’ to ASK mode.

In ASK mode, an automatic threshold control circuit (ATC) is used to set the detection reference voltage to a value where a good signal-to-noise ratio is achieved. This circuit effectively suppresses any kind of inband noise signals or competing transmitters. If the S/N (ratio to suppress inband noise signals) exceeds 10 dB, the data signal can be detected properly.

The FSK demodulator is intended to be used for an FSK deviation of 10 kHz ≤ Δf ≤ 100 kHz. In FSK mode the data signal can be detected if the S/N (ratio to suppress inband noise signals) exceeds 2 dB. This value is guaranteed for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its passband can be adopted to the characteristics of the data signal. The data filter consists of a 1st-order highpass and a 2nd-order lowpass filter

The highpass filter cut-off frequency is defined by an external capacitor connected to Pin CDEM. The cut-off frequency of the highpass filter is defined by the following formula:

$$fcu\_DF = \frac{1}{2 \times \pi \times 30\ k\Omega \times CDEM}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the lowpass filter is defined by the selected baud-rate range (BR_Range). The BR_Range is defined in the OPMODE register (refer to chapter ‘Configuration of the Receiver’). The BR_Range must be set in accordance to the used baud rate.

The T5743N is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of V_{DC_min} = 33% and V_{DC_max} = 66%. The sensitivity may be reduced by up to 2 dB in that condition.

Each BR_Range is also defined by a minimum and a maximum edge-to-edge time (t_{ee_sig}). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

Receiving Characteristics

The RF receiver T5743N can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity. The selectivity with and without a SAW front-end filter is illustrated in figure 8. This example relates to ASK mode. FSK mode exhibits similar behavior. Note that the mirror frequency is reduced by 40 dB. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 4 dB must be considered.

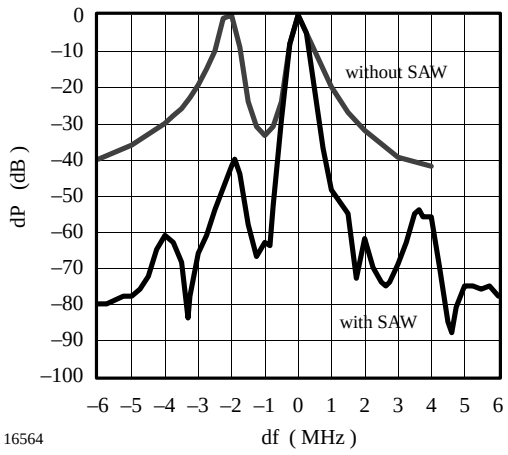


Figure 8. Receiving frequency response

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated to be the sum of the deviation of the crystal and the XTO deviation of the T5743N. Low-cost crystals are specified to be within ±100 ppm. The XTO deviation of the T5743N is an additional deviation due to the XTO circuit. This deviation is specified to be ±30 ppm. If a crystal of ±100 ppm is used, the total deviation is ±130 ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected the receiver remains active and transfers the data to the connected µC. If there is no valid signal present the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected µC is disabled during that time.

All relevant parameters of the polling logic can be configured by the connected µC. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

Regarding the number of connection wires to the µC, the receiver is very flexible. It can be either operated by a single bi-directional line to save ports to the connected µC or it can be operated by up to five uni-directional ports.

Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. According to figure 9, this clock cycle T_{Clk} is derived from the crystal oscillator (XTO) in combination with a divider. The division factor is controlled by the logical state at Pin MODE. According to chapter ‘RF Front End’, the frequency of the crystal oscillator (f_{XTO}) is defined by the RF input signal (f_{RFin}) which also defines the operating frequency of the local oscillator (f_{LO}).

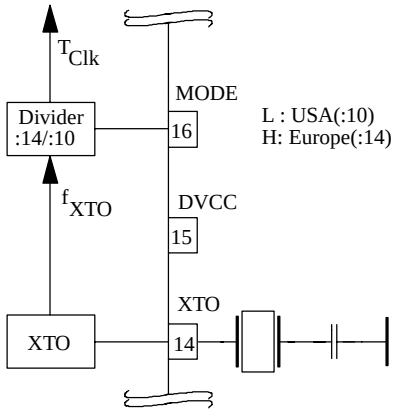


Figure 9. Generation of the basic clock cycle

Pin MODE can now be set in accordance with the desired clock cycle T_{Clk}. T_{Clk} controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency (f_{IF0})

Most applications are dominated by two transmission frequencies: f_{Send} = 315 MHz is mainly used in USA, f_{Send} = 433.92 MHz in Europe. In order to ease the usage of all T_{Clk}-dependent parameters on this electrical characteristics display three conditions for each parameter.

- Application USA
  (f_{XTO} = 4.90625 MHz, MODE = L, T_{Clk} = 2.0383 µs)
- Application Europe
  (f_{XTO} = 6.76438 MHz, MODE = H, T_{Clk} = 2.0697 µs)
- Other applications
  (T_{Clk} is dependent on f_{XTO} and on the logical state of Pin MODE. The electrical characteristic is given as a function of T_{Clk}).

The clock cycle of some function blocks depends on the selected baud-rate range (BR_Range) which is defined in the OPMODE register. This clock cycle T_{XClk} is defined by the following formulas for further reference:

BR_Range = BR_Range0: $T_{XClk} = 8 \times T_{Clk}$
BR_Range1: $T_{XClk} = 4 \times T_{Clk}$
BR_Range2: $T_{XClk} = 2 \times T_{Clk}$
BR_Range3: $T_{XClk} = 1 \times T_{Clk}$

Polling Mode

According to figure 10, the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode the signal processing circuitry is disabled for the time period T_{Sleep} while consuming low current of $I_S = I_{Soff}$. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit by bit contra a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies check by check as it is a statistical process. An average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. During $T_{Startup}$ and $T_{Bit\text{-}check}$ the current consumption is $I_S = I_{Son}$. The condition of the receiver is indicated on Pin IC_ACTIVE. The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bitcheck})}{T_{Sleep} + T_{Startup} + T_{Bitcheck}}$$

During T_{Sleep} and $T_{Startup}$ the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters T_{Sleep}, $T_{Startup}$, $T_{Bit\text{-}check}$ and the start-up time of a connected µC ($T_{Start,\mu C}$). Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Start\_\mu C}$$

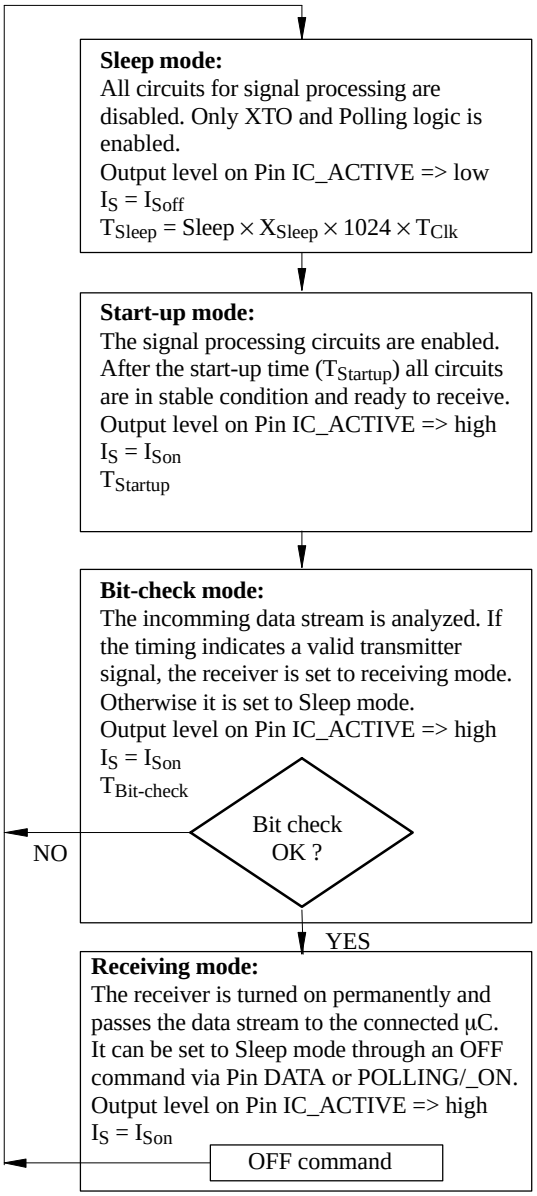
Sleep Mode

The length of period T_{Sleep} is defined by the 5-bit word Sleep of the OPMODE register, the extension factor XSleep (according to table 9), and the basic clock cycle T_{Clk}. It is calculated to be:

$$T_{Sleep} = Sleep \times X_{Sleep} \times 1024 \times T_{Clk}$$

In US- and European applications, the maximum value of T_{Sleep} is about 60 ms if XSleep is set to 1. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting XSleep to 8. XSleep can be set to 8 by bit $XSleep_{Std}$ to'1'.

According to table 8, the highest register value of sleep sets the receiver into a permanent sleep condition. The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line and may also be used for µC polling – via Pin POLLING/_ON, the receiver can be switched on and off.



Sleep: 5-bit word defined by Sleep0 to Sleep4 in OPMODE register

X_{Sleep}: Extension factor defined by $XSleep_{Std}$ according to table 9

T_{Clk}: Basic clock cycle defined by f_{XTO} and Pin MODE

$T_{Startup}$: Is defined by the selected baud rate range and T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register.

$T_{Bit-check}$: Depends on the result of the bit check

If the bit check is ok, $T_{Bit-check}$ depends on the number of bits to be checked ($N_{Bit-check}$) and on the utilized data rate.

If the bit check fails, the average time period for that check depends on the selected baud-rate range and on T_{Clk}. The baud-rate range is defined by Baud0 and Baud1 in the OPMODE register.

Figure 10. Polling mode flow chart

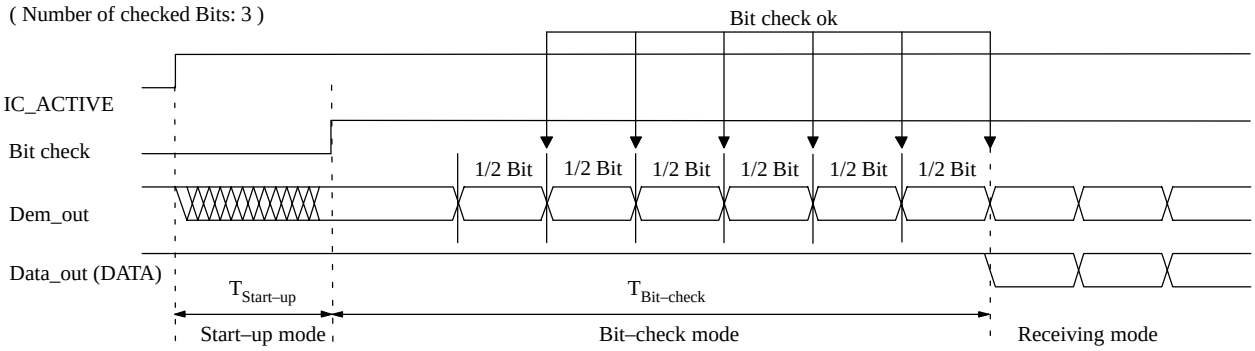


Figure 11. Timing diagram for complete successful bit check

Bit-Check Mode

In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge tests before the receiver switches to receiving mode is also programmable.

Configuring the Bit Check

Assuming a modulation scheme that contains 2 edges per bit, two time frame checks are verifying one bit. This is valid for Manchester, Bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable $N_{Bit\text{-}check}$ in the OPMODE register. This implies 0, 6, 12 and 18 edge to edge checks respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In polling mode, the bit-check time is not dependent on $N_{Bit\text{-}check}$. Figure 11 shows an example where 3 bits are tested successfully and the data signal is transferred to Pin DATA.

According to figure 12, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time t_{ee} is in between the lower bit-check limit T_{Lim_min} and the upper bit-check limit T_{Lim_max}, the check will be continued. If t_{ee} is smaller than T_{Lim_min} or t_{ee} exceeds T_{Lim_max}, the bit check will be terminated and the receiver switches to sleep mode.

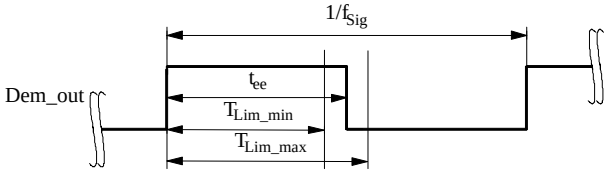


Figure 12. Valid time window for bit check

For best noise immunity it is recommended to use a low span between T_{Lim_min} and T_{Lim_max}. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A ‘11111...’ or a ‘10101...’ sequence in Manchester or Bi-phase is a good choice concerning that advice. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ± 25% regarding the expected edge-to-edge time t_{ee}. Using pre-burst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$$T_{Lim\_min} = Lim\_min \times T_{XClk}$$
$$T_{Lim\_max} = (Lim\_max - 1) \times T_{XClk}$$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XClk}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XClk}. The minimum edge-to-edge time t_{ee} ($t_{DATA\_L\_min}$, $t_{DATA\_H\_min}$) is defined according to the chapter ‘Receiving Mode’. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

If the calculated value for Lim_min is < 19, it is recommended to check 6 or 9 bits ($N_{Bit\text{-}check}$) to prevent switching to receiving mode due to noise.

Figures 13, 14 and 15 illustrate the bit check for the bit-check limits Lim_min = 14 and Lim_max = 24. When the IC is enabled, the signal processing circuits are enabled during $T_{Startup}$. The output of the ASK/ FSK demodulator (Dem_out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle T_{XClk}.

Figure 13 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In figure 14 the bit check fails as the value CV_lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in figure 15.

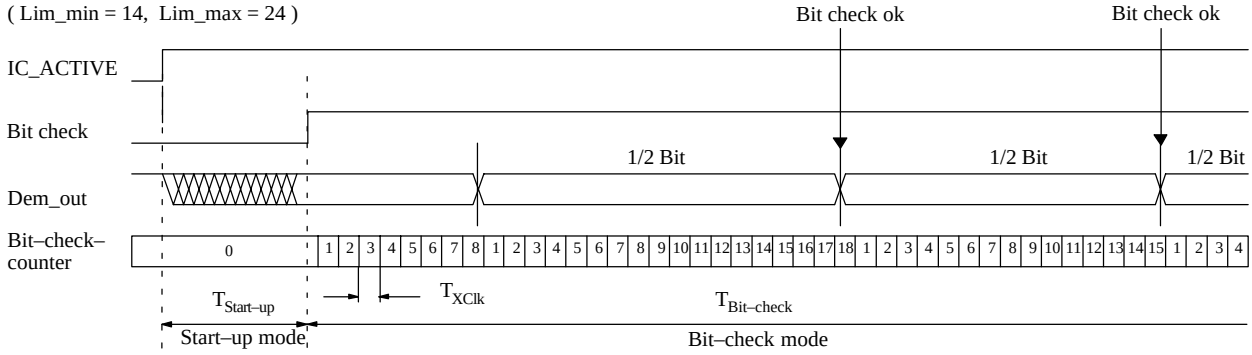


Figure 13. Timing diagram during bit check

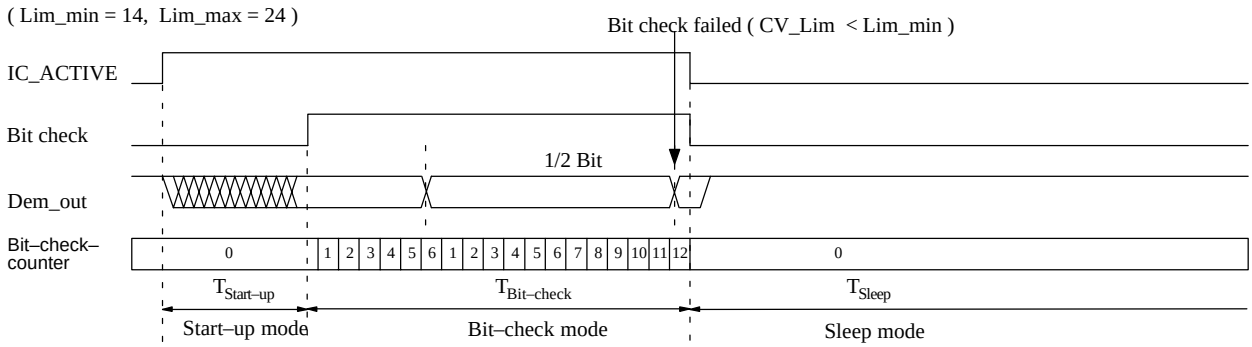


Figure 14. Timing diagram for failed bit check (condition: CV_Lim < Lim_min)

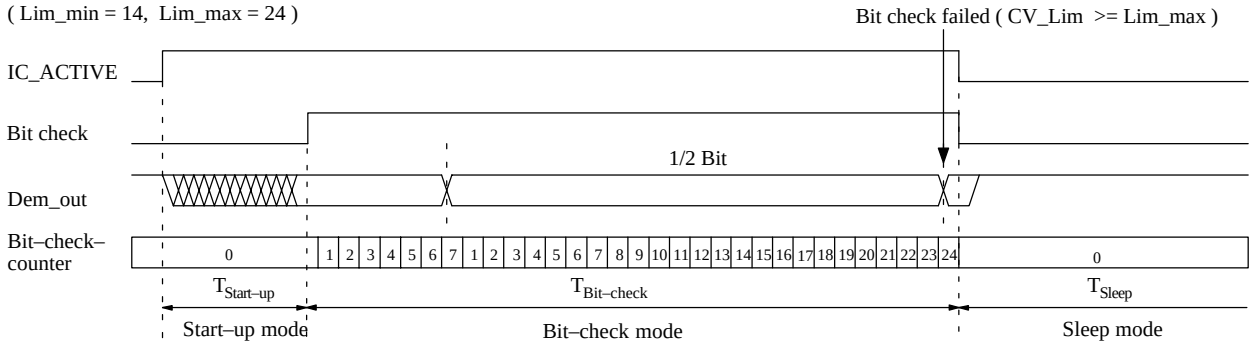


Figure 15. Timing diagram for failed bit check (condition: CV_Lim >= Lim_max)

Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/ FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected baud-rate range and on T_{Clk}. A higher baud-rate range causes a lower value for $T_{Bit\text{-}check}$ resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Sig}, and the count of the checked bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$ requiring a higher value for the transmitter pre-burst $T_{Preburst}$.

Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the receiver switches to receiving mode. According to figure 11, the internal data signal is switched to Pin DATA in that case and the data clock is available after the start bit has been detected (figure 22). A connected µC can be woken up by the negative edge at Pin DATA or by the data clock at Pin DATA_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

Digital Signal Processing

The data from the ASK/ FSK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud-rate range (BR_Range). Figure 16 illustrates how Dem_out is synchronized by the extended clock cycle T_{XClk}. This clock is also used for the bit-check counter. Data can change its state only after T_{XClk} has elapsed. The edge-to-edge time period t_{ee} of the Data signal as a result is always an integral multiple of T_{XClk}.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA\_min}$. This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected µC.

The maximum time period for DATA to stay Low is limited to $T_{DATA\_L\_max}$. This function is employed to ensure a finite response time in programming or switching off the receiver via Pin DATA. $T_{DATA\_L\_max}$ is thereby longer than the maximum time period indicated by the transmitter data stream. Figure 18 gives an example where Dem_out remains Low after the receiver has switched to receiving mode.

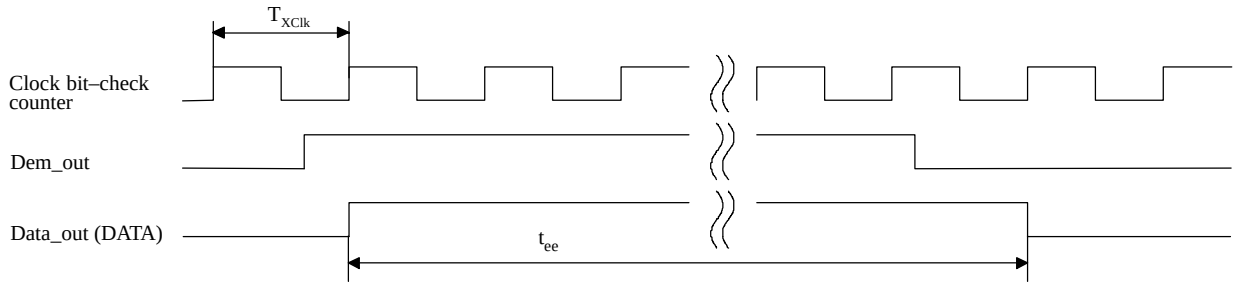


Figure 16. Synchronization of the demodulator output

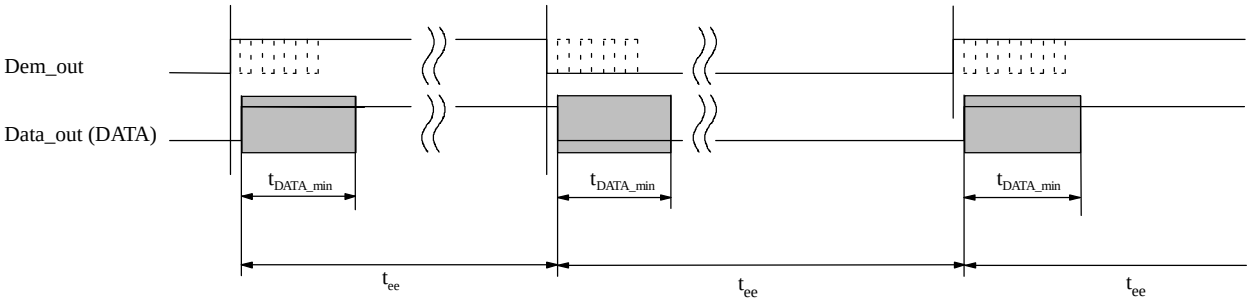


Figure 17. Debouncing of the demodulator output

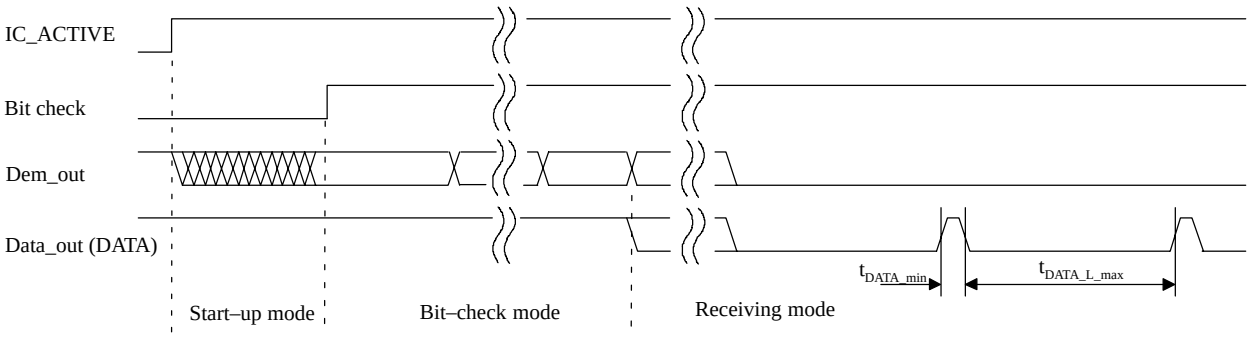


Figure 18. Steady L state limited DATA output pattern after transmission

After the end of a data transmission, the receiver remains active. Depending of the bit Noise_Disable in the OPMODE register, the output signal at Pin DATA is high or random noise pulses appear at Pin DATA (see chapter 'Digital Noise Supression'). The edge-to-edge time period t_{ee} of the majority of these noise pulses is equal or slightly higher than T_{DATA_min}.

Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via Pin DATA or via Pin POLLING/_ON.

When using Pin DATA, this pin must be pulled to Low for the period t1 by the connected µC. Figure 19 illustrates the timing of the OFF command (see also figure 34). The minimum value of t1 depends on BR_Range. The maximum value for t1 is not limited but it is recommended not to exceed the specified value to prevent erasing the reset marker. Note also that an internal reset for the OPMODE and the LIMIT register will be generated if t1 exceeds the specified values. This item is explained in more detail in the chapter 'Configuration of the Receiver'. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to be '1' during the register configuration. Only one sync pulse (t3) is issued.

The duration of the OFF command is determined by the sum of t1, t2 and t10. After the OFF command the sleep time T_{Sleep} elapses. Note that the capacitive load at Pin DATA is limited (see chapter 'Data Interface').

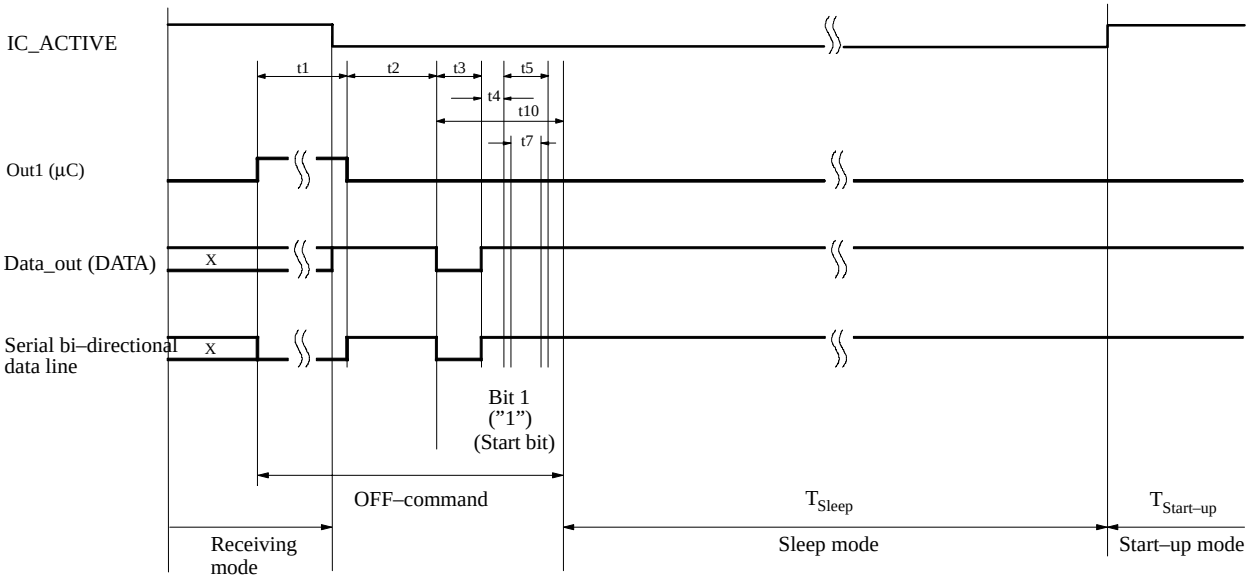


Figure 19. Timing diagram of the OFF-command via Pin DATA

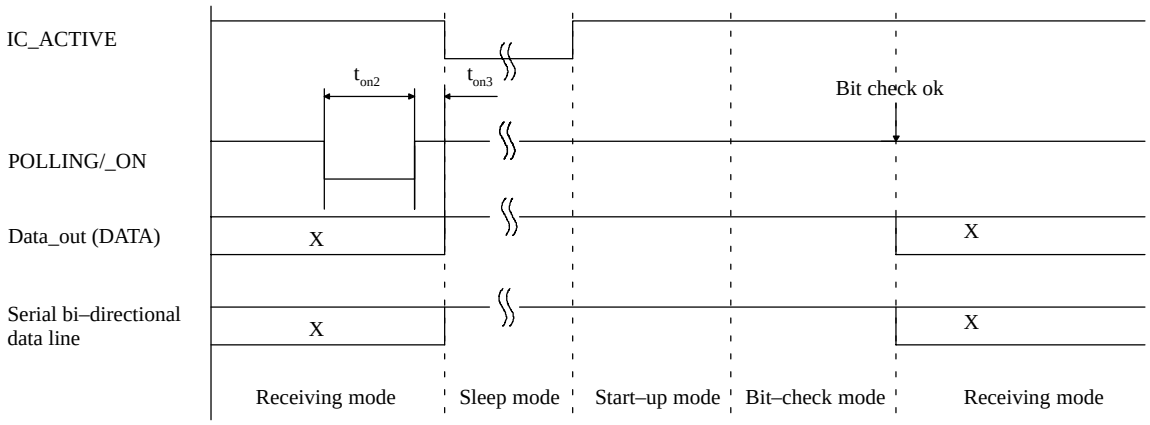


Figure 20. Timing diagram of the OFF-command via Pin POLLING/_ON

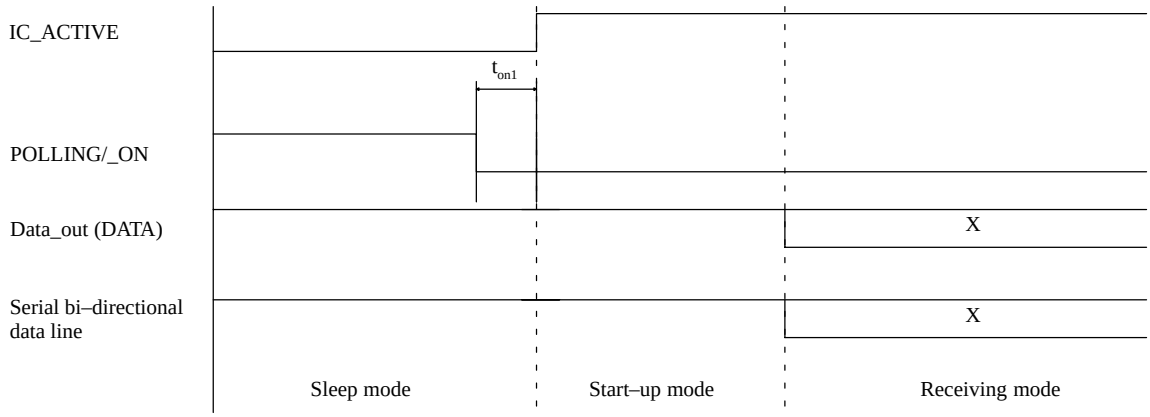


Figure 21. Activating the receiving mode via Pin POLLING/_ON

Figure 20 illustrates how to set the receiver back to polling mode via Pin POLLING/_ON. The Pin POLLING/_ON must be held to low for the time period t_{on2}. After the positive edge on Pin POLLING/_ON and the delay t_{on3}, the polling mode is active and the sleep time T_{Sleep} elapses.

This command is faster than using Pin DATA at the cost of an additional connection to the µC.

Figure 21 illustrates how to set the receiver to receiving mode via the Pin POLLING/_ON. The Pin POLLING/_ON must be held to Low. After the delay t_{on1} , the receiver changes from sleep mode to start–up mode regardless the programmed values for T_{Sleep} and $N_{Bit–check}$. As long as POLLING/_ON is held to Low, the values for T_{Sleep} and $N_{Bit–check}$ will be ignored, but not deleted (see also chapter 'Digital Noise Suppression').

If the receiver is polled exclusively by a µC, T_{Sleep} must be programmed to 31 (permanent sleep mode). In this case the receiver remains in sleep mode as long as POLLING/_ON is held to High.

Data Clock

The Pin DATA_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a µC can easily synchronize the data stream. This clock can only be used for **Manchester and Bi-phase** coded signals.

Generation of the data clock:

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at Pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, like in the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in figure 22, only two distances between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used for the bit check. They can be programmed in the LIMIT-register (Lim_min and Lim_max, see tables 11 and 12).

The limits for 2T are calculated as follows:

Lower limit of 2T:

$Lim\_min\_2T = (Lim\_min + Lim\_max) – (Lim\_max – Lim\_min) / 2$

Upper limit of 2T:

$Lim\_max\_2T= (Lim\_min + Lim\_max) + (Lim\_max – Lim\_min) / 2$

(If the result for 'Lim_min_2T' or 'Lim_max_2T' is not an integer value, it will be round up)

The data clock is available, after the data clock control logic has detected the distance 2T (Start bit) and is issued with the delay t_{Delay} after the edge on Pin DATA (see figure 22).

If the data clock control logic detects a timing or logical error (Manchester code violation), like illustrated in figures 23 and 24, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see figure 25).

It is recommended to use the function of the data clock only in conjunction with the bit check 3, 6 or 9. If the bit check is set to 0 or the receiver is set to receiving mode via the Pin POLLING/_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

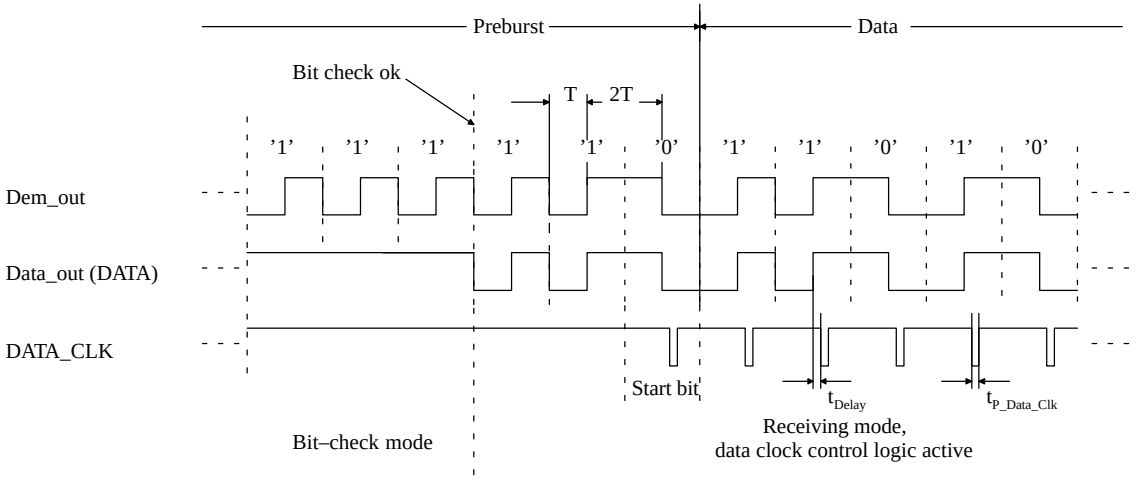


Figure 22. Timing diagram of the data clock

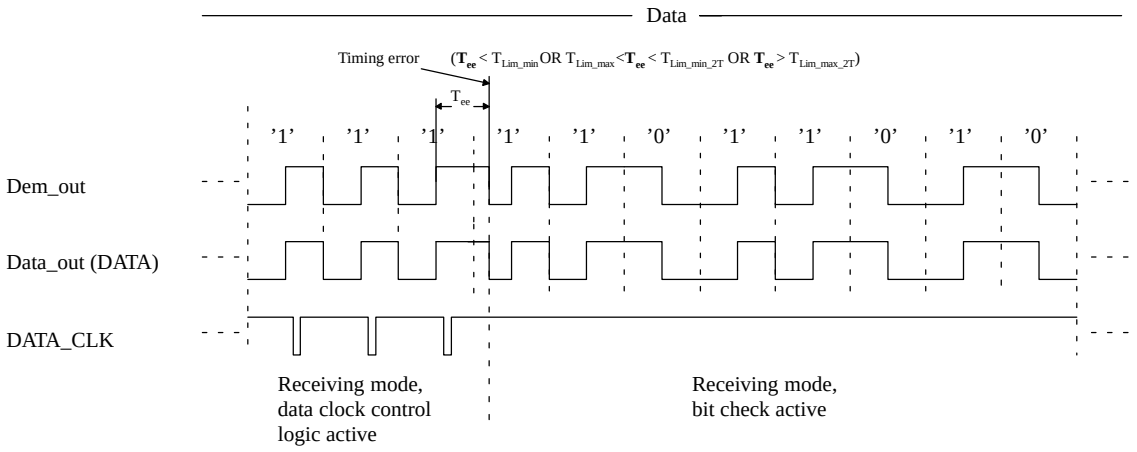


Figure 23. Data clock disappears because of a timing error

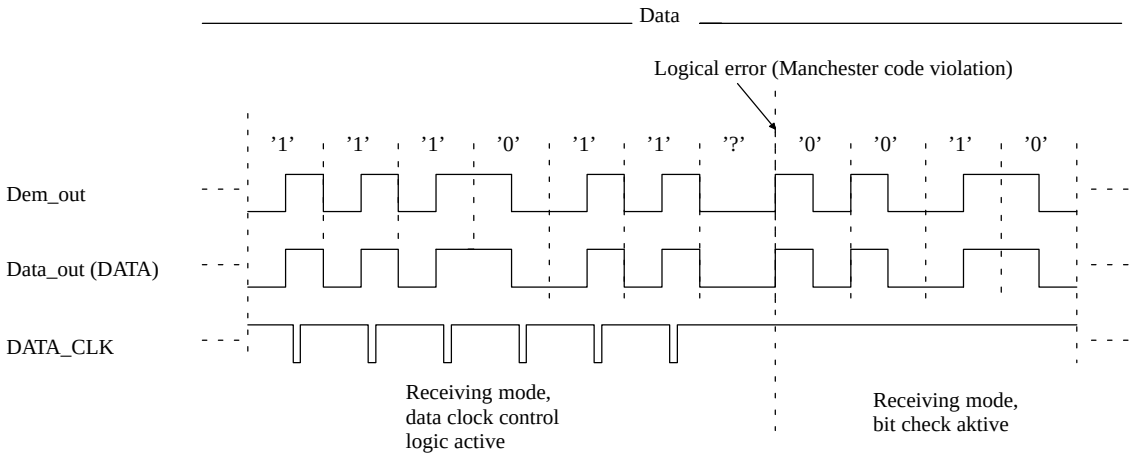


Figure 24. Data clock disappears because of a logical error

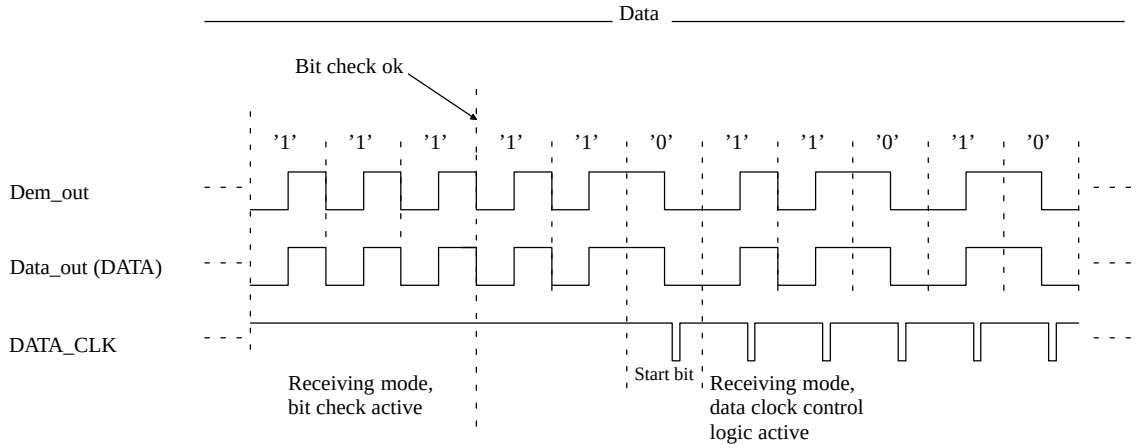


Figure 25. Output of the data clock after a successful bit check

The delay of the data clock is calculated as follows:

$t_{Delay} = t_{Delay1} + t_{Delay2}$

t_{Delay1} is the delay between the internal signals Data_Out and Data_In. For the rising edge, t_{Delay1} depends on the capacitive load C_L at Pin DATA and the external pull–up resistor R_{pup}. For the falling edge, t_{Delay1} depends additionally on the external voltage V_X (see figures 26, 27 and 34). When the level of Data_In is equal to the level of Data_Out, the data clock is issued after an additional delay t_{Delay2}.

Note that the capacitive load at Pin DATA is limited. If the maximum tolerated capacitive load at Pin DATA is exceeded, the data clock disappears (see chapter 'Data Interface').

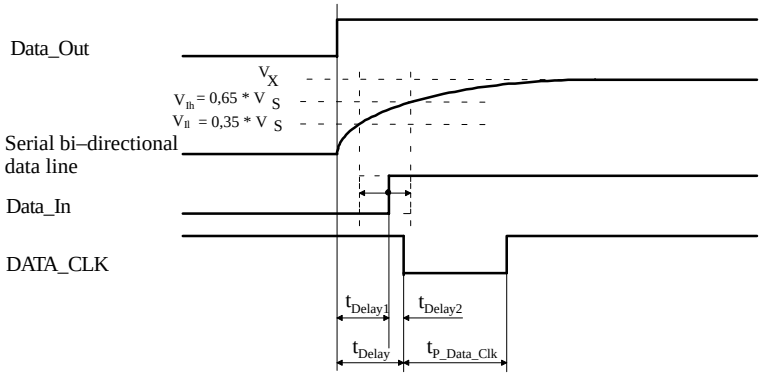


Figure 26. Timing characteristic of the data clock (rising edge on Pin DATA)

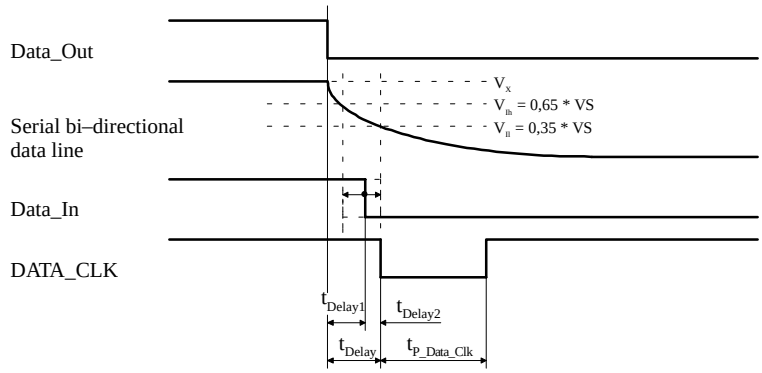


Figure 27. Timing characteristic of the data clock (falling edge of the Pin DATA)

Digital Noise Suppression

After a data transmission, digital noise appears on the data output (see figure 28). To prevent that digital noise keeps the connected µC busy, it can be suppressed in two different ways.

1. Automatic noise suppression (figure 29):

If the bit Noise_Disable (table 10) in the OPMODE register is set to 1 (default), the receiver changes to bit-check mode at the end of a valid data stream. The digital noise is suppressed and the level at Pin DATA is High in that case. The receiver changes back to receiving mode, if the bit check was successful.
This way to suppress the noise is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

Figure 30 illustrates the behavior of the data output at the end of a data stream. Note that if the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on Pin DATA. The length of the pulse depends on the selected baud-rate range.

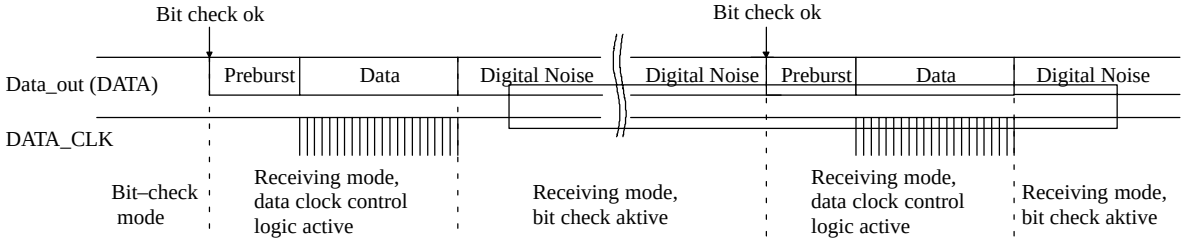


Figure 28. Output of digital noise at the end of the data stream

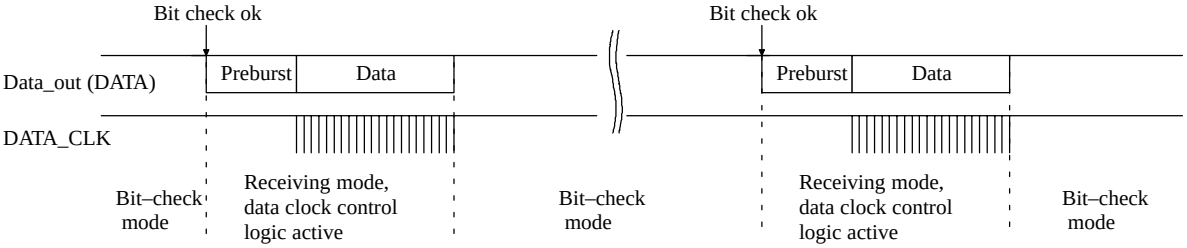


Figure 29. Automatic noise suppression

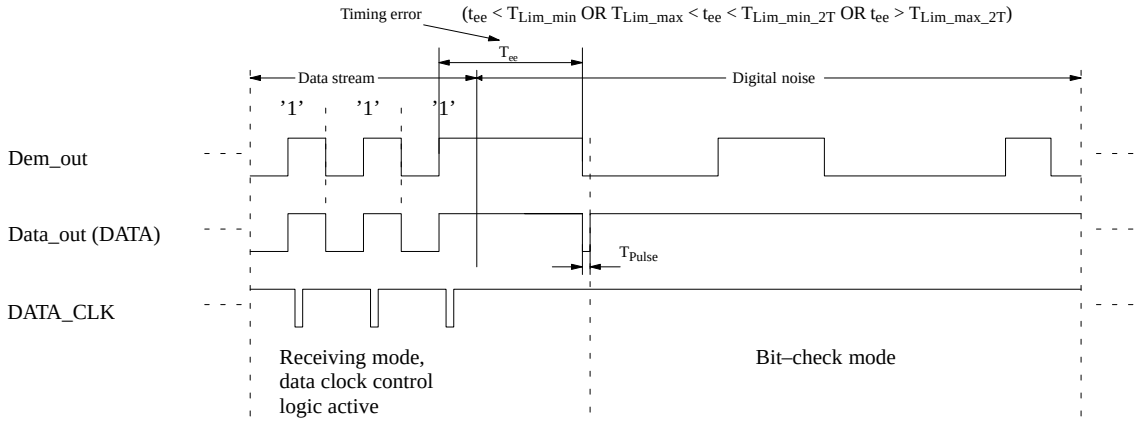


Figure 30. Occurence of a pulse at the end of the data stream

2. Controlled noise suppression by the µC (figure 31):

If the bit Noise_Disable (see table 10) in the OPMODE register is set to 0, digital noise appears at the end of a valid data stream. To suppress the noise, the Pin POLLING/_ON must be set to Low. The receiver remains in receiving mode. Then, the OFF-command causes the change to the start-up mode. The programmed sleep time (see table 8) will not be executed because the level at Pin POLLING/_ON is low, but the bit check is active in that case. The OFF-command activates the bit check also if the Pin POLLING/_ON is held to Low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the Pin POLLING/_ON must be set to High.

This way to suppress the noise is recommended if the data stream is not Manchester or Bi-phase coded.

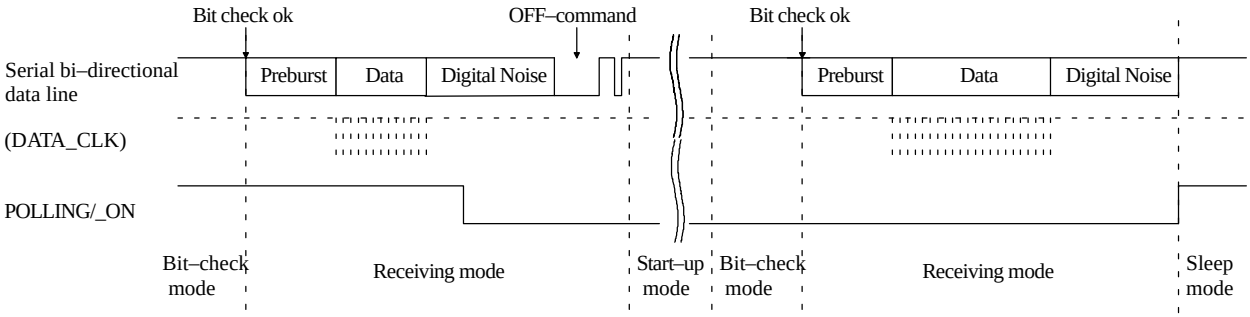


Figure 31. Controlled noise suppression

Configuration of the Receiver

The T5743N receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bidirectional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a power-on reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. Table 4 shows the structure of the registers. According to table 2 bit 1 defines if the receiver is set back to polling mode via the OFF command (see chapter 'Receiving Mode') or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. To get a high programming reliability, Bit15 (Stop bit), at the end of the programming operation, must be set to 0.

Table 2 Effect of Bit 1 and Bit 2 on programming the registers

Bit 1	Bit 2	Action
1	x	The receiver is set back to polling mode (OFF command)
0	1	The OPMODE register is programmed
0	0	The LIMIT register is programmed

Table 3 Effect of Bit 15 on programming the register

Bit 15	Action
0	The values will be written into the register (OPMODE or LIMIT)
1	The values will not be written into the register

Table 4 Effect of the configuration words within the registers

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15
OFF–command														
1														
		OPMODE register												
0	1	BR_Range		$N_{Bit-check}$		Modu-lation	Sleep					X Sleep	Noise Suppres-sion	0
		Baud1	Baud0	BitChk 1	BitChk 0	ASK/_ FSK	Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	$X_{Sleep\ Std}$	Noise_D isable	
Default values of Bit 3...14		0	0	0	1	0	0	0	1	1	0	0	1	
		LIMIT register												
0	0	Lim_min						Lim_max						0
		Lim_ min5	Lim_ min4	Lim_ min3	Lim_ min2	Lim_ min1	Lim_ min0	Lim_ max5	Lim_ max4	Lim_ max3	Lim_ max2	Lim_ max1	Lim_ max0	
Default values of Bit 3...14		0	1	0	1	0	1	1	0	1	0	0	1	

Tables 5 to 12 illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR_Range sets the appropriate baud–rate range and simultaneously defines XLim. XLim is used to define the bit–check limits T_{Lim_min} and T_{Lim_max} as shown in table 11 and table 12.

Table 5 Effect of the configuration word BR_Range

BR_Range		Baud-Rate Range / Extension Factor for Bit-Check Limits (XLim)
Baud1	Baud0	
0	0	BR_Range0 (application USA / Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud) XLim = 8 (default)
0	1	BR_Range1 (application USA / Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud) XLim = 4
1	0	BR_Range2 (application USA / Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud) XLim = 2
1	1	BR_Range3 (Application USA / Europe: BR_Range3 = 5.6 kBaud to 10 kBaud) XLim = 1

Table 6 Effect of the configuration word $N_{Bit-check}$

$N_{Bit-check}$		Number of Bits to be Checked
BitChk1	BitChk0	
0	0	0
0	1	3 (default)
1	0	6
1	1	9

Table 7 Effect of the configuration bit Modulation

Modulation	Selected Modulation
ASK/_FSK	
0	FSK (default)
1	ASK

Table 8 Effect of the configuration word Sleep

Sleep					Start Value for Sleep Counter (T_{Sleep} = Sleep × Xsleep × 1024 × T_{Clk})
Sleep4	Sleep3	Sleep2	Sleep1	Sleep0	
0	0	0	0	0	0 (Receiver is continuously polling until a valid signal occurs)
0	0	0	0	1	1 (T_{Sleep} ≈ 2ms for XSleep =1 in US- / European applications)
0	0	0	1	0	2
0	0	0	1	1	3
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
0	0	1	1	0	6 (USA: T_{Sleep} = 12.52 ms, Europe: T_{Sleep} = 12.72 ms) (default)
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31 (Permanent sleep mode)

Table 9 Effect of the configuration bit XSleep

XSleep	Extension Factor for Sleep Time (T_{Sleep} = Sleep × Xsleep × 1024 × T_{Clk})
$XSleep_{Std}$	
0	1 (default)
1	8

Table 10 Effect of the configuration bit Noise Suppression

Noise Suppression	Suppression of the Digital Noise at Pin DATA
Noise_Disable	
0	Noise suppression is inactive
1	Noise suppression is active (default)

Table 11 Effect of the configuration word Lim_min

Lim_min *) (Lim_min < 10 is not applicable)						Lower Limit Value for Bit Check
Lim_min5	Lim_min4	Lim_min3	Lim_min2	Lim_min1	Lim_min0	(T_{Lim_min} = Lim_min × XLim × T_{Clk})
0	0	1	0	1	0	10
0	0	1	0	1	1	11
0	0	1	1	0	0	12
. .	. .	. .	. .	. .	. .	
0	1	0	1	0	1	21 (default) (USA: T_{Lim_min} = 342 µs, Europe: T_{Lim_min} = 348 µs)
. .	. .	. .	. .	. .	. .	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

*) Lim_min is also be used to determine the margins of the data clock control logic (see chapter ’Data Clock’)

Table 12 Effect of the configuration word Lim_max

Lim_max *) (Lim_max < 12 is not applicable)						Upper Limit Value for Bit Check
Lim_max5	Lim_max4	Lim_max3	Lim_max2	Lim_max1	Lim_max0	(T_{Lim_max} = (Lim_max – 1) × XLim × T_{Clk})
0	0	1	1	0	0	12
0	0	1	1	0	1	13
0	0	1	1	1	0	14
. .	. .	. .	. .	. .	. .	
1	0	1	0	0	1	41 (Default) (USA: T_{Lim_max} = 652 µs, Europe: T_{Lim_max} = 662 µs)
. .	. .	. .	. .	. .	. .	
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

*) Lim_max is also be used to determine the margins of the data clock control logic (see chapter ’Data Clock’)

Conservation of the Register Information

The T5743N implies an integrated power-on reset and brown-out detection circuitry to provide a mechanism to preserve the RAM register information.

According to figure 32**,** a power–on reset (POR) is generated if the supply voltage V_S drops below the threshold voltage $V_{ThReset}$. The default parameters are programmed into the configuration registers in that condition. Once V_S exceeds $V_{ThReset}$ the POR is canceled after the minimum reset period t_{Rst}. A POR is also generated when the supply voltage of the receiver is turned on.

To indicate that condition, the receiver displays a reset marker (RM) at Pin DATA after a reset. The RM is represented by the fixed frequency f_{RM} at a 50% duty-cycle. RM can be canceled via a Low pulse t1 at Pin DATA. The RM implies the following characteristics:

- f_{RM} is lower than the lowest feasible frequency of a data signal. By this means, RM cannot be misinterpreted by the connected µC.
- If the receiver is set back to polling mode via Pin DATA, RM cannot be canceled by accident if t1 is applied according to the proposal in the section ’Programming the Configuration Registers’.

By means of that mechanism the receiver cannot lose its register information without communicating that condition via the reset marker RM.

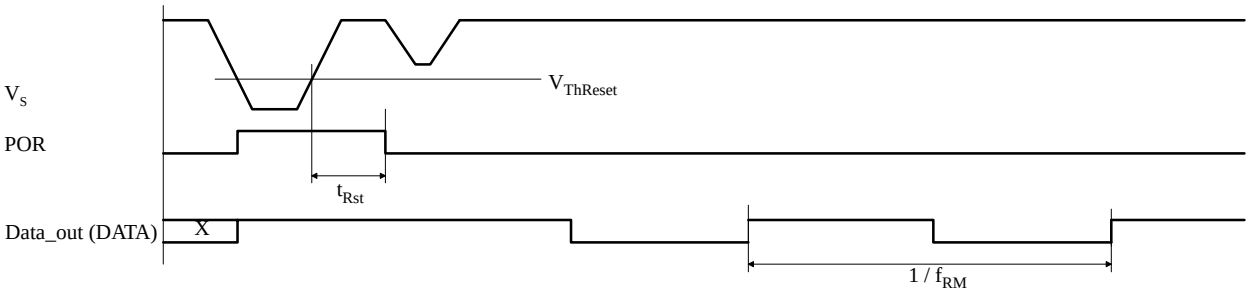


Figure 32. Generation of the power-on reset

Programming the Configuration Register

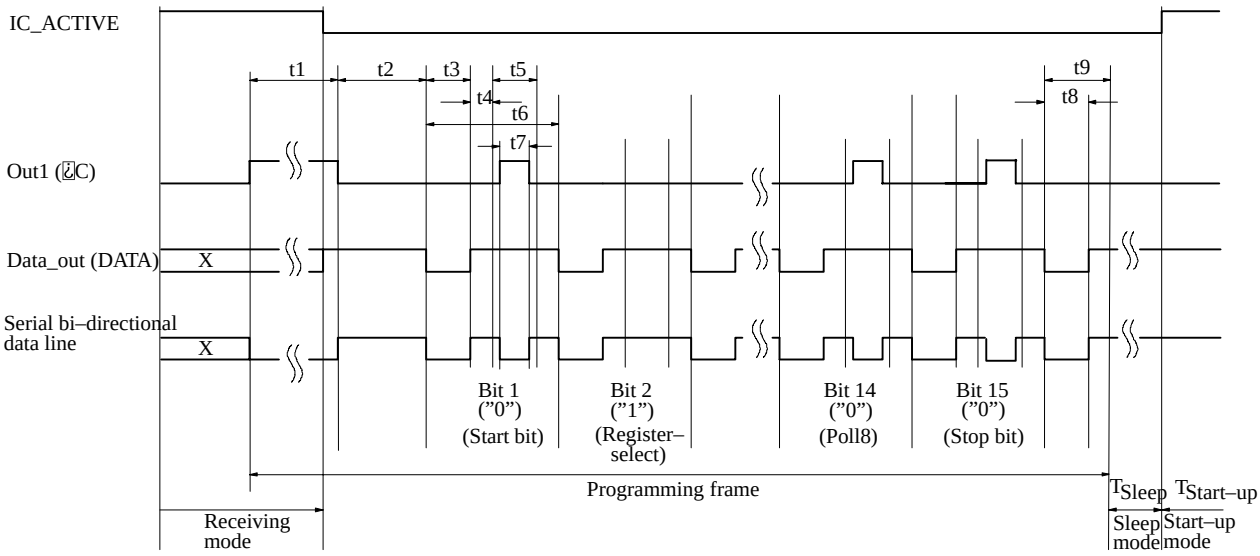


Figure 33. Timing of the register programming

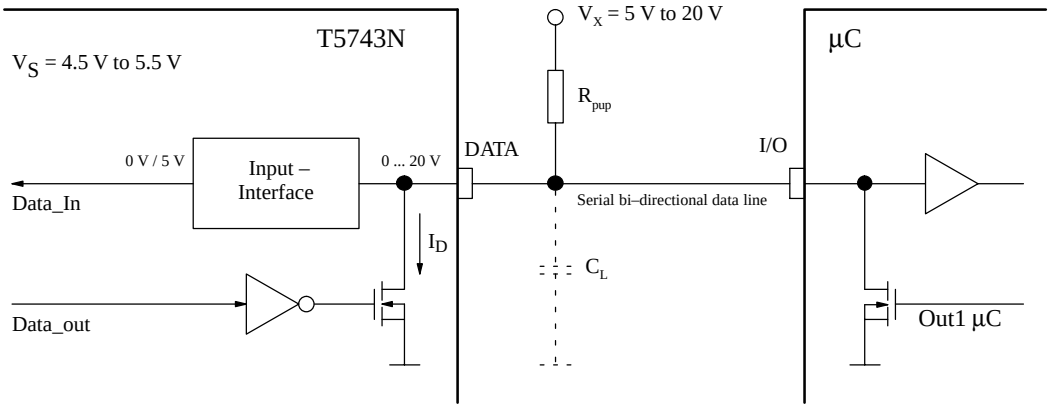


Figure 34. Data interface

The configuration registers are programmed serially via the bi-directional data line according to figure 33 and figure 34.

To start programming, the serial data line DATA is pulled to Low for the time period t1 by the µC. When DATA has been released, the receiver becomes the master device. When the programming delay period t2 has elapsed, it emits 15 subsequent synchronization pulses with the pulse length t3. After each of these pulses, a programming window occurs. The delay until the program window starts is determined by t4, the duration is defined by t5. Within the programming window, the individual bits are set. If the µC pulls down Pin DATA for the time period t7 during t5, the according bit is set to '0'. If no programming pulse t7 is issued, this bit is set to '1'. All 15 bits are subsequently programmed this way. The time frame to program a bit is defined by t6.

Bit 15 is followed by the equivalent time window t9. During this window, the equivalence acknowledge pulse t8 (E_Ack) occurs if the just programmed mode word is equivalent to the mode word that was already stored in that register. E_Ack should be used to verify that the mode word was correctly transferred to the register. The register must be programmed twice in that case.

Programming of a register is possible both in sleep– and in active–mode of the receiver.

During programming, the LNA, LO, lowpass filter IF-amplifier and the FSK/ASK Manchester demodulator are disabled.

The programming start pulse t1 initiates the programming of the configuration registers. If bit 1 is set to '1', it represents the OFF–command to set the receiver back to polling mode at the same time. For the length of the programming start pulse t1, the following convention should be considered:

- $t1(min) < t1 < 5632 \times T_{Clk}$: t1(min) is the minimum specified value for the relevant BR_Range

Programming respectively OFF-command is initiated if the receiver is not in reset mode.If the receiver is in reset mode, programming respectively Off-command is not initiated and the reset marker RM is still present at Pin DATA.

This period is generally used to switch the receiver to polling mode or to start the programming of a register. In reset condition, RM is not cancelled by accident.

- $t1 > 7936 \times T_{Clk}$

Programming respectively OFF–command is initiated in any case. The registers OPMODE and LIMIT are set to the default values. RM is cancelled if present.

This period is used if the connected µC detected RM.If the receiver operates in default mode, this time period for t1 can generally be used.

Note that the capacitive load at Pin DATA is limited.

Data Interface

The data interface (see figure 34) is designed for automotive requirements. It can be connected via the pull–up resistor R_{pup} up to 20V and is short–circuit–protected.

The applicable pull–up resistor R_{pup} depends on the load capacity C_L at Pin DATA and the selected BR_range (see table 13). More detailed information about the calculation of the maximum load capacity at Pin DATA is given in the 'Application Hints U3743BM'.

Table 13 Applicable R_{pup}

	BR_range	Applicable R_{pup}
$C_L \leq 1nF$	B0	1.6 kΩ to 47 kΩ
	B1	1.6 kΩ to 22 kΩ
	B2	1.6 kΩ to 12 kΩ
	B3	1.6 kΩ to 5.6 kΩ
$C_L \leq 100pF$	B0	1.6 kΩ to 470 kΩ
	B1	1.6 kΩ to 220 kΩ
	B2	1.6 kΩ to 120 kΩ
	B3	1.6 kΩ to 56 kΩ

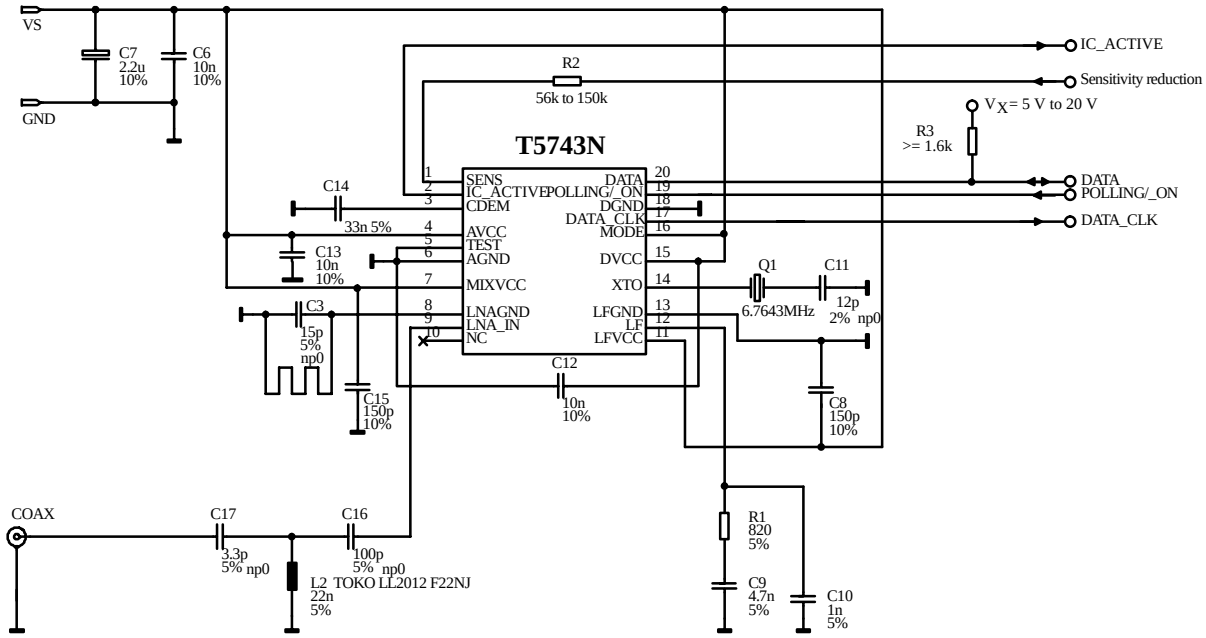


Figure 35. Application circuit: f_{RF} = 433.92 MHz without SAW filter

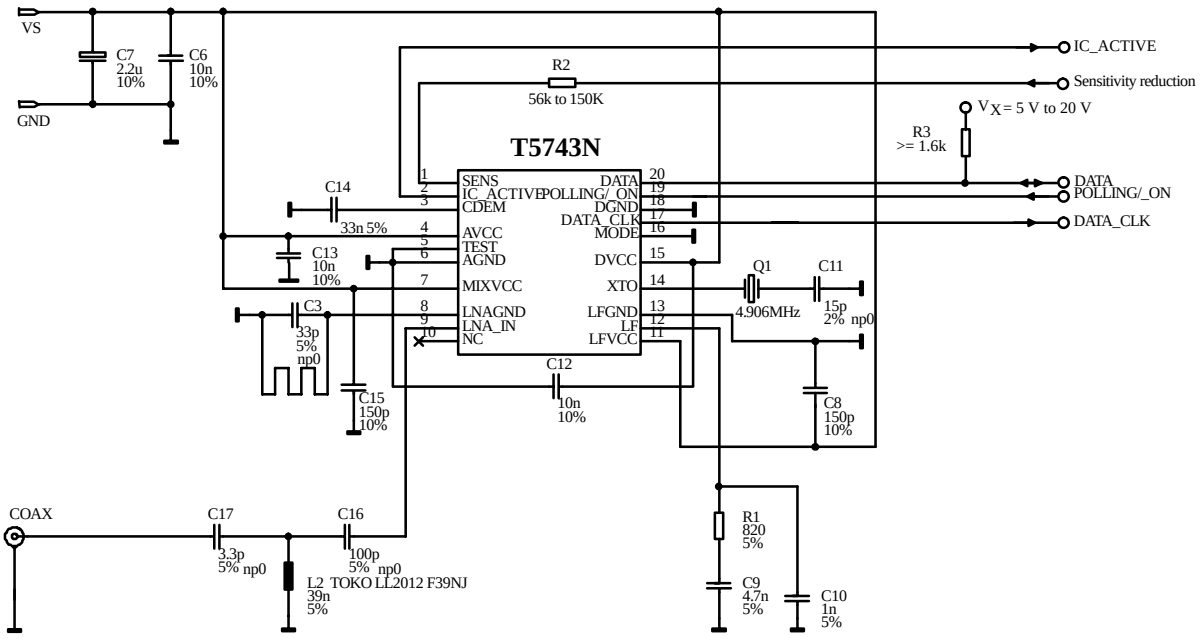


Figure 36. Application circuit: f_{RF} = 315 MHz without SAW filter

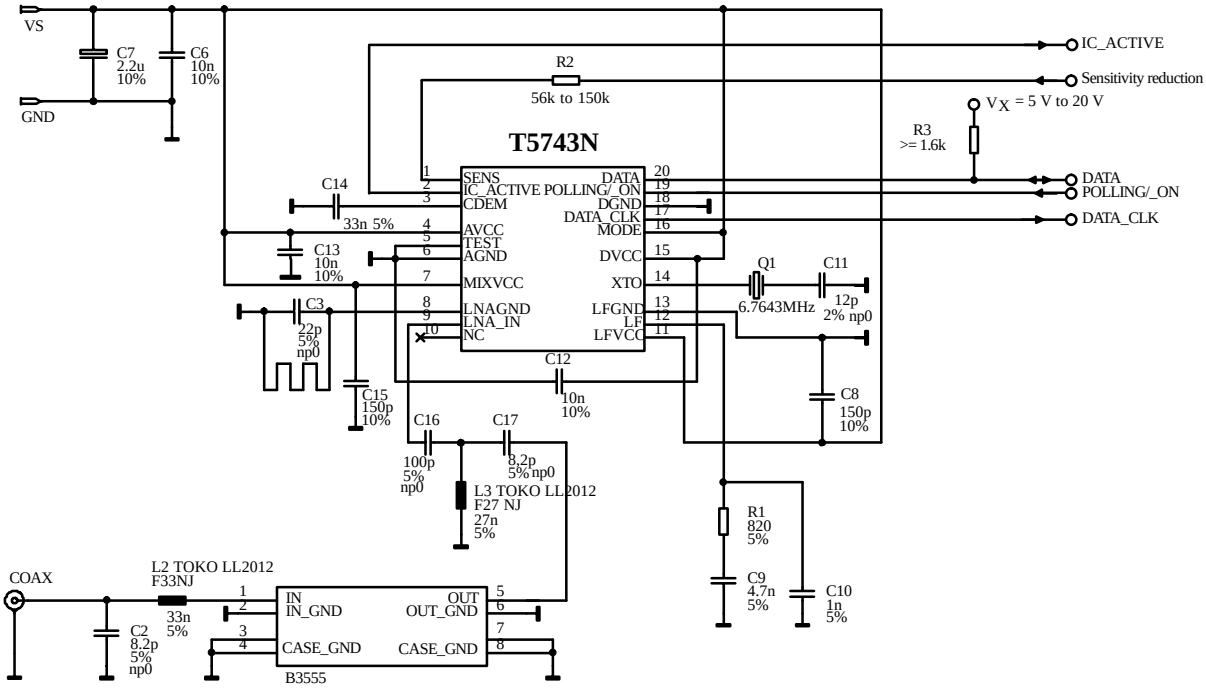


Figure 37. Application circuit: f_{RF} = 433.92 MHz with SAW filter

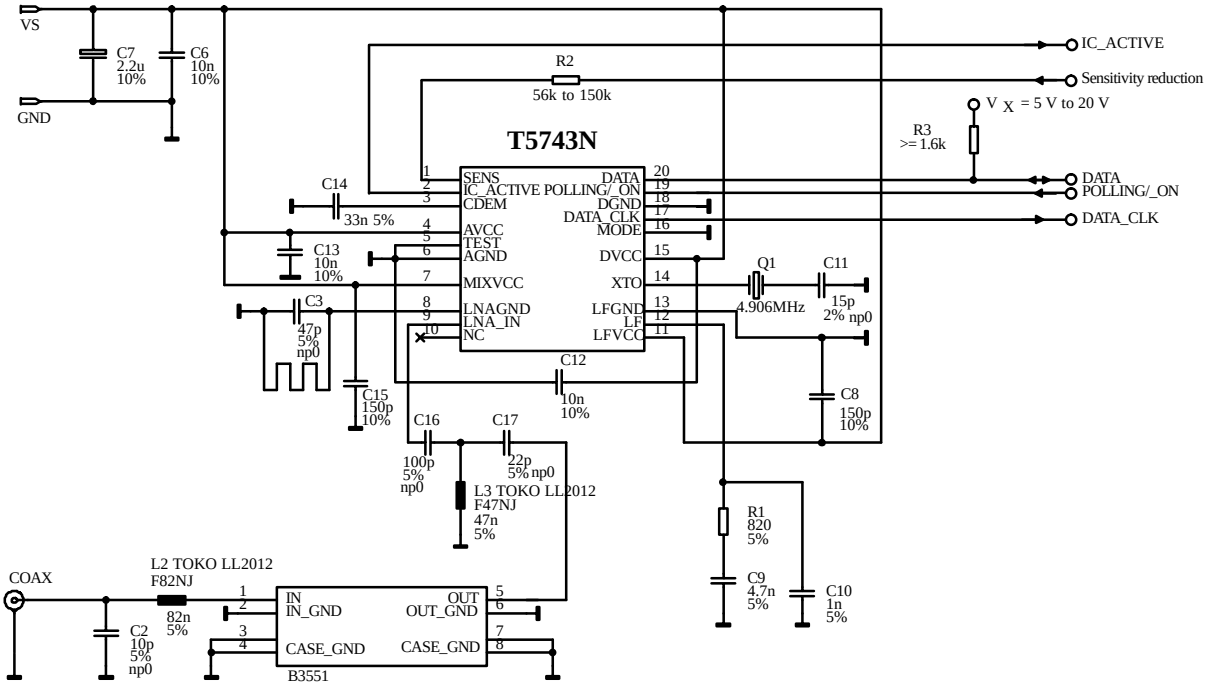


Figure 38. Application circuit: f_{RF} = 315 MHz with SAW filter

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	V_S		6	V
Power dissipation	P_{tot}		1000	mW
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	+125	°C
Ambient temperature	T_{amb}	–40	+105	°C
Maximum input level, input matched to 50 Ω	P_{in_max}		10	dBm

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	100	K/W

Electrical Characteristics

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameter	Test Conditions	Symbol	6.76438 MHz Osc. (MODE: 1)			4.90625 MHz Osc. (MODE: 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Basic clock cycle of the digital circuitry												
Basic clock cycle	MODE = 0 (USA) MODE = 1 (Europe)	T_{Clk}	 2.0697		 2.0697	2.0383		2.0383	$1/f_{XTO}/10$ $1/f_{XTO}/14$		$1/f_{XTO}/10$ $1/f_{XTO}/14$	µs µs
Extended basic clock cycle	BR_Range0 BR_Range1 BR_Range2 BR_Range3	T_{XClk}	16.6 8.3 4.1 2.1		16.6 8.3 4.1 2.1	16.3 8.2 4.1 2.0		16.3 8.2 4.1 2.0	$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$		$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$	µs µs µs µs
Polling mode												
Sleep time see figures 10, 19 and 33	Sleep and XSleep are defined in the OPMODE register	T_{Sleep}	Sleep × X_{Sleep} × 1024 × 2.0697		Sleep × X_{Sleep} × 1024 × 2.0697	Sleep × X_{Sleep} × 1024 × 2.0383		Sleep × X_{Sleep} × 1024 × 2.0383	Sleep × X_{Sleep} × 1024 × T_{Clk}		Sleep × X_{Sleep} × 1024 × T_{Clk}	ms
Start-up time see figures 10 and 11	BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{Startup}$	1855 1061 1061 663		1855 1061 1061 663	1827 1045 1045 653		1827 1045 1045 653	896.5 512.5 512.5 320.5 $\times T_{Clk}$		896.5 512.5 512.5 320.5 $\times T_{Clk}$	µs µs µs µs µs
Time for bit check see figure 10	Average bit-check time while polling, no RF applied, see figures 14 and 15 BR_Range0 BR_Range1 BR_Range2 BR_Range3	$T_{Bit\text{-}check}$		 0.45 0.24 0.14 0.08			 0.45 0.24 0.14 0.08					 ms ms ms ms
	Bit-check time for a valid input signal f_{Sig}, see figure 11 $N_{Bit\text{-}check}$ = 0 $N_{Bit\text{-}check}$ = 3 $N_{Bit\text{-}check}$ = 6 $N_{Bit\text{-}check}$ = 9	$T_{Bit\text{-}check}$	 $3/f_{Sig}$ $6/f_{Sig}$ $9/f_{Sig}$		 $3.5/f_{Sig}$ $6.5/f_{Sig}$ $9.5/f_{Sig}$	 $3/f_{Sig}$ $6/f_{Sig}$ $9/f_{Sig}$		 $3.5/f_{Sig}$ $6.5/f_{Sig}$ $9.5/f_{Sig}$	 $1 \times T_{XClk}$ $3/f_{Sig}$ $6/f_{Sig}$ $9/f_{Sig}$		 $1 \times T_{Clk}$ $3.5/f_{Sig}$ $6.5/f_{Sig}$ $9.5/f_{Sig}$	 ms ms ms ms

Electrical Characteristics (continued)

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameter	Test Conditions	Symbol	6.76438 MHz Osc. (MODE: 1)			4.90625 MHz Osc. (MODE: 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Receiving mode												
Intermediate frequency	MODE=0 (USA) MODE=1 (Europe)	f_{IF}		1.0			1.0		$f_{XTO} \times 64 / 314$ $f_{XTO} \times 64 / 432.92$			MHz MHz
Baud-rate range	BR_Range0 BR_Range1 BR_Range2 BR_Range3	BR_Range	1.0 1.8 3.2 5.6		1.8 3.2 5.6 10.0	1.0 1.8 3.2 5.6		1.8 3.2 5.6 10.0	BR_Range0 × 2 µs / T_{Clk} BR_Range1 × 2 µs / T_{Clk} BR_Range2 × 2 µs / T_{Clk} BR_Range3 × 2 µs / T_{Clk}			kBaud kBaud kBaud kBaud
Minimum time period between edges at Pin DATA See figures 7, 17 and 18 (With the exception of parameter T_{Pulse})	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	t_{DATA_min}	165 83 41.4 20.7		165 83 41.4 20.7	163 81 40.7 20.4		163 81 40.7 20.4	$10 \times T_{XClk}$ $10 \times T_{XClk}$ $10 \times T_{XClk}$ $10 \times T_{XClk}$		$10 \times T_{XClk}$ $10 \times T_{XClk}$ $10 \times T_{XClk}$ $10 \times T_{XClk}$	µs µs µs µs
Maximum Low period at Pin DATA See figures 7 and 18	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	$t_{DATA\_L\_max}$	2152 1076 538 270		2152 1076 538 270	2120 1060 530 265		2120 1060 530 265	130 × T_{XClk} 130 × T_{XClk} 130 × T_{XClk} 130 × T_{XClk}		130 × T_{XClk} 130 × T_{XClk} 130 × T_{XClk} 130 × T_{XClk}	µs µs µs µs
Delay to activate the start-up mode See figure 21		Ton1	19.7		21.8	19.4		21.5	$9.5 \times T_{Clk}$		$10.5 \times T_{Clk}$	µs
OFF– command at Pin POLLING/_ON See figure 20		Ton2	16.6			16.4			$8 \times T_{Clk}$			µs
Delay to activate the sleep mode See figure 20		Ton3	17.6		19.7	17.4		19.4	$8.5 \times T_{Clk}$		$9.5 \times T_{Clk}$	µs
Pulse on Pin DATA at the end of a data stream See figure 30	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	T_{Pulse}	16.6 8.3 4.1 2.1		16.6 8.3 4.1 2.1	16.3 8.2 4.1 2.0		16.3 8.2 4.1 2.0	$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$		$8 \times T_{Clk}$ $4 \times T_{Clk}$ $2 \times T_{Clk}$ $1 \times T_{Clk}$	µs µs µs µs

Electrical Characteristics (continued)

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameter	Test Conditions	Symbol	6.76438 MHz Osc. (MODE: 1)			4.90625 MHz Osc. (MODE: 0)			Variable Oscillator			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Configuration of the receiver												
Frequency of the reset marker	See figure 31	f_{RM}	117.9		117.9	119.8		119.8	$\frac{1}{4096 \times T_{Clk}}$		$\frac{1}{4096 \times T_{Clk}}$	Hz
Programming start pulse See figures 19 and 33	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3 after POR	t1	 3367 2277 1735 1464 16.43		 11650 11650 11650 11650	 3311 2243 1709 1442 16,18		 11470 11470 11470 11470	 $1624 \times T_{Clk}$ $1100 \times T_{Clk}$ $838 \times T_{Clk}$ $707 \times T_{Clk}$ $7936 \times T_{Clk}$		 $5632 \times T_{Clk}$ $5632 \times T_{Clk}$ $5632 \times T_{Clk}$ $5632 \times T_{Clk}$	 µs µs µs µs µs
Programming delay period	See figures 19 and 33	t2	795		798	783		786	$384.5 \times T_{Clk}$		$385.5 \times T_{Clk}$	µs
Synchronization pulse		t3	265		265	261		261	$128 \times T_{Clk}$		$128 \times T_{Clk}$	µs
Delay until of the program window starts		t4	131		131	129		129	$63.5 \times T_{Clk}$		$63.5 \times T_{Clk}$	µs
Programming window		t5	530		530	522		522	$256 \times T_{Clk}$		$256 \times T_{Clk}$	µs
Time frame of a bit (figure 33)		t6	1060		1060	1044		1044	$512 \times T_{Clk}$		$512 \times T_{Clk}$	µs
Programming pulse (figures 19 and 33)		t7	132		529	130		521	$64 \times T_{Clk}$		$256 \times T_{Clk}$	µs
Equivalent acknowledge pulse: E_Ack (figure 33)		t8	265		265	261		261	$128 \times T_{Clk}$		$128 \times T_{Clk}$	µs
Equivalent time window (figure 33)		t9	534		534	526		526	$258 \times T_{Clk}$		$258 \times T_{Clk}$	µs
OFF-bit programming window (figure 19)		t10	930		930	916		916	$449.5 \times T_{Clk}$		$449.5 \times T_{Clk}$	µs
Data clock												
Minimum delay time between edge @ DATA and DATA_CLK See figures 26 and 27	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	t_{Delay2}	 0 0 0 0		 16.6 8.3 4.15 2.07	 0 0 0 0		 16.3 8.2 4.08 2.04	 0 0 0 0		 $1 \times T_{XClk}$ $1 \times T_{XClk}$ $1 \times T_{XClk}$ $1 \times T_{XClk}$	 µs µs µs µs
Pulswidth of negative pulse @ Pin DATA_CLK See figures 26 and 27	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3	$t_{P\_DATA\_CLK}$	 66.2 33.1 16.56 8.3		 66.2 33.1 16.56 8.3	 65.2 32.6 16.3 8.2		 65.2 32.6 16.3 8.2	 $4 \times T_{XClk}$ $4 \times T_{XClk}$ $4 \times T_{XClk}$ $4 \times T_{XClk}$		 $4 \times T_{XClk}$ $4 \times T_{XClk}$ $4 \times T_{XClk}$ $4 \times T_{XClk}$	 µs µs µs µs

Electrical Characteristics (continued)

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Sleep mode (XTO and polling logic active)	IS_{off}		170	276	µA
	IC active (start-up-, bit check-, receiving mode) Pin DATA = H FSK ASK	IS_{on}		7.5 7.1	9.1 8.7	mA mA
LNA mixer (input matched according to figure 6)						
Third-order intercept point	LNA/ mixer/ IF amplifier	IIP3		–28		dBm
LO spurious emission @ RF_{In}	Required according to I–ETS 300220	IS_{LORF}		–73	–57	dBm
Noise figure LNA and mixer (DSB)		NF		7		dB
LNA_IN input impedance	@ 433.92 MHz @ 315 MHz	Zi_{LNA_IN}		1.0 || 1.56 1.3 || 1.0		kΩ || pF kΩ || pF
1 dB compression point (LNA, mixer, IF amplifier)	Referred to RF_{in}	IP_{1db}		–40		dBm
Maximum input level	BER ≤ 10^{-3}, FSK mode ASK mode	P_{in_max}			–22 –20	dBm dBm
Local oscillator						
Operating frequency range VCO		f_{VCO}	299		449	MHz
Phase noise VCO / LO	f_{osc} = 432.92 MHz @ 1 MHz @ 10 MHz	L (fm)		 –93 –113	 –90 –110	 dBC/Hz dBC/Hz
Spurious of the VCO	@ ± f_{XTO}			–55	–47	dBC
VCO gain		K_{VCO}		190		MHz/V
Loop bandwidth of the PLL	For best LO noise (design parameter) R1 = 820 Ω C9 = 4.7 nF C10 = 1 nF	B_{Loop}		100		kHz
Capacitive load at Pin LF	The capacitive load at Pin LF is limited if bit check is used. The limitation therefore also applies to self polling.	C_{LF_tot}			10	nF
XTO operating frequency	XTO crystal frequency, appropriate load capacitance must be connected to XTAL f_{XTAL} = 6.764375 MHz (EU) f_{XTAL} = 4.90625 MHz (US)	f_{XTO}	–30 ppm	f_{XTAL}	+30 ppm	MHz
Series resonance resistor of the crystal	f_{XTO} = 6.764 MHz 4.906 MHz	R_S			150 220	Ω Ω
Static capacitance at Pin XTO to GND		C_0			6.5	pF

Electrical Characteristics (continued)

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Analog signal processing						
Input sensitivity ASK	Input matched according to figure 6 ASK (level of carrier) BER ≤ 10^{-3} f_{in} = 433.92 MHz / 315 MHz V_S = 5 V, T_{amb} = 25°C f_{IF} = 1 MHz					
	BR_Range0	P_{Ref_ASK}	–108	–110	–112	dBm
	BR_Range1		–106.5	–108.5	–110.5	dBm
	BR_Range2		–106	–108	–110	dBm
	BR_Range3		–104	–106	–108	dBm
Sensitivity variation ASK for the full operating range compared to T_{amb} = 25°C, V_S = 5 V	f_{in} = 433.92 MHz / 315 MHz f_{IF} = 1 MHz $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	ΔP_{Ref}	+2.5		–1.5	dB
Sensitivity variation ASK for full operating range including IF filter compared to T_{amb} = 25°C, V_S = 5 V,	f_{in} = 433.92 MHz / 315 MHz f_{IF} = 0.79 MHz to 1.21 MHz f_{IF} = 0.73 MHz to 1.27 MHz $P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$	ΔP_{Ref}	+5.5 +7.5		–1.5 –1.5	dB dB
Input sensitivity FSK	Input matched according to figure 6, BER ≤ 10^{-3} f_{in} = 433.92 MHz / 315 MHz V_S = 5 V, T_{amb} = 25°C f_{IF} = 1 MHz					
	BR_Range0 df = +/– 16 kHz df = +/– 10 kHz to +/– 100 kHz	P_{Ref_FSK}	–101 –99	–104	–105.5 –105.5	dBm dBm
	BR_Range1 df = +/– 16 kHz df = +/– 10 kHz to +/– 100 kHz	P_{Ref_FSK}	–99 –97	–102	–103.5 –103.5	dBm dBm
	BR_Range2 df = +/– 16 kHz df = +/– 10 kHz to +/– 100 kHz	P_{Ref_FSK}	–97.5 –95.5	–100.5	–102 –102	dBm dBm
	BR_Range3 df = +/– 16 kHz df = +/– 10 kHz to +/– 100 kHz	P_{Ref_FSK}	–95.5 –93.5	–98.5	–100 –100	dBm dBm
Sensitivity variation FSK for the full operating range compared to T_{amb} = 25°C, V_S = 5 V	f_{in} = 433.92 MHz/ 315 MHz f_{IF} = 1 MHz $P_{FSK} = P_{Ref\_FSK} + \Delta P_{Ref}$	ΔP_{Ref}	+3		–1.5	dB
Sensitivity variation FSK for the full operating range including IF filter compared to T_{amb} = 25°C, V_S = 5 V	f_{in} = 433.92 MHz/ 315 MHz f_{IF} = 0.85 MHz to 1.15 MHz f_{IF} = 0.80 MHz to 1.20 MHz f_{IF} = 0.74 MHz to 1.26 MHz $P_{FSK} = P_{Ref\_FSK} + \Delta P_{Ref}$	ΔP_{Ref}	+6 +8 +11		–2 –2 –2	dB dB dB

Electrical Characteristics (continued)

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
S/N ratio to suppress inband noise signals. Noise signals may have any modulation scheme	ASK mode FSK mode	SNR_{ASK} SNR_{FSK}			12 3	dB dB
Dynamic range RSSI ampl.		DR_{RSSI}		60		dB
Lower cut-off frequency of the data filter	$f_{cu\_DF} = \frac{1}{2 \times \pi \times 30k\Omega \times CDEM}$ CDEM = 33 nF	f_{cu_DF}	0.11	0.16	0.20	kHz
Recommended CDEM for best performance	BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	CDEM		39 22 12 8.2		nF nF nF nF
Edge-to-edge time period of the input data signal for full sensitivity	BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	t_{ee_sig}	270 156 89 50		1000 560 320 180	µs µs µs µs
Upper cut-off frequency data filter	Upper cut-off frequency programmable in 4 ranges via a serial mode word BR_Range0 (default) BR_Range1 BR_Range2 BR_Range3	f_u	 2.8 4.8 8.0 15.0	 3.4 6.0 10.0 19.0	 4.0 7.2 12.0 23.0	 kHz kHz kHz kHz
Reduced sensitivity	R_{Sense} connected from Pin Sens to V_S, input matched according to figure 6					dBm (peak level)
	R_{Sense} = 56 kΩ, f_{in} = 433.92 MHz,	P_{Ref_Red}	–67	–72	–77	dBm
	R_{Sense} = 100 kΩ, f_{in} = 433.92 MHz	P_{Ref_Red}	–76	–81	–86	dBm
	R_{Sense} = 56 kΩ, f_{in} = 315 MHz	P_{Ref_Red}	–68	–73	–78	dBm
	R_{Sense} = 100 kΩ, f_{in} = 315 MHz	P_{Ref_Red}	–77	–82	–87	dBm
Reduced sensitivity variation over full operating range	R_{Sense} = 56 kΩ R_{Sense} = 100 kΩ $P_{Red} = P_{Ref\_Red} + \Delta P_{Red}$	ΔP_{Red}	5 6	0 0	0 0	dB dB
Reduced sensitivity variation for different values of R_{Sense}	Values relative to R_{Sense} = 56 kΩ R_{Sense} = 56 kΩ R_{Sense} = 68 kΩ R_{Sense} = 82 kΩ R_{Sense} = 100 kΩ R_{Sense} = 120 kΩ R_{Sense} = 150 kΩ $P_{Red} = P_{Ref\_Red} + \Delta P_{Red}$	 ΔP_{Red} ΔP_{Red} ΔP_{Red} ΔP_{Red} ΔP_{Red} ΔP_{Red}	 0 –3.5 –6.0 –9.0 –11.0 –13.5			 dB dB dB dB dB dB
Threshold voltage for reset		$V_{ThRESET}$	1.95	2.8	3.75	V

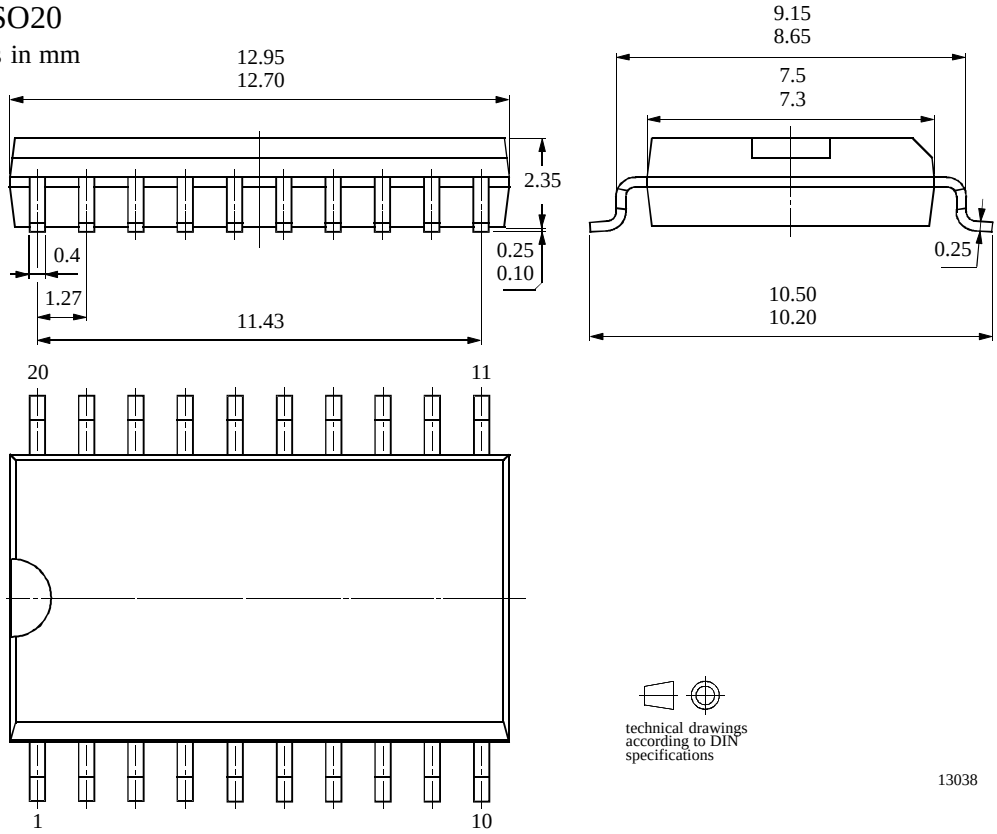
Electrical Characteristics (continued)

All parameters refer to GND, T_{amb} = –40°C to +105°C, V_S = 4.5 V to 5.5 V, f_0 = 433.92 MHz and f_0 = 315 MHz, unless otherwise specified. (For typical values: V_S = 5 V, T_{amb} = 25°C)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Digital ports						
Data output – Saturation voltage Low – max voltage @ Pin DATA – quiescent current – short–circuit current – ambient temp. in case of permanent short–circuit	 $I_{ol} \le 12$ mA I_{ol} = 2 mA V_{oh} = 20 V V_{ol} = 0.8 to 20 V V_{oh} = 0V to 20 V	 V_{ol} V_{ol} V_{oh} I_{qu} I_{ol_lim} t_{amb_sc}	 13 	 0.35 0.08 30 	 0.8 0.3 20 20 45 85	 V V V µA mA °C
Data input – Input voltage Low – Input voltage High		 V_{Il} V_{ich}	 $0.65 \times V_S$	 	 $0.35 \times V_S$ 	 V V
DATA_CLK output – Saturation voltage Low – Saturation voltage High	 IDATA_CLK = 1mA IDATA_CLK = –1mA	 V_{ol} V_{oh}	 V_S–0.4 V 	 0.1 V_S–0.15 V	 0.4 	 V V
IC_ACTIVE output – Saturation voltage Low – Saturation voltage High	 IIC_ACTIVE = 1mA IIC_ACTIVE = –1mA	 V_{ol} V_{oh}	 V_S–0.4 V 	 0.1 V_S–0.15 V	 0.4 	 V V
POLLING/_ON input – Low level input voltage – High level input voltage	 Receiving mode Polling mode	 V_{Il} V_{Ih}	 $0.8 \times V_S$	 	 $0.2 \times V_S$ 	 V V
MODE input – Low level input voltage – High level input voltage	 Division factor = 10 Division factor = 14	 V_{Il} V_{Ih}	 $0.8 \times V_S$	 	 $0.2 \times V_S$ 	 V V
TEST input – Low level input voltage	Test input must always be set to Low	V_{Il}			$0.2 \times V_S$	V

Package Information

Package SO20
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.atmel–wm.com

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