

ZL30165 Quad Clock Translator

Short Form Data Sheet

April 2013

Features

- · Four independent clock channels
- Four programmable digital PLLs/Numerically Controlled Oscillators (NCOs)
- Programmable synthesizers generate any clockrate from 1 kHz to 750 MHz
- Four precision synthesizers generate clocks with low jitter of 0.63 ps RMS for 10 G PHYs
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 750 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter at 5.2 Hz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Eight reference inputs configurable as single ended or differential

Ordering Information

ZL30165GDG2 144 Pin LBGA

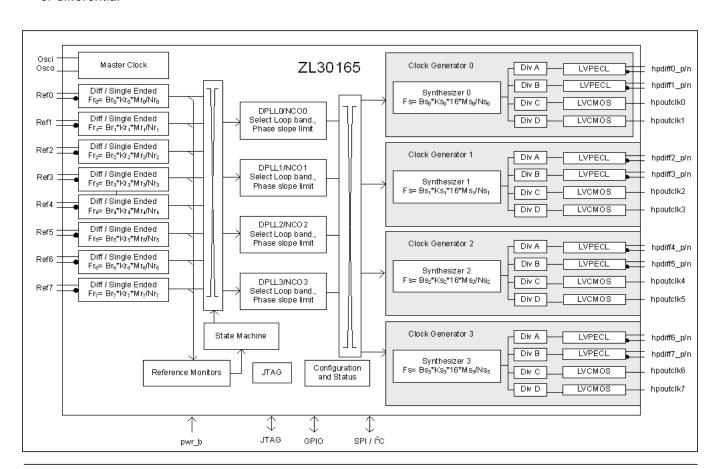
Trays

Pb Free Tin/Silver/Copper -40°C to +85°C Package Size: 13 x 13 mm

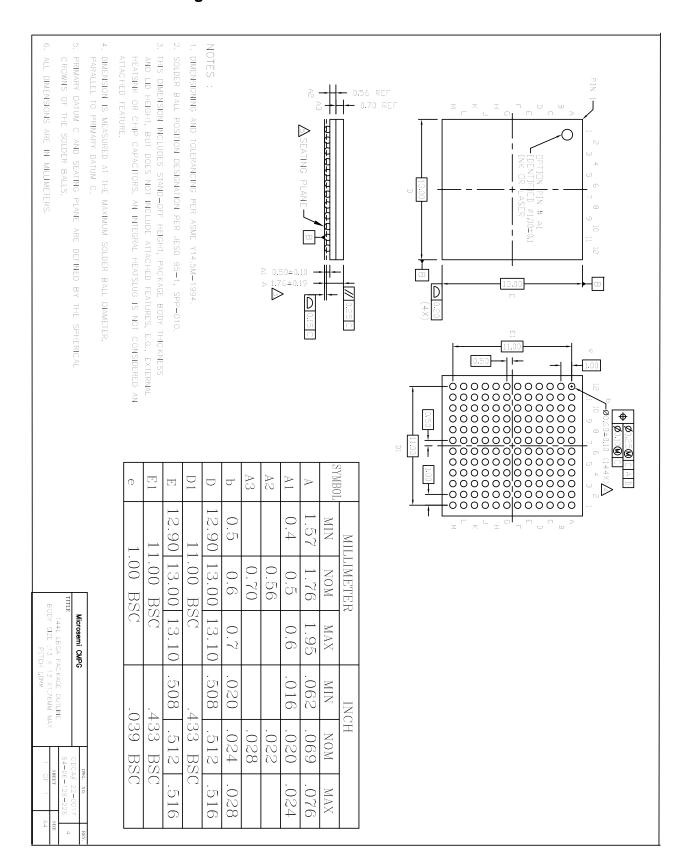
- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Field programmable via SPI/I²C interface

Applications

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI



1.0 Mechanical Drawing





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