FAIRCHILD SEMICONDUCTOR®

March 2007

74AC520, 74ACT520
8-Bit Identity Comparator

Features

- Compares two 8-bit words in 6.5ns typ.
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24mA
- ACT520 has TTL-compatible inputs

General Description

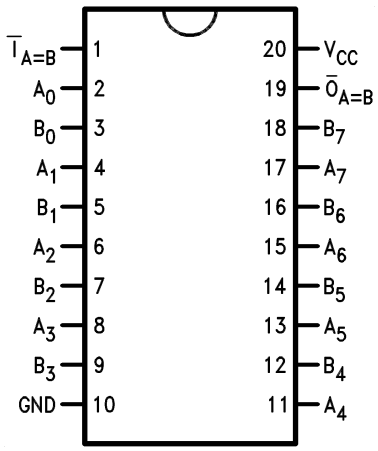
The AC/ACT520 are expandable 8-bit comparators. They compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Ordering Information

Order Number	Package Number	Package Description
74AC520SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT520SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT520SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT520PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

Connection Diagram



Pin Descriptions

Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$T_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

Truth Table

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	$A = B^{(1)}$	L
L	$A \neq B$	H
H	$A = B^{(1)}$	H
H	$A \neq B$	H

H = HIGH Voltage Level

L = LOW Voltage Level

Note:

1. $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

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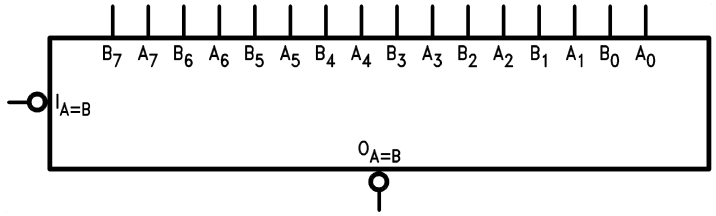
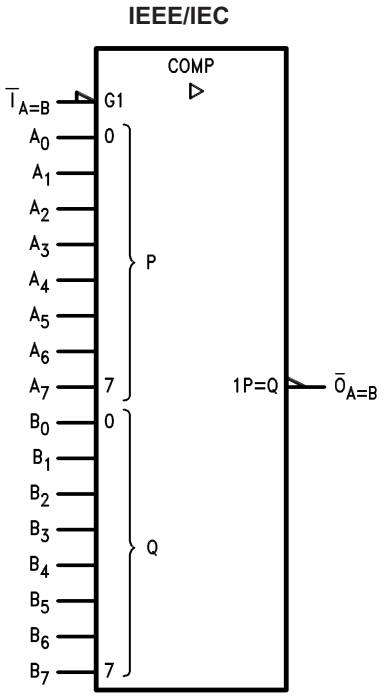
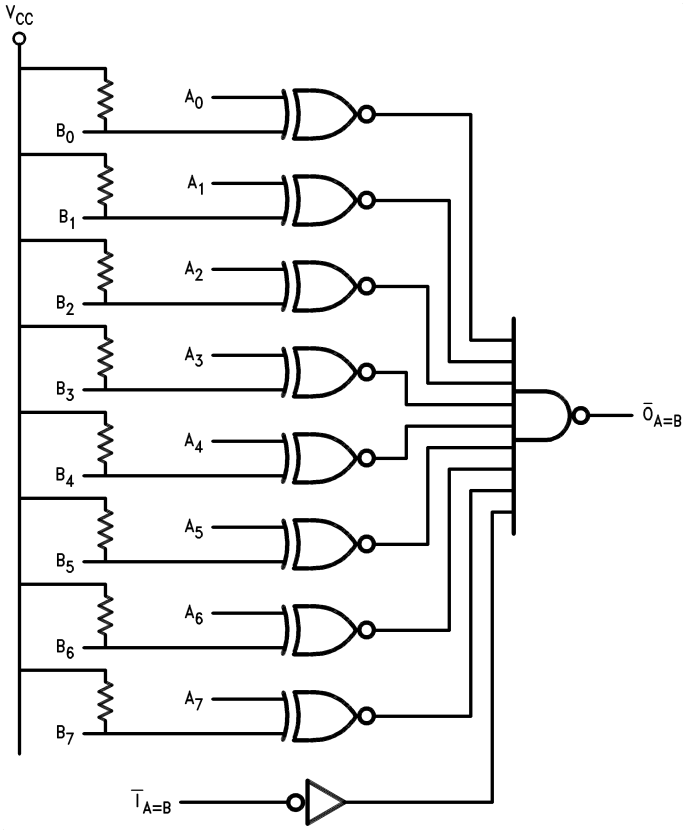
Logic Symbols





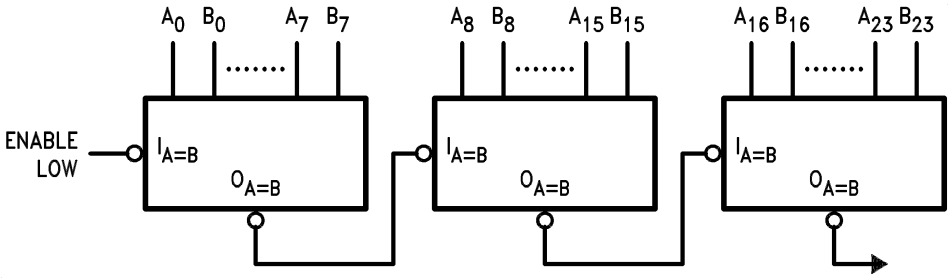
Logic Diagram



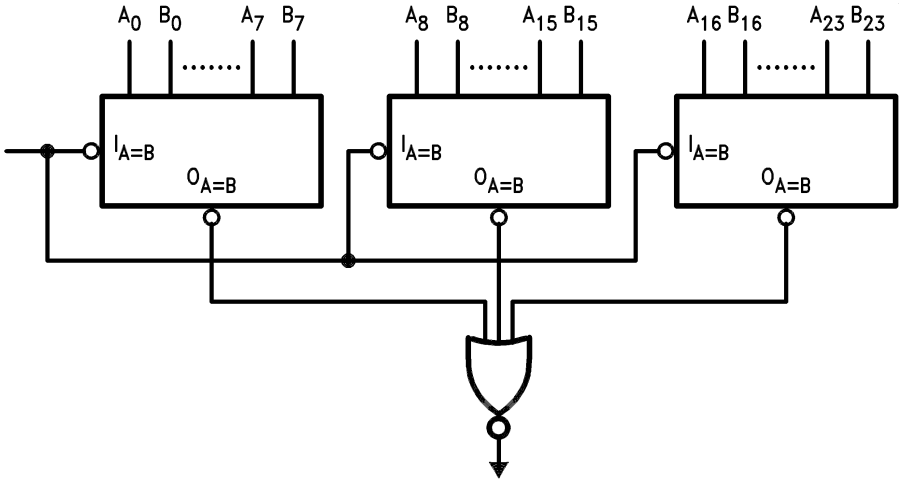
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Applications

Ripple Expansion



Parallel Expansion



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	
	AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices:	125mV/ns
	V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	I_{OUT} = –50µA	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –12mA		2.56	2.46	
		4.5	I_{OH} = –24mA		3.86	3.76	
		5.5	I_{OH} = –24mA[2]		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	I_{OUT} = 50µA	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	V_{IN} = V_{IL} or V_{IH}: I_{OL} = 12mA		0.36	0.44	
		4.5	I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA[2]		0.36	0.44	
I_{IN}[4]	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND, A Inputs Only		±0.1	±1.0	µA
I_{IH}	Maximum Input HIGH Leakage Current	5.5	V_I = V_{CC}, B Inputs Only		10.0	10.0	µA
I_{IL}	Maximum Input LOW Leakage Current	5.5	V_I = V_{CC}, B Inputs Only	–0.3	–0.6	–1.0	mA
I_{OLD}	Minimum Dynamic Output Current[3]	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC}		4.0	40.0	µA
I_{CC}[4]	Maximum Quiescent Supply Current	5.5	V_{IN} = GND	2.3	4.8	8.0	mA

Notes:

2. All outputs loaded; thresholds on input associated with output under test.

3. Maximum test duration 2.0ms, one output loaded at a time.

4. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = –50µA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –24mA		3.86	3.76	
		5.5	I_{OH} = –24mA(5)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50µA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA(5)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	µA
I_{IH}	Maximum Input HIGH Leakage Current	5.5	V_I = V_{CC}, B Inputs Only		10.0	10.0	µA
I_{IL}	Maximum Input LOW Leakage Current	5.5	V_I = V_{CC}, B Inputs Only	–0.3	–0.6	–1.0	mA
I_{CCT}	Maximum I_{CC}/Input	5.5	V_I = V_{CC} – 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current(6)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	µA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = GND	2.3	4.8	8.0	mA

Notes:

5. All outputs loaded; thresholds on input associated with output under test.

6. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[7]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, A_n or B_n to $\overline{O}_{A=B}$	3.3	4.0	7.5	11.5	3.0	13.0	ns
		5.0	2.5	5.5	8.5	2.0	9.5	
t_{PHL}	Propagation Delay, A_n or B_n to $\overline{O}_{A=B}$	3.3	4.5	8.0	12.0	3.5	13.5	ns
		5.0	3.0	5.5	9.0	2.5	10.0	
t_{PLH}	Propagation Delay, $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.5	5.5	8.5	2.5	9.5	ns
		5.0	2.5	4.5	6.5	2.0	7.0	
t_{PHL}	Propagation Delay, $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.5	5.5	8.5	2.5	9.5	ns
		5.0	2.5	4.5	6.5	2.0	7.0	

Note:

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[8]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50 pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	5.5	8.5	2.5	9.5	ns
t_{PHL}	Propagation Delay, A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	6.0	10.0	2.5	11.5	ns
t_{PLH}	Propagation Delay, $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.0	4.0	6.0	2.0	6.5	ns
t_{PHL}	Propagation Delay, $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.5	5.0	7.5	2.0	8.5	ns

Note:

8. Voltage range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	40	pF

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

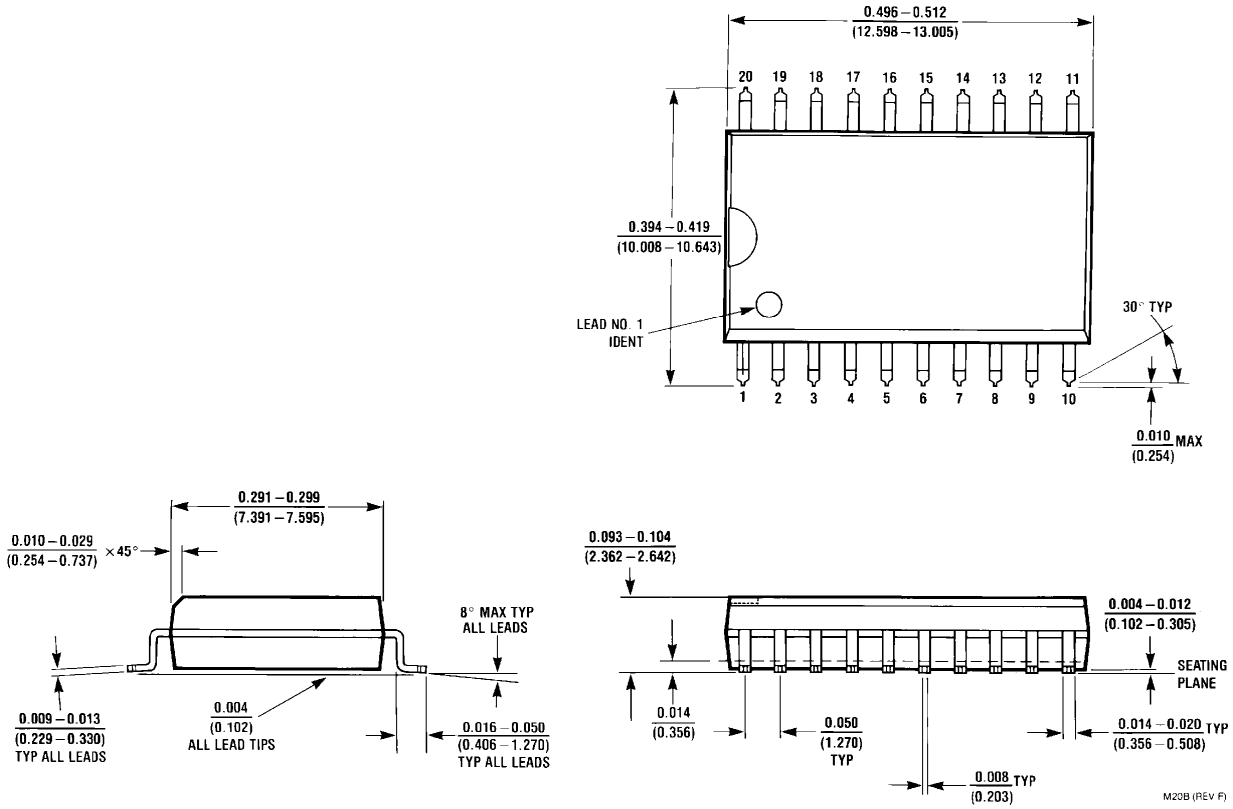
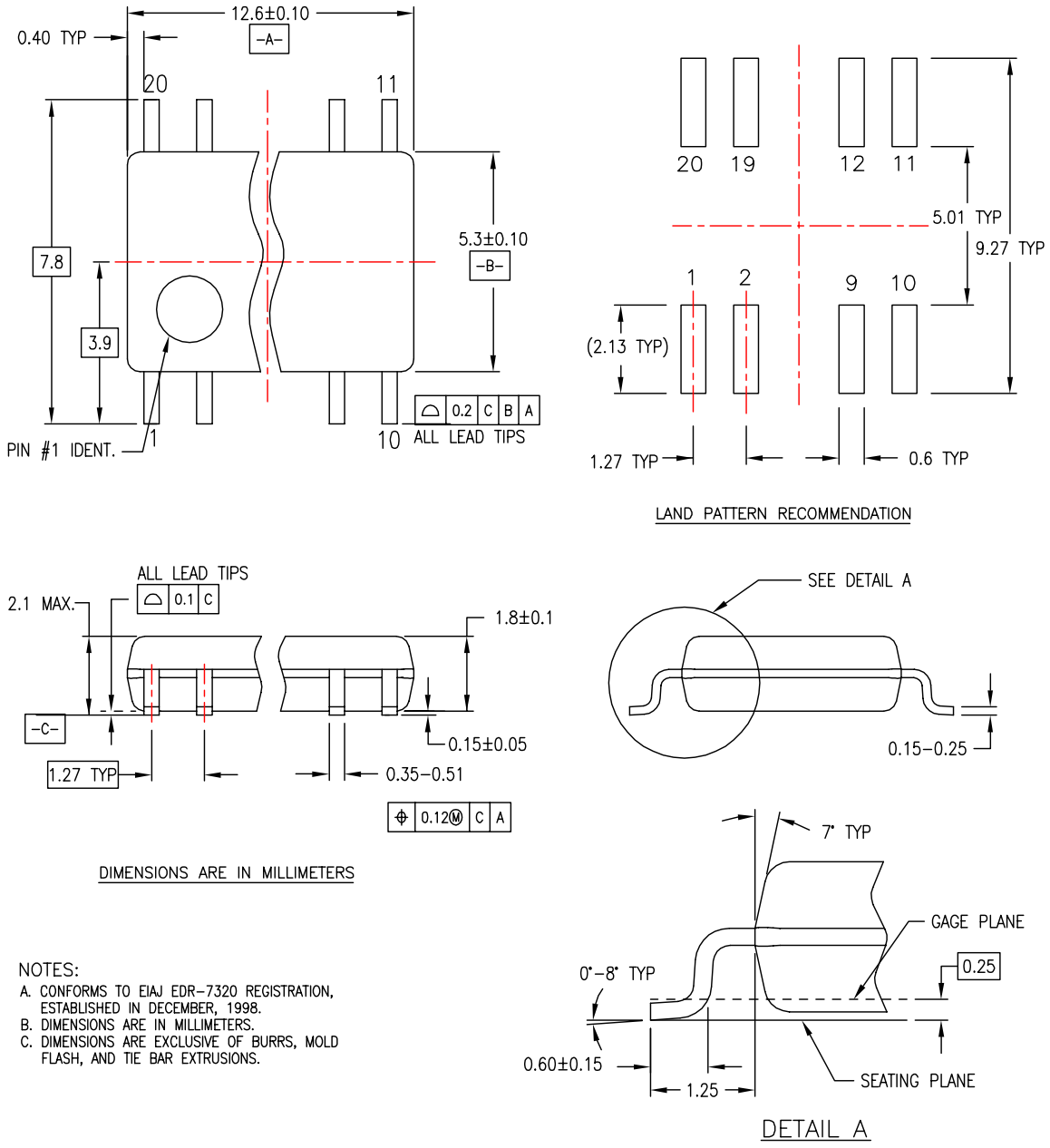


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

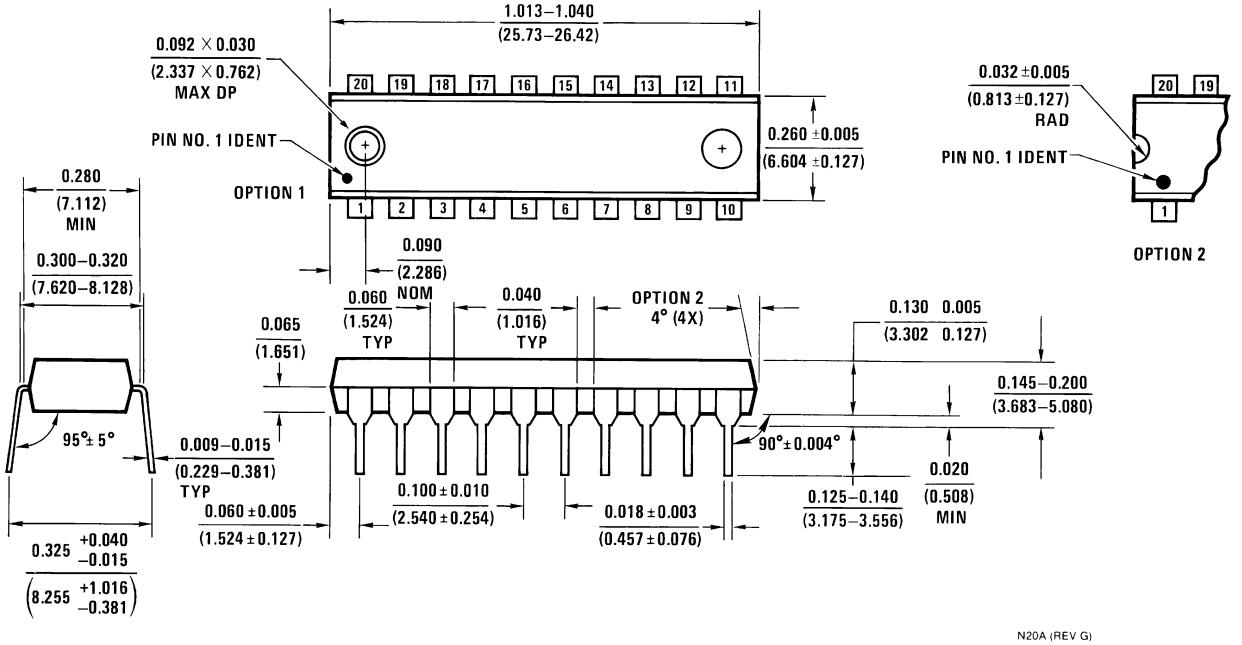


Figure 3. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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SuperSOT™-8
SyncFET™
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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