# 74LV132-Q100

## Quad 2-input NAND Schmitt trigger

Rev. 1 — 11 November 2013 Product data sheet

## 1. General description

The 74LV132-Q100 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC132-Q100 and 74HCT132-Q100.

The 74LV132-Q100 contains four 2-input NAND gates which accept standard input signals. These gates are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage $V_{T+}$ and the negative voltage $V_{T-}$ is defined as the input hysteresis voltage $V_H$.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC}$ = 2.7 V and $V_{CC}$ = 3.6 V
- Typical output ground bounce < 0.8 V at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C
- Typical HIGH-level output voltage ($V_{OH}$) undershoot: > 2 V at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

## 3. Applications

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LV132D-Q100 | −40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LV132PW-Q100 | −40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74LV132BQ-Q100 | −40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

## 5. Functional diagram

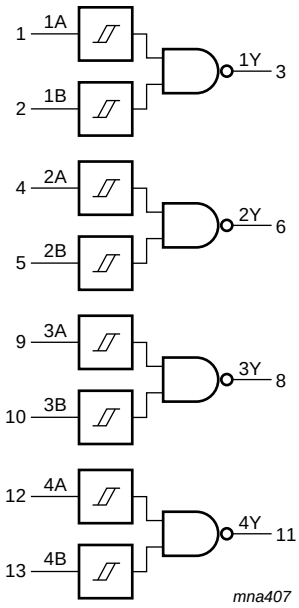



**Fig 1. Logic symbol**

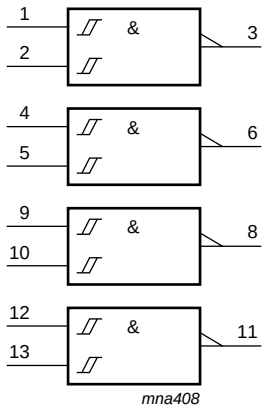



**Fig 2. IEC logic symbol**

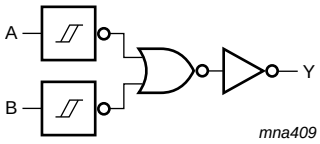



**Fig 3. Logic diagram (one gate)**

# 6. Pinning information

## 6.1 Pinning

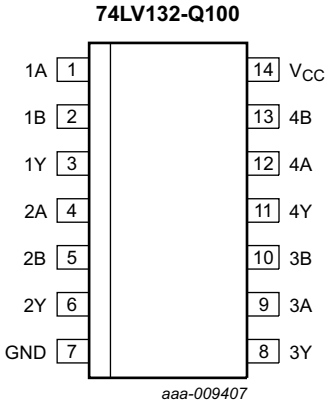
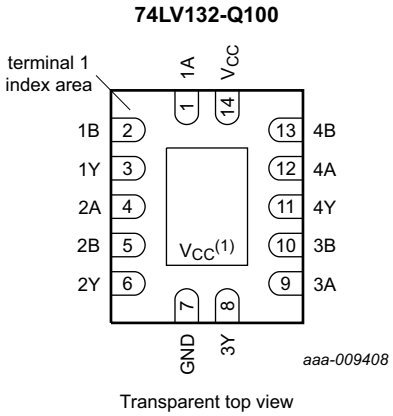



Fig 4. Pin configuration SO14 and TSSOP14




Transparent top view

(1) The die substrate is attached to the exposed die pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN14

## 6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| 1A | 1 | data input |
| 1B | 2 | data input |
| 1Y | 3 | data output |
| 2A | 4 | data input |
| 2B | 5 | data input |
| 2Y | 6 | data output |
| GND | 7 | ground (0 V) |
| 3Y | 8 | data output |
| 3A | 9 | data input |
| 3B | 10 | data input |
| 4Y | 11 | data output |
| 4A | 12 | data input |
| 4B | 13 | data input |
| $V_{CC}$ | 14 | supply voltage |

# 7. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

| Input | | Output |
|---|---|---|
| **nA** | **nB** | **nY** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

# 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±50 | mA |
| $I_O$ | output current | $V_O = –0.5$ V to $(V_{CC} + 0.5$ V) | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 50 | mA |
| $I_{GND}$ | ground current | | | –50 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = –40$ °C to +125 °C | | | | |
| | SO14 package | | [2] | - | 500 | mW |
| | TSSOP14 package | | [3] | - | 500 | mW |
| | DHVQFN14 package | | [4] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

[3] $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

[4] $P_{tot}$ derates linearly with 4.5 mW/K above 60 °C.

# 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | [1] | 1.0 | 3.3 | 5.5 | V |
| $V_I$ | input voltage | | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | | −40 | +25 | +125 | °C |

[1] The static characteristics are guaranteed from $V_{CC}$ = 1.2 V to $V_{CC}$ = 5.5 V. LV devices are guaranteed to function down to $V_{CC}$ = 1.0 V (with input levels GND or $V_{CC}$).

# 10. Static characteristics

**Table 6. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{T+}$ or $V_{T-}$ | | | | | | |
| | | $I_O$ = −100 μA; $V_{CC}$ = 1.2 V | - | 1.2 | - | - | - | V |
| | | $I_O$ = −100 μA; $V_{CC}$ = 2.0 V | 1.8 | 2.0 | - | 1.8 | - | V |
| | | $I_O$ = −100 μA; $V_{CC}$ = 2.7 V | 2.5 | 2.7 | - | 2.5 | - | V |
| | | $I_O$ = −100 μA; $V_{CC}$ = 3.0 V | 2.8 | 3.0 | - | 2.8 | - | V |
| | | $I_O$ = −100 μA; $V_{CC}$ = 4.5 V | 4.3 | 4.5 | - | 4.3 | - | V |
| | | $I_O$ = −6 mA; $V_{CC}$ = 3.0 V | 2.4 | 2.82 | - | 2.2 | - | V |
| | | $I_O$ = −12 mA; $V_{CC}$ = 4.5 V | 3.6 | 4.2 | - | 3.5 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{T+}$ or $V_{T-}$ | | | | | | |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.2 V | - | 0 | - | - | - | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 2.7 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 3.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 3.0 V | - | 0.25 | 0.40 | - | 0.50 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 4.5 V | - | 0.35 | 0.55 | - | 0.65 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 1.0 | μA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 20.0 | - | 40 | μA |
| $\Delta I_{CC}$ | additional supply current | per input; $V_I = V_{CC}$ − 0.6 V; $V_{CC}$ = 2.7 V to 3.6 V | - | - | 500 | - | 850 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

# 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; for test circuit, see Figure 7.*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nA, nB to nY; see Figure 6 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 65 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 18 | 34 | - | 43 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 15 | 24 | - | 30 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 15 pF | [3] | - | 10 | - | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 12 | 20 | - | 25 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | - | 9.0 | 14 | - | 17 | ns |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 24 | - | - | - | pF |

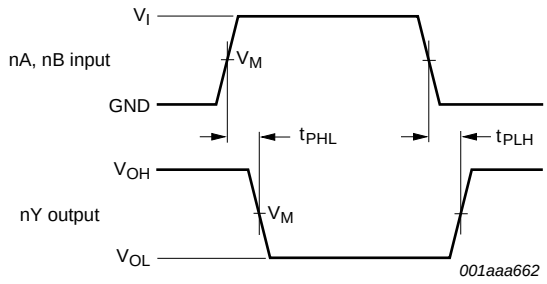
[1] All typical values are measured at $T_{amb}$ = 25 °C.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V and $V_{CC}$ = 5.0 V).

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in V
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

# 12. Waveforms



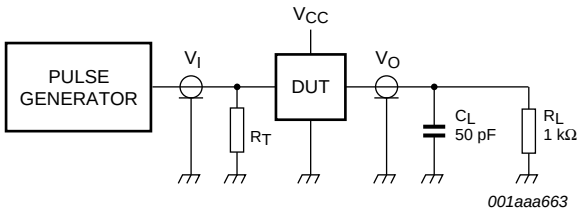

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 6. The input (nA, nB) to output (nY) propagation delays**

**Table 8. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V |
| ≥ 4.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

**Fig 7. Load circuit for switching times**

**Table 9. Test data**

| Supply voltage | Input | |
|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ |
| < 2.7 V | $V_{CC}$ | ≤ 2.5 ns |
| 2.7 V to 3.6 V | 2.7 V | ≤ 2.5 ns |
| ≥ 4.5 V | $V_{CC}$ | ≤ 2.5 ns |

## 13. Transfer characteristics

**Table 10. Transfer characteristics**

*GND = 0 V; for test circuit, see Figure 7.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{T+}$ | positive-going threshold voltage | see Figure 6 | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 0.70 | - | - | - | V |
| | | $V_{CC}$ = 2.0 V | 0.8 | 1.10 | 1.4 | 0.8 | 1.4 | V |
| | | $V_{CC}$ = 2.7 V | 1.0 | 1.45 | 2.0 | 1.0 | 2.0 | V |
| | | $V_{CC}$ = 3.0 V | 1.2 | 1.60 | 2.2 | 1.2 | 2.2 | V |
| | | $V_{CC}$ = 3.6 V | 1.5 | 1.95 | 2.4 | 1.5 | 2.4 | V |
| | | $V_{CC}$ = 4.5 V | 1.7 | 2.50 | 3.2 | 1.7 | 3.2 | V |
| | | $V_{CC}$ = 5.5 V | 2.1 | 3.00 | 3.9 | 2.1 | 3.9 | V |

**Table 10. Transfer characteristics** *…continued*

*GND = 0 V; for test circuit, see Figure 7.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{T-}$ | negative-going threshold voltage | see Figure 6 | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 0.34 | - | - | - | V |
| | | $V_{CC}$ = 2.0 V | 0.3 | 0.65 | 0.9 | 0.3 | 0.9 | V |
| | | $V_{CC}$ = 2.7 V | 0.4 | 0.90 | 1.4 | 0.4 | 1.4 | V |
| | | $V_{CC}$ = 3.0 V | 0.6 | 1.05 | 1.5 | 0.6 | 1.5 | V |
| | | $V_{CC}$ = 3.6 V | 0.8 | 1.30 | 1.8 | 0.8 | 1.8 | V |
| | | $V_{CC}$ = 4.5 V | 0.9 | 1.60 | 2.0 | 0.9 | 2.0 | V |
| | | $V_{CC}$ = 5.5 V | 1.2 | 2.00 | 2.6 | 1.2 | 2.6 | V |
| $V_H$ | hysteresis voltage | ($V_{T+} - V_{T-}$); see Figure 6 | | | | | | |
| | | $V_{CC}$ = 1.2 V | - | 0.3 | - | - | - | V |
| | | $V_{CC}$ = 2.0 V | 0.2 | 0.55 | 0.8 | 0.2 | 0.8 | V |
| | | $V_{CC}$ = 2.7 V | 0.3 | 0.60 | 1.1 | 0.3 | 1.1 | V |
| | | $V_{CC}$ = 3.0 V | 0.4 | 0.65 | 1.2 | 0.4 | 1.2 | V |
| | | $V_{CC}$ = 3.6 V | 0.4 | 0.70 | 1.2 | 0.4 | 1.2 | V |
| | | $V_{CC}$ = 4.5 V | 0.4 | 0.80 | 1.4 | 0.4 | 1.4 | V |
| | | $V_{CC}$ = 5.5 V | 0.6 | 1.00 | 1.5 | 0.6 | 1.5 | V |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

## 14. Waveforms transfer characteristics

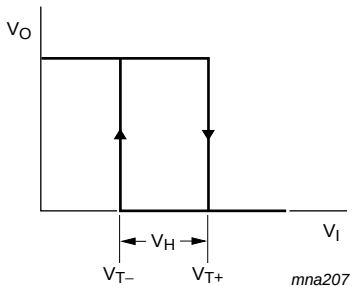
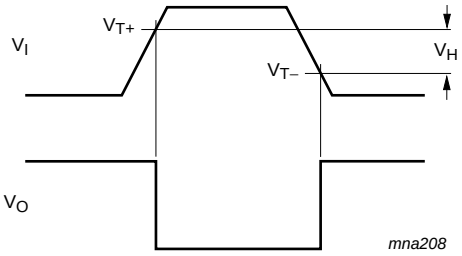
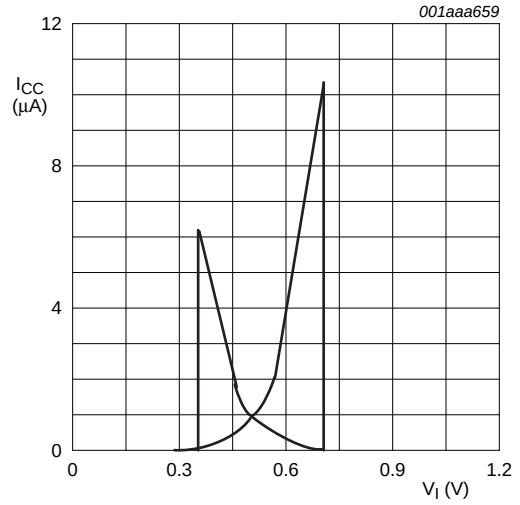



**Fig 8. Transfer characteristic**



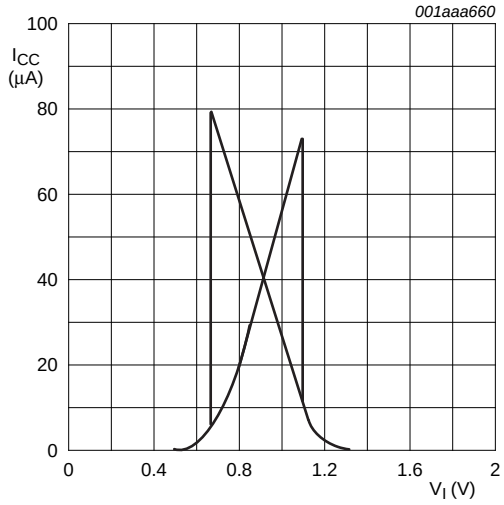

$V_{T+}$ and $V_{T-}$ limits at 70 % and 20 %.

**Fig 9. Definition of $V_{T+}$, $V_{T-}$ and $V_H$**



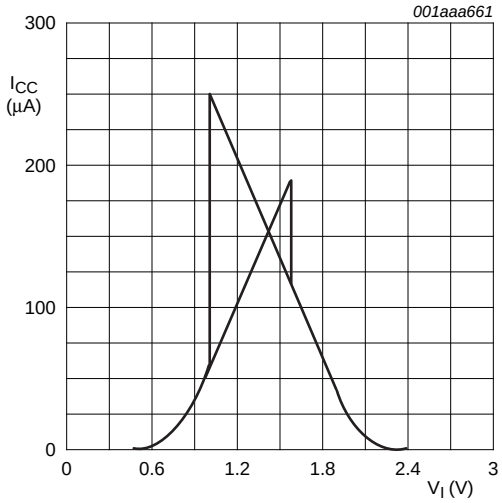

$V_{CC}$ = 1.2 V.

**Fig 10. Typical 74LV132-Q100 transfer characteristics**




$V_{CC}$ = 2.0 V.

**Fig 11. Typical 74LV132-Q100 transfer characteristics**

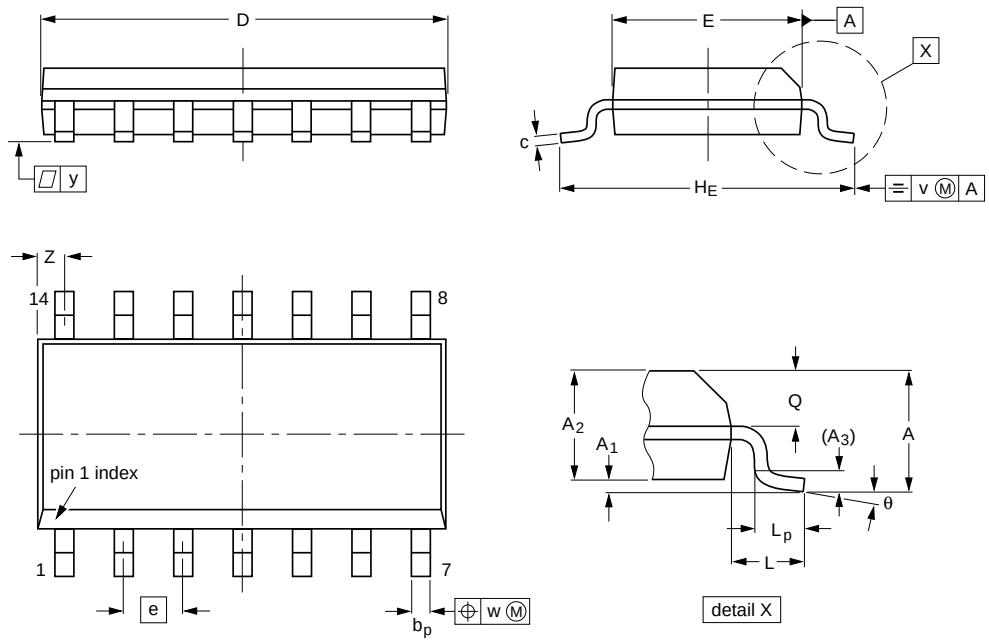



$V_{CC}$ = 3.0 V.

**Fig 12. Typical 74LV132-Q100 transfer characteristics**

# 15. Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

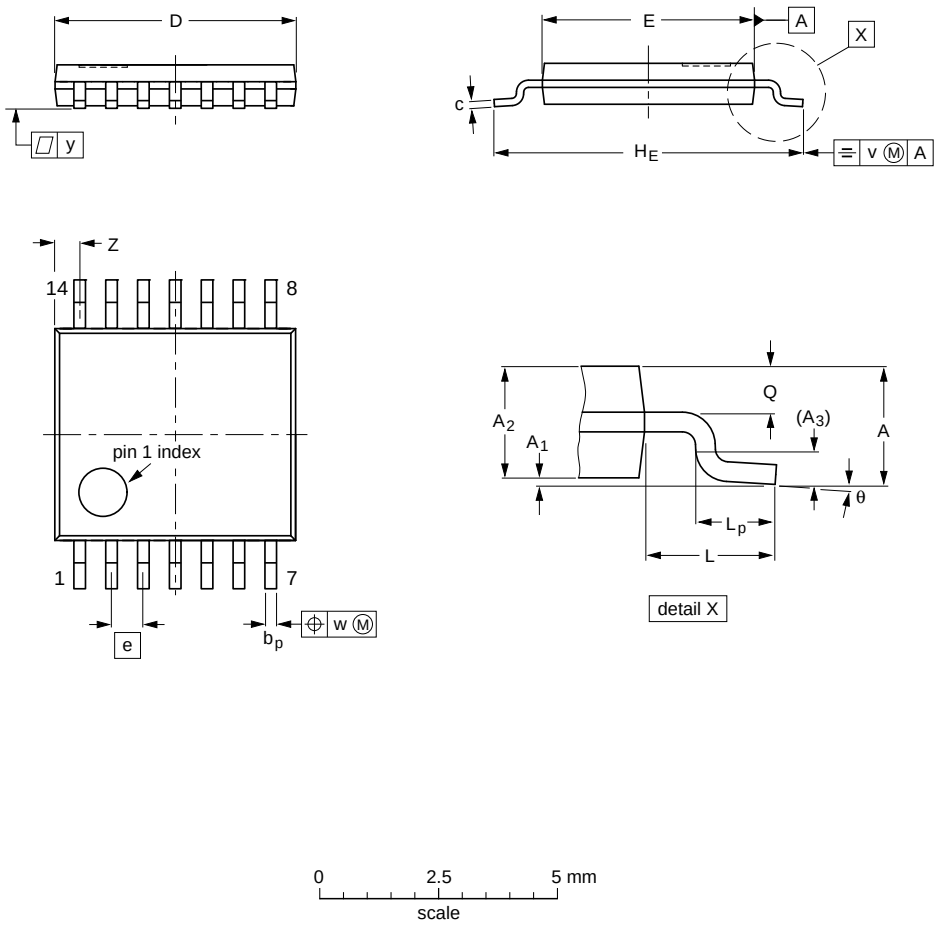
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 13. Package outline SOT108-1 (SO14)**

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | $8^o$<br>$0^o$ |

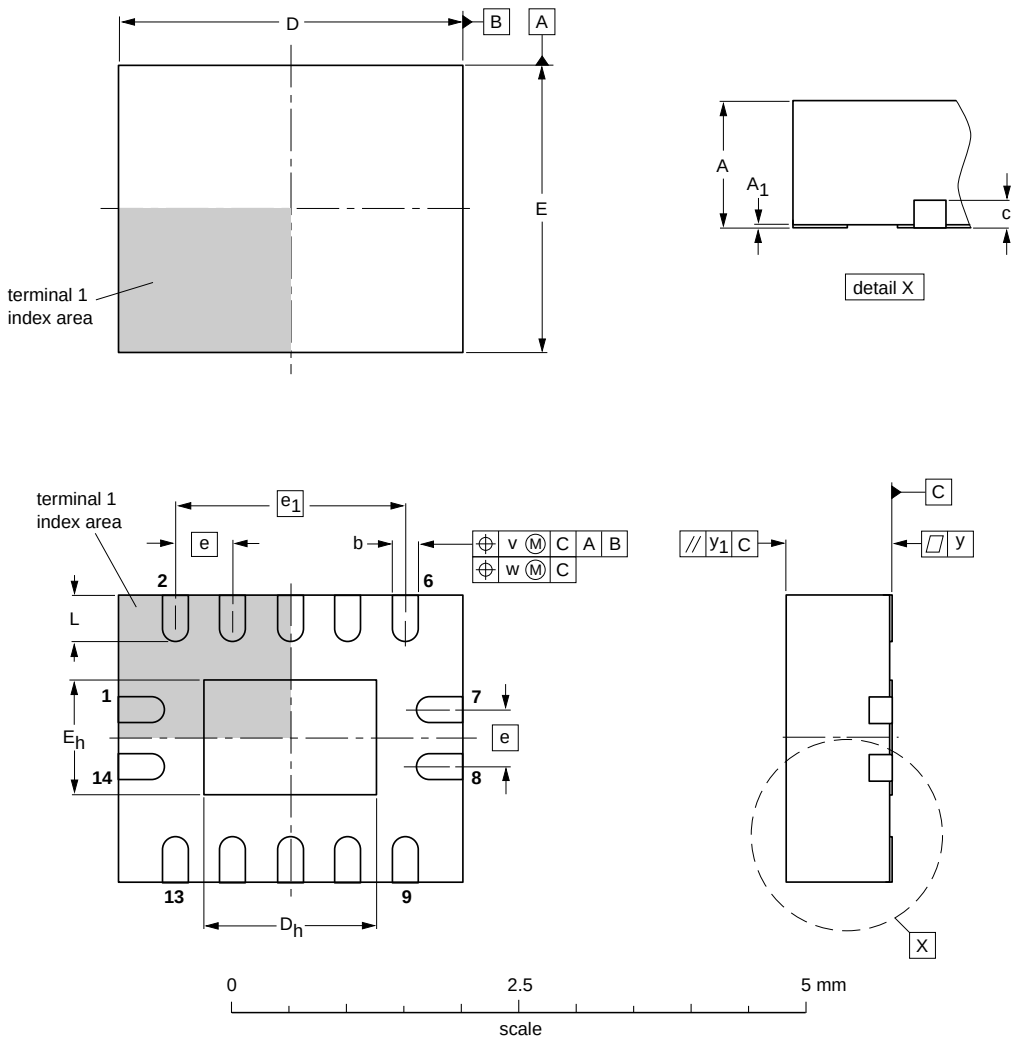
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 14. Package outline SOT402-1 (TSSOP14)**

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm** **SOT762-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.1<br>2.9 | 1.65<br>1.35 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT762-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 15. Package outline SOT762-1 (DHVQFN14)**

# 16. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

# 17. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LV132_Q100 v.1 | 20131111 | Product data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 20. Contents





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