BUK9MPP-65PLL

Dual TrenchPLUS FET Logic Level FET

Rev. 03 — 15 July 2010 Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

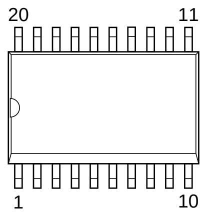
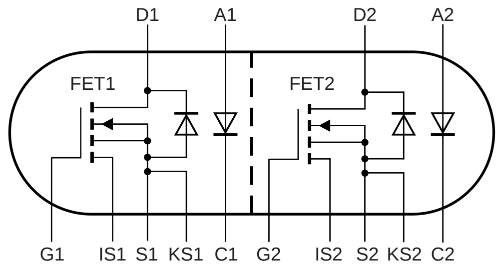
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; see Figure 17; see Figure 16	-	23	27	mΩ
I_D/I_{sense}	ratio of drain current to sense current	T_j = 25 °C; V_{GS} = 5 V; see Figure 18	3587	3986	4385	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	65	-	-	V

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1	 SOT163-1 (SO20)	 003aaa745
2	IS1	current sense 1		
3	D1	drain		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9MPP-65PLL	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
FET1 and FET2						
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	65	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ; 25 °C ≤ T_j ≤ 150 °C		-	65	V
V_{GS}	gate-source voltage			-15	15	V
I_D	drain current	V_{GS} = 5 V; T_{sp} = 25 °C; see Figure 1	[1][2]	-	8.6	A
		V_{GS} = 5 V; T_{sp} = 100 °C; see Figure 1	[1][2]	-	5.4	A
I_{DM}	peak drain current	T_{sp} = 25 °C; single pulse; t_p ≤ 10 µs; see Figure 4		-	135.7	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 2		-	3.84	W
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage			-	100	V
FET1 and FET2 source-drain diode						
I_S	source current	T_{sp} = 25 °C	[1][2]	-	5.4	A
I_{SM}	peak source current	single pulse; t_p ≤ 10 µs; T_{sp} = 25 °C		-	135.7	A
FET1 and FET2 avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 8.6 A; V_{sup} = 65 V; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; see Figure 3	[3][4][5]	-	0.293	J
FET1 and FET2 electrostatic discharge						
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; all pins		-	0.15	kV
		HBM; C = 100 pF; R = 1.5 kΩ; pins 8, 11 and 15 to pins 6, 7, 12, 13 and 14 shorted		-	4	kV
		HBM; C = 100 pF; R = 1.5 kΩ; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted		-	4	kV

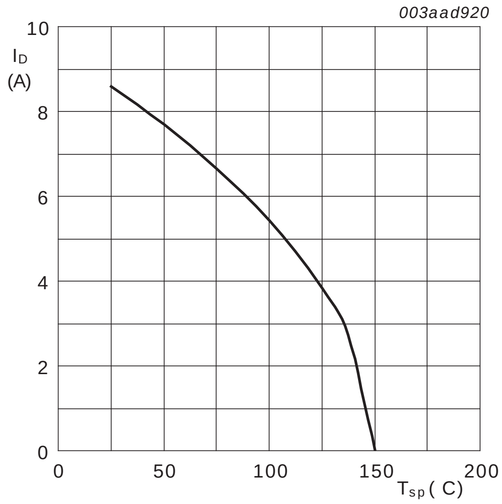
[1] Single device conducting.

[2] Current is limited by package.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

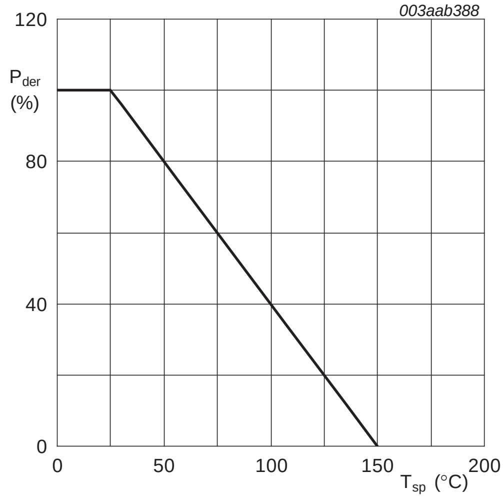
[4] Repetitive rating defined in avalanche rating figure.

[5] Refer to application note AN10273 for further information.



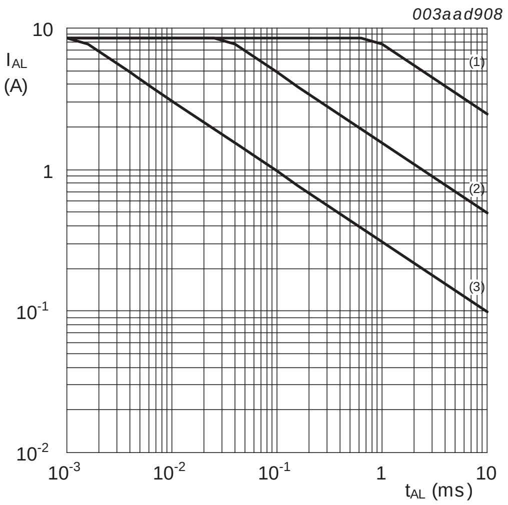
$V_{GS} \geq 5\ V$

Fig 1. Continuous drain current as a function of solder point temperature, FET1 and FET2



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature, FET1 and FET2

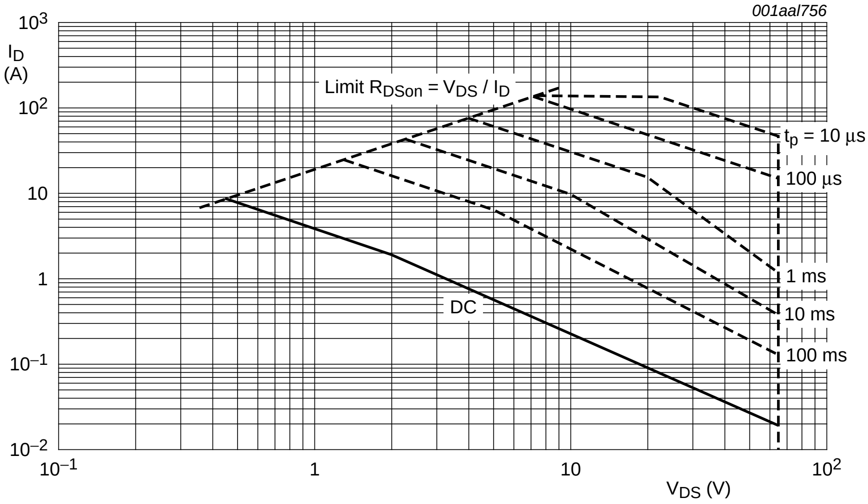


(1) Single−pulse; $T_j = 25\ °C$.

(2) Single−pulse; $T_j = 150\ °C$.

(3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function as a function of avalanche time, FET1 and FET2



$T_{sp} = 25\,°C; I_{DM}$ is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	33	K/W
		FET2	-	-	33	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; both channels conducting; zero heat sink area; see Figure 5; see Figure 6	-	73	-	K/W
		mounted on a printed-circuit board; both channels conducting; 200 mm² copper heat sink area; see Figure 7; see Figure 6	-	60	-	K/W
		mounted on a printed-circuit board; both channels conducting; 400 mm² copper heat sink area; see Figure 8; see Figure 6	-	51	-	K/W
		mounted on a printed-circuit board; one channel conducting; zero heat sink area; see Figure 5; see Figure 6	-	105	-	K/W
		mounted on a printed-circuit board; one channel conducting; 200 mm² copper heat sink area; see Figure 7; see Figure 6	-	90	-	K/W
		mounted on a printed-circuit board; one channel conducting; 400 mm² copper heat sink area; see Figure 8	-	70	-	K/W

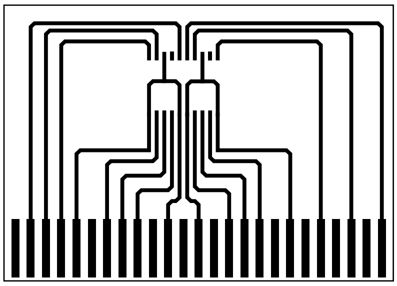
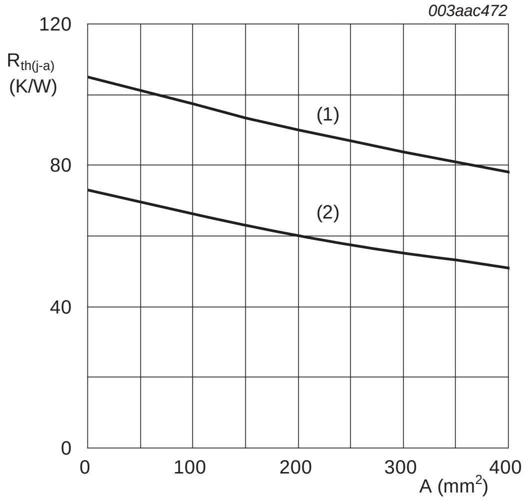


Fig 5. PCB used for thermal tests; zero heat sink area



(1) One channel conducting dissipating 500mW.

(2) Both channels conducting each dissipating 500mW.

Zero air flow

Fig 6. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area

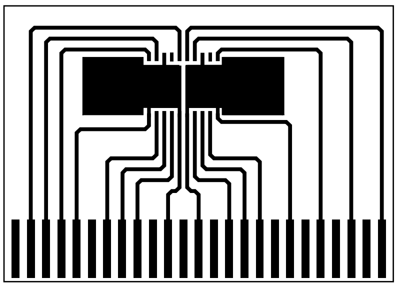


Fig 7. PCB used for thermal tests; heat sink area 200 mm²

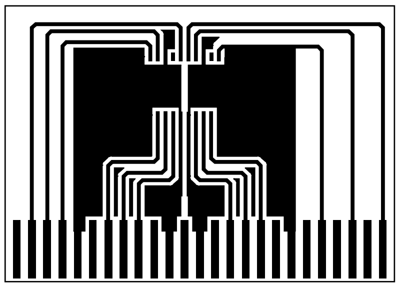


Fig 8. PCB used for thermal tests; heat sink area 400 mm²

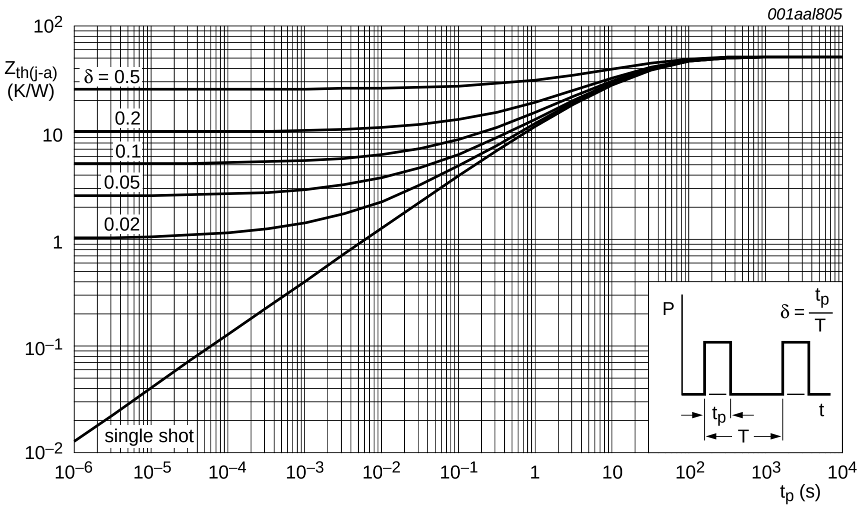


Fig 9. Transient thermal impedance from junction to ambient as a function of pulse duration

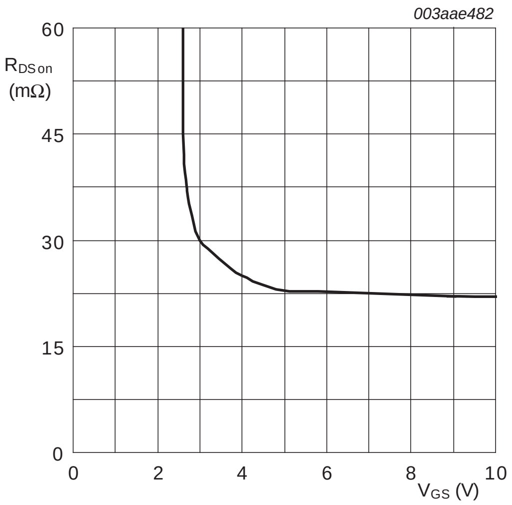
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FET1 and FET2 static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	65	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	59	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 14; see Figure 15	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 14; see Figure 15	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 14; see Figure 15	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 52 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	3	µA
		V_{DS} = 52 V; V_{GS} = 0 V; T_j = 150 °C	-	-	125	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	300	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C; see Figure 16; see Figure 17	-	-	29.8	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; see Figure 17; see Figure 16	-	23	27	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 150 °C; see Figure 16; see Figure 17	-	-	52.5	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; see Figure 16; see Figure 17	-	-	24.7	mΩ
I_D/I_{sense}	ratio of drain current to sense current	V_{GS} = 5 V; T_j = 25 °C; see Figure 18	3587	3986	4385	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	I_F = 250 µA; 25 °C ≤ T_j ≤ 150 °C; see Figure 19	-5.4	-5.7	-6	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	I_F = 250 µA; T_j = 25 °C; see Figure 19	2.855	2.9	2.945	V
FET1 and FET2 dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 52 V; V_{GS} = 5 V; see Figure 20	-	21	-	nC
Q_{GS}	gate-source charge		-	3.6	-	nC
Q_{GD}	gate-drain charge		-	7.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 21	-	1710	-	pF
C_{oss}	output capacitance		-	223	-	pF
C_{rss}	reverse transfer capacitance		-	75	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 6 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	26	-	ns
t_r	rise time		-	33	-	ns
$t_{d(off)}$	turn-off delay time	V_{DS} = 30 V; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	101	-	ns
t_f	fall time	V_{DS} = 30 V; R_L = 6 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	46	-	ns
L_D	internal drain inductance	from pin to center of die	-	0.9	-	nH

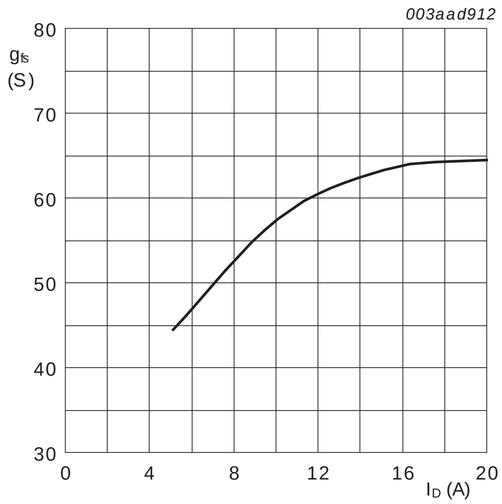
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_S	internal source inductance	from source lead to source bonding pad	-	2	-	nH
FET1 and FET2 source-drain diode						
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 22	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V	-	44	-	ns
Q_r	recovered charge	I_S = 10 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V	-	0.09	-	nC



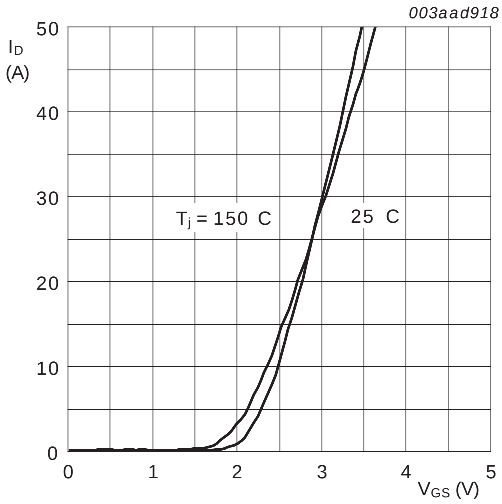
$T_j = 25\,°C; I_D = 5A$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2



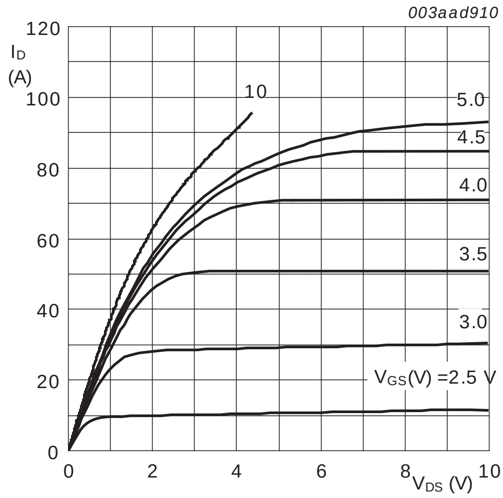
$T_j = 25\,°C; V_{DS} = 25V$

Fig 11. Forward transconductance as a function of drain current; typical values, FET1 and FET2



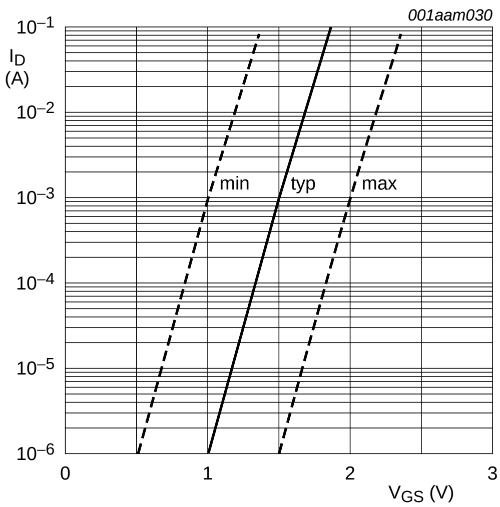
$V_{DS} = 25V$

Fig 12. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2



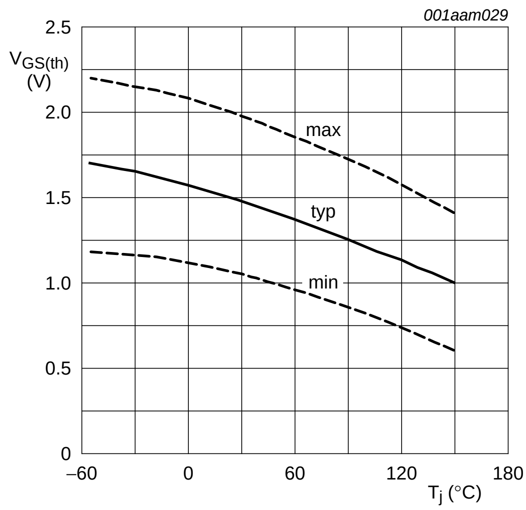
$T_j = 25\,°C; t_p = 300\mu s$

Fig 13. Output characteristics: drain current as a function of drain-source voltage; typical values,FET1 and FET2



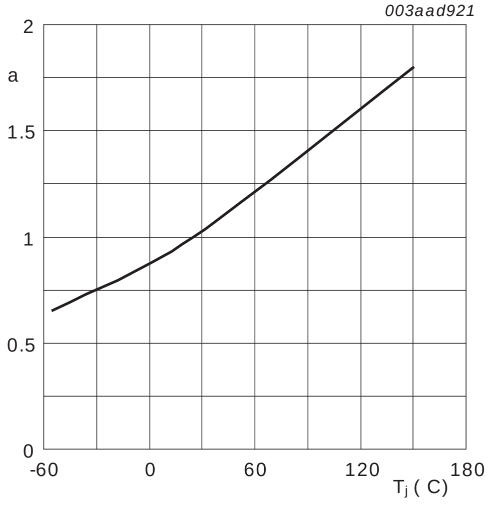
$T_j = 25\,°C; V_{DS} = V_{GS}$

Fig 14. Sub-threshold drain current as a function of gate-source voltage.



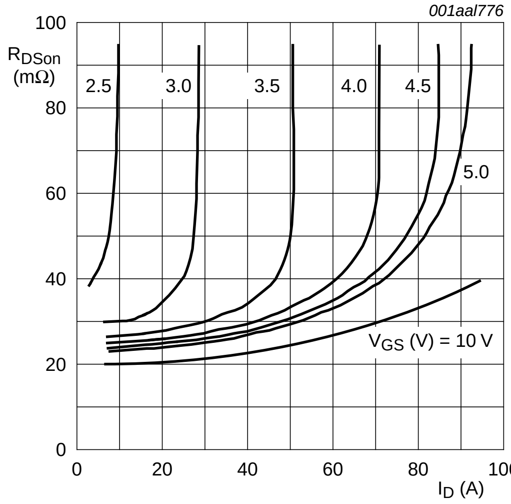
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 15. Gate-source threshold voltage as a function of junction temperature.



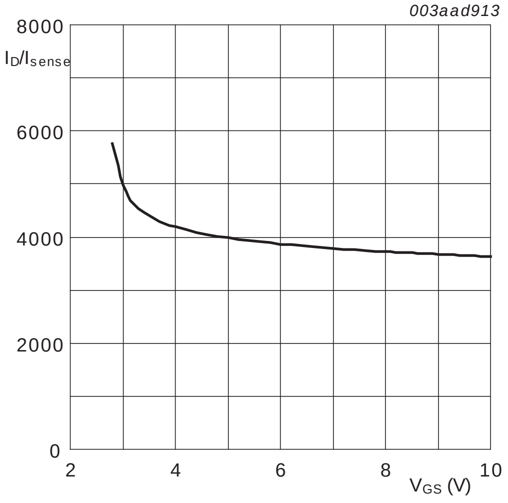
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 16. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



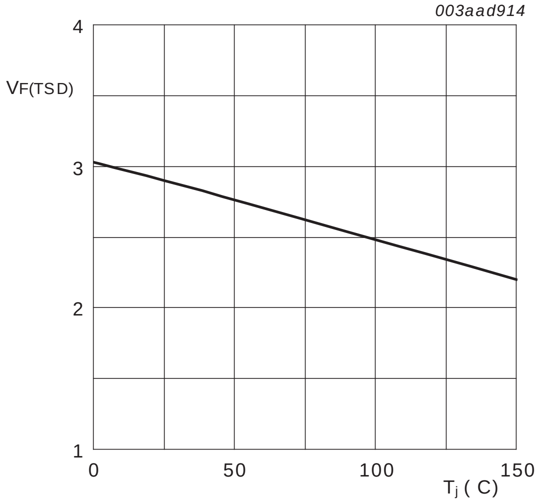
$$T_j = 25°C; V_{DS} = 5V$$

Fig 17. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



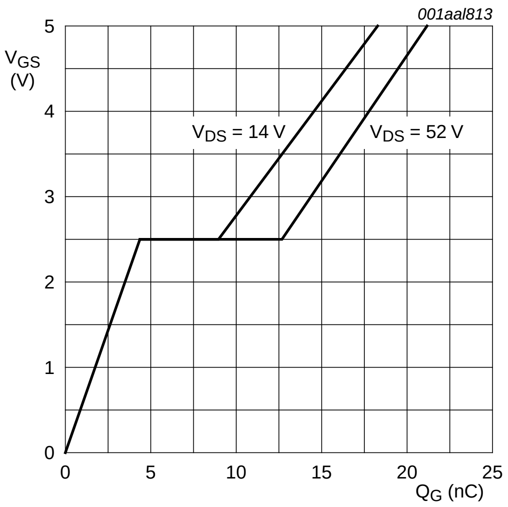
$$T_j = 25°C; I_D = 5A$$

Fig 18. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2



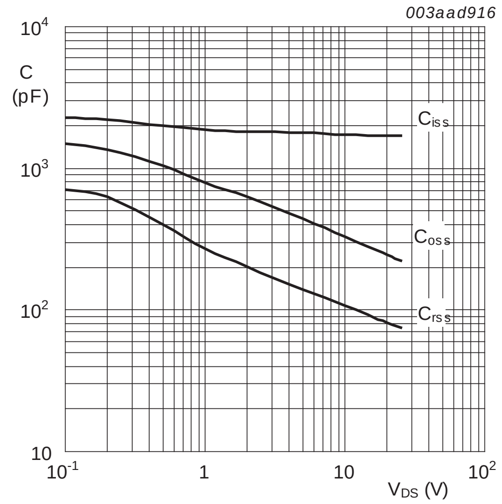
$$I_F = 250\mu A$$

Fig 19. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2



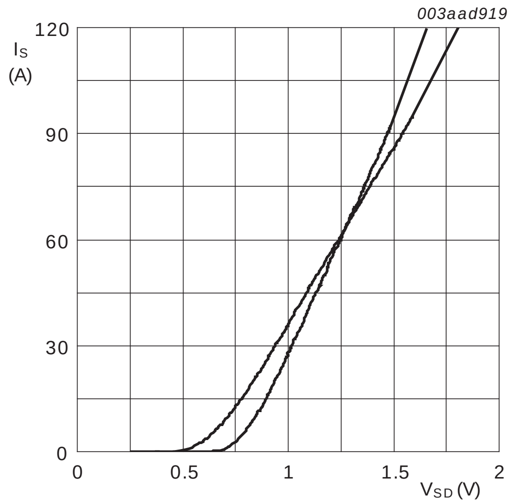
$T_j = 25\,°C; I_D = 5 A$

Fig 20. Gate-source voltage as a function of turn-on gate charge; typical values, FET1 and FET2



$V_{GS} = 0 V; f = 1 MHz$

Fig 21. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

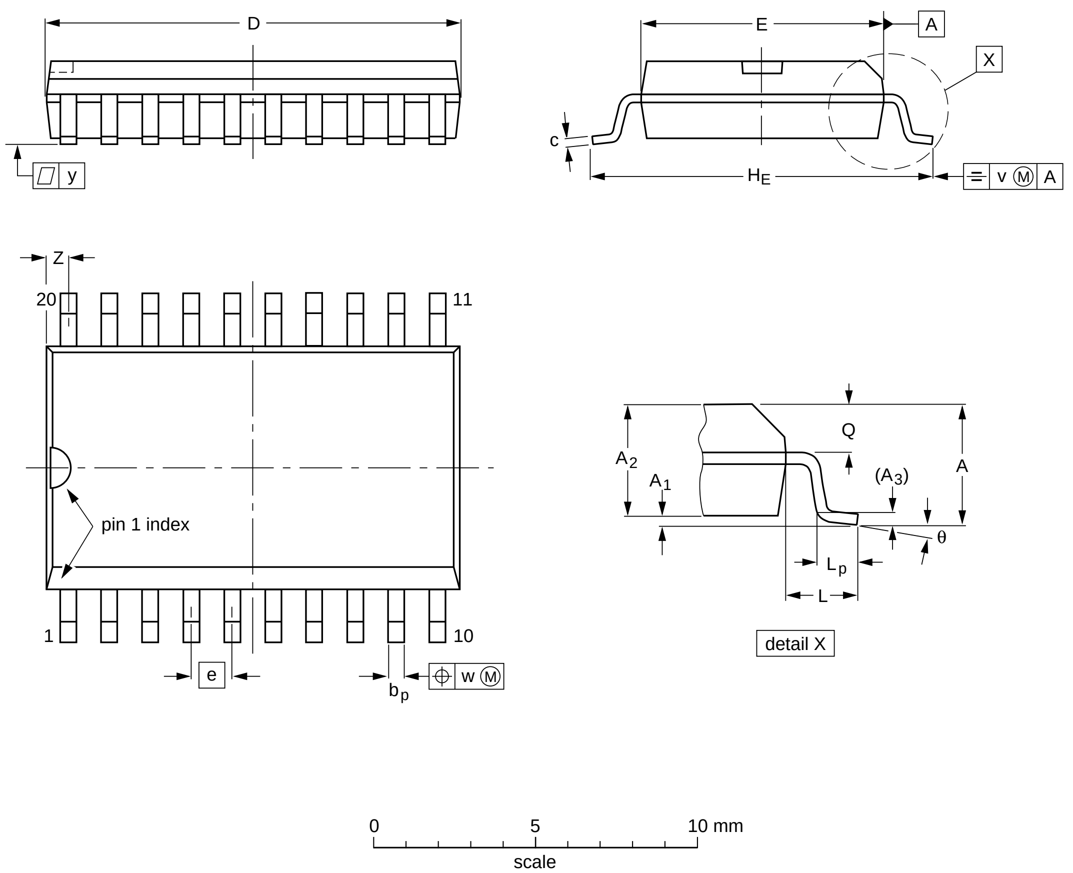


$V_{GS} = 0 V$

Fig 22. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

7. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT163-1 (SO20)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MPP-65PLL v.3	20100715	Product data sheet	-	BUK9MPP-65PLL v.2
Modifications:	• Various changes to content.			
BUK9MPP-65PLL v.2	20100617	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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