INTEGRATED CIRCUITS

DATA SHEET

74LVT103.3V Triple 3-input NAND gate

Product specification

1996 May 29

IC24 Data Handbook



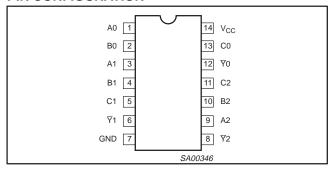


74LVT10

QUICK REFERENCE DATA

SYMBOL	PARAMETER	PARAMETER CONDITIONS $T_{amb} = 25^{\circ}C;$ $GND = 0V$						
[†] PLH [†] PHL	Propagation delay An, Bn, Cn to Yn	C _L = 50pF; V _{CC} = 3.3V	3.8 3.3	ns				
C _{IN}	Input capacitance	V _I = 0V or 3.0V	2	pF				
I _{CCL}	Total supply current	Outputs Low; V _{CC} = 3.6V	1	mA				

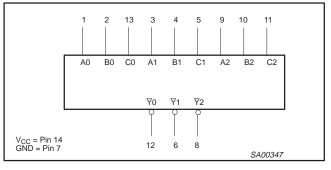
PIN CONFIGURATION



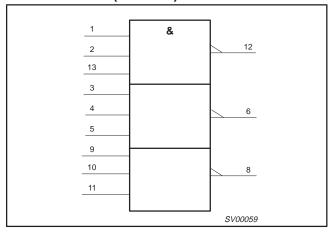
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 9, 10, 11, 13	An, Bn, Cn	Data inputs
6, 8, 12	₹n	Data outputs
7	GND	Ground (0V)
14	V _{CC}	Positive supply voltage

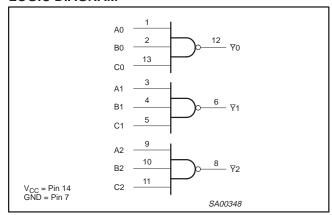
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

	INPUTS		OUTPUTS
Dna	Dnb	Dnc	Qn
L	L	L	Н
L	L	Н	Н
L	Н	L	Н
L	Н	Н	Н
Н	L	L	Н
Н	L	Н	Н
Н	Н	L	Н
Н	Н	Н	L

NOTES:

H = High voltage levelL = Low voltage level

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVT10 D	74LVT10 D	SOT108-1
14-Pin Plastic SSOP	–40°C to +85°C	74LVT10 DB	74LVT10 DB	SOT337-1
14-Pin Plastic TSSOP	-40°C to +85°C	74LVT10 PW	74LVT10PW DH	SOT402-1

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ABSOLUTE MAXIMUM RATINGS1, 2

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
VI	DC input voltage ³		-0.5 to +7.0	V
lok	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	−0.5 to +7.0	V
	DC output ourrent	Output in High state	-32	A
Гоит	DC output current	Output in Low state	64	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	ITS	UNIT
STIMBUL	PARAMETER	MIN	MAX	UNII
V _{CC}	DC supply voltage	2.7	3.6	V
V _I	Input voltage	0	5.5	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		-20	mA
I _{OL}	Low-level output current		32	mA
Δt/Δν	Input transition rise or fall rate; Outputs enabled		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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^{1.} Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions Voltages are referenced to GND (ground = 0V)

			L			
SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -	+85°C	UNIT	
			MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	$V_{CC} = 2.7V; I_{IK} = -18mA$			-1.2	V
		$V_{CC} = 2.7 \text{ to } 3.6 \text{V}; I_{OH} = -100 \mu\text{A}$	V _{CC} -0.2	V _{CC}		
V _{OH}	High-level output voltage	$V_{CC} = 2.7V; I_{OH} = -6mA$	2.4	2.5		V
		$V_{CC} = 3.0V; I_{OH} = -20mA$	2.0	2.3		
		$V_{CC} = 2.7V; I_{OL} = 100\mu A$		0.05	0.2	
V _{OL}	Low-level output voltage	V _{CC} = 2.7V; I _{OL} = 24mA		0.3	0.5	V
		$V_{CC} = 3.0V; I_{OL} = 32mA$		0.35	0.5	
,	Input lookage ourrent	$V_{CC} = 0 \text{ or } 3.6V; V_I = 5.5V$		0.1	10	
l '1	Input leakage current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or GND}$		0.01	±1	μΑ
I _{OFF}	Output off current	$V_{CC} = 0V$; V_I or $V_O = 0$ to 4.5V		1	±100	μΑ
Іссн	Quiescent aunaly aurrent	$V_{CC} = 3.6V$; Outputs High, $V_{I} = GND$ or V_{CC} , $I_{O} = 0$		0.001	0.02	mA
I _{CCL}	Quiescent supply current	V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC} , I_{O} = 0		1	2	IIIA
Δl _{CC}	Additional supply current per input pin ²	V_{CC} = 3V to 3.6V; One input at V_{CC} –0.6V, Other inputs at V_{CC} or GND		0.1	0.2	mA
C _I	Input capacitance	V _I = 3V or 0		2		pF

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
 This is the increase in supply current for each input at the specificed voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

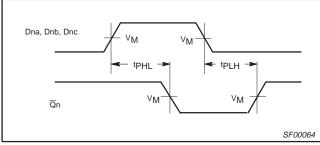
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500 Ω ; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	Vcc	= 3.3V ± 0	.3V	V _{CC} = 2.7V	UNIT
			MIN	TYP ¹	MAX	MAX	
t _{PLH} t _{PHL}	Propagation delay An, Bn, Cn to ₹n	1	1.0 1.0	3.8 3.3	5.2 4.4	6.2 4.4	ns

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

 $V_{M} = 1.5V, V_{IN} = GND \text{ to } 2.7V$



Waveform 1. Propagation Delay for Inverting Outputs

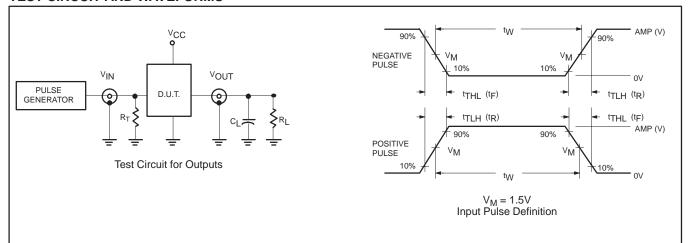
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TEST CIRCUIT AND WAVEFORMS



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DEFINITIONS

 R_L = Load resistor; see AC CHARACTERISTICS for value.

 $C_L = Load$ capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

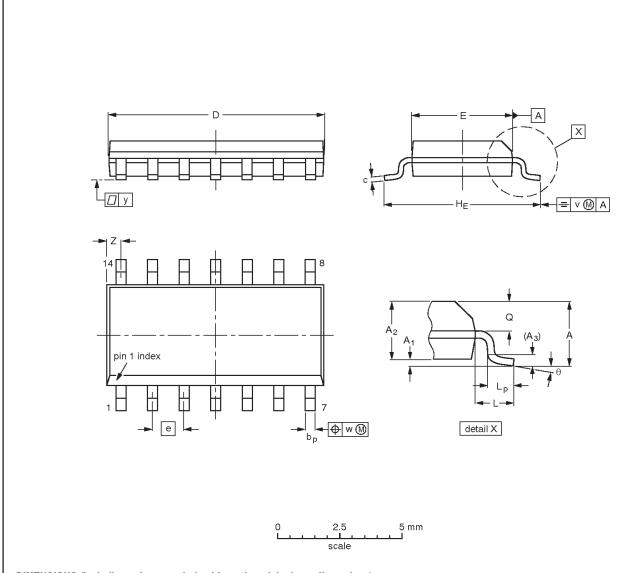
FAMILY	INPUT PULSE REQUIREMENTS											
FAMILI	Amplitude	Rep. Rate	t _W	t _R	t _F							
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns							

SV00022

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

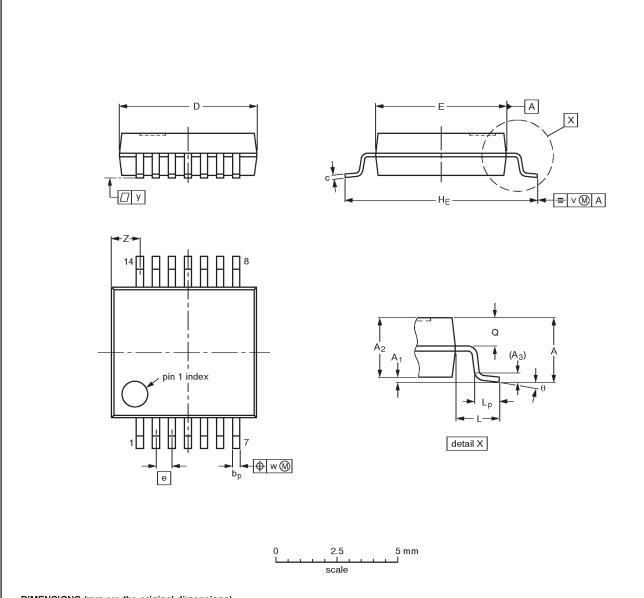
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT108-1	076E06S	MS-012AB				-95-01-23- 97-05-22	

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	рb	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

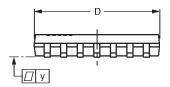
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

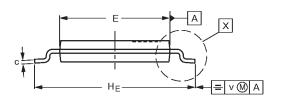
OUTLINE		EUROPEAN	ISSUE DATE				
VERSION	IEC	JEDEC	EIAJ		PROJECTION	1930E DATE	
SOT337-1		MO-150AB				95-02-04 96-01-18	

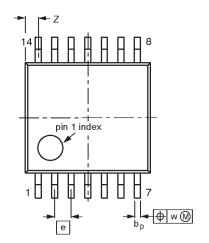
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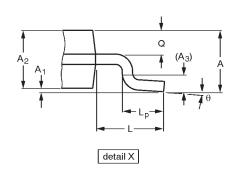
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

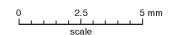
SOT402-1











DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α1	A ₂	A ₃	bр	c	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC EIAJ				PROJECTION
SOT402-1		MO-153				94-07-12 95-04-04

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NOTES

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DEFINITIONS						
Data Sheet Identification	Product Status	Definition				
Objective Specification Formative or in Design		This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.				
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.				
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(print code) Date of release: July 1994

Document order number: 9397-750-04844