

BLA1011-200; BLA1011S-200

Avionics LDMOS transistor

Rev. 9 — 1 September 2015

AMPELON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS avionics power transistor for transmitter applications at frequencies from 1030 MHz to 1090 MHz.

Table 1. Typical performance

RF performance at $T_h = 25\text{ °C}$ in a common source class-AB test circuit; $I_{DQ} = 150\text{ mA}$; typical values.

Mode of operation	Conditions	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
Pulsed class-AB: 1030 MHz to 1090 MHz	$t_p = 50\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$	36	200	15	50	35	6
	$t_p = 128\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$	36	250	14	50	35	6
	$t_p = 340\text{ }\mu\text{s}$; $\delta = 1\text{ }\%$	36	250	14	50	35	6

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

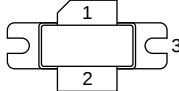
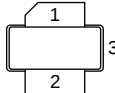
- Typical pulsed class-AB performance at a frequencies from 1030 MHz to 1090 MHz, a supply voltage of 36 V and an I_{DQ} of 150 mA:
 - ◆ Load power $\geq 200\text{ W}$
 - ◆ Gain $\geq 13\text{ dB}$
 - ◆ Efficiency $\geq 45\text{ }\%$
 - ◆ Rise time $\leq 50\text{ ns}$
 - ◆ Fall time $\leq 50\text{ ns}$
- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting flange eliminates DC isolators, reducing common mode inductance

1.3 Applications

- Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
BLA1011-200 (SOT502A)			
1	drain		
2	gate		
3	source		
[1]			
sym039			
BLA1011S-200 (SOT502B)			
1	drain		
2	gate		
3	source		
[1]			
sym039			

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA1011-200	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA1011S-200	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

4.1 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	75	V
V_{GS}	gate-source voltage		-	± 22	V
P_{tot}	total power dissipation	$T_h \leq 25^\circ\text{C}$; $t_p = 50 \mu\text{s}$; $\delta = 2\%$	-	700	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	junction temperature		-	200	$^\circ\text{C}$

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-h)}$	thermal impedance from junction to heatsink	$T_h = 25\text{ }^{\circ}\text{C}$	[1] 0.15	K/W

[1] Thermal resistance is determined under RF operating conditions; $t_p = 50\text{ }\mu\text{s}$, $\delta = 10\text{ }\%$.

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 3\text{ mA}$	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 300\text{ mA}$	4	-	5	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 36\text{ V}$	-	-	1	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	45	-	-	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	1	μA
g_{fs}	transfer conductance	$V_{DS} = 10\text{ V}$; $I_D = 10\text{ A}$	-	9	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 9\text{ V}$; $I_D = 10\text{ A}$	-	60	-	$\text{m}\Omega$

7. Application information

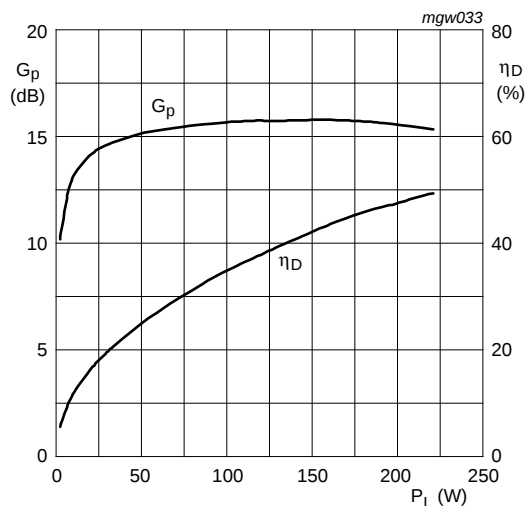
Table 7. Application information

RF performance in a common source pulsed class-AB circuit; ($t_p = 50\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$); $f = 1030\text{ MHz}$ and 1090 MHz ; $T_h = 25\text{ }^{\circ}\text{C}$; $Z_{th(mb-h)} = 0.15\text{ K/W}$; $I_{Dq} = 150\text{ mA}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	36	-	V
P_L	load power	$t_p = 50\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$	-	200		W
G_p	power gain	$P_L = 200\text{ W}$	13	-		dB
η_D	drain efficiency	$t_p = 50\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$	45	-		%
t_r	rise time		-	-	50	ns
t_f	fall time		-	-	50	ns

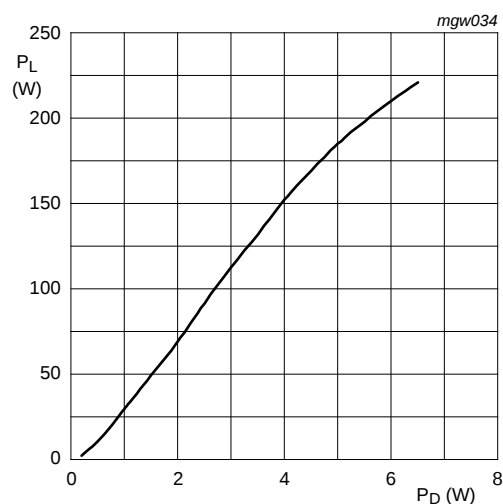
7.1 Ruggedness in class-AB operation

The BLA1011-200 and BLA1011S-200 are capable of withstanding a load mismatch corresponding to $VSWR = 5 : 1$ through all phases under the following conditions: $V_{DS} = 36\text{ V}$; $f = 1030\text{ MHz}$ to 1090 MHz at rated load power.



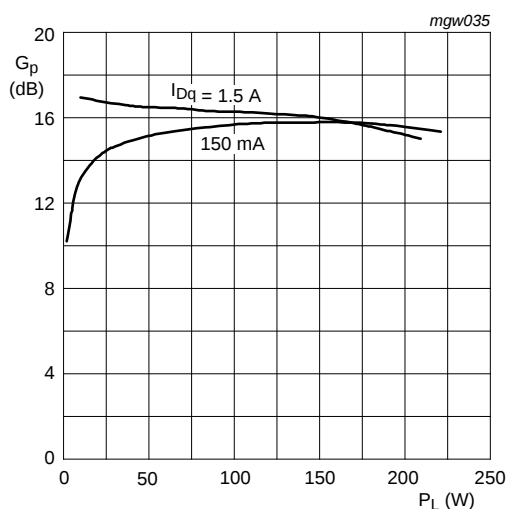
$V_{DS} = 36 \text{ V}$; $I_{Dq} = 150 \text{ mA}$; $f = 1060 \text{ MHz}$; $t_p = 50 \text{ } \mu\text{s}$; $\delta = 2 \%$

Fig 1. Power gain and drain efficiency as functions of load power; typical values



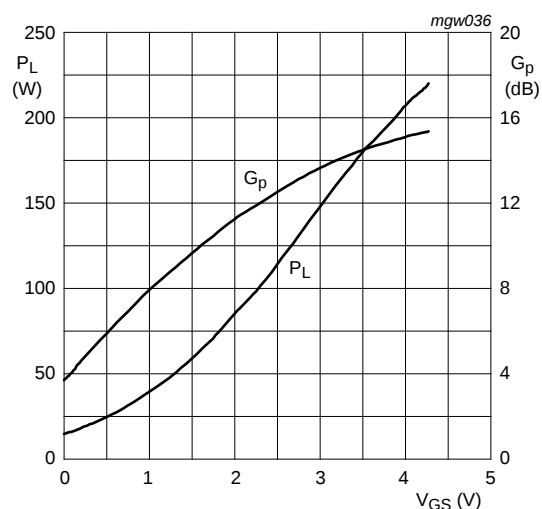
$V_{DS} = 36 \text{ V}$; $I_{Dq} = 150 \text{ mA}$; $f = 1060 \text{ MHz}$; $t_p = 50 \text{ } \mu\text{s}$; $\delta = 2 \%$

Fig 2. Load power as a function of drive power; typical values



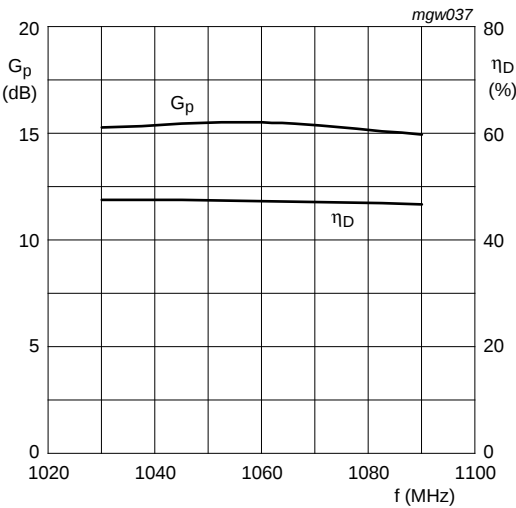
$V_{DS} = 36 \text{ V}$; $f = 1060 \text{ MHz}$; $t_p = 50 \text{ } \mu\text{s}$; $\delta = 2 \%$

Fig 3. Power gain as a function of load power; typical values



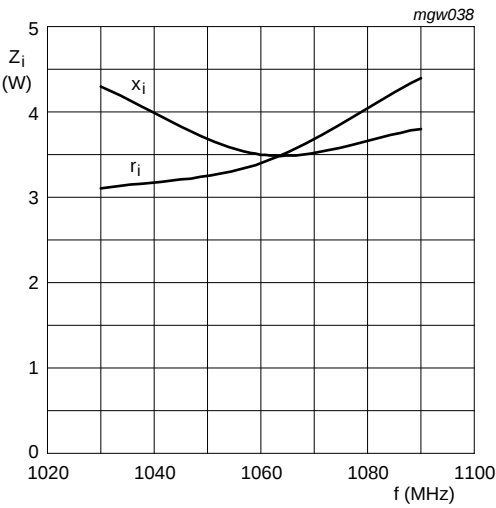
$V_{DS} = 36 \text{ V}$; $I_{Dq} = 150 \text{ mA}$; $P_i = 5.5 \text{ W}$; $f = 1060 \text{ MHz}$; $t_p = 50 \text{ } \mu\text{s}$; $\delta = 2 \%$

Fig 4. Load power and power gain as functions of gate-source voltage; typical values



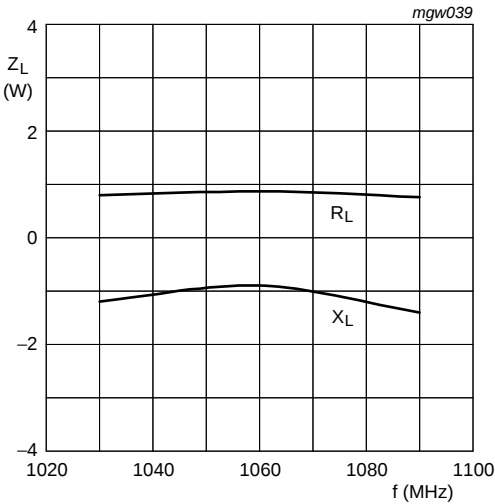
$V_{DS} = 36\text{ V}$; $I_{Dq} = 150\text{ mA}$; $P_L = 200\text{ W}$; $t_p = 50\text{ }\mu\text{s}$;
 $\delta = 2\text{ }\%$

Fig 5. Power gain and drain efficiency a functions of frequency; typical values



$V_{DS} = 36\text{ V}$; $I_{Dq} = 150\text{ mA}$; $P_L = 200\text{ W}$; $t_p = 50\text{ }\mu\text{s}$;
 $\delta = 2\text{ }\%$

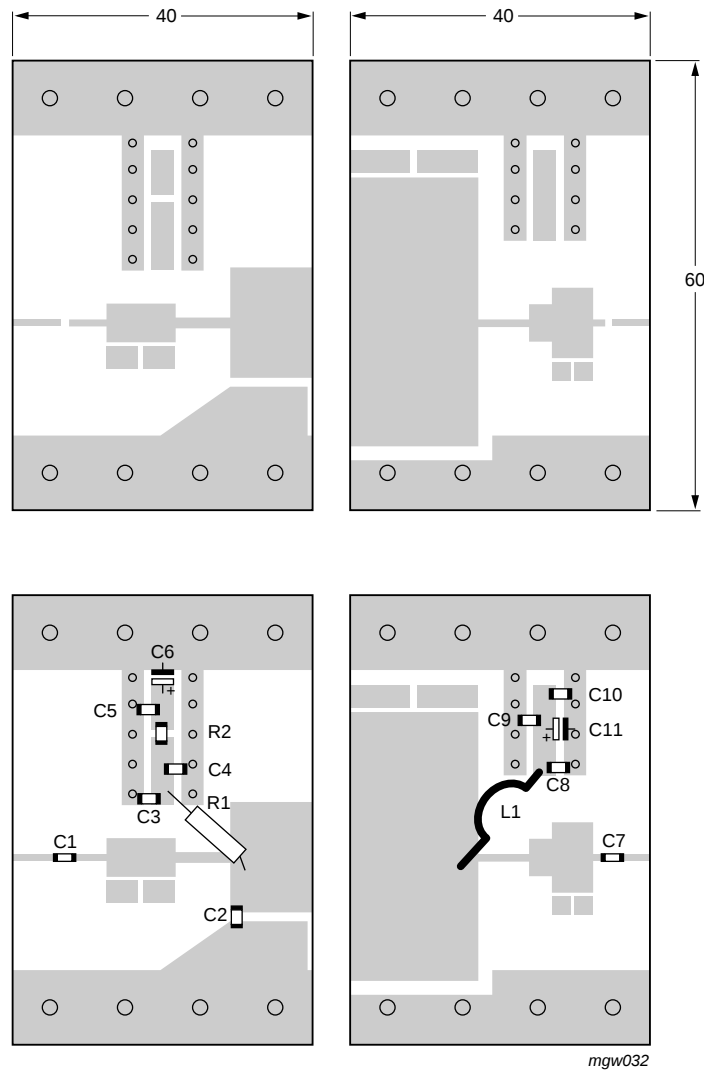
Fig 6. Input Impedance as a function of frequency (series components); typical values



$V_{DS} = 36\text{ V}$; $I_{Dq} = 150\text{ mA}$; $P_L = 200\text{ W}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$

Fig 7. Load impedance as a function of frequency (series components); typical values

8. Test information



Dimensions in mm.

The components are situated on one side of the copper-clad Duroid Printed-Circuit Board (PCB) with $\epsilon_r = 6.2$ and thickness 0.64 mm.

The other side is unetched and serves as a ground plane.

See [Table 8](#) for list of components.

Fig 8. Component layout for 1030 MHz to 1090 MHz test circuit

Table 8. List of components (see [Figure 8](#))

Component	Description	Value	Dimensions
C1	multilayer ceramic chip capacitor	[1] 39 pF	
C2	multilayer ceramic chip capacitor	[2] 4.3 pF	
C3	multilayer ceramic chip capacitor	[1] 11 pF	
C4, C7	multilayer ceramic chip capacitor	[1] 62 pF	
C5	multilayer ceramic chip capacitor	[1] 100 pF	
C6	electrolytic capacitor	47 μ F; 20 V	
C8	multilayer ceramic chip capacitor	[2] 20 pF	
C9	multilayer ceramic chip capacitor	[1] 47 pF	
C10	multilayer ceramic chip capacitor	[3] 1.2 nF	
C11	electrolytic capacitor	47 μ F; 63V	
L1	Ω -shaped enamelled 1 mm copper wire		length = 38 mm
R1	metal film resistor	301 Ω	
R2	SMD 0508 resistor	18 Ω	

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 700 or capacitor of same quality.

9. Package outline

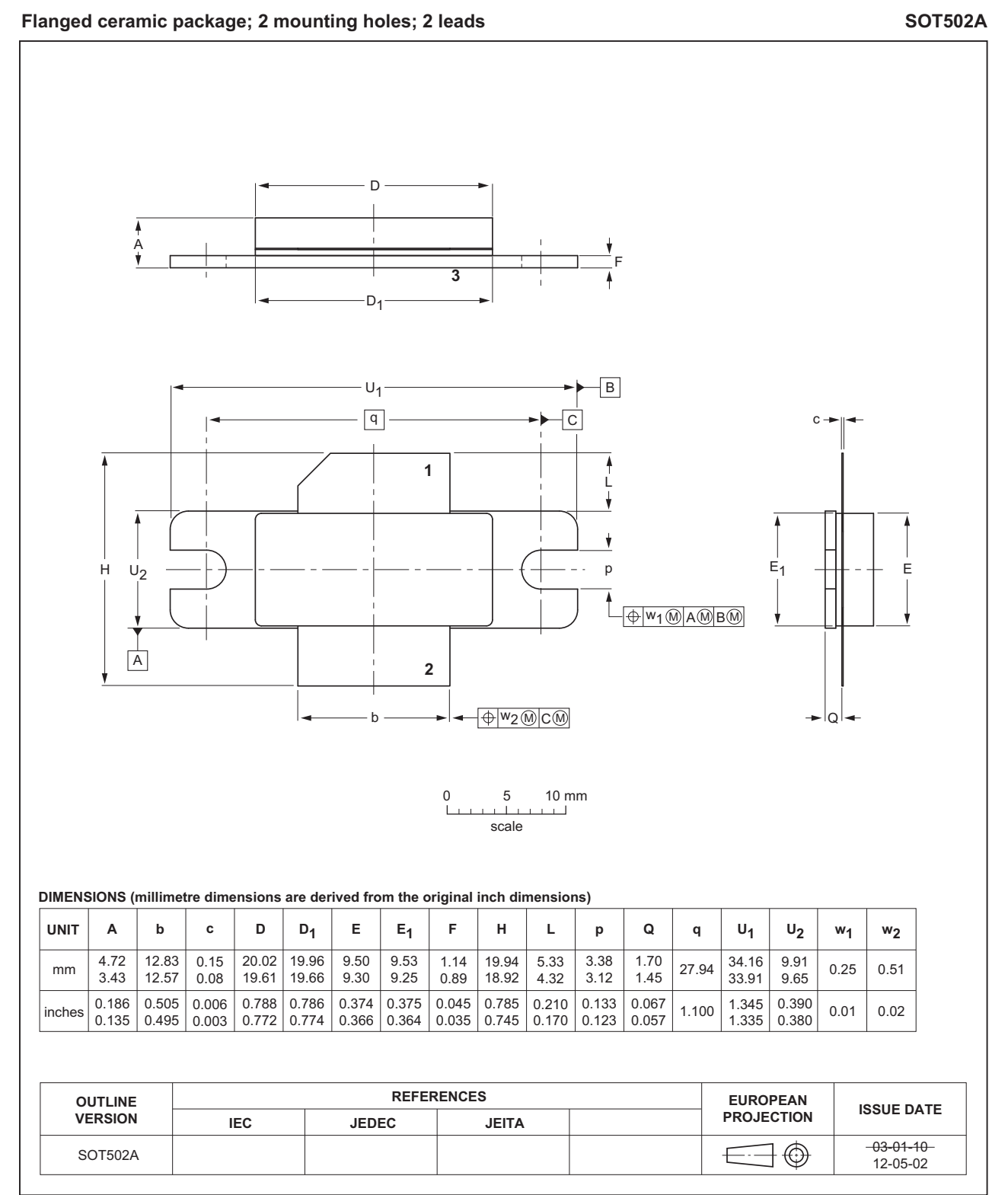
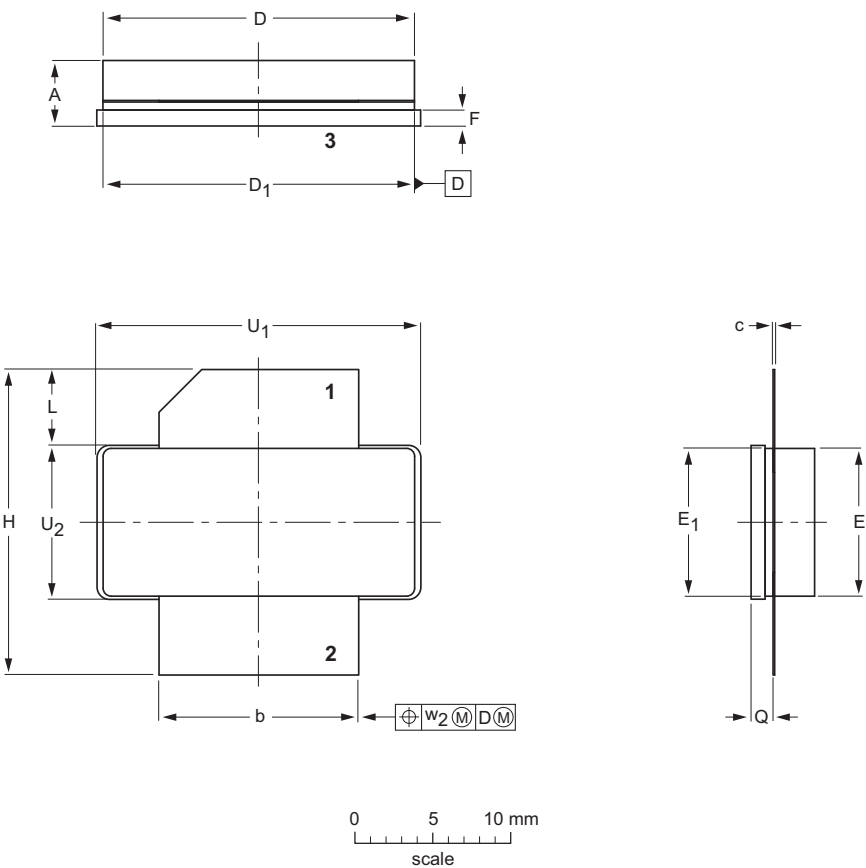


Fig 9. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						07-05-09 12-05-02

Fig 10. Package outline SOT502B

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
I_{Dq}	quiescent drain current
LDMOS	Laterally Diffused Metal Oxide Semiconductor
RF	Radio Frequency
SMD	Surface Mount Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BLA1011-200_BLA1011S-200#9	20150901	Product data sheet	-	-	BLA1011-200_8
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. - Legal texts have been adapted to the new company name where appropriate.				
BLA1011-200_BLA1011S-200_8	20051026	Product data sheet	-	-	BLA1011-200_7
BLA1011-200_7	20031111	Product specification	-	9397 750 12246	BLA1011-200_6
BLA1011-200_6	20020318	Product specification	-	9397 750 09414	BLA1011-200_5
BLA1011-200_5	20010515	Product specification	-	9397 750 08376	BLA1011-200_4
BLA1011-200_4	20010417	Product specification	-	9397 750 08139	BLA1011-200_N_3
BLA1011-200_N_3	20010302	Product specification	-	9397 750 08109	BLA1011-200_N_2
BLA1011-200_N_2	20001201	Product specification	-	9397 750 07638	BLA1011-200_N_1
BLA1011-200_N_1	20000906	Product specification	-	9397 750 07326	-

12. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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