

DSP56367

24-Bit Audio Digital Signal Processor

1 Overview

This document briefly describes the DSP56367 24-bit digital signal processor (DSP). The DSP56367 is a member of the DSP56300 family of programmable CMOS DSPs. The DSP56367 is targeted to applications that require digital audio compression/decompression, sound field processing, acoustic equalization and other digital audio algorithms. The DSP56367 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock at 1.8 V and 100 million instructions per second (MIPS) using an internal 100 MHz clock at 1.5 V.

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Data Sheet Conventions

This data sheet uses the following conventions:

- OVERBAR** Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
- “asserted” Means that a high true (active high) signal is high or that a low true (active low) signal is low
- “deasserted” Means that a high true (active high) signal is low or that a low true (active low) signal is high

| Examples: | Signal/Symbol | Logic State | Signal State | Voltage* |
|-----------|-------------------------|-------------|--------------|-------------------|
| | $\overline{\text{PIN}}$ | True | Asserted | V_{IL} / V_{OL} |
| | $\overline{\text{PIN}}$ | False | Deasserted | V_{IH} / V_{OH} |
| | PIN | True | Asserted | V_{IH} / V_{OH} |
| | PIN | False | Deasserted | V_{IL} / V_{OL} |

Note:*Values for V_{IL} , V_{OL} , V_{IH} , and V_{OH} are defined by individual product specifications.

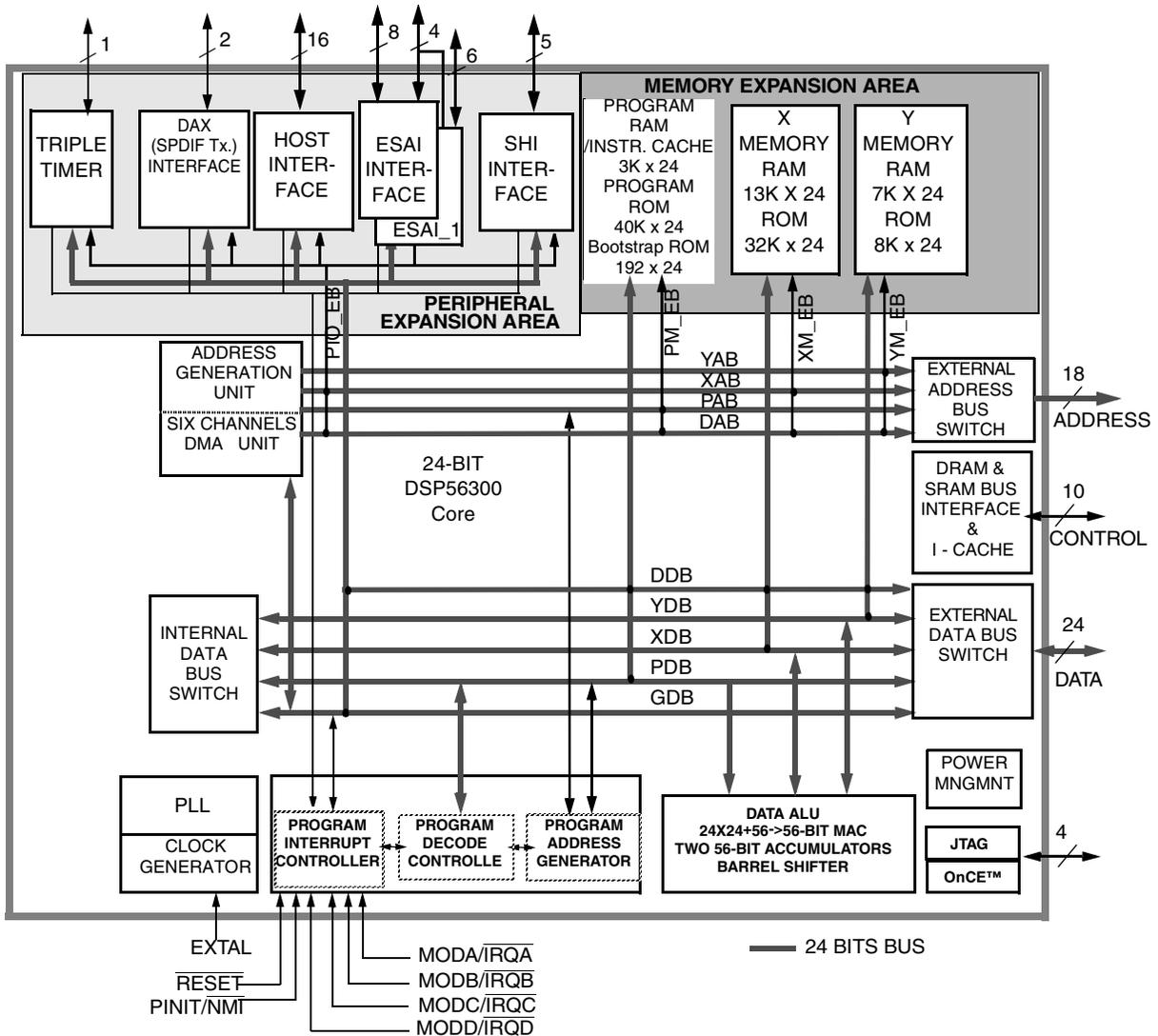


Figure 1-1 DSP56367 Block Diagram

1.1 Features

Core features are described fully in the *DSP56300 Family Manual*.

1.2 DSP56300 modular chassis

- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at internal logic supply (QVCCL) of 1.8V.
- 100 Million Instructions Per Second (MIPS) with a 100 MHz clock at internal logic supply (QVCCL) of 1.5V.
- Object Code Compatible with the 56K core.
- Data ALU with a 24×24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
- Program Control with position independent code support and instruction cache support.
- Six-channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i : $i=0$ to 7). Reduces clock noise.
- Internal address tracing support and OnCE™ for Hardware/Software debugging.
- JTAG port.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.

1.3 On-chip Memory Configuration

- $7K \times 24$ Bit Y-Data RAM and $8K \times 24$ Bit Y-Data ROM.
- $13K \times 24$ Bit X-Data RAM and $32K \times 24$ Bit X-Data ROM.
- $40K \times 24$ Bit Program ROM.
- $3K \times 24$ Bit Program RAM and 192×24 Bit Bootstrap ROM. 1K of Program RAM may be used as Instruction Cache or for Program ROM patching.
- $2K \times 24$ Bit from Y Data RAM and $5K \times 24$ Bit from X Data RAM can be switched to Program RAM resulting in up to $10K \times 24$ Bit of Program RAM.

1.4 Off-chip memory expansion

- External Memory Expansion Port.
- Off-chip expansion up to two $16M \times 24$ -bit word of Data memory.
- Off-chip expansion up to $16M \times 24$ -bit word of Program memory.
- Simultaneous glueless interface to SRAM and DRAM.

1.5 Peripheral modules

- Serial Audio Interface (ESAI): up to 4 receivers and up to 6 transmitters, master or slave. I²S, Sony, AC97, network and other programmable protocols.

- Serial Audio Interface I(ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. I²S, Sony, AC97, network and other programmable protocols
The ESAI_1 shares four of the data pins with ESAI, and ESAI_1 does NOT support HCKR and HCKT (high frequency clocks)
- Serial Host Interface (SHI): SPI and I²C protocols, multi master capability, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Byte-wide parallel Host Interface (HDI08) with DMA support.
- Triple Timer module (TEC).
- Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
- Pins of unused peripherals (except SHI) may be programmed as GPIO lines.

1.6 144-pin plastic LQFP package

1.7 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56367 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56367 Documentation

| Document Name | Description | Order Number |
|---|---|--|
| DSP56300 Family Manual | Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set | DSP56300FM |
| DSP56367 Product Brief | Brief description of the chip | DSP56367P |
| DSP56367 User's Manual | DSP56367 User's Manual | DSP56367UM |
| DSP56367 Technical Data Sheet (this document) | Electrical and timing specifications; pin and package descriptions | DSP56367 |
| IBIS Model | Input Output Buffer Information Specification | For software or simulation models, contact sales or go to www.freescale.com . |

2 Signal/Connection Descriptions

2.1 Signal Groupings

The input and output signals of the DSP56367 are organized into functional groups, which are listed in [Table 2-1](#) and illustrated in [Figure 2-1](#).

The DSP56367 is operated from a 1.8V supply; however, some of the inputs can tolerate 3.3V. A special notice for this feature is added to the signal descriptions of those inputs.

Remember, the DSP56367 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock at 1.8 V and 100 million instructions per second (MIPS) using an internal 100 MHz clock at 1.3.3V.

Table 2-1 DSP56367 Functional Signal Groupings

| Functional Group | | Number of Signals | Detailed Description |
|---------------------------------|---------------------|-------------------|----------------------------|
| Power (V _{CC}) | | 20 | Table 2-2 |
| Ground (GND) | | 18 | Table 2-3 |
| Clock and PLL | | 3 | Table 2-4 |
| Address bus | Port A ¹ | 18 | Table 2-5 |
| Data bus | | 24 | Table 2-6 |
| Bus control | | 10 | Table 2-7 |
| Interrupt and mode control | | 5 | Table 2-8 |
| HDI08 | Port B ² | 16 | Table 2-9 |
| SHI | | 5 | Table 2-10 |
| ESAI | Port C ³ | 12 | Table 2-11 |
| ESAI_1 | Port E ⁴ | 6 | Table 2-12 |
| Digital audio transmitter (DAX) | Port D ⁵ | 2 | Table 2-13 |
| Timer | | 1 | Table 2-14 |
| JTAG/OnCE Port | | 4 | Table 2-15 |

¹ Port A is the external memory interface port, including the external address bus, data bus, and control signals.

² Port B signals are the GPIO port signals which are multiplexed with the HDI08 signals.

³ Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.

⁴ Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.

⁵ Port D signals are the GPIO port signals which are multiplexed with the DAX signals.

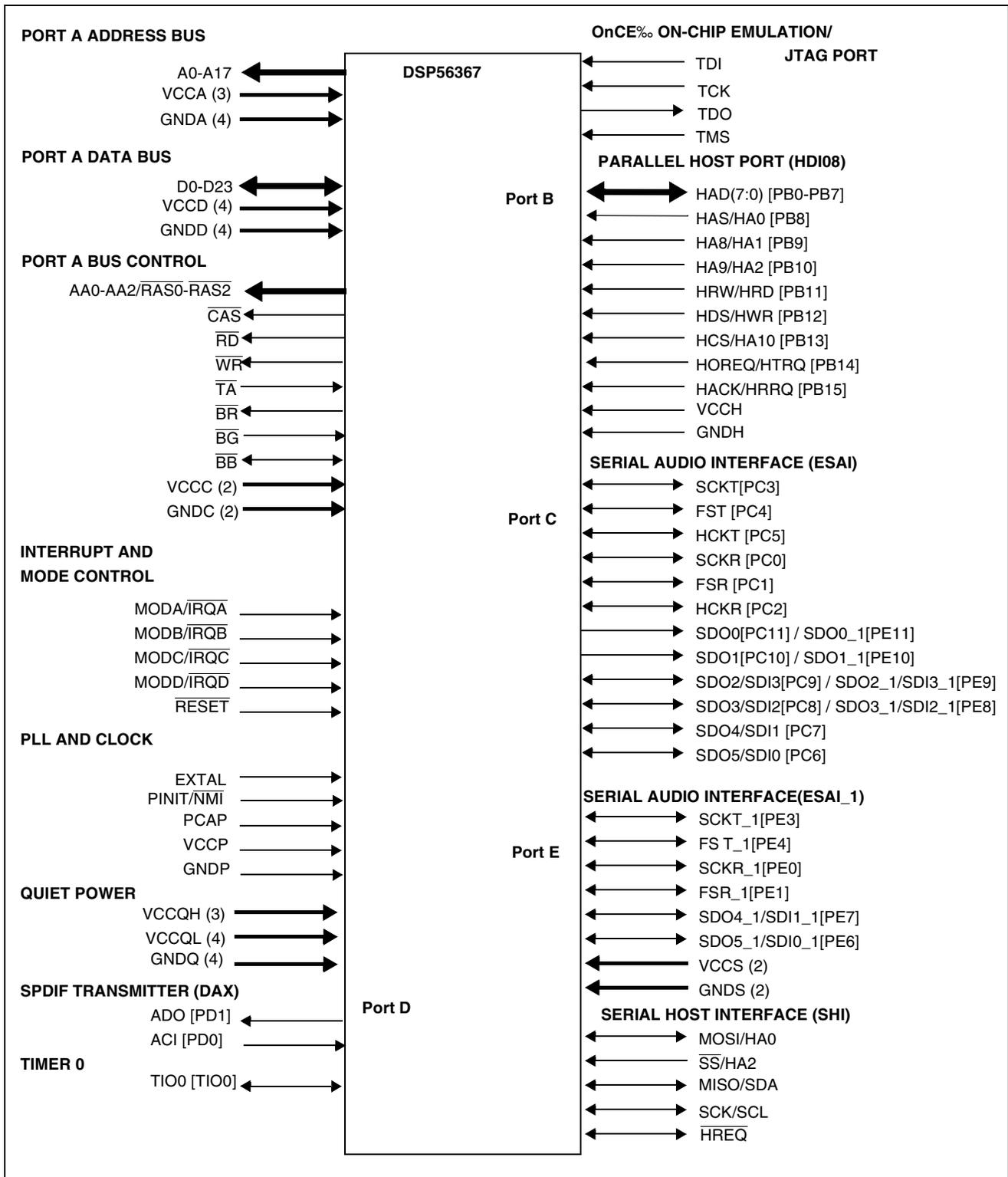


Figure 2-1 Signals Identified by Functional Group

2.2 Power

Table 2-2 Power Inputs

| Power Name | Description |
|----------------|---|
| V_{CCP} | PLL Power — V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input. |
| V_{CCQL} (4) | Quiet Core (Low) Power — V_{CCQL} is an isolated power for the internal processing logic. This input must be tied externally to all other V_{CCQL} power pins and the V_{CCP} power pin only. Do not tie with other power pins. The user must provide adequate external decoupling capacitors. There are four V_{CCQL} inputs. |
| V_{CCQH} (3) | Quiet External (High) Power — V_{CCQH} is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are three V_{CCQH} inputs. |
| V_{CCA} (3) | Address Bus Power — V_{CCA} is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are three V_{CCA} inputs. |
| V_{CCD} (4) | Data Bus Power — V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCD} inputs. |
| V_{CCC} (2) | Bus Control Power — V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCC} inputs. |
| V_{CCH} | Host Power — V_{CCH} is an isolated power for the HDI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCH} input. |
| V_{CCS} (2) | SHI, ESAI, ESAI_1, DAX and Timer Power — V_{CCS} is an isolated power for the SHI, ESAI, ESAI_1, DAX and Timer. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCS} inputs. |

2.3 Ground

Table 2-3 Grounds

| Ground Name | Description |
|-------------|---|
| GND_P | PLL Ground — GND_P is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 μ F capacitor located as close as possible to the chip package. There is one GND_P connection. |
| GND_Q (4) | Quiet Ground — GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections. |
| GND_A (4) | Address Bus Ground — GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections. |
| GND_D (4) | Data Bus Ground — GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_D connections. |

Table 2-3 Grounds (continued)

| Ground Name | Description |
|----------------------|---|
| GND _C (2) | Bus Control Ground —GND _C is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND _C connections. |
| GND _H | Host Ground —GND _H is an isolated ground for the HD08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND _H connection. |
| GND _S (2) | SHI, ESAI, ESAI_1, DAX and Timer Ground —GND _S is an isolated ground for the SHI, ESAI, ESAI_1, DAX and Timer. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND _S connections. |

2.4 Clock and PLL

Table 2-4 Clock and PLL Signals

| Signal Name | Type | State During Reset | Signal Description |
|--------------------------------|-------|--------------------|---|
| EXTAL | Input | Input | External Clock Input —An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. |
| PCAP | Input | Input | PLL Capacitor —PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V _{CCP} . If the PLL is not used, PCAP may be tied to V _{CC} , GND, or left floating. |
| PINIT/ $\overline{\text{NMI}}$ | Input | Input | PLL Initial/Nonmaskable Interrupt —During assertion of $\overline{\text{RESET}}$, the value of PINIT/ $\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, the PINIT/ $\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock. |

2.5 External Memory Expansion Port (Port A)

When the DSP56367 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant port A signals: A0–A17, D0–D23, AA0/ $\overline{\text{RAS0}}$ –AA2/ $\overline{\text{RAS2}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$.

2.6 External Address Bus

Table 2-5 External Address Bus Signals

| Signal Name | Type | State During Reset | Signal Description |
|-------------|--------|--------------------|---|
| A0–A17 | Output | Tri-States | Address Bus —When the DSP is the bus master, A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed. |

2.7 External Data Bus

Table 2-6 External Data Bus Signals

| Signal Name | Type | State during Reset | Signal Description |
|-------------|--------------|--------------------|---|
| D0–D23 | Input/Output | Tri-Stated | Data Bus —When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated. |

2.8 External Bus Control

Table 2-7 External Bus Control Signals

| Signal Name | Type | State During Reset | Signal Description |
|---|--------|--------------------|--|
| AA0–AA2/ $\overline{\text{RAS0}}\text{--}\overline{\text{RAS2}}$ | Output | Tri-Stated | Address Attribute or Row Address Strobe —When defined as AA, these signals can be used as chip selects or additional address lines. When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity. |
| $\overline{\text{CAS}}$ | Output | Tri-Stated | Column Address Strobe — When the DSP is the bus master, $\overline{\text{CAS}}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the bus mastership enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated. |
| $\overline{\text{RD}}$ | Output | Tri-Stated | Read Enable —When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D0–D23). Otherwise, $\overline{\text{RD}}$ is tri-stated. |
| $\overline{\text{WR}}$ | Output | Tri-Stated | Write Enable —When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D0–D23). Otherwise, $\overline{\text{WR}}$ is tri-stated. |
| $\overline{\text{TA}}$ | Input | Ignored Input | <p>Transfer Acknowledge—If the DSP is the bus master and there is no external bus activity, or the DSP is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2, . . .infinity) may be added to the wait states inserted by the BCR by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to the internal system clock. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the bus control register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles.</p> <p>In order to use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion, otherwise improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously, depending on the setting of the TAS bit in the operating mode register (OMR).</p> <p>$\overline{\text{TA}}$ functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.</p> |

Table 2-7 External Bus Control Signals (continued)

| Signal Name | Type | State During Reset | Signal Description |
|-----------------|--------------|---------------------|---|
| \overline{BR} | Output | Output (deasserted) | Bus Request — \overline{BR} is an active-low output, never tri-stated. \overline{BR} is asserted when the DSP requests bus mastership. \overline{BR} is deasserted when the DSP no longer needs the bus. \overline{BR} may be asserted or deasserted independent of whether the DSP56367 is a bus master or a bus slave. Bus “parking” allows \overline{BR} to be deasserted even though the DSP56367 is the bus master. (See the description of bus “parking” in the \overline{BB} signal description.) The bus request hold (BRH) bit in the BCR allows \overline{BR} to be asserted under software control even though the DSP does not need the bus. \overline{BR} is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. \overline{BR} is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, \overline{BR} is deasserted and the arbitration is reset to the bus slave state. |
| \overline{BG} | Input | Ignored Input | Bus Grant — \overline{BG} is an active-low input. \overline{BG} is asserted by an external bus arbitration circuit when the DSP56367 becomes the next bus master. When \overline{BG} is asserted, the DSP56367 must wait until \overline{BB} is deasserted before taking bus mastership. When \overline{BG} is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. For proper \overline{BG} operation, the asynchronous bus arbitration enable bit (ABE) in the OMR register must be set. |
| \overline{BB} | Input/Output | Input | Bus Busy — \overline{BB} is a bidirectional active-low input/output. \overline{BB} indicates that the bus is active. Only after \overline{BB} is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep \overline{BB} asserted after ceasing bus activity regardless of whether \overline{BR} is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus. The deassertion of \overline{BB} is done by an “active pull-up” method (i.e., \overline{BB} is driven high and then released and held high by an external pull-up resistor). For proper \overline{BB} operation, the asynchronous bus arbitration enable bit (ABE) in the OMR register must be set. \overline{BB} requires an external pull-up resistor. |

2.9 Interrupt and Mode Control

The interrupt and mode control signals select the chip’s operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 2-8 Interrupt and Mode Control

| Signal Name | Type | State During Reset | Signal Description |
|---|-------|--------------------|--|
| $\overline{\text{MODA}}/\overline{\text{IRQA}}$ | Input | Input | <p>Mode Select A/External Interrupt Request A—$\overline{\text{MODA}}/\overline{\text{IRQA}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. $\overline{\text{MODA}}/\overline{\text{IRQA}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. If the processor is in the stop standby state and the $\overline{\text{MODA}}/\overline{\text{IRQA}}$ pin is pulled to GND, the processor will exit the stop state.</p> <p><i>This input is 3.3V tolerant.</i></p> |
| $\overline{\text{MODB}}/\overline{\text{IRQB}}$ | Input | Input | <p>Mode Select B/External Interrupt Request B—$\overline{\text{MODB}}/\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. $\overline{\text{MODB}}/\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted.</p> <p>This input is 3.3V tolerant.</p> |
| $\overline{\text{MODC}}/\overline{\text{IRQC}}$ | Input | Input | <p>Mode Select C/External Interrupt Request C—$\overline{\text{MODC}}/\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. $\overline{\text{MODC}}/\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted.</p> <p>This input is 3.3V tolerant.</p> |
| $\overline{\text{MODD}}/\overline{\text{IRQD}}$ | Input | Input | <p>Mode Select D/External Interrupt Request D—$\overline{\text{MODD}}/\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. $\overline{\text{MODD}}/\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted.</p> <p>This input is 3.3V tolerant.</p> |
| $\overline{\text{RESET}}$ | Input | Input | <p>Reset—$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted.</p> <p><i>This input is 3.3V tolerant.</i></p> |

2.10 Parallel Host Interface (HDI08)

The HDI08 provides a fast, 8-bit, parallel data port that may be connected directly to the host bus. The HDI08 supports a variety of standard buses and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware.

Table 2-9 Host Interface

| Signal Name | Type | State During Reset | Signal Description |
|------------------------------|--------------------------------|----------------------|--|
| H0–H7 | Input/Output | GPIO Disconnected | <p>Host Data—When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, tri-state data bus.</p> <p>Host Address/Data—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the address/data bidirectional, multiplexed, tri-state bus.</p> <p>Port B 0–7—When the HDI08 is configured as GPIO, these signals are individually programmable as input, output, or internally disconnected. The default state after reset for these signals is GPIO disconnected. These inputs are 3.3V tolerant.</p> |
| HAD0–HAD7 | Input/Output | | |
| PB0–PB7 | Input, Output, or Disconnected | | |
| HA0 | Input | GPIO Disconnected | <p>Host Address Input 0—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.</p> <p>Host Address Strobe—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable, but is configured active-low ($\overline{\text{HAS}}$) following reset.</p> <p>Port B 8—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.</p> |
| $\overline{\text{HAS}}$ /HAS | Input | | |
| PB8 | Input, Output, or Disconnected | | |
| HA1 | Input | GPIO Disconnected | <p>Host Address Input 1—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.</p> <p>Host Address 8—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.</p> <p>Port B 9—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.</p> |
| HA8 | Input | | |
| PB9 | Input, Output, or Disconnected | | |

Table 2-9 Host Interface (continued)

| Signal Name | Type | State During Reset | Signal Description |
|----------------------------------|--------------------------------|----------------------|---|
| HA2 | Input | GPIO Disconnected | Host Address Input 2 —When the HDI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus. |
| HA9 | Input | | Host Address 9 —When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus. |
| PB10 | Input, Output, or Disconnected | | Port B 10 —When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant. |
| HRW | Input | GPIO Disconnected | Host Read/Write —When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/Write (HRW) input. |
| $\overline{\text{HRD}}$ / HRD | Input | | Host Read Data —When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host read data strobe (HRD) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HRD}}$) after reset. |
| PB11 | Input, Output, or Disconnected | | Port B 11 —When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant. |
| $\overline{\text{HDS}}$ / HDS | Input | GPIO Disconnected | Host Data Strobe —When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HDS}}$) following reset. |
| $\overline{\text{HWR}}$ / HWR | Input | | Host Write Data —When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HWR}}$) following reset. |
| PB12 | Input, Output, or Disconnected | | Port B 12 —When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant. |

Table 2-9 Host Interface (continued)

| Signal Name | Type | State During Reset | Signal Description |
|--------------------------------------|--------------------------------|----------------------|---|
| HCS | Input | GPIO Disconnected | <p>Host Chip Select—When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable, but is configured active-low ($\overline{\text{HCS}}$) after reset.</p> <p>Host Address 10—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.</p> <p>Port B 13—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.</p> |
| HA10 | Input | | |
| PB13 | Input, Output, or Disconnected | | |
| $\overline{\text{HOREQ}}$ / HOREQ | Output | GPIO Disconnected | <p>Host Request—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host request (HOREQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HOREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.</p> <p>Transmit Host Request—When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.</p> <p>Port B 14—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.</p> |
| $\overline{\text{HTRQ}}$ / HTRQ | Output | | |
| PB14 | Input, Output, or Disconnected | | |
| $\overline{\text{HACK}}$ / HACK | Input | GPIO Disconnected | <p>Host Acknowledge—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable, but is configured as active-low ($\overline{\text{HACK}}$) after reset.</p> <p>Receive Host Request—When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.</p> <p>Port B 15—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.</p> |
| $\overline{\text{HRRQ}}$ / HRRQ | Output | | |
| PB15 | Input, Output, or Disconnected | | |

2.11 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I²C mode.

Table 2-10 Serial Host Interface Signals

| Signal Name | Signal Type | State During Reset | Signal Description |
|-------------|----------------------------|--------------------|--|
| SCK | Input or Output | Tri-Stated | <p>SPI Serial Clock—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select (\overline{SS}) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.</p> |
| SCL | Input or Output | Tri-Stated | <p>I²C Serial Clock—SCL carries the clock for I²C bus transactions in the I²C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{CC} through a pull-up resistor.</p> <p>This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state.</p> <p>This input is 3.3V tolerant.</p> |
| MISO | Input or Output | Tri-Stated | <p>SPI Master-In-Slave-Out—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when \overline{SS} is deasserted. An external pull-up resistor is not required for SPI operation.</p> |
| SDA | Input or Open-Drain Output | Tri-Stated | <p>I²C Data and Acknowledge—In I²C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I²C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event.</p> <p>This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state.</p> <p>This input is 3.3V tolerant.</p> |

Table 2-10 Serial Host Interface Signals (continued)

| Signal Name | Signal Type | State During Reset | Signal Description |
|-------------------|-----------------|--------------------|--|
| MOSI | Input or Output | Tri-Stated | SPI Master-Out-Slave-In —When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode. |
| HA0 | Input | | I²C Slave Address 0 —This signal uses a Schmitt-trigger input when configured for the I ² C mode. When configured for I ² C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I ² C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 3.3V tolerant. |
| \overline{SS} | Input | Tri-Stated | SPI Slave Select —This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If \overline{SS} is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state. |
| HA2 | Input | | I²C Slave Address 2 —This signal uses a Schmitt-trigger input when configured for the I ² C mode. When configured for the I ² C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I ² C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 3.3V tolerant. |
| \overline{HREQ} | Input or Output | Tri-Stated | Host Request —This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, \overline{HREQ} is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, \overline{HREQ} is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of \overline{HREQ} to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for external pull-up in this state. This input is 3.3V tolerant. |

2.12 Enhanced Serial Audio Interface

Table 2-11 Enhanced Serial Audio Interface Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|--------------------------------|----------------------|---|
| HCKR | Input or Output | GPIO Disconnected | <p>High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.</p> <p>Port C 2—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| PC2 | Input, Output, or Disconnected | | |
| HCKT | Input or Output | GPIO Disconnected | <p>High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.</p> <p>Port C 5—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| PC5 | Input, Output, or Disconnected | | |
| FSR | Input or Output | GPIO Disconnected | <p>Frame Sync for Receiver—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1).</p> <p>When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.</p> <p>Port C 1—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| PC1 | Input, Output, or Disconnected | | |

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|--------------------------------|----------------------|--|
| FST | Input or Output | GPIO Disconnected | <p>Frame Sync for Transmitter—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).</p> <p>Port C 4—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| PC4 | Input, Output, or Disconnected | | |
| SCKR | Input or Output | GPIO Disconnected | <p>Receiver Serial Clock—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1).</p> <p>When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.</p> <p>Port C 0—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| PC0 | Input, Output, or Disconnected | | |
| SCKT | Input or output | GPIO Disconnected | <p>Transmitter Serial Clock—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.</p> <p>Port C 3—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| PC3 | Input, Output, or Disconnected | | |
| SDO5 | Output | GPIO Disconnected | <p>Serial Data Output 5—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.</p> <p>Serial Data Input 0—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.</p> <p>Port C 6—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |
| SDI0 | Input | | |
| PC6 | Input, Output, or Disconnected | | |

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

| Signal Name | Signal Type | State during Reset | Signal Description |
|---|---|--------------------|--|
| SDO4 SDI1 PC7 | Output Input Input, Output, or Disconnected | GPIO Disconnected | <p>Serial Data Output 4—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.</p> <p>Serial Data Input 1—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.</p> <p>Port C 7—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.</p> |
| SDO3/ SDO3_1 SDI2/ SDI2_1 PC8/PE8 | Output Input Input, Output, or Disconnected | GPIO Disconnected | <p>Serial Data Output 3—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 3.</p> <p>Serial Data Input 2—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Input 2.</p> <p>Port C 8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 8 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.</p> |
| SDO2/ SDO2_1 SDI3/ SDI3_1 PC9/PE9 | Output Input Input, Output, or Disconnected | GPIO Disconnected | <p>Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 2.</p> <p>Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Input 3.</p> <p>Port C 9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 9 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.</p> |
| SDO1/ SDO1_1 PC10/ PE10 | Output Input, Output, or disconnected | GPIO Disconnected | <p>Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 1.</p> <p>Port C 10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 10 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.</p> |

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

| Signal Name | Signal Type | State during Reset | Signal Description |
|-----------------|-----------------------------------|----------------------|---|
| SDO0/ SDO0_1 | Output | GPIO Disconnected | Serial Data Output 0 —SDO0 is used to transmit data from the TX0 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 0. |
| PC11/ PE11 | Input, Output, or Disconnected | | Port C 11 —When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 11 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant. |

2.13 Enhanced Serial Audio Interface_1

Table 2-12 Enhanced Serial Audio Interface_1 Signals

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|-----------------------------------|----------------------|---|
| FSR_1 | Input or Output | GPIO Disconnected | Frame Sync for Receiver_1 —This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode. |
| PE1 | Input, Output, or Disconnected | | Port E 1 —When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V. |
| FST_1 | Input or Output | GPIO Disconnected | Frame Sync for Transmitter_1 —This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR). |
| PE4 | Input, Output, or Disconnected | | Port E 4 —When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V. |

Table 2-12 Enhanced Serial Audio Interface_1 Signals (continued)

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------------------|---|--------------------|--|
| SCKR_1 PE0 | Input or Output Input, Output, or Disconnected | GPIO Disconnected | <p>Receiver Serial Clock_1—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1).</p> <p>When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.</p> <p>Port E 0—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input cannot tolerate 3.3V.</p> |
| SCKT_1 PE3 | Input or Output Input, Output, or Disconnected | GPIO Disconnected | <p>Transmitter Serial Clock_1—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.</p> <p>Port E 3—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input cannot tolerate 3.3V.</p> |
| SDO5_1 SDI0_1 PE6 | Output Input Input, Output, or Disconnected | GPIO Disconnected | <p>Serial Data Output 5_1—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.</p> <p>Serial Data Input 0_1—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.</p> <p>Port E 6—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input cannot tolerate 3.3V.</p> |
| SDO4_1 SDI1_1 PE7 | Output Input Input, Output, or Disconnected | GPIO Disconnected | <p>Serial Data Output 4_1—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.</p> <p>Serial Data Input 1_1—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.</p> <p>Port E 7—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This input is 3.3V tolerant.</p> |

2.14 SPDIF Transmitter Digital Audio Interface

Table 2-13 Digital Audio Interface (DAX) Signals

| Signal Name | Type | State During Reset | Signal Description |
|-------------|--------------------------------|--------------------|---|
| ACI | Input | GPIO Disconnected | Audio Clock Input —This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency ($256 \times F_s$, $384 \times F_s$ or $512 \times F_s$, respectively). |
| PD0 | Input, Output, or Disconnected | GPIO Disconnected | Port D 0 —When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant. |
| ADO | Output | GPIO Disconnected | Digital Audio Data Output —This signal is an audio and non-audio output in the form of AES/EBU, CP340 and IEC958 data in a biphase mark format. |
| PD1 | Input, Output, or Disconnected | GPIO Disconnected | Port D 1 —When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant. |

2.15 Timer

Table 2-14 Timer Signal

| Signal Name | Type | State during Reset | Signal Description |
|-------------|-----------------|--------------------|--|
| TIO0 | Input or Output | Input | Timer 0 Schmitt-Trigger Input/Output —When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to Vcc through a pull-up resistor in order to ensure a stable logic level at this input. This input is 3.3 V tolerant. |

2.16 JTAG/OnCE Interface

Table 2-15 JTAG/OnCE Interface

| Signal Name | Signal Type | State during Reset | Signal Description |
|-------------|-------------|--------------------|--|
| TCK | Input | Input | Test Clock —TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. This input is 3.3V tolerant. |
| TDI | Input | Input | Test Data Input —TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 3.3V tolerant. |
| TDO | Output | Tri-Stated | Test Data Output —TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK. |
| TMS | Input | Input | Test Mode Select —TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 3.3V tolerant. |

NOTES

3 Specifications

3.1 Introduction

The DSP56367 is a high density CMOS device with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Finalized specifications may be published after further characterization and device qualifications are completed.

3.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{CC}). The suggested value for a pull-up or pull-down resistor is 10 k Ω .

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3-1 Maximum Ratings

| Rating ¹ | Symbol | Value ^{1, 2} | Unit |
|--|---|-----------------------------|------|
| Supply Voltage | V_{CCQL}, V_{CCP} | -0.3 to + 2.0 | V |
| | $V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, V_{CCS}$ | -0.3 to + 4.0 | V |
| All "3.3V tolerant" input voltages | V_{IN} | GND - 0.3 to $V_{CC} + 0.7$ | V |
| Current drain per pin excluding V_{CC} and GND | I | 10 | mA |
| Operating temperature range ³ | T_J | -40 to + 95 | °C |
| Storage temperature | T_{STG} | -55 to +125 | °C |

¹ GND = 0 V, VCCP, VCCQL = 1.8 V ±5%, T_J = -40°C to +95°C, CL = 50 pF
All other VCC = 3.3 V ± 5%, T_J = -40°C to +95°C, CL = 50 pF

² Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

³ Temperatures below -0°C are qualified for consumer applications.

3.3 Thermal Characteristics

Table 3-2 Thermal Characteristics

| Characteristic | Symbol | TQFP Value | Unit |
|---|----------------------------------|------------|------|
| Natural Convection, Junction-to-ambient thermal resistance ^{1,2} | $R_{\theta JA}$ or θ_{JA} | 45.0 | °C/W |
| Junction-to-case thermal resistance ³ | $R_{\theta JC}$ or θ_{JC} | 10.0 | °C/W |
| Natural Convection, Thermal characterization parameter ⁴ | Ψ_{JT} | 3.0 | °C/W |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

³ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁴ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4 DC Electrical Characteristics

Table 3-3 DC Electrical Characteristics¹

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|--|--------------------|---|---------|
| Supply voltages • Core (V_{CCQL}) • PLL(V_{CCP}) | V_{CC} | 1.71 | 1.8 | 1.89 | V |
| Supply voltages • V_{CCQH} • V_{CCA} • V_{CCD} • V_{CCC} • V_{CCH} • V_{CCS} | V_{CC} | 3.14 | 3.3 | 3.46 | V |
| Input high voltage • D(0:23), \overline{BG} , \overline{BB} , \overline{TA} , ESAI_1 (except SDO4_1) • $\overline{MOD^2/IRQ^2}$, \overline{RESET} , $\overline{PINIT/NMI}$ and all JTAG/ESAI_1/Timer/HDI08/DAX/(only SDO4_1)/SHI(SPI mode) • SHI(I2C mode) • EXTAL | V_{IH} V_{IHP} V_{IHP} V_{IHx} | 2.0 2.0 1.5 $0.8 \times V_{CCQH}$ | — — — — | V_{CCQH} $V_{CCQH} + 03$ max for both V_{IHP} $V_{CCQH} + 03$ max for both V_{IHP} $0.8 \times V_{CCQH}$ | V |
| Input low voltage • D(0:23), \overline{BG} , \overline{BB} , \overline{TA} , ESAI_1 (except SDO4_1) • $\overline{MOD^2/IRQ^2}$, \overline{RESET} , $\overline{PINIT/NMI}$ and all JTAG/ESAI/Timer/HDI08/DAX/ESAI_1 (only SDO4_1)/SHI(SPI mode) • SHI(I2C mode) • EXTAL | V_{IL} V_{ILP} V_{ILP} V_{ILx} | -0.3 -0.3 -0.3 -0.3 | — — — — | 0.8 0.8 $0.3 \times V_{CC}$ $0.2 \times V_{CCQH}$ | V |
| Input leakage current | I_{IN} | -10 | — | 10 | μ A |
| High impedance (off-state) input current (@ 2.4 V / 0.4 V) | I_{TSI} | -10 | — | 10 | μ A |
| Output high voltage ³ | V_{OH} | 2.4 | — | — | V |
| Output low voltage ³ | V_{OL} | — | — | 0.4 | V |
| Internal supply current ⁴ at internal clock of 150MHz • In Normal mode • In Wait mode • In Stop mode ⁵ | I_{CCI} I_{CCW} I_{CCS} | — — — | 58.0 7.3 2.0 | 115 20 4 | mA |
| PLL supply current | | — | 1 | 2.5 | mA |
| Input capacitance ⁶ | C_{IN} | — | — | 10 | pF |

¹ $V_{CCQL} = 1.8 \text{ V} \pm 5\%$, $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50 \text{ pF}$
All other $V_{CC} = 3.3 \text{ V} \pm 5\%$, $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50 \text{ pF}$

² Refers to $\overline{MODA/IRQA}$, $\overline{MODB/IRQB}$, $\overline{MODC/IRQC}$, and $\overline{MODD/IRQD}$ pins.

AC Electrical Characteristics

- ³ This characteristic does not apply to PCAP.
- ⁴ The [Appendix A, "Power Consumption Benchmark"](#) section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with $V_{CCQL} = 1.8V$, $V_{CC(Other)} = 3.3V$ at $T_J = 25^\circ C$. Maximum internal supply current is measured with $V_{CCQL} = 1.89V$, $V_{CC(Other)} = 3.46V$ at $T_J = 95^\circ C$.
- ⁵ In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).
- ⁶ Periodically sampled and not 100% tested

3.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.4 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56367 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

NOTE

Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

3.6 Internal Clocks

Table 3-4 Internal Clocks

| Characteristics | Symbol | Expression ^{1, 2} | | |
|--|--------|--|----------------------------------|--|
| | | Min | Typ | Max |
| Internal operation frequency with PLL enabled | f | — | $(Ef \times MF)/(PDF \times DF)$ | — |
| Internal operation frequency with PLL disabled | f | — | $Ef/2$ | — |
| Internal clock high period | T_H | — | ET_C | — |
| • With PLL disabled | | — | ET_C | — |
| • With PLL enabled and $MF \leq 4$ | | $0.49 \times ET_C \times PDF \times DF/MF$ | — | $0.51 \times ET_C \times PDF \times DF/MF$ |
| • With PLL enabled and $MF > 4$ | | $0.47 \times ET_C \times PDF \times DF/MF$ | — | $0.53 \times ET_C \times PDF \times DF/MF$ |
| Internal clock low period | T_L | — | ET_C | — |
| • With PLL disabled | | — | ET_C | — |
| • With PLL enabled and $MF \leq 4$ | | $0.49 \times ET_C \times PDF \times DF/MF$ | — | $0.51 \times ET_C \times PDF \times DF/MF$ |
| • With PLL enabled and $MF > 4$ | | $0.47 \times ET_C \times PDF \times DF/MF$ | — | $0.53 \times ET_C \times PDF \times DF/MF$ |
| Internal clock cycle time with PLL enabled | T_C | — | $ET_C \times PDF \times DF/MF$ | — |

Table 3-4 Internal Clocks (continued)

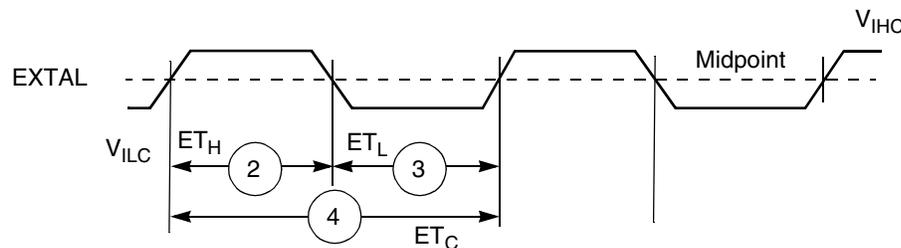
| Characteristics | Symbol | Expression ^{1, 2} | | |
|---|-----------|----------------------------|-----------------|-----|
| | | Min | Typ | Max |
| Internal clock cycle time with PLL disabled | T_C | — | $2 \times ET_C$ | — |
| Instruction cycle time | I_{CYC} | — | T_C | — |

¹ DF = Division Factor
Ef = External frequency
 ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
 T_C = internal clock cycle

² Refer to the DSP56300 Family Manual for a detailed discussion of the PLL.

3.7 External Clock Operation

The DSP56367 system clock is an externally supplied square wave voltage source connected to EXTAL (Figure 3-1).



Note: The midpoint is $0.5 (V_{IHC} + V_{ILC})$.

Figure 3-1 External Clock Timing

Table 3-5 Clock Operation

| No. | Characteristics | Symbol | Min | Max |
|-----|---|--------|--------------------|---------------------------|
| 1 | Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 2 ns maximum. | Ef | 2.0 ns | 150.0 |
| 2 | EXTAL input high ^{1, 2} <ul style="list-style-type: none"> With PLL disabled (46.7%–53.3% duty cycle³) With PLL enabled (42.5%–57.5% duty cycle³) | ET_H | 3.11 ns 2.83 ns | ∞ 157.0 μ s |
| 3 | EXTAL input low ^{1, 2} <ul style="list-style-type: none"> With PLL disabled (46.7%–53.3% duty cycle³) With PLL enabled (42.5%–57.5% duty cycle³) | ET_L | 3.11 ns 2.83 ns | ∞ 157.0 μ s |

Phase Lock Loop (PLL) Characteristics

Table 3-5 Clock Operation (continued)

| No. | Characteristics | Symbol | Min | Max |
|-----|--|-----------|---------------------|---------------------------|
| 4 | EXTAL cycle time ² <ul style="list-style-type: none"> • With PLL disabled • With PLL enabled | ET_C | 6.7 ns 6.7 ns | ∞ 273.1 μ s |
| 7 | Instruction cycle time = $I_{CYC} = T_C^4$ <ul style="list-style-type: none"> • With PLL disabled • With PLL enabled | I_{CYC} | 13.33 ns 6.67 ns | ∞ 8.53 μ s |

¹ Measured at 50% of the input transition.

² The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.

³ The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

⁴ The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.

3.8 Phase Lock Loop (PLL) Characteristics

Table 3-6 PLL Characteristics

| Characteristics | Min | Max | Unit |
|---|--|---|------|
| V_{CO} frequency when PLL enabled ($MF \times E_f \times 2/PDF$) | 30 | 300 | MHz |
| PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}^1) <ul style="list-style-type: none"> • @ $MF \leq 4$ • @ $MF > 4$ | $(MF \times 580) - 100$ $MF \times 830$ | $(MF \times 780) - 140$ $MF \times 1470$ | pF |

¹ C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
 $(MF \times 680) - 120$, for $MF \leq 4$, or
 $MF \times 1100$, for $MF > 4$.

3.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing¹

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|---|--|--|----------------------------|---|
| 8 | Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value ² | — | — | 26.0 | ns |
| 9 | Required $\overline{\text{RESET}}$ duration ³ <ul style="list-style-type: none"> Power on, external clock generator, PLL disabled Power on, external clock generator, PLL enabled Power on, Internal oscillator During STOP, XTAL disabled During STOP, XTAL enabled During normal operation | $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$ | 333.4 6.7 500 500 16.7 16.7 | — — — — — — | ns μs μs μs ns ns |
| 10 | Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion) ⁴ <ul style="list-style-type: none"> Minimum Maximum | $3.25 \times TC + 2.0$ $20.25 \times TC + 10$ | 23.7 — | — 145.0 | ns |
| 11 | Syn reset setup time from RESET <ul style="list-style-type: none"> Maximum | T_C | — | 6.7 | ns |
| 12 | Syn reset deassert delay time <ul style="list-style-type: none"> Minimum Maximum | $3.25 \times T_C + 1.0$ $20.25 \times T_C + 5.0$ | 22.7 — | — 140.0 | ns |
| 13 | Mode select setup time | | 30.0 | — | ns |
| 14 | Mode select hold time | | 0.0 | — | ns |
| 15 | Minimum edge-triggered interrupt request assertion width | | 4.4 | — | ns |
| 16 | Minimum edge-triggered interrupt request deassertion width | | 4.4 | — | ns |
| 17 | Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid <ul style="list-style-type: none"> Caused by first interrupt instruction fetch Caused by first interrupt instruction execution | $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$ | 30.3 50.3 | — — | ns |
| 18 | Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution | $10 \times T_C + 5.0$ | 71.7 | — | ns |
| 19 | Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts ^{5, 6, 7} | $(WS + 3.75) \times T_C - 10.94$ | — | Note 8 | ns |
| 20 | Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts ^{5, 6, 7} | $(WS + 3.25) \times T_C - 10.94$ | — | Note 8 | ns |

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing¹ (continued)

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|---|---|------------------|--------------------------------------|----------------|
| 21 | Delay from \overline{WR} assertion to interrupt request deassertion for level sensitive fast interrupts ^{5, 6, 7} <ul style="list-style-type: none"> • DRAM for all WS • SRAM WS = 1 • SRAM WS = 2, 3 • SRAM WS \geq 4 | $(WS + 3.5) \times T_C - 10.94$ N/A $1.75 \times T_C - 4.0$ $2.75 \times T_C - 4.0$ | — | Note 8 Note 8 Note 8 Note 8 | ns |
| 22 | Synchronous int setup time from IRQs NMI assertion to the CLKOUT trans. | $0.6 \times T_C - 0.1$ | 3.9 | — | ns |
| 23 | Synch. int delay time from the CLKOUT trans ² to the first external address out valid caused by first inst fetch <ul style="list-style-type: none"> • Minimum • Maximum | $9.25 \times T_C + 1.0$ $24.75 \times T_C + 5.0$ | 62.7 — | — 170.0 | ns |
| 24 | Duration for \overline{IRQA} assertion to recover from Stop state | $0.6 \times T_C - 0.1$ | 3.9 | — | ns |
| 25 | Delay from \overline{IRQA} assertion to fetch of first instruction (when exiting Stop) ^{2, 8} <ul style="list-style-type: none"> • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay) | $PLC \times ET_C \times PDF + (128 K - PLC/2) \times T_C$ $PLC \times ET_C \times PDF + (23.75 +/- 0.5) \times T_C$ $(8.25 \pm 0.5) \times T_C$ | — — 51.7 | — — 58.3 | ms ms ns |
| 26 | Duration of level sensitive \overline{IRQA} assertion to ensure interrupt service (when exiting Stop) ^{2, 8} <ul style="list-style-type: none"> • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay) | $PLC \times ET_C \times PDF + (128 K - PLC/2) \times T_C$ $PLC \times ET_C \times PDF + (20.5 +/- 0.5) \times T_C$ $5.5 \times T_C$ | — — 36.7 | — — | ms ms ns |
| 27 | Interrupt Requests Rate <ul style="list-style-type: none"> • HDI08, ESAI, ESAI_1, SHI, DAX, Timer • DMA • \overline{IRQ}, \overline{NMI} (edge trigger) • \overline{IRQ} (level trigger) | $12T_C$ $8T_C$ $8T_C$ $12T_C$ | — — — — | 80.0 53.0 53.0 80.0 | ns |

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing¹ (continued)

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|---|--------------------------------------|------|------------------------------|------|
| 28 | DMA Requests Rate <ul style="list-style-type: none"> Data read from HDI08, ESAI, ESAI_1, SHI, DAX Data write to HDI08, ESAI, ESAI_1, SHI, DAX Timer \overline{IRQ}, \overline{NMI} (edge trigger) | $6T_C$ $7T_C$ $2T_C$ $3T_C$ | — | 40.0 46.7 13.3 20.0 | ns |
| 29 | Delay from \overline{IRQA} , \overline{IRQB} , \overline{IRQC} , \overline{IRQD} , \overline{NMI} assertion to external memory (DMA source) access address out valid | $4.25 \times T_C + 2.0$ | 30.3 | — | ns |

¹ $V_{CCQH} = 3.3 \text{ V} \pm 5\%$; $V_{CC} = 1.8 \text{ V} \pm 5\%$; $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50 \text{ pF}$

² Periodically sampled and not 100% tested.

³ \overline{RESET} duration is measured during the time in which \overline{RESET} is asserted, V_{CC} is valid, and the EXTAL input is active and valid. When the V_{CC} is valid, but the other “required \overline{RESET} duration” conditions (as specified above) have not been yet met, the device circuitry will not be in an initialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

⁴ If PLL does not lose lock.

⁵ When using fast interrupts and \overline{IRQA} , \overline{IRQB} , \overline{IRQC} , and \overline{IRQD} are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

⁶ WS = number of wait states (measured in clock cycles, number of T_C).

⁷ Use expression to compute maximum value.

⁸ This timing depends on several settings:

For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs: the stop delay counter completes count or PLL lock procedure completion.

PLC value for PLL disable is 0.

The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 150 MHz it is $4096/150 \text{ MHz} = 27.3 \mu\text{s}$). During the stabilization period, T_C , T_H , and T_L will not be constant, and their width may vary, so timing may vary as well.

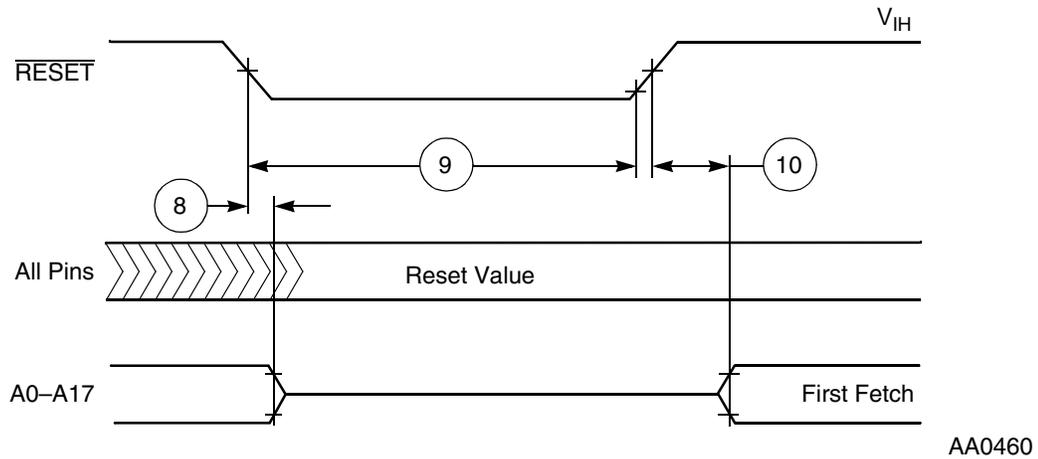
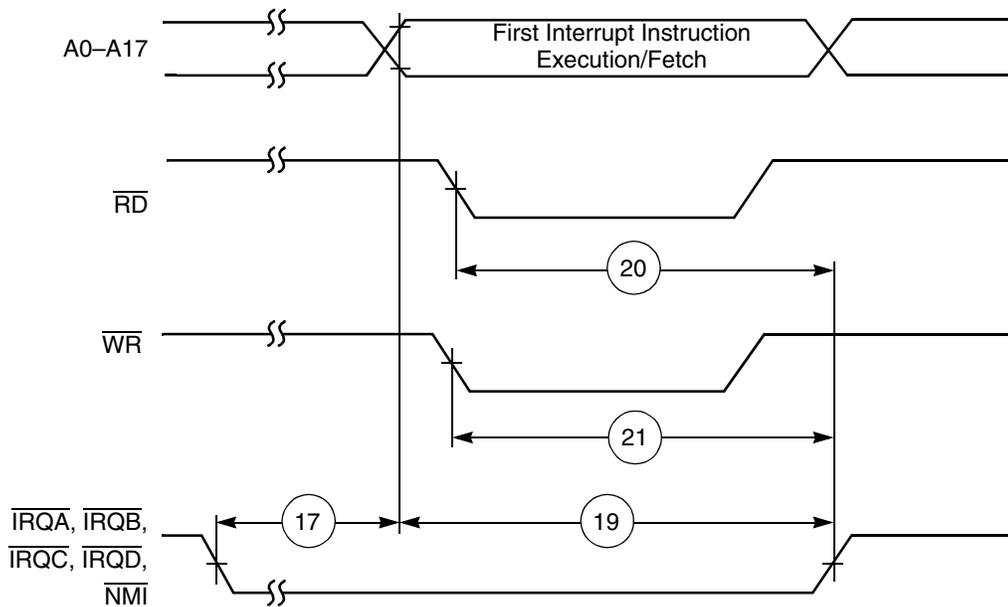
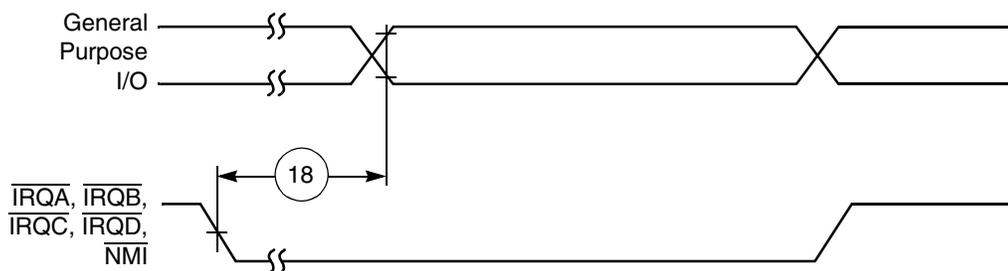


Figure 3-2 Reset Timing

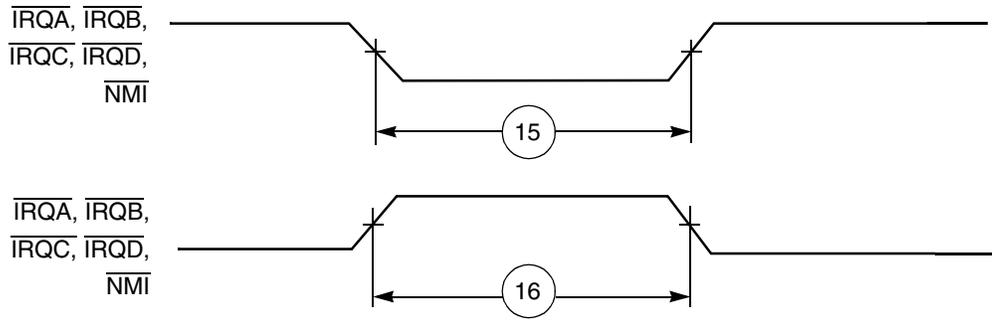


a) First Interrupt Instruction Execution



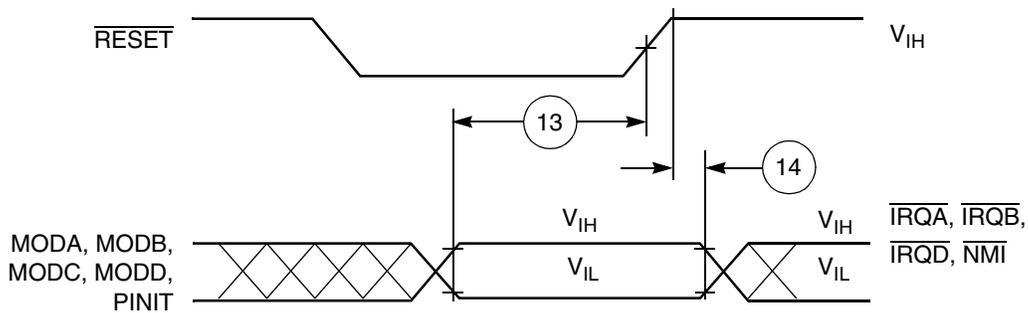
b) General Purpose I/O

Figure 3-3 External Fast Interrupt Timing



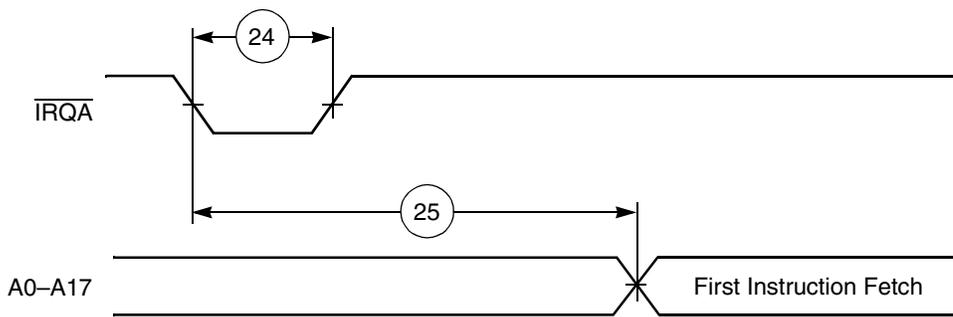
AA0463

Figure 3-4 External Interrupt Timing (Negative Edge-Triggered)



AA0465

Figure 3-5 Operating Mode Select Timing



AA0466

Figure 3-6 Recovery from Stop State Using \overline{IRQA} Interrupt Service

External Memory Expansion Port (Port A)

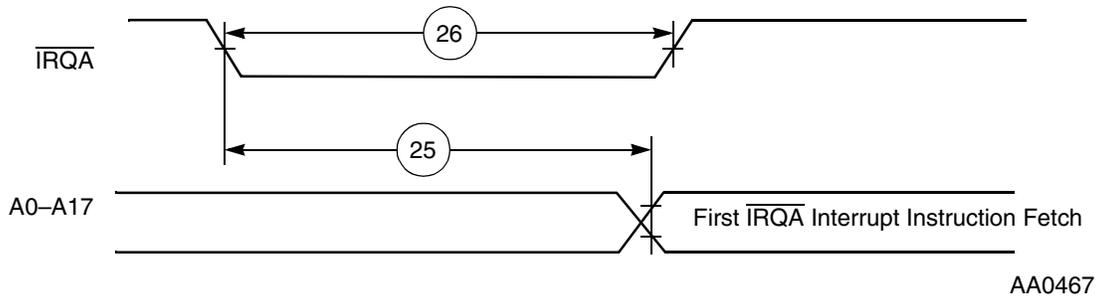


Figure 3-7 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

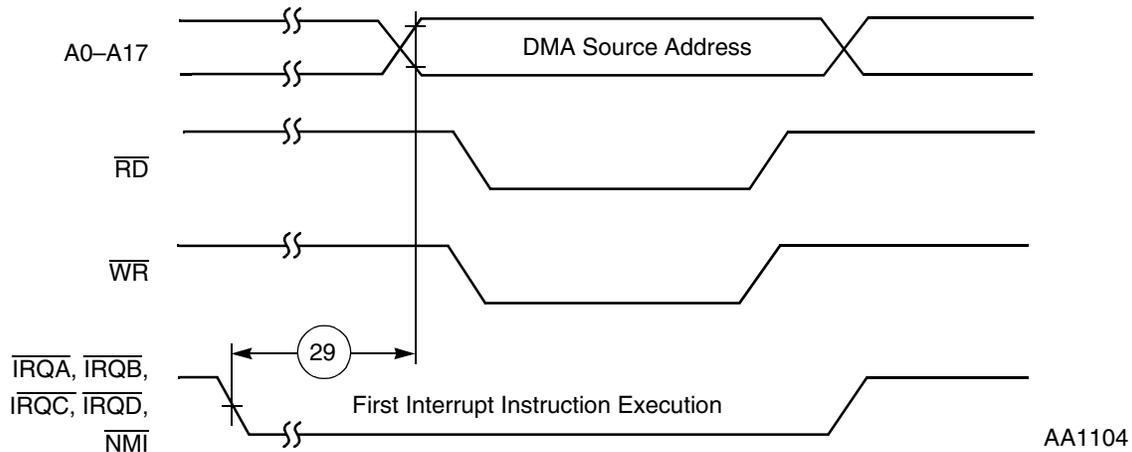


Figure 3-8 External Memory Access (DMA Source) Timing

3.10 External Memory Expansion Port (Port A)

3.10.1 SRAM Timing

Table 3-8 SRAM Read and Write Accesses

| No. | Characteristics | Symbol | Expression ¹ | 150 MHz | | Unit |
|-----|--|------------------|--|---------|-----|------|
| | | | | Min | Max | |
| 100 | Address valid and AA assertion pulse width | t_{RC}, t_{WC} | $(WS + 2) \times T_C - 4.0$ [$2 \leq WS \leq 7$] | 22.7 | — | ns |
| | | | $(WS + 3) \times T_C - 4.0$ [$WS \geq 8$] | 69.3 | — | ns |
| 101 | Address and AA valid to $\overline{\text{WR}}$ assertion | t_{AS} | $0.75 \times T_C - 2.0$ [$2 \leq WS \leq 3$] | 3.0 | — | ns |
| | | | $1.25 \times T_C - 2.0$ [$WS \geq 4$] | 6.3 | — | ns |
| 102 | $\overline{\text{WR}}$ assertion pulse width | t_{WP} | $WS \times T_C - 4.0$ [$2 \leq WS \leq 3$] | 9.3 | — | ns |
| | | | $(WS - 0.5) \times T_C - 4.0$ [$WS \geq 4$] | 19.3 | — | ns |
| 103 | $\overline{\text{WR}}$ deassertion to address not valid | t_{WR} | $1.25 \times T_C - 4.0$ [$2 \leq WS \leq 7$] | 4.3 | — | ns |
| | | | $2.25 \times T_C - 4.0$ [$WS \geq 8$] | 11.0 | — | ns |

Table 3-8 SRAM Read and Write Accesses (continued)

| No. | Characteristics | Symbol | Expression ¹ | 150 MHz | | Unit |
|-----|--|-------------------|--|---------|------|------|
| | | | | Min | Max | |
| 104 | Address and AA valid to input data valid | t_{AA}, t_{AC} | $(WS + 0.75) \times T_C - 5.0 [WS \geq 2]$ | — | 13.3 | ns |
| 105 | \overline{RD} assertion to input data valid | t_{OE} | $(WS + 0.25) \times T_C - 5.0 [WS \geq 2]$ | — | 10.0 | ns |
| 106 | \overline{RD} deassertion to data not valid (data hold time) | t_{OHZ} | | 0.0 | — | ns |
| 107 | Address valid to \overline{WR} deassertion ² | t_{AW} | $(WS + 0.75) \times T_C - 4.0 [WS \geq 2]$ | 14.3 | — | ns |
| 108 | Data valid to \overline{WR} deassertion (data setup time) | $t_{DS} (t_{DW})$ | $(WS - 0.25) \times T_C - 3.0 [WS \geq 2]$ | 8.7 | — | ns |
| 109 | Data hold time from \overline{WR} deassertion | t_{DH} | $1.25 \times T_C - 2.0 [2 \leq WS \leq 7]$ | 6.3 | — | ns |
| | | | $2.25 \times T_C - 2.0 [WS \geq 8]$ | 13.0 | — | ns |
| 110 | \overline{WR} assertion to data active | — | $0.25 \times T_C - 3.7 [2 \leq WS \leq 3]$ | -2.0 | — | ns |
| | | | $-0.25 \times T_C - 3.7 [WS \geq 4]$ | -5.4 | — | ns |
| 111 | \overline{WR} deassertion to data high impedance | — | $0.25 \times T_C + 0.2 [2 \leq WS \leq 3]$ | — | 1.9 | ns |
| | | | $1.25 \times T_C + 0.2 [4 \leq WS \leq 7]$ | — | 8.5 | ns |
| | | | $2.25 \times T_C + 0.2 [WS \geq 8]$ | — | 15.2 | ns |
| 112 | Previous \overline{RD} deassertion to data active (write) | — | $1.25 \times T_C - 4.0 [2 \leq WS \leq 3]$ | 4.3 | — | ns |
| | | | $2.25 \times T_C - 4.0 [4 \leq WS \leq 7]$ | 11.0 | — | ns |
| | | | $3.25 \times T_C - 4.0 [WS \geq 8]$ | 17.7 | — | ns |
| 113 | \overline{RD} deassertion time | | $1.75 \times T_C - 4.0 [2 \leq WS \leq 7]$ | 7.7 | — | ns |
| | | | $2.75 \times T_C - 4.0 [WS \geq 8]$ | 14.3 | — | ns |
| 114 | \overline{WR} deassertion time | | $2.0 \times T_C - 4.0 [2 \leq WS \leq 3]$ | 9.3 | — | ns |
| | | | $2.5 \times T_C - 4.0 [4 \leq WS \leq 7]$ | 12.7 | — | ns |
| | | | $3.5 \times T_C - 4.0 [WS \geq 8]$ | 19.3 | — | ns |
| 115 | Address valid to \overline{RD} assertion | | $0.5 \times T_C - 2.0$ | 1.3 | — | ns |
| 116 | \overline{RD} assertion pulse width | | $(WS + 0.25) \times T_C - 4.0$ | 11.0 | — | ns |
| 117 | \overline{RD} deassertion to address not valid | | $1.25 \times T_C - 2.0 [2 \leq WS \leq 7]$ | 6.3 | — | ns |
| | | | $2.25 \times T_C - 2.0 [WS \geq 8]$ | 13.0 | — | ns |
| 118 | \overline{TA} setup before \overline{RD} or \overline{WR} deassertion ³ | | $0.25 \times T_C + 2.0$ | 3.7 | — | ns |
| 119 | \overline{TA} hold after \overline{RD} or \overline{WR} deassertion | | | 0.0 | — | ns |

¹ WS is the number of wait states specified in the BCR. The value is given for the minimum for a given category. (For example, for a category of $[2 \leq WS \leq 7]$ timing is specified for 2 wait states.) Two wait states is the minimum otherwise.

² Timings 100, 107 are guaranteed by design, not tested.

³ In the case of \overline{TA} negation: timing 118 is relative to the deassertion edge of \overline{RD} or \overline{WR} were \overline{TA} to remain active.

External Memory Expansion Port (Port A)

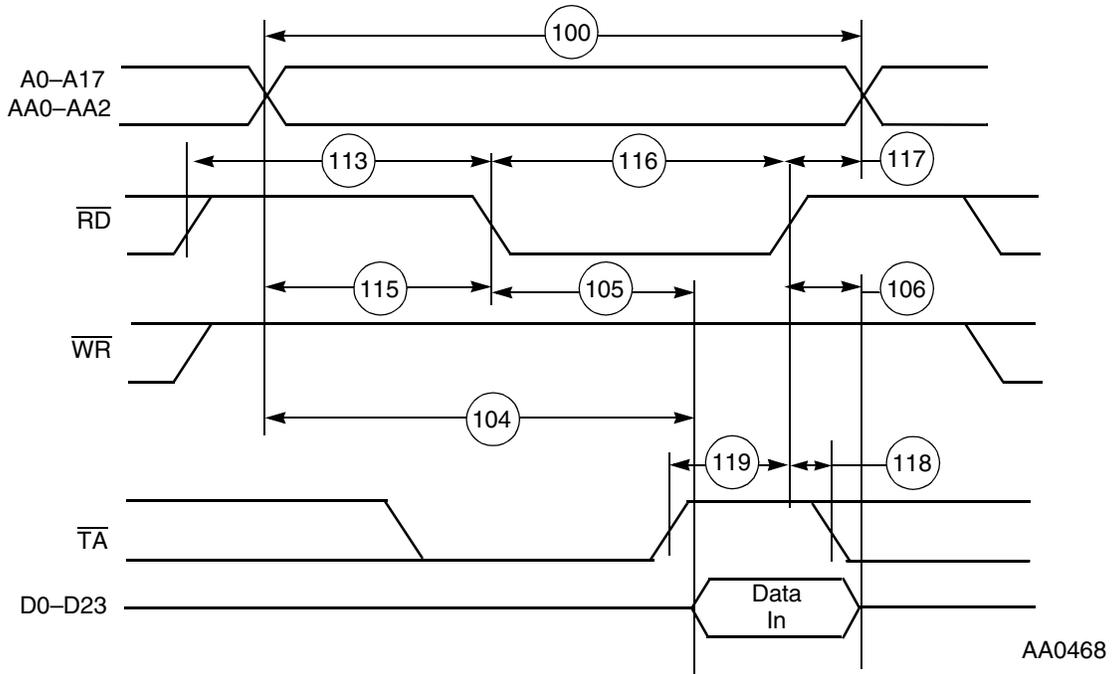


Figure 3-9 SRAM Read Access

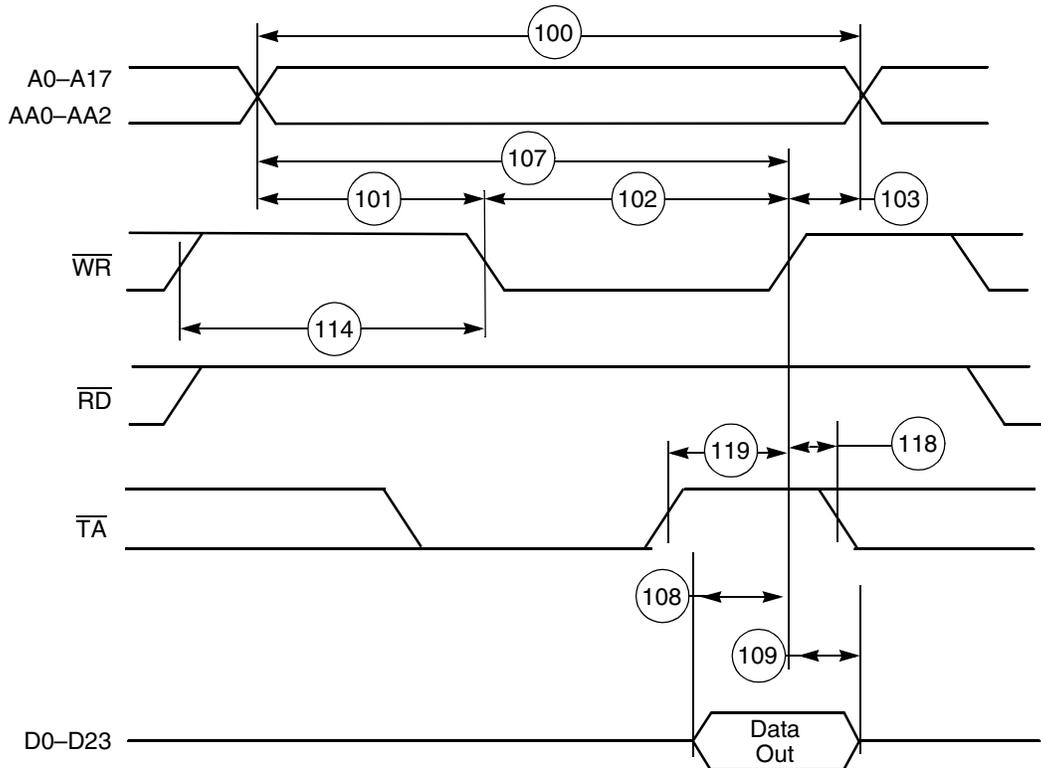


Figure 3-10 SRAM Write Access

3.10.2 DRAM Timing

The selection guides provided in [Figure 3-11](#) and [Figure 3-14](#) should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

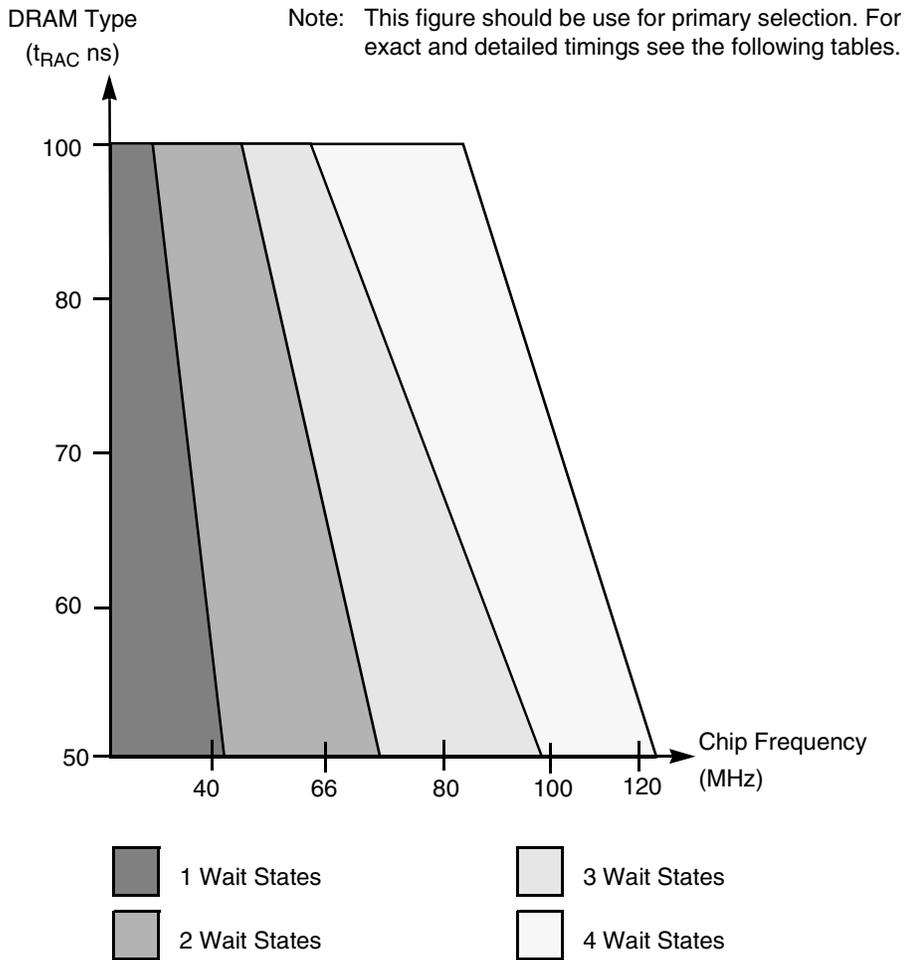


Figure 3-11 DRAM Page Mode Wait States Selection Guide

Table 3-9 DRAM Page Mode Timings, Three Wait States^{1, 2, 3}

| No. | Characteristics | Symbol | Expression ⁴ | 100 MHz | | Unit |
|-----|---|------------|-------------------------|---------|------|------|
| | | | | Min | Max | |
| 131 | Page mode cycle time for two consecutive accesses of the same direction | t_{PC} | $2 \times T_C$ | 20.0 | — | ns |
| | Page mode cycle time for mixed (read and write) accesses | | $1.25 \times T_C$ | 12.5 | — | |
| 132 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $2 \times T_C - 7.0$ | — | 13.0 | ns |
| 133 | Column address valid to data valid (read) | t_{AA} | $3 \times T_C - 7.0$ | — | 23.0 | ns |
| 134 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | ns |
| 135 | Last \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 136 | Previous \overline{CAS} deassertion to \overline{RAS} deassertion | t_{RHCP} | $4.5 \times T_C - 4.0$ | 41.0 | — | ns |
| 137 | \overline{CAS} assertion pulse width | t_{CAS} | $2 \times T_C - 4.0$ | 16.0 | — | ns |
| 138 | Last \overline{CAS} deassertion to \overline{RAS} assertion ⁵ <ul style="list-style-type: none"> • BRW[1:0] = 00, 01— not applicable • BRW[1:0] = 10 • BRW[1:0] = 11 | t_{CRP} | | | | ns |
| | | | $4.75 \times T_C - 6.0$ | 41.5 | — | |
| | | | $6.75 \times T_C - 6.0$ | 61.5 | — | |
| 139 | \overline{CAS} deassertion pulse width | t_{CP} | $1.5 \times T_C - 4.0$ | 11.0 | — | ns |
| 140 | Column address valid to \overline{CAS} assertion | t_{ASC} | $T_C - 4.0$ | 6.0 | — | ns |
| 141 | \overline{CAS} assertion to column address not valid | t_{CAH} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 142 | Last column address valid to \overline{RAS} deassertion | t_{RAL} | $4 \times T_C - 4.0$ | 36.0 | — | ns |
| 143 | \overline{WR} deassertion to \overline{CAS} assertion | t_{RCS} | $1.25 \times T_C - 4.0$ | 8.5 | — | ns |
| 144 | \overline{CAS} deassertion to \overline{WR} assertion | t_{RCH} | $0.75 \times T_C - 4.0$ | 3.5 | — | ns |
| 145 | \overline{CAS} assertion to \overline{WR} deassertion | t_{WCH} | $2.25 \times T_C - 4.2$ | 18.3 | — | ns |
| 146 | \overline{WR} assertion pulse width | t_{WP} | $3.5 \times T_C - 4.5$ | 30.5 | — | ns |
| 147 | Last \overline{WR} assertion to \overline{RAS} deassertion | t_{RWL} | $3.75 \times T_C - 4.3$ | 33.2 | — | ns |
| 148 | \overline{WR} assertion to \overline{CAS} deassertion | t_{CWL} | $3.25 \times T_C - 4.3$ | 28.2 | — | ns |
| 149 | Data valid to \overline{CAS} assertion (write) | t_{DS} | $0.5 \times T_C - 4.0$ | 1.0 | — | ns |
| 150 | \overline{CAS} assertion to data not valid (write) | t_{DH} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 151 | \overline{WR} assertion to \overline{CAS} assertion | t_{WCS} | $1.25 \times T_C - 4.3$ | 8.2 | — | ns |
| 152 | Last \overline{RD} assertion to \overline{RAS} deassertion | t_{ROH} | $3.5 \times T_C - 4.0$ | 31.0 | — | ns |

Table 3-9 DRAM Page Mode Timings, Three Wait States^{1, 2, 3} (continued)

| No. | Characteristics | Symbol | Expression ⁴ | 100 MHz | | Unit |
|-----|--|----------|-------------------------|---------|------|------|
| | | | | Min | Max | |
| 153 | \overline{RD} assertion to data valid | t_{GA} | $2.5 \times T_C - 7.0$ | — | 18.0 | ns |
| 154 | \overline{RD} deassertion to data not valid ⁶ | t_{GZ} | | 0.0 | — | ns |
| 155 | \overline{WR} assertion to data active | | $0.75 \times T_C - 0.3$ | 7.2 | — | ns |
| 156 | \overline{WR} deassertion to data high impedance | | $0.25 \times T_C$ | — | 2.5 | ns |

¹ The number of wait states for Page mode access is specified in the DCR.

² The refresh period is specified in the DCR.

³ The asynchronous delays specified in the expressions are valid for DSP56367.

⁴ All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).

⁵ BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page-access.

⁶ \overline{RD} deassertion will always occur after \overline{CAS} deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ} .

Table 3-10 DRAM Page Mode Timings, Four Wait States^{1, 2, 3}

| No. | Characteristics | Symbol | Expression ⁴ | 100 MHz | | Unit |
|-----|--|------------|-------------------------|---------|------|------|
| | | | | Min | Max | |
| 131 | Page mode cycle time for two consecutive accesses of the same direction | t_{PC} | $5 \times T_C$ | 50.0 | — | ns |
| | Page mode cycle time for mixed (read and write) accesses | | $4.5 \times T_C$ | 45.0 | — | |
| 132 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $2.75 \times T_C - 5.7$ | — | 21.8 | ns |
| 133 | Column address valid to data valid (read) | t_{AA} | $3.75 \times T_C - 5.7$ | — | 31.8 | ns |
| 134 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | ns |
| 135 | Last \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $3.5 \times T_C - 4.0$ | 31.0 | — | ns |
| 136 | Previous \overline{CAS} deassertion to \overline{RAS} deassertion | t_{RHCP} | $6 \times T_C - 4.0$ | 56.0 | — | ns |
| 137 | \overline{CAS} assertion pulse width | t_{CAS} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 138 | Last \overline{CAS} deassertion to \overline{RAS} assertion ⁵ • BRW[1-0] = 00, 01—Not applicable • BRW[1-0] = 10 • BRW[1-0] = 11 | t_{CRP} | — | — | — | — |
| | | | $5.25 \times T_C - 6.0$ | 46.5 | — | ns |
| | | | $7.25 \times T_C - 6.0$ | 66.5 | — | ns |
| 139 | \overline{CAS} deassertion pulse width | t_{CP} | $2 \times T_C - 4.0$ | 16.0 | — | ns |
| 140 | Column address valid to \overline{CAS} assertion | t_{ASC} | $T_C - 4.0$ | 6.0 | — | ns |

Table 3-10 DRAM Page Mode Timings, Four Wait States^{1, 2, 3} (continued)

| No. | Characteristics | Symbol | Expression ⁴ | 100 MHz | | Unit |
|-----|--|------------------|----------------------------------|---------|------|------|
| | | | | Min | Max | |
| 141 | $\overline{\text{CAS}}$ assertion to column address not valid | t_{CAH} | $3.5 \times T_{\text{C}} - 4.0$ | 31.0 | — | ns |
| 142 | Last column address valid to $\overline{\text{RAS}}$ deassertion | t_{RAL} | $5 \times T_{\text{C}} - 4.0$ | 46.0 | — | ns |
| 143 | $\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion | t_{RCS} | $1.25 \times T_{\text{C}} - 4.0$ | 8.5 | — | ns |
| 144 | $\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion | t_{RCH} | $1.25 \times T_{\text{C}} - 3.7$ | 8.8 | — | ns |
| 145 | $\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCH} | $3.25 \times T_{\text{C}} - 4.2$ | 28.3 | — | ns |
| 146 | $\overline{\text{WR}}$ assertion pulse width | t_{WP} | $4.5 \times T_{\text{C}} - 4.5$ | 40.5 | — | ns |
| 147 | Last $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{RWL} | $4.75 \times T_{\text{C}} - 4.3$ | 43.2 | — | ns |
| 148 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion | t_{CWL} | $3.75 \times T_{\text{C}} - 4.3$ | 33.2 | — | ns |
| 149 | Data valid to $\overline{\text{CAS}}$ assertion (write) | t_{DS} | $0.5 \times T_{\text{C}} - 4.5$ | 0.5 | — | ns |
| 150 | $\overline{\text{CAS}}$ assertion to data not valid (write) | t_{DH} | $3.5 \times T_{\text{C}} - 4.0$ | 31.0 | — | ns |
| 151 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion | t_{WCS} | $1.25 \times T_{\text{C}} - 4.3$ | 8.2 | — | ns |
| 152 | Last $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{ROH} | $4.5 \times T_{\text{C}} - 4.0$ | 41.0 | — | ns |
| 153 | $\overline{\text{RD}}$ assertion to data valid | t_{GA} | $3.25 \times T_{\text{C}} - 5.7$ | — | 26.8 | ns |
| 154 | $\overline{\text{RD}}$ deassertion to data not valid ⁶ | t_{GZ} | | 0.0 | — | ns |
| 155 | $\overline{\text{WR}}$ assertion to data active | | $0.75 \times T_{\text{C}} - 1.5$ | 6.0 | — | ns |
| 156 | $\overline{\text{WR}}$ deassertion to data high impedance | | $0.25 \times T_{\text{C}}$ | — | 2.5 | ns |

¹ The number of wait states for Page mode access is specified in the DCR.

² The refresh period is specified in the DCR.

³ The asynchronous delays specified in the expressions are valid for DSP56367.

⁴ All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $3 \times T_{\text{C}}$ for read-after-read or write-after-write sequences). An expressions is used to calculate the maximum or minimum value listed, as appropriate.

⁵ BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

⁶ $\overline{\text{RD}}$ deassertion always occurs after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ} .

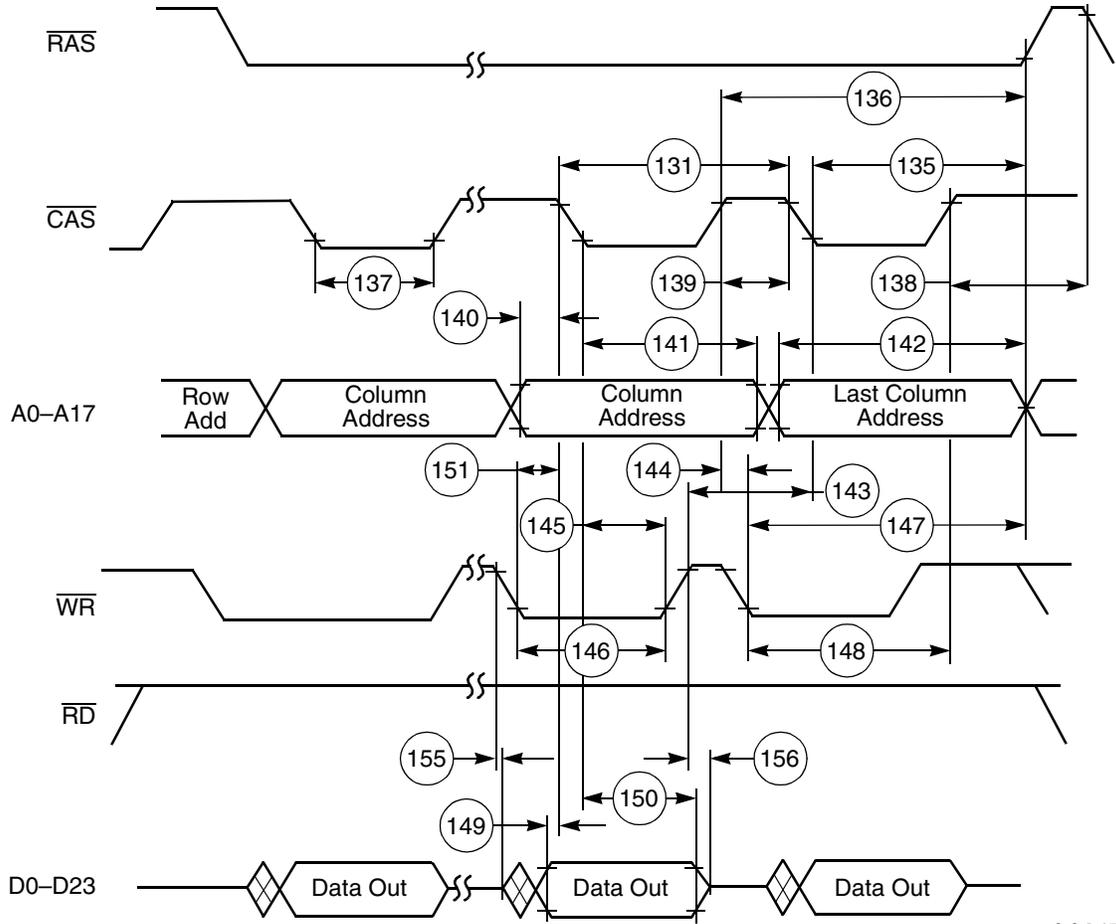


Figure 3-12 DRAM Page Mode Write Accesses

External Memory Expansion Port (Port A)

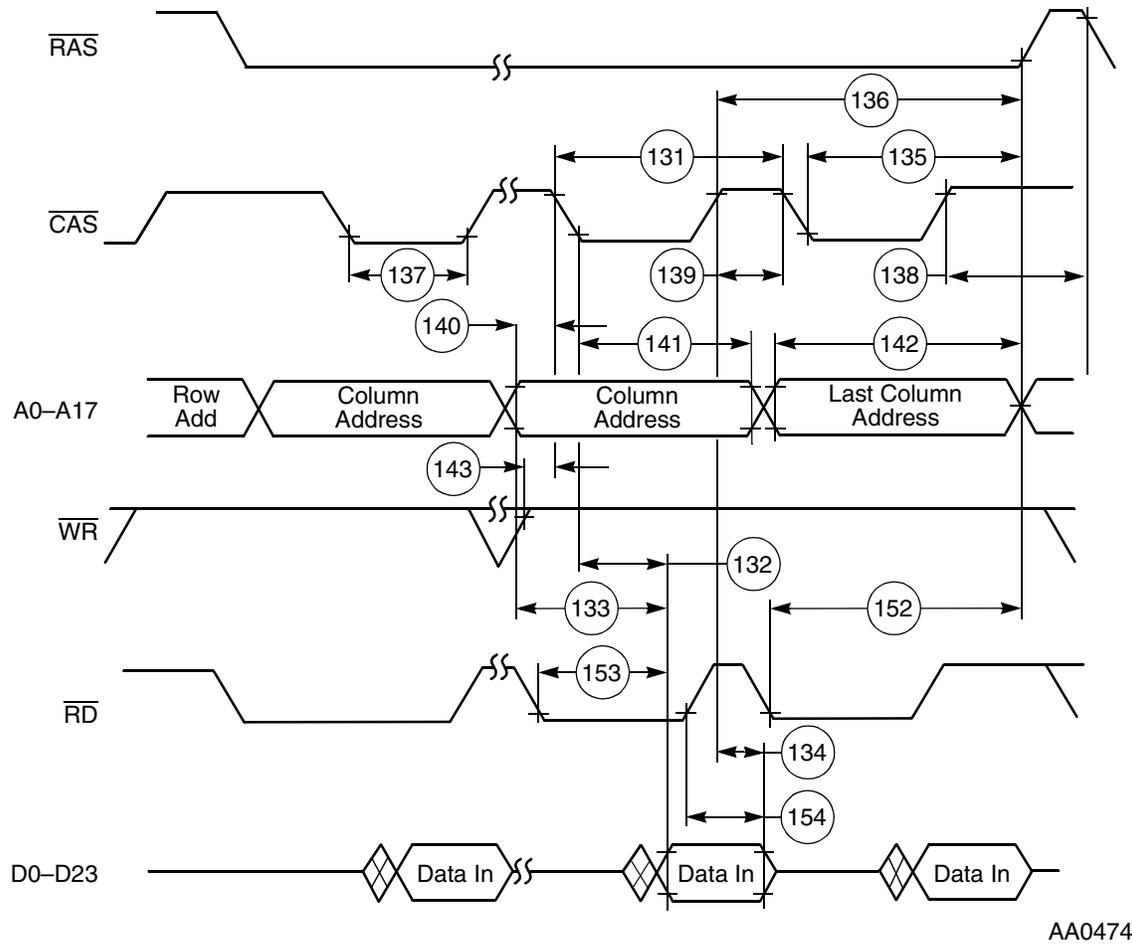
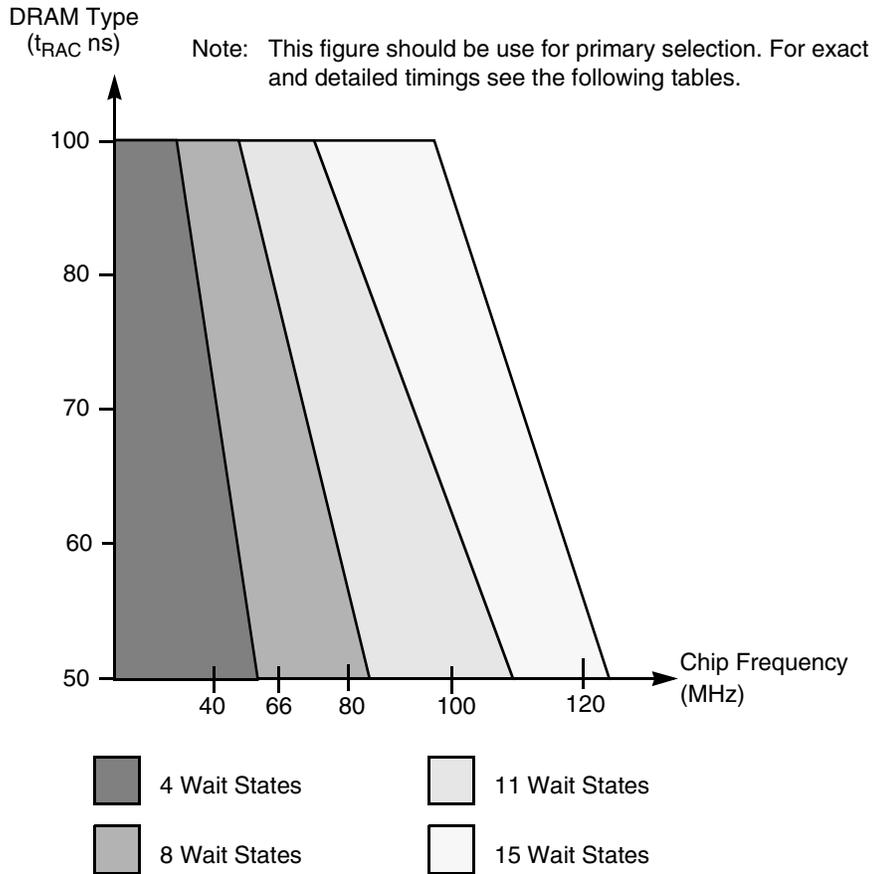


Figure 3-13 DRAM Page Mode Read Accesses



AA0475

Figure 3-14 DRAM Out-of-Page Wait States Selection Guide

Table 3-11 DRAM Out-of-Page and Refresh Timings, Four Wait States^{1, 2}

| No. | Characteristics | Symbol | Expression | 20 MHz ³ | | 30 MHz ³ | | Unit |
|-----|---|-----------|-------------------------|---------------------|-------|---------------------|------|------|
| | | | | Min | Max | Min | Max | |
| 157 | Random read or write cycle time | t_{RC} | $5 \times T_C$ | 250.0 | — | 166.7 | — | ns |
| 158 | \overline{RAS} assertion to data valid (read) | t_{RAC} | $2.75 \times T_C - 7.5$ | — | 130.0 | — | 84.2 | ns |
| 159 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $1.25 \times T_C - 7.5$ | — | 55.0 | — | 34.2 | ns |
| 160 | Column address valid to data valid (read) | t_{AA} | $1.5 \times T_C - 7.5$ | — | 67.5 | — | 42.5 | ns |
| 161 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | 0.0 | — | ns |
| 162 | \overline{RAS} deassertion to \overline{RAS} assertion | t_{RP} | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 163 | \overline{RAS} assertion pulse width | t_{RAS} | $3.25 \times T_C - 4.0$ | 158.5 | — | 104.3 | — | ns |
| 164 | \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |

Table 3-11 DRAM Out-of-Page and Refresh Timings, Four Wait States^{1, 2} (continued)

| No. | Characteristics | Symbol | Expression | 20 MHz ³ | | 30 MHz ³ | | Unit |
|-----|--|------------------|-------------------------|---------------------|------|---------------------|------|------|
| | | | | Min | Max | Min | Max | |
| 165 | $\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion | t_{CSH} | $2.75 \times T_C - 4.0$ | 133.5 | — | 87.7 | — | ns |
| 166 | $\overline{\text{CAS}}$ assertion pulse width | t_{CAS} | $1.25 \times T_C - 4.0$ | 58.5 | — | 37.7 | — | ns |
| 167 | $\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion | t_{RCD} | $1.5 \times T_C \pm 2$ | 73.0 | 77.0 | 48.0 | 52.0 | ns |
| 168 | $\overline{\text{RAS}}$ assertion to column address valid | t_{RAD} | $1.25 \times T_C \pm 2$ | 60.5 | 64.5 | 39.7 | 43.7 | ns |
| 169 | $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion | t_{CRP} | $2.25 \times T_C - 4.0$ | 108.5 | — | 71.0 | — | ns |
| 170 | $\overline{\text{CAS}}$ deassertion pulse width | t_{CP} | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 171 | Row address valid to $\overline{\text{RAS}}$ assertion | t_{ASR} | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 172 | $\overline{\text{RAS}}$ assertion to row address not valid | t_{RAH} | $1.25 \times T_C - 4.0$ | 58.5 | — | 37.7 | — | ns |
| 173 | Column address valid to $\overline{\text{CAS}}$ assertion | t_{ASC} | $0.25 \times T_C - 4.0$ | 8.5 | — | 4.3 | — | ns |
| 174 | $\overline{\text{CAS}}$ assertion to column address not valid | t_{CAH} | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 175 | $\overline{\text{RAS}}$ assertion to column address not valid | t_{AR} | $3.25 \times T_C - 4.0$ | 158.5 | — | 104.3 | — | ns |
| 176 | Column address valid to $\overline{\text{RAS}}$ deassertion | t_{RAL} | $2 \times T_C - 4.0$ | 96.0 | — | 62.7 | — | ns |
| 177 | $\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion | t_{RCS} | $1.5 \times T_C - 3.8$ | 71.2 | — | 46.2 | — | ns |
| 178 | $\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion | t_{RCH} | $0.75 \times T_C - 3.7$ | 33.8 | — | 21.3 | — | ns |
| 179 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$ assertion | t_{RRH} | $0.25 \times T_C - 3.7$ | 8.8 | — | 4.6 | — | ns |
| 180 | $\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCH} | $1.5 \times T_C - 4.2$ | 70.8 | — | 45.8 | — | ns |
| 181 | $\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCR} | $3 \times T_C - 4.2$ | 145.8 | — | 95.8 | — | ns |
| 182 | $\overline{\text{WR}}$ assertion pulse width | t_{WP} | $4.5 \times T_C - 4.5$ | 220.5 | — | 145.5 | — | ns |
| 183 | $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{RWL} | $4.75 \times T_C - 4.3$ | 233.2 | — | 154.0 | — | ns |
| 184 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion | t_{CWL} | $4.25 \times T_C - 4.3$ | 208.2 | — | 137.4 | — | ns |
| 185 | Data valid to $\overline{\text{CAS}}$ assertion (write) | t_{DS} | $2.25 \times T_C - 4.0$ | 108.5 | — | 71.0 | — | ns |
| 186 | $\overline{\text{CAS}}$ assertion to data not valid (write) | t_{DH} | $1.75 \times T_C - 4.0$ | 83.5 | — | 54.3 | — | ns |
| 187 | $\overline{\text{RAS}}$ assertion to data not valid (write) | t_{DHR} | $3.25 \times T_C - 4.0$ | 158.5 | — | 104.3 | — | ns |
| 188 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion | t_{WCS} | $3 \times T_C - 4.3$ | 145.7 | — | 95.7 | — | ns |
| 189 | $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh) | t_{CSR} | $0.5 \times T_C - 4.0$ | 21.0 | — | 12.7 | — | ns |
| 190 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh) | t_{RPC} | $1.25 \times T_C - 4.0$ | 58.5 | — | 37.7 | — | ns |

Table 3-11 DRAM Out-of-Page and Refresh Timings, Four Wait States^{1, 2} (continued)

| No. | Characteristics | Symbol | Expression | 20 MHz ³ | | 30 MHz ³ | | Unit |
|-----|--|-----------|-------------------------|---------------------|-------|---------------------|-------|------|
| | | | | Min | Max | Min | Max | |
| 191 | \overline{RD} assertion to \overline{RAS} deassertion | t_{ROH} | $4.5 \times T_C - 4.0$ | 221.0 | — | 146.0 | — | ns |
| 192 | \overline{RD} assertion to data valid | t_{GA} | $4 \times T_C - 7.5$ | — | 192.5 | — | 125.8 | ns |
| 193 | \overline{RD} deassertion to data not valid ⁴ | t_{GZ} | | 0.0 | — | 0.0 | — | ns |
| 194 | \overline{WR} assertion to data active | | $0.75 \times T_C - 0.3$ | 37.2 | — | 24.7 | — | ns |
| 195 | \overline{WR} deassertion to data high impedance | | $0.25 \times T_C$ | — | 12.5 | — | 8.3 | ns |

¹ The number of wait states for out of page access is specified in the DCR.

² The refresh period is specified in the DCR.

³ Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (Figure 3-14).

⁴ \overline{RD} deassertion will always occur after \overline{CAS} deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ} .

Table 3-12 DRAM Out-of-Page and Refresh Timings, Eleven Wait States^{1, 2, 3}

| No. | Characteristics | Symbol | Expression | 100 MHz | | Unit |
|-----|---|-----------|---------------------------|---------|------|------|
| | | | | Min | Max | |
| 157 | Random read or write cycle time | t_{RC} | $12 \times T_C$ | 120.0 | — | ns |
| 158 | \overline{RAS} assertion to data valid (read) | t_{RAC} | $6.25 \times T_C - 7.0$ | — | 55.5 | ns |
| 159 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $3.75 \times T_C - 7.0$ | — | 30.5 | ns |
| 160 | Column address valid to data valid (read) | t_{AA} | $4.5 \times T_C - 7.0$ | — | 38.0 | ns |
| 161 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | ns |
| 162 | \overline{RAS} deassertion to \overline{RAS} assertion | t_{RP} | $4.25 \times T_C - 4.0$ | 38.5 | — | ns |
| 163 | \overline{RAS} assertion pulse width | t_{RAS} | $7.75 \times T_C - 4.0$ | 73.5 | — | ns |
| 164 | \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $5.25 \times T_C - 4.0$ | 48.5 | — | ns |
| 165 | \overline{RAS} assertion to \overline{CAS} deassertion | t_{CSH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 166 | \overline{CAS} assertion pulse width | t_{CAS} | $3.75 \times T_C - 4.0$ | 33.5 | — | ns |
| 167 | \overline{RAS} assertion to \overline{CAS} assertion | t_{RCD} | $2.5 \times T_C \pm 4.0$ | 21.0 | 29.0 | ns |
| 168 | \overline{RAS} assertion to column address valid | t_{RAD} | $1.75 \times T_C \pm 4.0$ | 13.5 | 21.5 | ns |
| 169 | \overline{CAS} deassertion to \overline{RAS} assertion | t_{CRP} | $5.75 \times T_C - 4.0$ | 53.5 | — | ns |
| 170 | \overline{CAS} deassertion pulse width | t_{CP} | $4.25 \times T_C - 4.0$ | 38.5 | — | ns |
| 171 | Row address valid to \overline{RAS} assertion | t_{ASR} | $4.25 \times T_C - 4.0$ | 38.5 | — | ns |
| 172 | \overline{RAS} assertion to row address not valid | t_{RAH} | $1.75 \times T_C - 4.0$ | 13.5 | — | ns |

Table 3-12 DRAM Out-of-Page and Refresh Timings, Eleven Wait States^{1, 2, 3} (continued)

| No. | Characteristics | Symbol | Expression | 100 MHz | | Unit |
|-----|--|------------------|-----------------------------------|---------|------|------|
| | | | | Min | Max | |
| 173 | Column address valid to $\overline{\text{CAS}}$ assertion | t_{ASC} | $0.75 \times T_{\text{C}} - 4.0$ | 3.5 | — | ns |
| 174 | $\overline{\text{CAS}}$ assertion to column address not valid | t_{CAH} | $5.25 \times T_{\text{C}} - 4.0$ | 48.5 | — | ns |
| 175 | $\overline{\text{RAS}}$ assertion to column address not valid | t_{AR} | $7.75 \times T_{\text{C}} - 4.0$ | 73.5 | — | ns |
| 176 | Column address valid to $\overline{\text{RAS}}$ deassertion | t_{RAL} | $6 \times T_{\text{C}} - 4.0$ | 56.0 | — | ns |
| 177 | $\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion | t_{RCS} | $3.0 \times T_{\text{C}} - 4.0$ | 26.0 | — | ns |
| 178 | $\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}^4$ assertion | t_{RCH} | $1.75 \times T_{\text{C}} - 4.0$ | 13.5 | — | ns |
| 179 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}^4$ assertion | t_{RRH} | $0.25 \times T_{\text{C}} - 2.0$ | 0.5 | — | ns |
| 180 | $\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCH} | $5 \times T_{\text{C}} - 4.2$ | 45.8 | — | ns |
| 181 | $\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCR} | $7.5 \times T_{\text{C}} - 4.2$ | 70.8 | — | ns |
| 182 | $\overline{\text{WR}}$ assertion pulse width | t_{WP} | $11.5 \times T_{\text{C}} - 4.5$ | 110.5 | — | ns |
| 183 | $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{RWL} | $11.75 \times T_{\text{C}} - 4.3$ | 113.2 | — | ns |
| 184 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion | t_{CWL} | $10.25 \times T_{\text{C}} - 4.3$ | 103.2 | — | ns |
| 185 | Data valid to $\overline{\text{CAS}}$ assertion (write) | t_{DS} | $5.75 \times T_{\text{C}} - 4.0$ | 53.5 | — | ns |
| 186 | $\overline{\text{CAS}}$ assertion to data not valid (write) | t_{DH} | $5.25 \times T_{\text{C}} - 4.0$ | 48.5 | — | ns |
| 187 | $\overline{\text{RAS}}$ assertion to data not valid (write) | t_{DHR} | $7.75 \times T_{\text{C}} - 4.0$ | 73.5 | — | ns |
| 188 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion | t_{WCS} | $6.5 \times T_{\text{C}} - 4.3$ | 60.7 | — | ns |
| 189 | $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh) | t_{CSR} | $1.5 \times T_{\text{C}} - 4.0$ | 11.0 | — | ns |
| 190 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh) | t_{RPC} | $2.75 \times T_{\text{C}} - 4.0$ | 23.5 | — | ns |
| 191 | $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{ROH} | $11.5 \times T_{\text{C}} - 4.0$ | 111.0 | — | ns |
| 192 | $\overline{\text{RD}}$ assertion to data valid | t_{GA} | $10 \times T_{\text{C}} - 7.0$ | — | 93.0 | ns |
| 193 | $\overline{\text{RD}}$ deassertion to data not valid ⁵ | t_{GZ} | | 0.0 | — | ns |
| 194 | $\overline{\text{WR}}$ assertion to data active | | $0.75 \times T_{\text{C}} - 0.3$ | 7.2 | — | ns |
| 195 | $\overline{\text{WR}}$ deassertion to data high impedance | | $0.25 \times T_{\text{C}}$ | — | 2.5 | ns |

¹ The number of wait states for out-of-page access is specified in the DCR.

² The refresh period is specified in the DCR.

³ The asynchronous delays specified in the expressions are valid for DSP56367.

⁴ Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

⁵ $\overline{\text{RD}}$ deassertion will always occur after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ} .

Table 3-13 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States^{1, 2}

| No. | Characteristics | Symbol | Expression ³ | 100 MHz | | Unit |
|-----|---|-----------|-------------------------|---------|------|------|
| | | | | Min | Max | |
| 157 | Random read or write cycle time | t_{RC} | $16 \times T_C$ | 160.0 | — | ns |
| 158 | \overline{RAS} assertion to data valid (read) | t_{RAC} | $8.25 \times T_C - 5.7$ | — | 76.8 | ns |
| 159 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $4.75 \times T_C - 5.7$ | — | 41.8 | ns |
| 160 | Column address valid to data valid (read) | t_{AA} | $5.5 \times T_C - 5.7$ | — | 49.3 | ns |
| 161 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | 0.0 | 0.0 | — | ns |
| 162 | \overline{RAS} deassertion to \overline{RAS} assertion | t_{RP} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 163 | \overline{RAS} assertion pulse width | t_{RAS} | $9.75 \times T_C - 4.0$ | 93.5 | — | ns |
| 164 | \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 165 | \overline{RAS} assertion to \overline{CAS} deassertion | t_{CSH} | $8.25 \times T_C - 4.0$ | 78.5 | — | ns |
| 166 | \overline{CAS} assertion pulse width | t_{CAS} | $4.75 \times T_C - 4.0$ | 43.5 | — | ns |
| 167 | \overline{RAS} assertion to \overline{CAS} assertion | t_{RCD} | $3.5 \times T_C \pm 2$ | 33.0 | 37.0 | ns |
| 168 | \overline{RAS} assertion to column address valid | t_{RAD} | $2.75 \times T_C \pm 2$ | 25.5 | 29.5 | ns |
| 169 | \overline{CAS} deassertion to \overline{RAS} assertion | t_{CRP} | $7.75 \times T_C - 4.0$ | 73.5 | — | ns |
| 170 | \overline{CAS} deassertion pulse width | t_{CP} | $6.25 \times T_C - 6.0$ | 56.5 | — | ns |
| 171 | Row address valid to \overline{RAS} assertion | t_{ASR} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 172 | \overline{RAS} assertion to row address not valid | t_{RAH} | $2.75 \times T_C - 4.0$ | 23.5 | — | ns |
| 173 | Column address valid to \overline{CAS} assertion | t_{ASC} | $0.75 \times T_C - 4.0$ | 3.5 | — | ns |
| 174 | \overline{CAS} assertion to column address not valid | t_{CAH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 175 | \overline{RAS} assertion to column address not valid | t_{AR} | $9.75 \times T_C - 4.0$ | 93.5 | — | ns |
| 176 | Column address valid to \overline{RAS} deassertion | t_{RAL} | $7 \times T_C - 4.0$ | 66.0 | — | ns |
| 177 | \overline{WR} deassertion to \overline{CAS} assertion | t_{RCS} | $5 \times T_C - 3.8$ | 46.2 | — | ns |
| 178 | \overline{CAS} deassertion to \overline{WR}^4 assertion | t_{RCH} | $1.75 \times T_C - 3.7$ | 13.8 | — | ns |
| 179 | \overline{RAS} deassertion to \overline{WR}^4 assertion | t_{RRH} | $0.25 \times T_C - 2.0$ | 0.5 | — | ns |
| 180 | \overline{CAS} assertion to \overline{WR} deassertion | t_{WCH} | $6 \times T_C - 4.2$ | 55.8 | — | ns |
| 181 | \overline{RAS} assertion to \overline{WR} deassertion | t_{WCR} | $9.5 \times T_C - 4.2$ | 90.8 | — | ns |
| 182 | \overline{WR} assertion pulse width | t_{WP} | $15.5 \times T_C - 4.5$ | 150.5 | — | ns |

Table 3-13 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States^{1, 2} (continued)

| No. | Characteristics | Symbol | Expression ³ | 100 MHz | | Unit |
|-----|--|-----------|--------------------------|---------|-------|------|
| | | | | Min | Max | |
| 183 | \overline{WR} assertion to \overline{RAS} deassertion | t_{RWL} | $15.75 \times T_C - 4.3$ | 153.2 | — | ns |
| 184 | \overline{WR} assertion to \overline{CAS} deassertion | t_{CWL} | $14.25 \times T_C - 4.3$ | 138.2 | — | ns |
| 185 | Data valid to \overline{CAS} assertion (write) | t_{DS} | $8.75 \times T_C - 4.0$ | 83.5 | — | ns |
| 186 | \overline{CAS} assertion to data not valid (write) | t_{DH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 187 | \overline{RAS} assertion to data not valid (write) | t_{DHR} | $9.75 \times T_C - 4.0$ | 93.5 | — | ns |
| 188 | \overline{WR} assertion to \overline{CAS} assertion | t_{WCS} | $9.5 \times T_C - 4.3$ | 90.7 | — | ns |
| 189 | \overline{CAS} assertion to \overline{RAS} assertion (refresh) | t_{CSR} | $1.5 \times T_C - 4.0$ | 11.0 | — | ns |
| 190 | \overline{RAS} deassertion to \overline{CAS} assertion (refresh) | t_{RPC} | $4.75 \times T_C - 4.0$ | 43.5 | — | ns |
| 191 | \overline{RD} assertion to \overline{RAS} deassertion | t_{ROH} | $15.5 \times T_C - 4.0$ | 151.0 | — | ns |
| 192 | \overline{RD} assertion to data valid | t_{GA} | $14 \times T_C - 5.7$ | — | 134.3 | ns |
| 193 | \overline{RD} deassertion to data not valid ⁵ | t_{GZ} | | 0.0 | — | ns |
| 194 | \overline{WR} assertion to data active | | $0.75 \times T_C - 1.5$ | 6.0 | — | ns |
| 195 | \overline{WR} deassertion to data high impedance | | $0.25 \times T_C$ | — | 2.5 | ns |

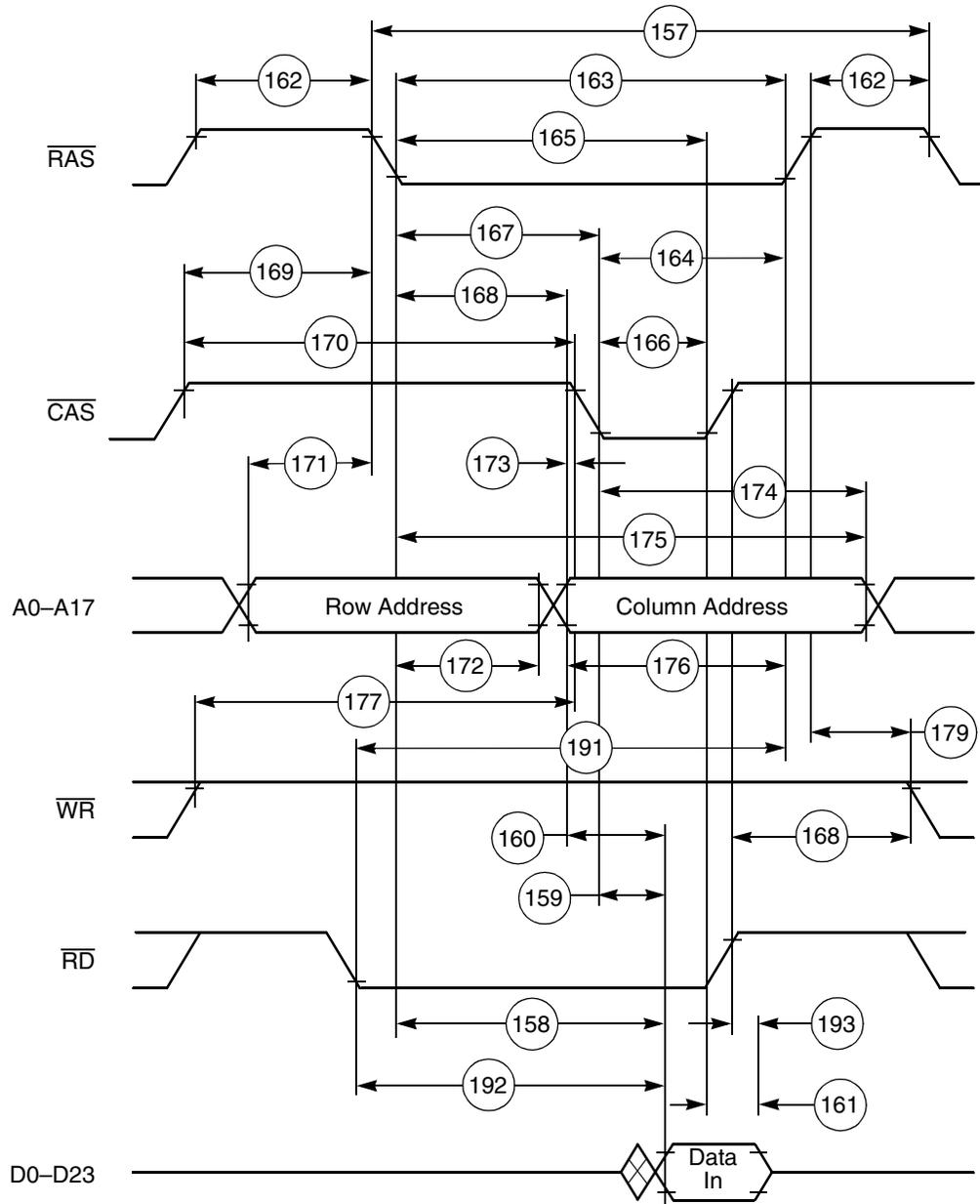
¹ The number of wait states for an out-of-page access is specified in the DCR.

² The refresh period is specified in the DCR.

³ An expression is used to compute the maximum or minimum value listed (or both if the expression includes \pm).

⁴ Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

⁵ \overline{RD} deassertion always occurs after \overline{CAS} deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ} .



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Figure 3-15 DRAM Out-of-Page Read Access

External Memory Expansion Port (Port A)

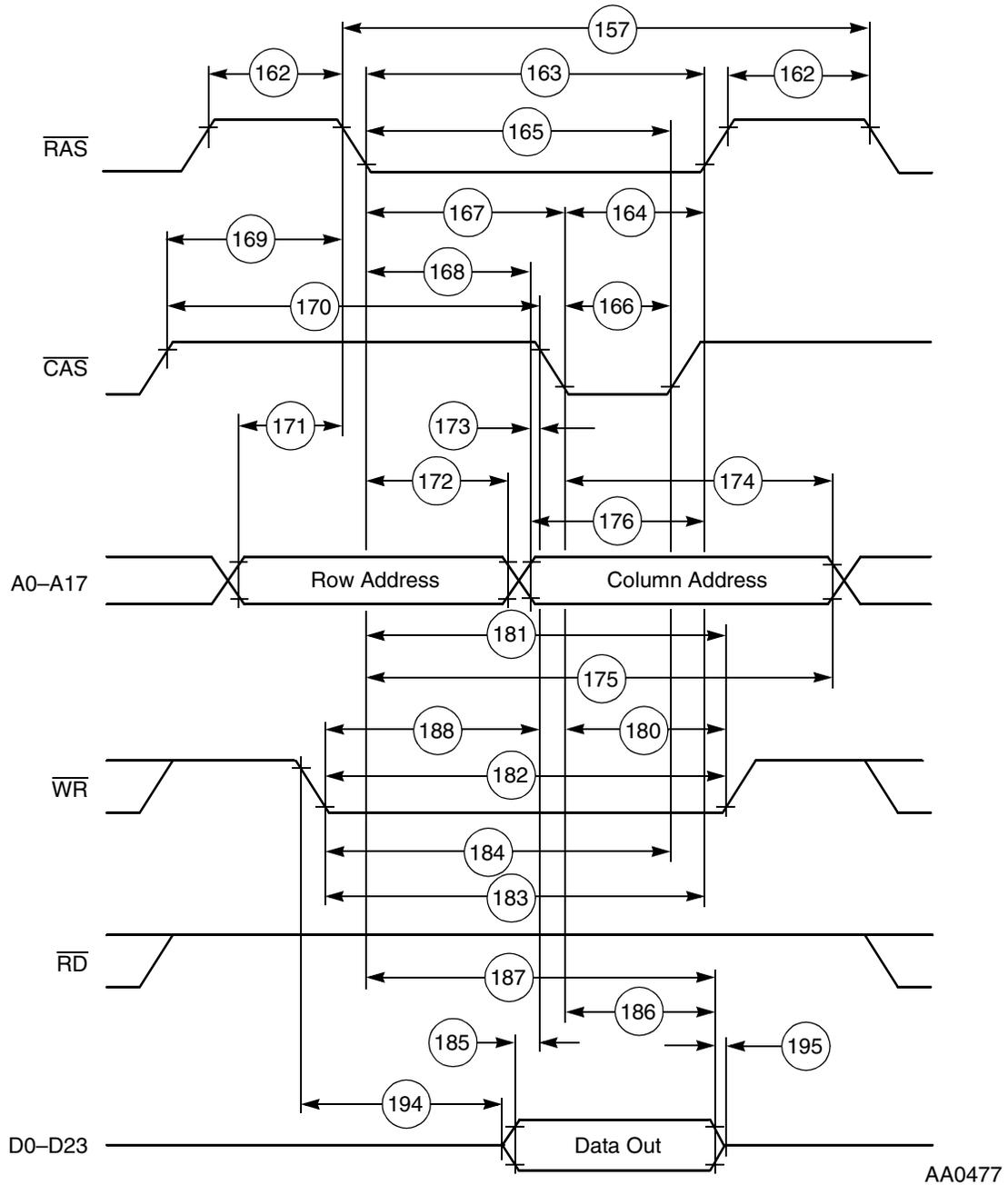
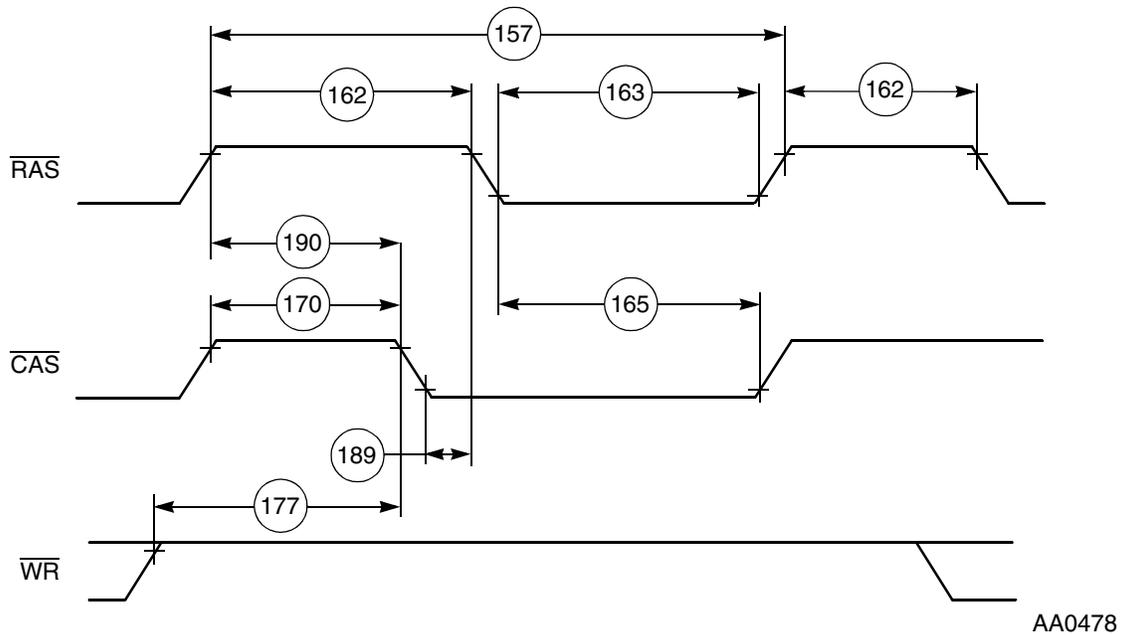


Figure 3-16 DRAM Out-of-Page Write Access



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Figure 3-17 DRAM Refresh Access

3.10.3 Arbitration Timings

Table 3-14 Asynchronous Bus Arbitration Timing^{1, 2, 3}

| No. | Characteristics | Expression | 150 MHz | | Unit |
|-----|---|-----------------|---------|------|------|
| | | | Min | Max | |
| 250 | $\overline{\text{BB}}$ assertion window from $\overline{\text{BG}}$ input negation. | $2.5 * T_c + 5$ | — | 21.7 | ns |
| 251 | Delay from $\overline{\text{BB}}$ assertion to $\overline{\text{BG}}$ assertion | $2 * T_c + 5$ | 18.3 | — | ns |

¹ Bit 13 in the OMR register must be set to enter Asynchronous Arbitration mode.

² If Asynchronous Arbitration mode is active, none of the timings in Table 3-14 is required.

³ In order to guarantee timings 250, and 251, it is recommended to assert $\overline{\text{BG}}$ inputs to different 56300 devices (on the same bus) in a non overlap manner as shown in Figure 3-18.

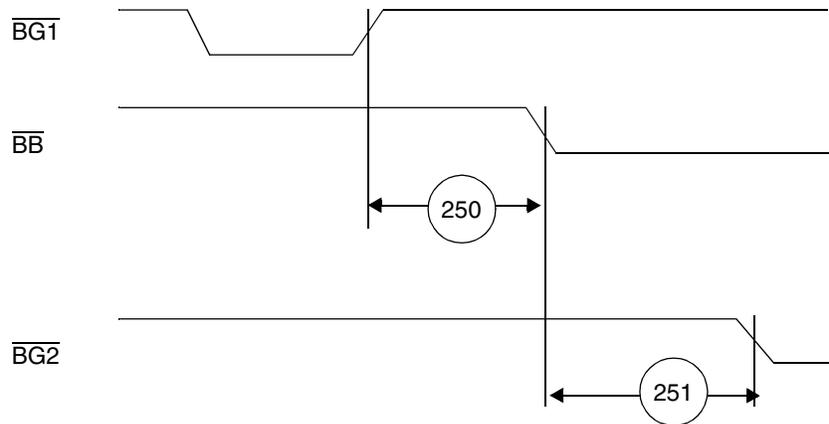


Figure 3-18 Asynchronous Bus Arbitration Timing

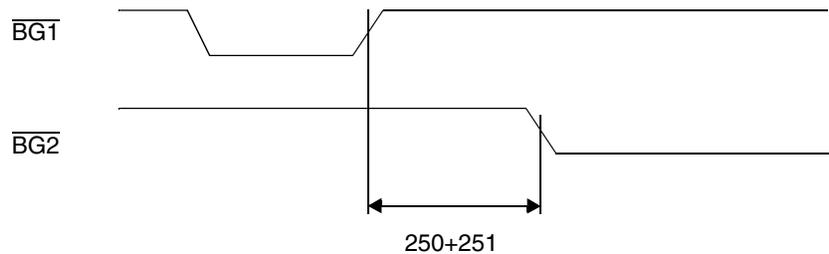


Figure 3-19 Asynchronous Bus Arbitration Timing

3.10.4 Background explanation for Asynchronous Bus Arbitration:

The asynchronous bus arbitration is enabled by internal synchronization circuits on \overline{BG} and \overline{BB} inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a 56300 part may assume mastership and assert \overline{BB} for some time after \overline{BG} is negated. This is the reason for timing 250.

Once \overline{BB} is asserted, there is a synchronization delay from \overline{BB} assertion to the time this assertion is exposed to other 56300 components which are potential masters on the same bus. If \overline{BG} input is asserted before that time, a situation of \overline{BG} asserted, and \overline{BB} negated, may cause another 56300 component to assume mastership at the same time. Therefore some non-overlap period between one \overline{BG} input active to another \overline{BG} input active is required. Timing 251 ensures that such a situation is avoided.

3.11 Parallel Host Interface (HDI08) Timing

Table 3-15 Host Interface (HDI08) Timing^{1, 2, 3}

| No. | Characteristics | Expression | 150 MHz | | Unit |
|-----|---|------------------------|--------------|--------|------|
| | | | Min | Max | |
| 317 | Read data strobe assertion width ⁴ $\overline{\text{HACK}}$ read assertion width | $T_C + 9.9$ | 16.7 | — | ns |
| 318 | Read data strobe deassertion width ⁴ $\overline{\text{HACK}}$ read deassertion width | — | 9.9 | — | ns |
| 319 | Read data strobe deassertion width ⁴ after “Last Data Register” reads ^{5, 6} , or between two consecutive CVR, ICR, or ISR reads ⁷ $\overline{\text{HACK}}$ deassertion width after “Last Data Register” reads ^{5, 6} | $2.5 \times T_C + 6.6$ | 23.3 | — | ns |
| 320 | Write data strobe assertion width ⁸ $\overline{\text{HACK}}$ write assertion width | — | 13.2 | — | ns |
| 321 | Write data strobe deassertion width ⁸ $\overline{\text{HACK}}$ write deassertion width <ul style="list-style-type: none"> • after ICR, CVR and “Last Data Register” writes⁵ • after IVR writes, or • after TXH:TXM writes (with HBE=0), or • after TXL:TXM writes (with HBE=1) | $2.5 \times T_C + 6.6$ | 23.3 16.5 | — — | ns |
| 322 | $\overline{\text{HAS}}$ assertion width | — | 9.9 | — | ns |
| 323 | $\overline{\text{HAS}}$ deassertion to data strobe assertion ⁹ | — | 0.0 | — | ns |
| 324 | Host data input setup time before write data strobe deassertion ⁸ Host data input setup time before $\overline{\text{HACK}}$ write deassertion | — | 9.9 | — | ns |
| 325 | Host data input hold time after write data strobe deassertion ⁸ Host data input hold time after $\overline{\text{HACK}}$ write deassertion | — | 3.3 | — | ns |
| 326 | Read data strobe assertion to output data active from high impedance ⁴ $\overline{\text{HACK}}$ read assertion to output data active from high impedance | — | 3.3 | — | ns |
| 327 | Read data strobe assertion to output data valid ⁴ $\overline{\text{HACK}}$ read assertion to output data valid | — | — | 24.2 | ns |
| 328 | Read data strobe deassertion to output data high impedance ⁴ $\overline{\text{HACK}}$ read deassertion to output data high impedance | — | — | 9.9 | ns |
| 329 | Output data hold time after read data strobe deassertion ⁴ Output data hold time after $\overline{\text{HACK}}$ read deassertion | — | 3.3 | — | ns |
| 330 | $\overline{\text{HCS}}$ assertion to read data strobe deassertion ⁴ | $T_C + 9.9$ | 16.7 | — | ns |
| 331 | $\overline{\text{HCS}}$ assertion to write data strobe deassertion ⁸ | — | 9.9 | — | ns |

Table 3-15 Host Interface (HDI08) Timing^{1, 2, 3} (continued)

| No. | Characteristics | Expression | 150 MHz | | Unit |
|-----|--|--|---------------------|-------------|------|
| | | | Min | Max | |
| 332 | $\overline{\text{HCS}}$ assertion to output data valid | — | — | 19.1 | ns |
| 333 | $\overline{\text{HCS}}$ hold time after data strobe deassertion ⁹ | — | 0.0 | — | ns |
| 334 | Address (AD7–AD0) setup time before $\overline{\text{HAS}}$ deassertion (HMUX=1) | — | 4.7 | — | ns |
| 335 | Address (AD7–AD0) hold time after $\overline{\text{HAS}}$ deassertion (HMUX=1) | — | 3.3 | — | ns |
| 336 | A10–A8 (HMUX=1), A2–A0 (HMUX=0), $\text{HR}/\overline{\text{W}}$ setup time before data strobe assertion ⁹ • Read • Write | — | 0 4.7 | — — | ns |
| 337 | A10–A8 (HMUX=1), A2–A0 (HMUX=0), $\text{HR}/\overline{\text{W}}$ hold time after data strobe deassertion ⁹ | — | 3.3 | — | ns |
| 338 | Delay from read data strobe deassertion to host request assertion for “Last Data Register” read ^{4, 5, 10} | T_C | 6.7 | — | ns |
| 339 | Delay from write data strobe deassertion to host request assertion for “Last Data Register” write ^{5, 8, 10} | $2 \times T_C$ | 13.4 | — | ns |
| 340 | Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0) ^{5, 9, 10} | — | — | 19.1 | ns |
| 341 | Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request) ^{5, 9, 10, 11} | — | — | 300.0 | ns |
| 342 | Delay from DMA $\overline{\text{HACK}}$ deassertion to HOREQ assertion • For “Last Data Register” read ⁵ • For “Last Data Register” write ⁵ • For other cases | $2 \times T_C + 19.1$ $1.5 \times T_C + 19.1$ | 32.5 29.2 0.0 | — — — | ns |
| 343 | Delay from DMA $\overline{\text{HACK}}$ assertion to HOREQ deassertion • HROD = 0 ⁵ | — | — | 20.2 | ns |
| 344 | Delay from DMA $\overline{\text{HACK}}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request ^{5, 11} | — | — | 300.0 | ns |

¹ See Host Port Usage Considerations in the DSP56367 User’s Manual.

² In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.

³ $V_{CC} = 1.8 \text{ V} \pm 5\%$; $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50 \text{ pF}$

⁴ The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.

⁵ The “last data register” is the register at address \$7, which is the last location to be read or written in data transfers.

⁶ This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.

⁷ This timing is applicable only if two consecutive reads from one of these registers are executed.

⁸ The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.

- ⁹ The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.
- ¹⁰ The host request is HOREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.
- ¹¹ In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the open-drain mode.

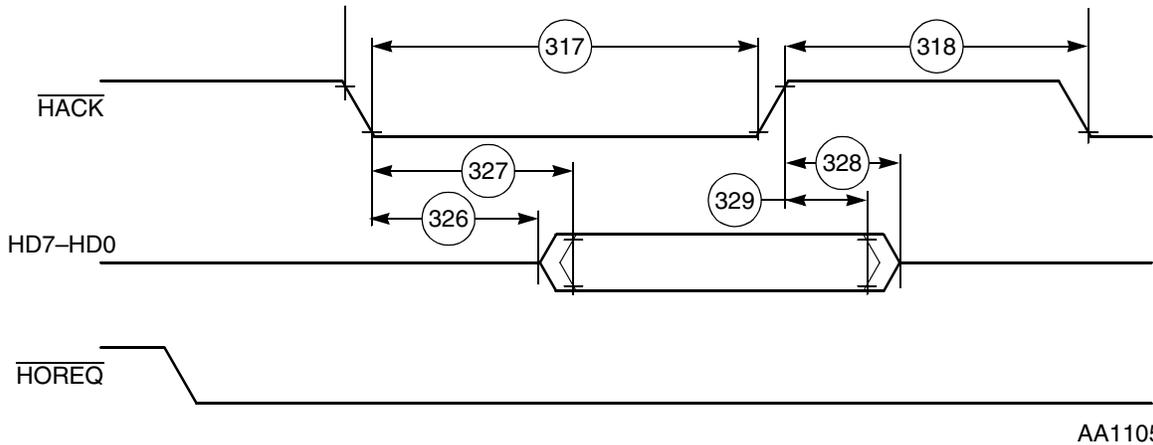


Figure 3-20 Host Interrupt Vector Register (IVR) Read Timing Diagram

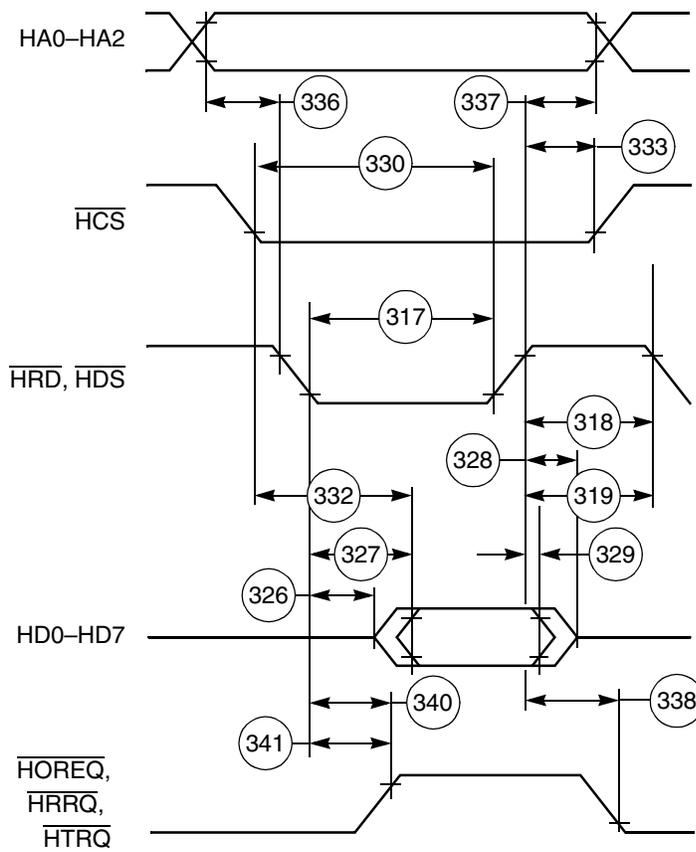
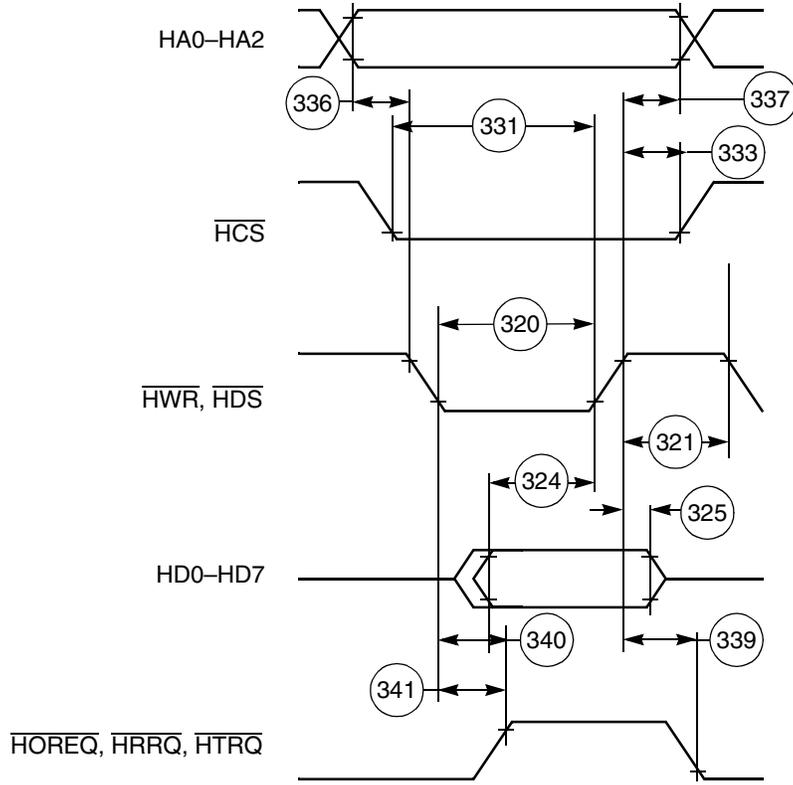


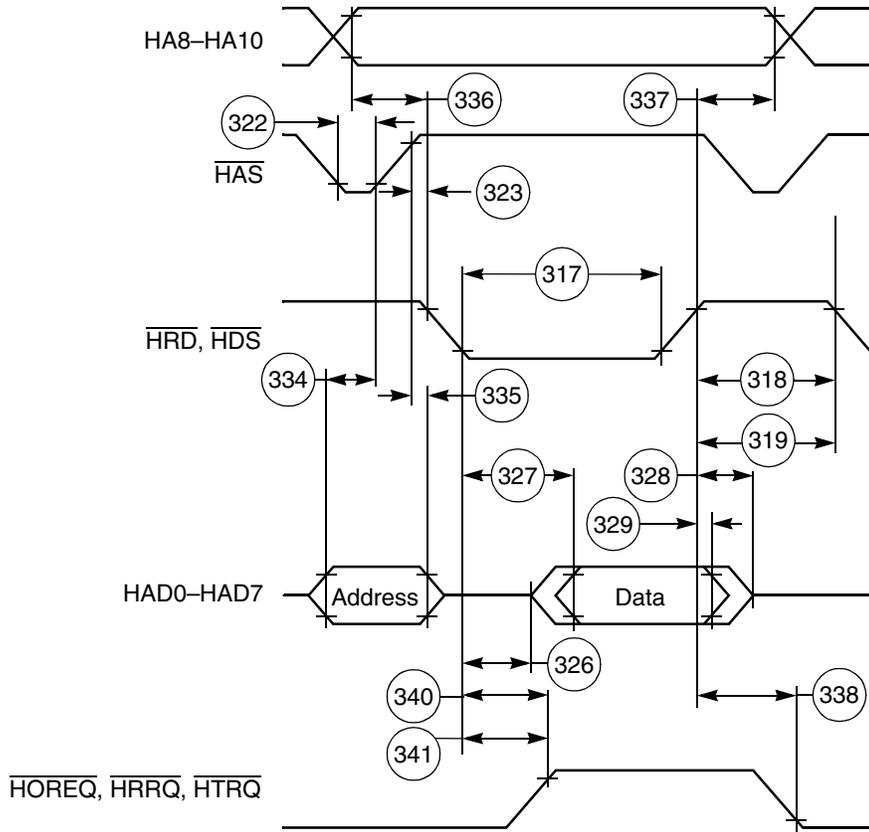
Figure 3-21 Read Timing Diagram, Non-Multiplexed Bus

Parallel Host Interface (HDI08) Timing



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Figure 3-22 Write Timing Diagram, Non-Multiplexed Bus



AA0486

Figure 3-23 Read Timing Diagram, Multiplexed Bus

Parallel Host Interface (HDI08) Timing

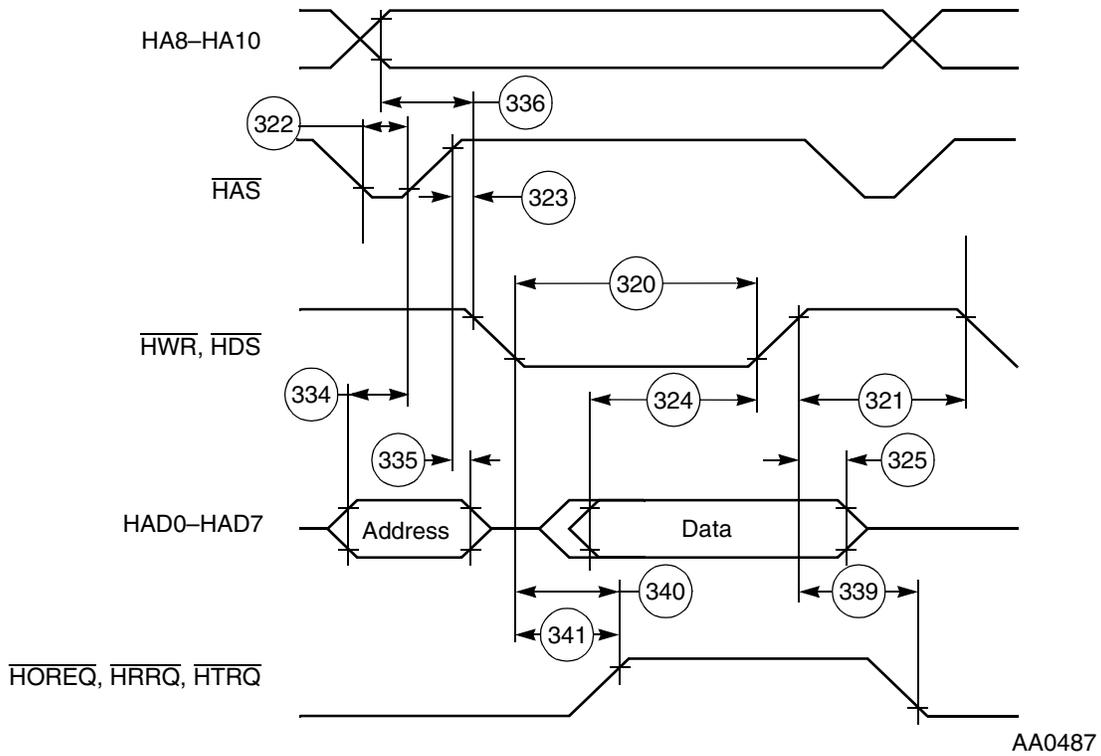


Figure 3-24 Write Timing Diagram, Multiplexed Bus

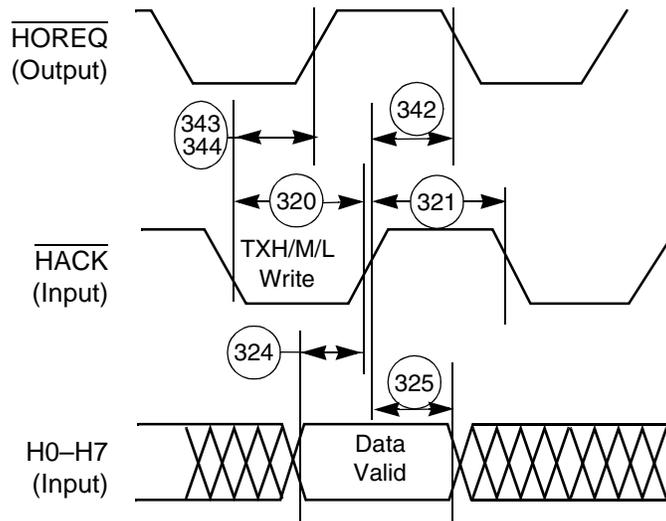


Figure 3-25 Host DMA Write Timing Diagram

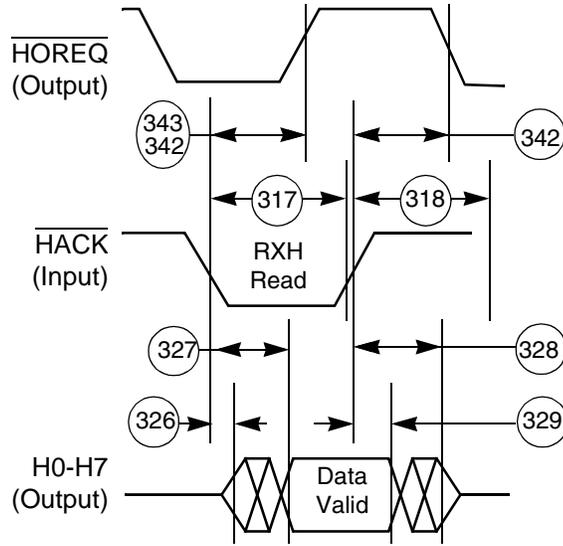


Figure 3-26 Host DMA Read Timing Diagram

3.12 Serial Host Interface SPI Protocol Timing

Table 3-16 Serial Host Interface SPI Protocol Timing

| No. | Characteristics ¹ | Mode | Filter Mode | Expression ² | Min | Max | Unit |
|-----|--|--------|----------------------------|---|------------------------|----------------|------|
| 140 | Tolerable spike width on clock or data in | — | Bypassed Narrow Wide | — — — | — — — | 0 50 100 | ns |
| 141 | Minimum serial clock cycle = $t_{SPICC}(\min)$ | Master | Bypassed Narrow Wide | $6 \times T_C + 46$ $6 \times T_C + 152$ $6 \times T_C + 223$ | 86.2 192.2 263.2 | — — — | ns |
| 142 | Serial clock high period | Master | Bypassed Narrow Wide | $0.5 \times t_{SPICC} - 10$ $0.5 \times t_{SPICC} - 10$ $0.5 \times t_{SPICC} - 10$ | 38 91 126.5 | — — — | ns |
| | | Slave | Bypassed Narrow Wide | $2.5 \times T_C + 12$ $2.5 \times T_C + 102$ $2.5 \times T_C + 189$ | 28.8 118.8 205.8 | — — — | ns |
| 143 | Serial clock low period | Master | Bypassed Narrow Wide | $0.5 \times t_{SPICC} - 10$ $0.5 \times t_{SPICC} - 10$ $0.5 \times t_{SPICC} - 10$ | 38 | — | ns |
| | | Slave | Bypassed Narrow Wide | $2.5 \times T_C + 12$ $2.5 \times T_C + 102$ $2.5 \times T_C + 189$ | 28.8 118.8 205.8 | — — — | ns |

Table 3-16 Serial Host Interface SPI Protocol Timing (continued)

| No. | Characteristics ¹ | Mode | Filter Mode | Expression ² | Min | Max | Unit |
|-----|---|------------------|-------------|-----------------------------|--------|------------|------|
| 144 | Serial clock rise/fall time | Master Slave | — — | — — | — — | 10 2000 | ns |
| 146 | \overline{SS} assertion to first SCK edge CPHA = 0 | Slave | Bypassed | $3.5 \times T_C + 15$ | 38.5 | — | ns |
| | Narrow | | 0 | 0 | — | | |
| | Wide | 0 | 0 | — | | | |
| 147 | Last SCK edge to \overline{SS} not asserted | Slave | Bypassed | 12 | 12 | — | ns |
| | | | Narrow | 102 | 102 | — | |
| | | | Wide | 189 | 189 | — | |
| 148 | Data input valid to SCK edge (data input set-up time) | Master/ Slave | Bypassed | 0 | 0 | — | ns |
| | | | Narrow | $\text{MAX}\{(20-T_C), 0\}$ | 13.3 | — | |
| | | | Wide | $\text{MAX}\{(40-T_C), 0\}$ | 33.3 | — | |
| 149 | SCK last sampling edge to data input not valid | Master/ Slave | Bypassed | $2.5 \times T_C + 10$ | 26.8 | — | ns |
| | | | Narrow | $2.5 \times T_C + 30$ | 46.8 | — | |
| | | | Wide | $2.5 \times T_C + 50$ | 66.8 | — | |
| 150 | \overline{SS} assertion to data out active | Slave | — | 2 | 2 | — | ns |
| 151 | \overline{SS} deassertion to data high impedance ³ | Slave | — | 9 | — | 9 | ns |
| 152 | SCK edge to data out valid (data out delay time) | Master/ Slave | Bypassed | $2 \times T_C + 33$ | — | 46.4 | ns |
| | | | Narrow | $2 \times T_C + 123$ | — | 136.4 | |
| | | | Wide | $2 \times T_C + 210$ | — | 223.4 | |
| 153 | SCK edge to data out not valid (data out hold time) | Master/ Slave | Bypassed | $T_C + 5$ | 11.7 | — | ns |
| | | | Narrow | $T_C + 55$ | 61.7 | — | |
| | | | Wide | $T_C + 106$ | 112.7 | — | |
| 154 | \overline{SS} assertion to data out valid (CPHA = 0) | Slave | — | $T_C + 33$ | — | 39.7 | ns |
| 157 | First SCK sampling edge to \overline{HREQ} output deassertion | Slave | Bypassed | $2.5 \times T_C + 30$ | — | 46.8 | ns |
| | | | Narrow | $2.5 \times T_C + 120$ | — | 136.8 | |
| | | | Wide | $2.5 \times T_C + 217$ | — | 233.8 | |
| 158 | Last SCK sampling edge to \overline{HREQ} output not deasserted (CPHA = 1) | Slave | Bypassed | $2.5 \times T_C + 30$ | 46.8 | — | ns |
| | | | Narrow | $2.5 \times T_C + 80$ | 96.8 | — | |
| | | | Wide | $2.5 \times T_C + 136$ | 152.8 | — | |
| 159 | \overline{SS} deassertion to \overline{HREQ} output not deasserted (CPHA = 0) | Slave | — | $2.5 \times T_C + 30$ | 46.8 | — | ns |

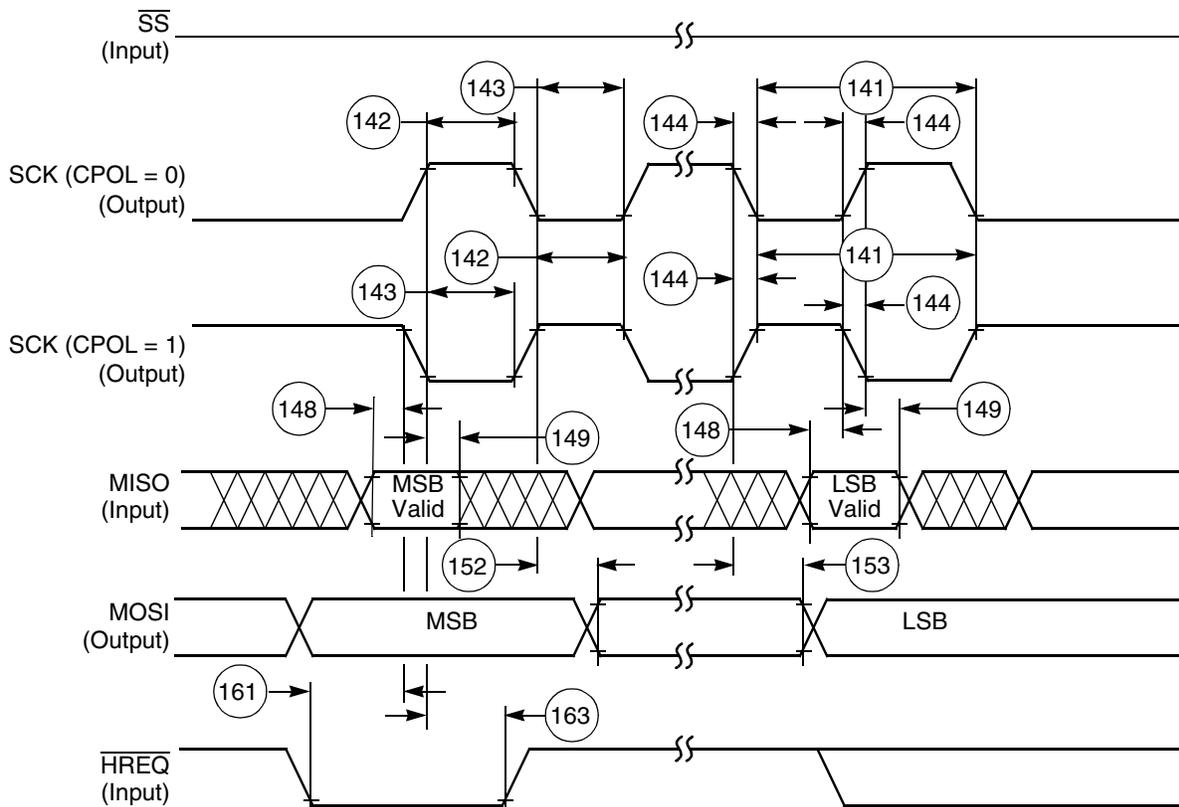
Table 3-16 Serial Host Interface SPI Protocol Timing (continued)

| No. | Characteristics ¹ | Mode | Filter Mode | Expression ² | Min | Max | Unit |
|-----|---|--------|-------------|--|-------|-----|------|
| 160 | \overline{SS} deassertion pulse width (CPHA = 0) | Slave | — | $T_C + 6$ | 12.7 | — | ns |
| 161 | HREQ in assertion to first SCK edge | Master | Bypassed | $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ | 97.8 | — | ns |
| | | | Narrow | $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ | 160.8 | — | ns |
| | | | Wide | $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ | 196.8 | — | ns |
| 162 | \overline{HREQ} in deassertion to last SCK sampling edge (\overline{HREQ} in set-up time) (CPHA = 1) | Master | — | 0 | 0 | — | ns |
| 163 | First SCK edge to \overline{HREQ} in not asserted (\overline{HREQ} in hold time) | Master | — | 0 | 0 | — | ns |

¹ $V_{CC} = 1.8 V \pm 5\%$; $T_J = -40^\circ C$ to $+95^\circ C$, $C_L = 50 pF$

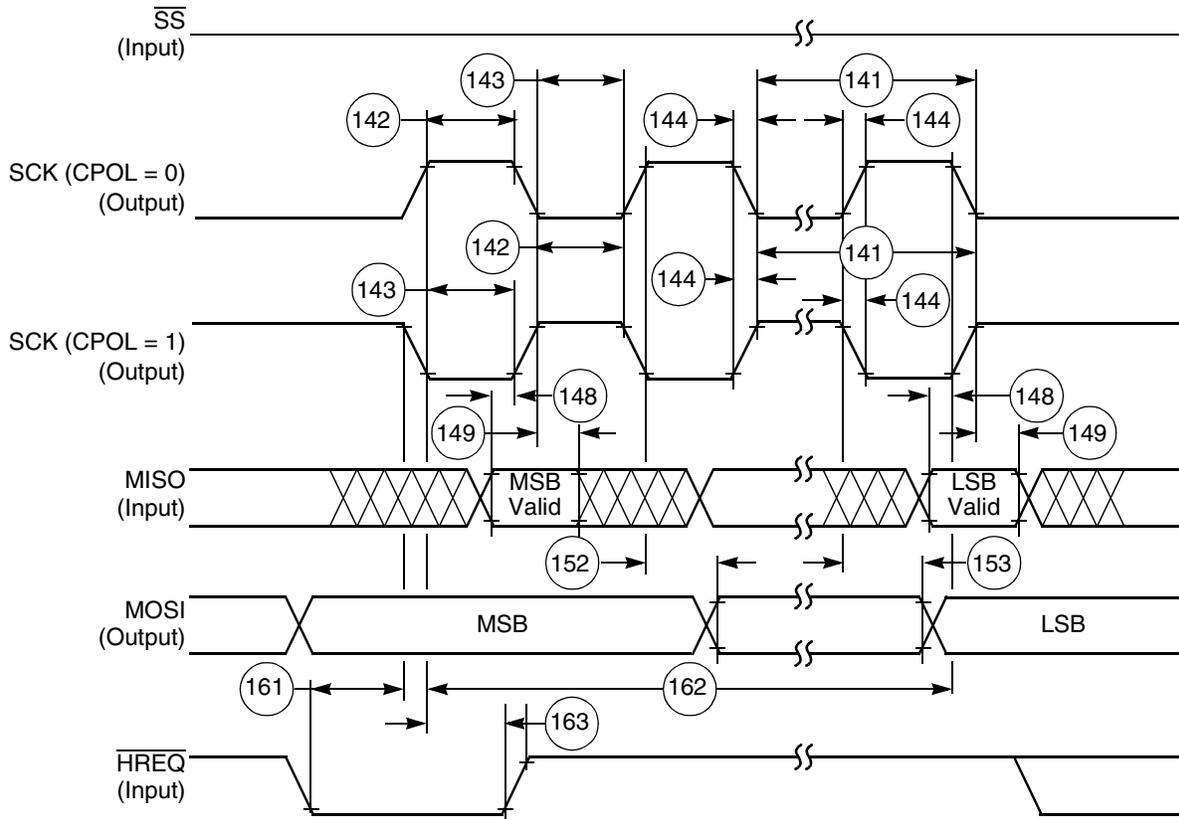
² The timing values calculated are based on simulation data at 150MHz. Tester restrictions limit SHI testing to lower clock frequencies.

³ Periodically sampled, not 100% tested



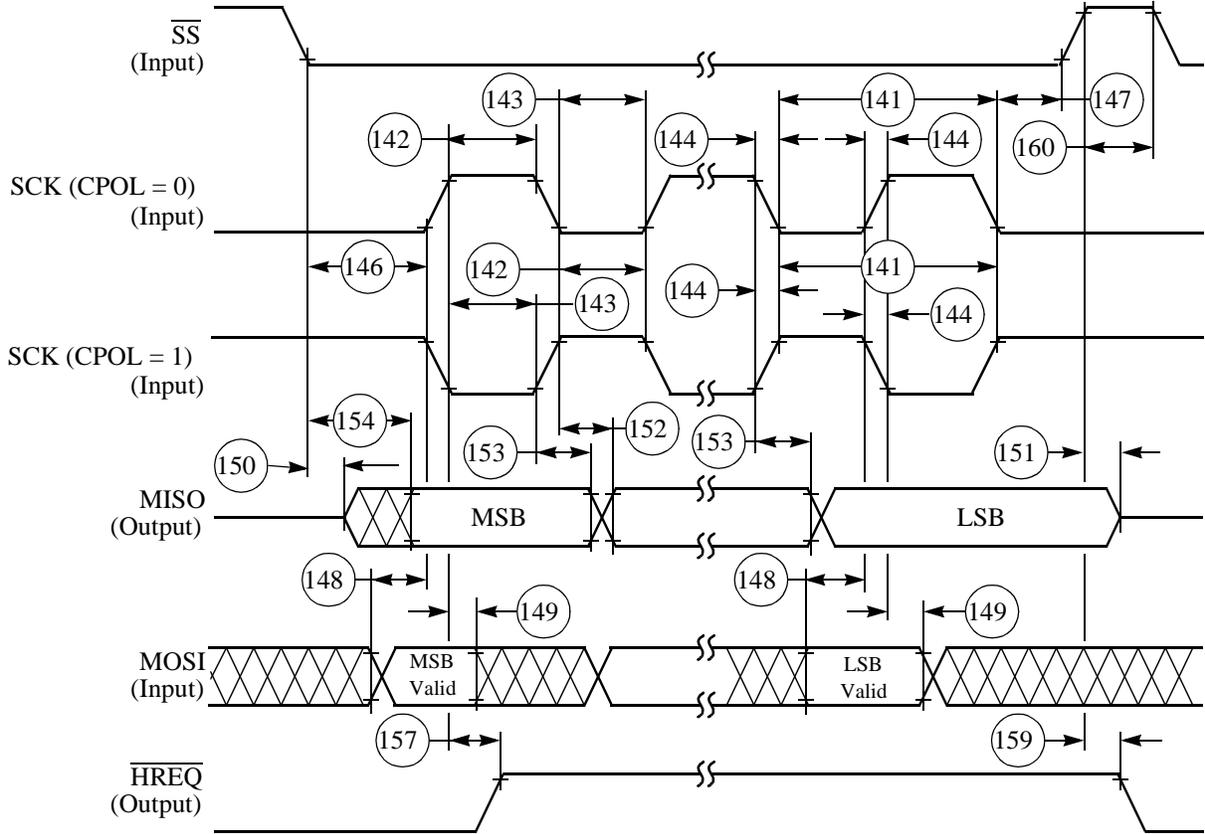
AA0271

Figure 3-27 SPI Master Timing (CPHA = 0)



AA0272

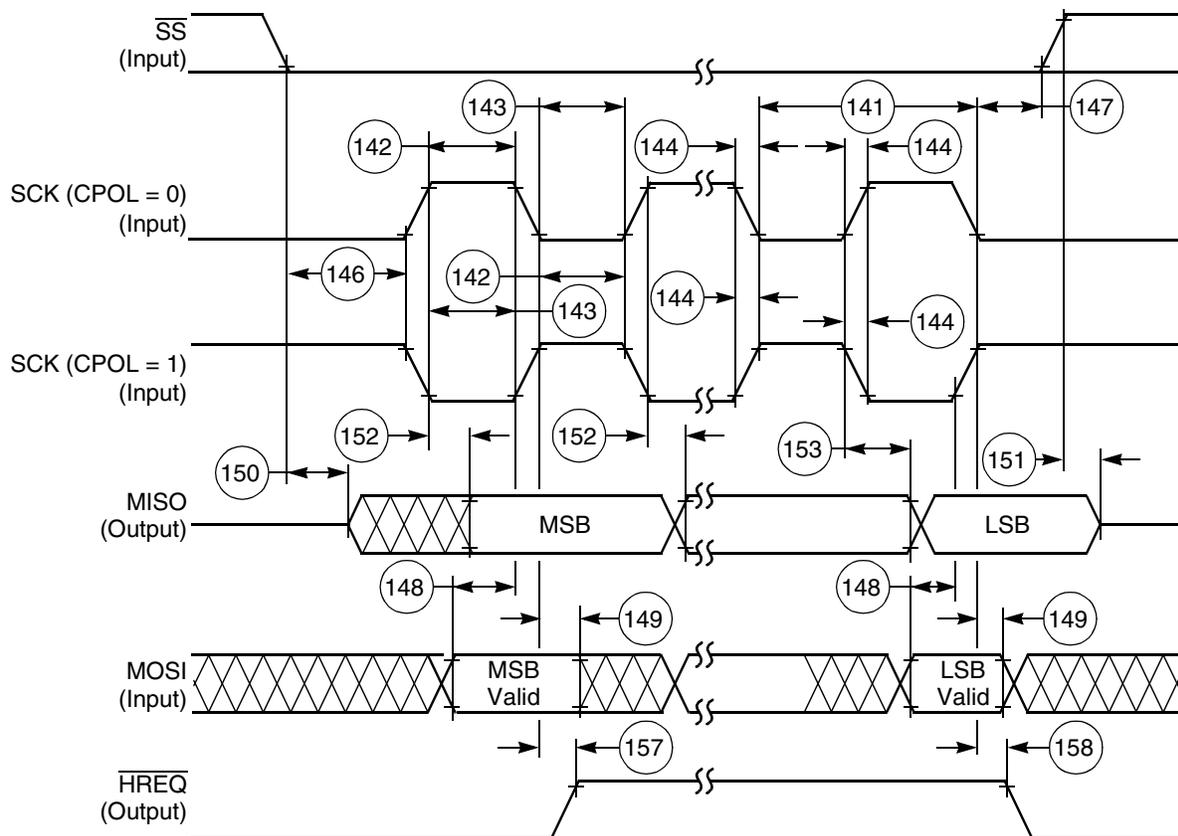
Figure 3-28 SPI Master Timing (CPHA = 1)



AA0273

Figure 3-29 SPI Slave Timing (CPHA = 0)

Serial Host Interface (SHI) I²C Protocol Timing



AA0274

Figure 3-30 SPI Slave Timing (CPHA = 1)

3.13 Serial Host Interface (SHI) I²C Protocol Timing

Table 3-17 SHI I²C Protocol Timing

| Standard I ² C | | | | | | | |
|---------------------------|---|-----------------------|--------------------------|-----|---------------------------|-----|------|
| No. | Characteristics ^{1, 2, 3} | Symbol/ Expression | Standard ^{4, 5} | | Fast-Mode ^{5, 6} | | Unit |
| | | | Min | Max | Min | Max | |
| | Tolerable spike width on SCL or SDA • Filters bypassed • Narrow filters enabled • Wide filters enabled | — | — | 0 | — | 0 | ns |
| 171 | SCL clock frequency | F _{SCL} | — | 100 | — | 400 | kHz |
| 171 | SCL clock cycle | T _{SCL} | 10 | — | 2.5 | — | μs |
| 172 | Bus free time | T _{BUF} | 4.7 | — | 1.3 | — | μs |
| 173 | Start condition set-up time | T _{SU;STA} | 4.7 | — | 0.6 | — | μs |
| 174 | Start condition hold time | T _{HD;STA} | 4.0 | — | 0.6 | — | μs |

Table 3-17 SHI I²C Protocol Timing (continued)

| Standard I ² C | | | | | | | |
|---------------------------|--|---|--------------------------|------|---------------------------|-----|------|
| No. | Characteristics ^{1, 2, 3} | Symbol/ Expression | Standard ^{4, 5} | | Fast-Mode ^{5, 6} | | Unit |
| | | | Min | Max | Min | Max | |
| 175 | SCL low period | T _{LOW} | 4.7 | — | 1.3 | — | μs |
| 176 | SCL high period | T _{HIGH} | 4.0 | — | 1.3 | — | μs |
| 177 | SCL and SDA rise time | T _R | — | 1000 | 20 + 0.1 × C _b | 300 | ns |
| 178 | SCL and SDA fall time | T _F | — | 300 | 20 + 0.1 × C _b | 300 | ns |
| 179 | Data set-up time | T _{SU;DAT} | 250 | — | 100 | — | ns |
| 180 | Data hold time | T _{HD;DAT} | 0.0 | — | 0.0 | 0.9 | μs |
| 181 | DSP clock frequency | F _{DSP} | | | | | MHz |
| | • Filters bypassed | | 10.6 | — | 28.5 | — | |
| | • Narrow filters enabled | | 11.8 | — | 39.7 | — | |
| | • Wide filters enabled | | 13.1 | — | 61.0 | — | |
| 182 | SCL low to data out valid | T _{VD;DAT} | — | 3.4 | — | 0.9 | μs |
| 183 | Stop condition setup time | T _{SU;STO} | 4.0 | — | 0.6 | — | μs |
| 184 | $\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ in set-up time) | t _{SU;RQI} | 0.0 | — | 0.0 | — | ns |
| 186 | First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion ² | T _{NG;RQO} | | | | | ns |
| | • Filters bypassed | 2 × T _C + 30 | — | 50 | — | 50 | |
| | • Narrow filters enabled | 2 × T _C + 120 | — | 140 | — | 140 | |
| | • Wide filters enabled | 2 × T _C + 208 | — | 228 | — | 228 | |
| 187 | Last SCL edge to HREQ output not deasserted ² | T _{AS;RQO} | | | | | ns |
| | • Filters bypassed | 2 × T _C + 30 | 50 | — | 50 | — | |
| | • Narrow filters enabled | 2 × T _C + 80 | 100 | — | 100 | — | |
| | • Wide filters enabled | 2 × T _C + 135 | 155 | — | 155 | — | |
| 188 | HREQ in assertion to first SCL edge | T _{AS;RQI} | | | | | ns |
| | • Filters bypassed | 0.5 × T _{I²CCP} - 0.5 × T _C - 21 | 4327 | — | 927 | — | |
| | • Narrow filters enabled | | 4282 | — | 882 | — | |
| | • Wide filters enabled | | 4238 | — | 838 | — | |
| 187 | First SCL edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time.) | t _{HO;RQI} | 0.0 | — | 0.0 | — | ns |

¹ V_{CC} = 1.8 V ± 5%; T_J = -40°C to +95°C, C_L = 50 pF² Pull-up resistor: R_P (min) = 1.5 kOhm³ Capacitive load: C_b (max) = 400 pF⁴ It is recommended to enable the wide filters when operating in the I²C Standard Mode.⁵ The timing values are derived from frequencies not exceeding 100 MHz.⁶ It is recommended to enable the narrow filters when operating in the I²C Fast Mode.

3.13.1 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP} , is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (\text{HDM}[7:0] + 1) \times (7 \times (1 - \text{HRS}) + 1)]$$

where

HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.

HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = \$00 to \$FF) may be selected.

In I²C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C (\text{if HDM}[7:0] = \$02 \text{ and HRS} = 1)$$

to

$$4096 \times T_C (\text{if HDM}[7:0] = \$FF \text{ and HRS} = 0)$$

The programmed serial clock cycle (T_{I^2CCP}), SCL rise time (T_R), and the filters selected should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in [Table 3-18](#).

Table 3-18 SCL Serial Clock Cycle (T_{SCL}) Generated as Master

| | |
|------------------------|--|
| Filters bypassed | $T_{I^2CCP} + 2.5 \times T_C + 45\text{ns} + T_R$ |
| Narrow filters enabled | $T_{I^2CCP} + 2.5 \times T_C + 135\text{ns} + T_R$ |
| Wide filters enabled | $T_{I^2CCP} + 2.5 \times T_C + 223\text{ns} + T_R$ |

EXAMPLE:

For DSP clock frequency of 100 MHz (i.e. $T_C = 10\text{ns}$), operating in a standard mode I²C environment ($F_{SCL} = 100\text{ kHz}$ (i.e. $T_{SCL} = 10\mu\text{s}$), $T_R = 1000\text{ns}$), with wide filters enabled:

$$T_{I^2CCP} = 10\mu\text{s} - 2.5 \times 10\text{ns} - 223\text{ns} - 1000\text{ns} = 8752\text{ns}$$

Choosing HRS = 0 gives

$$\text{HDM}[7:0] = (8752\text{ns}) / (2 \times 10\text{ns} \times 8) - 1 = 53.7$$

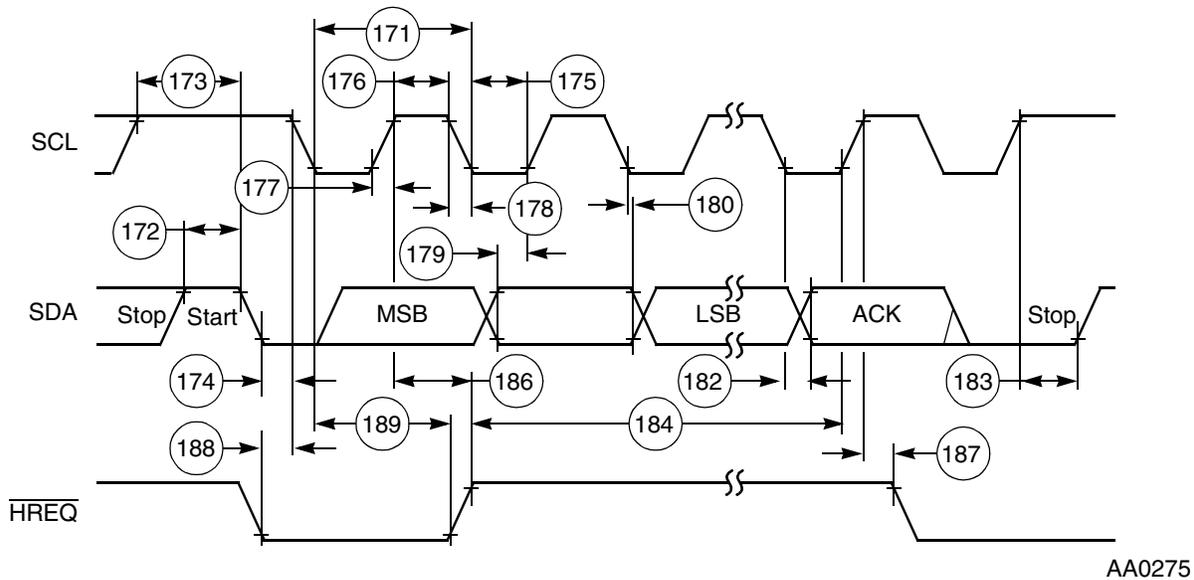
Thus the HDM[7:0] value should be programmed to \$36 (=54).

The resulting T_{I^2CCP} will be:

$$T_{I^2CCP} = [T_C \times 2 \times (\text{HDM}[7:0] + 1) \times (7 \times (1 - 0) + 1)]$$

$$T_{I^2CCP} = [10\text{ns} \times 2 \times (54 + 1) \times (7 \times (1 - 0) + 1)]$$

$$T_{I^2CCP} = [10\text{ns} \times 2 \times 54 \times 8] = 8640\text{ns}$$

Figure 3-31 I²C Timing

3.14 Enhanced Serial Audio Interface Timing

Table 3-19 Enhanced Serial Audio Interface Timing^{1, 2}

| No. | Characteristics ^{3, 4, 5} | Symbol | Expression | Min | Max | Condition ⁶ | Unit |
|-----|---|-------------|---|----------------------|--------------|------------------------|------|
| 430 | Clock cycle ⁷ | t_{SSICC} | $4 \times T_C$ $3 \times T_C$ $TXC: \max[3 \times t_c;$ $t_{454}]$ | 26.8 20.1 26.5 | — — — | i ck x ck x ck | ns |
| 431 | Clock high period • For internal clock • For external clock | — | $2 \times T_C - 10.0$ $1.5 \times T_C$ | 3.4 10.0 | — — | | ns |
| 432 | Clock low period • For internal clock • For external clock | — | $2 \times T_C - 10.0$ $1.5 \times T_C$ | 3.4 10.0 | — — | | ns |
| 433 | RXC rising edge to FSR out (bl) high | — | — | — — | 37.0 22.0 | x ck i ck a | ns |
| 434 | RXC rising edge to FSR out (bl) low | — | — | — — | 37.0 22.0 | x ck i ck a | ns |
| 435 | RXC rising edge to FSR out (wr) high ⁸ | — | — | — — | 39.0 24.0 | x ck i ck a | ns |
| 436 | RXC rising edge to FSR out (wr) low ⁸ | — | — | — — | 39.0 24.0 | x ck i ck a | ns |

Enhanced Serial Audio Interface Timing

Table 3-19 Enhanced Serial Audio Interface Timing^{1, 2} (continued)

| No. | Characteristics ^{3, 4, 5} | Symbol | Expression | Min | Max | Condition ⁶ | Unit |
|-----|--|--------|------------|-------------|--------------|------------------------|------|
| 437 | RXC rising edge to FSR out (wl) high | — | — | — — | 36.0 21.0 | x ck i ck a | ns |
| 438 | RXC rising edge to FSR out (wl) low | — | — | — — | 37.0 22.0 | x ck i ck a | ns |
| 439 | Data in setup time before RXC (SCK in synchronous mode) falling edge | — | — | 0.0 19.0 | — — | x ck i ck | ns |
| 440 | Data in hold time after RXC falling edge | — | — | 5.0 3.0 | — — | x ck i ck | ns |
| 441 | FSR input (bl, wr) high before RXC falling edge ⁸ | — | — | 23.0 1.0 | — — | x ck i ck a | ns |
| 442 | FSR input (wl) high before RXC falling edge | — | — | 23.0 1.0 | — — | x ck i ck a | ns |
| 443 | FSR input hold time after RXC falling edge | — | — | 3.0 0.0 | — — | x ck i ck a | ns |
| 444 | Flags input setup before RXC falling edge | — | — | 0.0 19.0 | — — | x ck i ck s | ns |
| 445 | Flags input hold time after RXC falling edge | — | — | 6.0 0.0 | — — | x ck i ck s | ns |
| 446 | TXC rising edge to FST out (bl) high | — | — | — — | 29.0 15.0 | x ck i ck | ns |
| 447 | TXC rising edge to FST out (bl) low | — | — | — — | 31.0 17.0 | x ck i ck | ns |
| 448 | TXC rising edge to FST out (wr) high ⁸ | — | — | — — | 31.0 17.0 | x ck i ck | ns |
| 449 | TXC rising edge to FST out (wr) low ⁸ | — | — | — — | 33.0 19.0 | x ck i ck | ns |
| 450 | TXC rising edge to FST out (wl) high | — | — | — — | 30.0 16.0 | x ck i ck | ns |
| 451 | TXC rising edge to FST out (wl) low | — | — | — — | 31.0 17.0 | x ck i ck | ns |
| 452 | TXC rising edge to data out enable from high impedance | — | — | — — | 31.0 17.0 | x ck i ck | ns |
| 453 | TXC rising edge to transmitter #0 drive enable assertion | — | — | — — | 34.0 20.0 | x ck i ck | ns |

Table 3-19 Enhanced Serial Audio Interface Timing^{1, 2} (continued)

| No. | Characteristics ^{3, 4, 5} | Symbol | Expression | Min | Max | Condition ⁶ | Unit |
|-----|---|--------|-------------------------------|-------------|--------------|------------------------|------|
| 454 | TXC rising edge to data out valid | — | $23 + 0.5 \times T_C$ 21.0 | — — | 26.5 21.0 | x ck i ck | ns |
| 455 | TXC rising edge to data out high impedance ⁹ | — | — | — — | 31.0 16.0 | x ck i ck | ns |
| 456 | TXC rising edge to transmitter #0 drive enable deassertion ⁹ | — | — | — — | 34.0 20.0 | x ck i ck | ns |
| 457 | FST input (bl, wr) setup time before TXC falling edge ⁸ | — | — | 2.0 21.0 | — — | x ck i ck | ns |
| 458 | FST input (wl) to data out enable from high impedance | — | — | — | 27.0 | — | ns |
| 459 | FST input (wl) to transmitter #0 drive enable assertion | — | — | — | 31.0 | — | ns |
| 460 | FST input (wl) setup time before TXC falling edge | — | — | 2.0 21.0 | — — | x ck i ck | ns |
| 461 | FST input hold time after TXC falling edge | — | — | 4.0 0.0 | — — | x ck i ck | ns |
| 462 | Flag output valid after TXC rising edge | — | — | — — | 32.0 18.0 | x ck i ck | ns |
| 463 | HCKR/HCKT clock cycle | — | — | 40.0 | — | | ns |
| 464 | HCKT input rising edge to TXC output | — | — | — | 27.5 | | ns |
| 465 | HCKR input rising edge to RXC output | — | — | — | 27.5 | | ns |

¹ The timing values calculated are based on simulation data at 150MHz. Tester restrictions limit ESAI testing to lower clock frequencies.

² ESAI_1 specs match those of ESAI_0.

³ $V_{CC} = 1.8 V \pm 5\%$; $T_J = -40^\circ C$ to $+95^\circ C$, $C_L = 50 pF$

⁴ i ck = internal clock

x ck = external clock

i ck a = internal clock, asynchronous mode (asynchronous implies that TXC and RXC are two different clocks)

i ck s = internal clock, synchronous mode (synchronous implies that TXC and RXC are the same clock)

⁵ bl = bit length

wl = word length

wr = word length relative

⁶ TXC(SCKT pin) = transmit clock

RXC(SCKR pin) = receive clock

FST(FST pin) = transmit frame sync

FSR(FSR pin) = receive frame sync

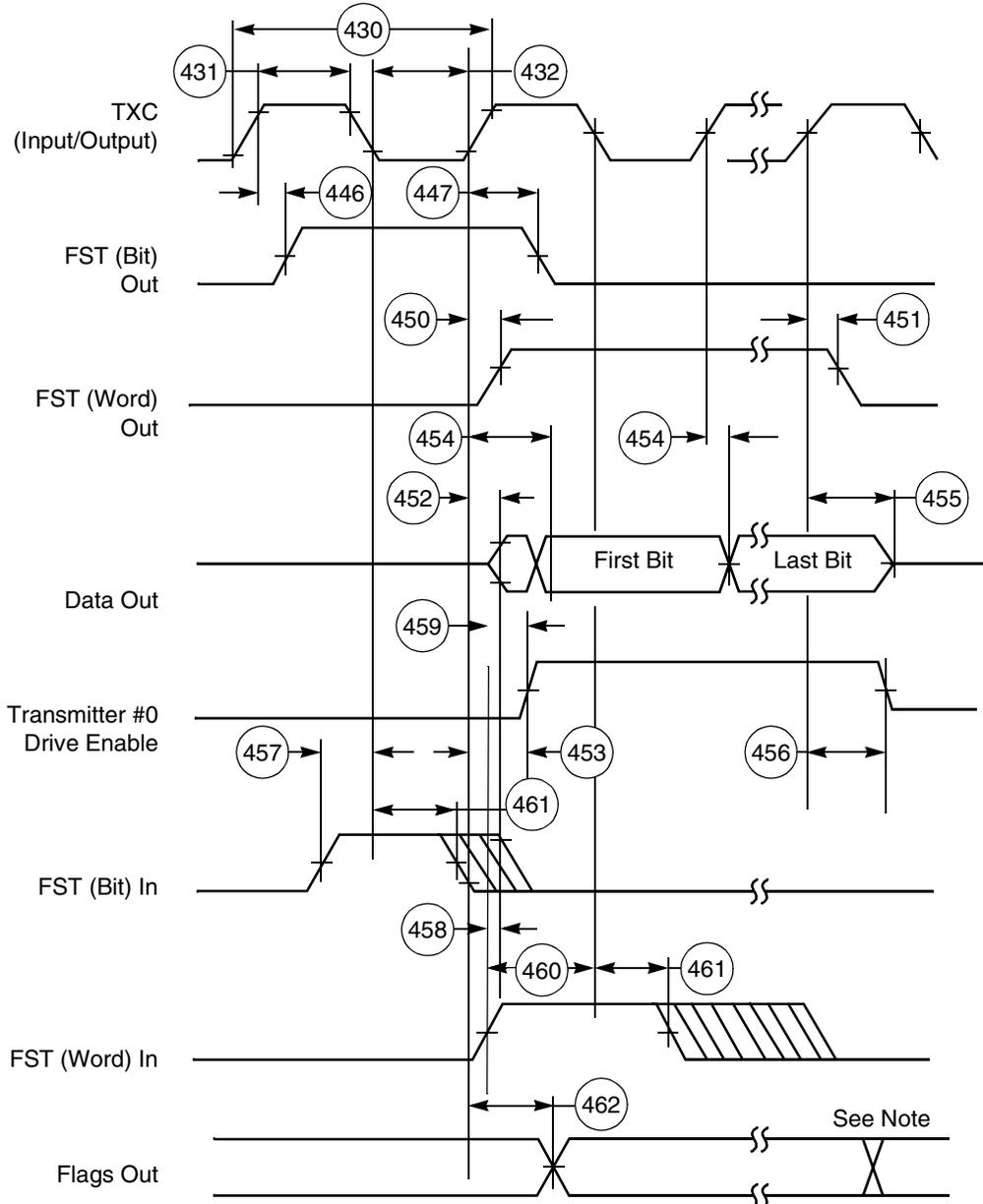
HCKT(HCKT pin) = transmit high frequency clock

HCKR(HCKR pin) = receive high frequency clock

⁷ For the internal clock, the external clock cycle is defined by lcy and the ESAI control register.

Enhanced Serial Audio Interface Timing

- ⁸ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
- ⁹ Periodically sampled and not 100% tested.



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

AA0490

Figure 3-32 ESAL Transmitter Timing

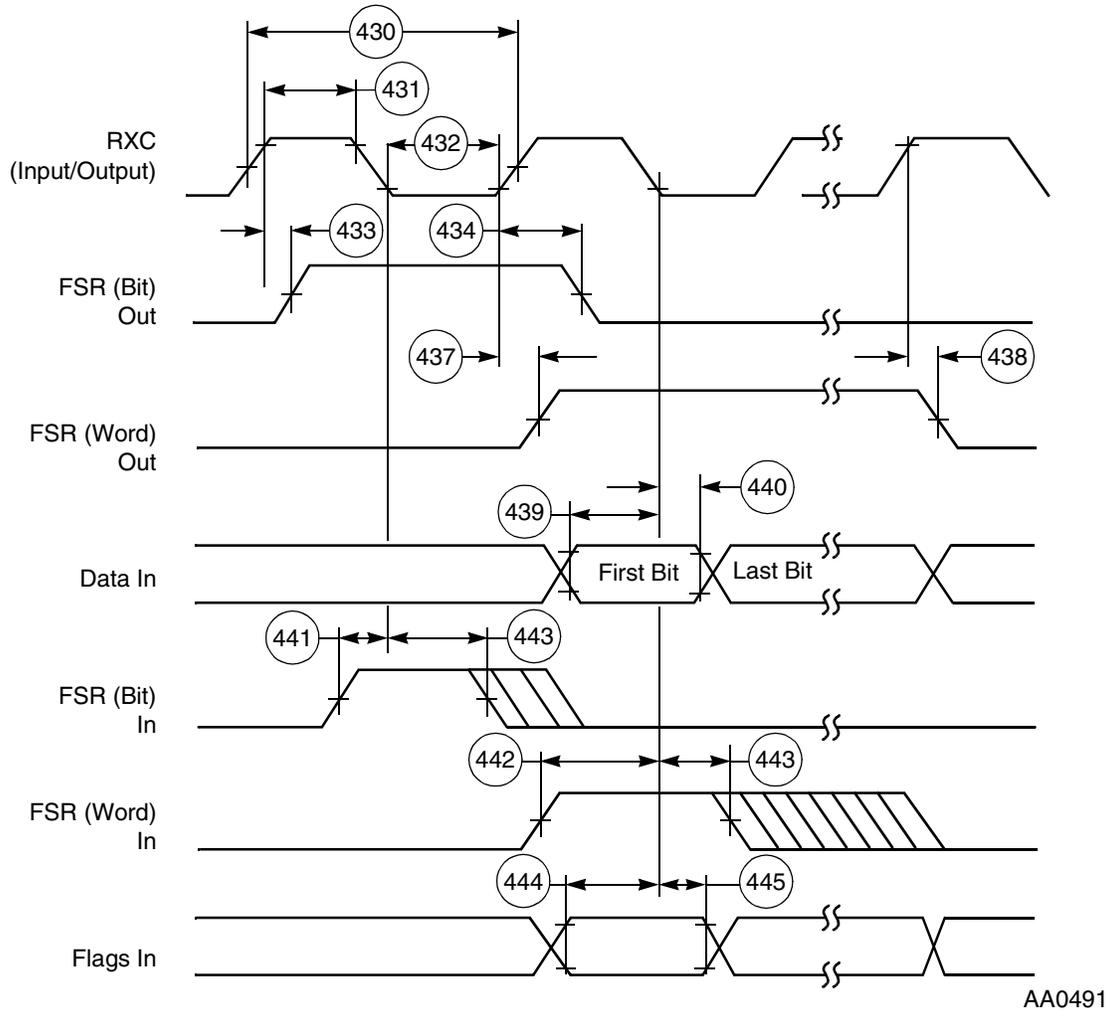


Figure 3-33 ESAI Receiver Timing

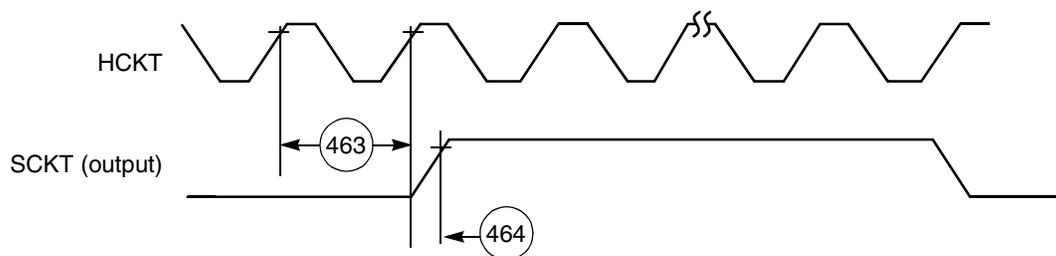


Figure 3-34 ESAI HCKT Timing

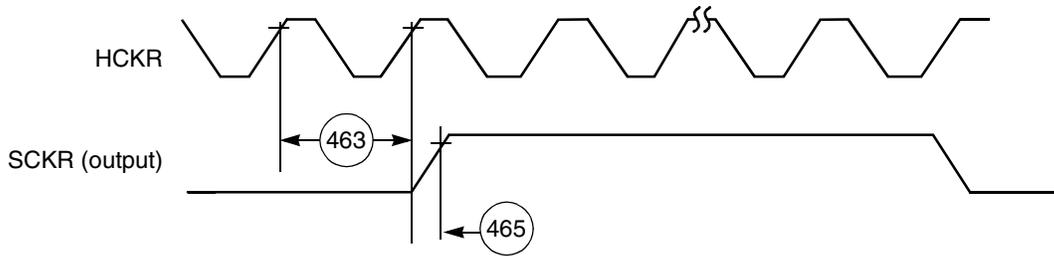


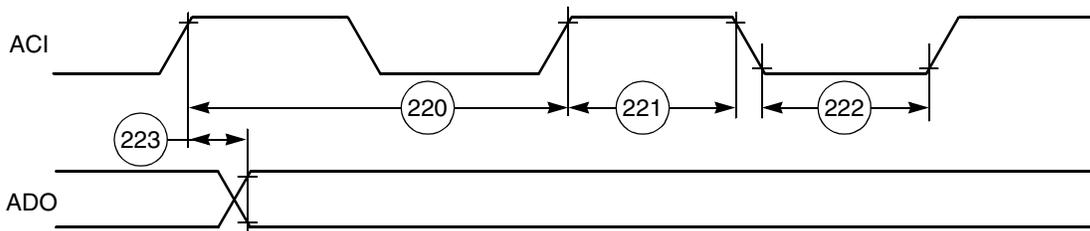
Figure 3-35 ESAI HCKR Timing

3.15 Digital Audio Transmitter Timing

Table 3-20 Digital Audio Transmitter Timing

| No. | Characteristic | Expression | 150 MHz | | Unit |
|-----|------------------------------|----------------------|---------|------|------|
| | | | Min | Max | |
| | ACI frequency ¹ | $1 / (2 \times T_C)$ | — | 75 | MHz |
| 220 | ACI period | $2 \times T_C$ | 13.4 | — | ns |
| 221 | ACI high duration | $0.5 \times T_C$ | 3.4 | — | ns |
| 222 | ACI low duration | $0.5 \times T_C$ | 3.4 | — | ns |
| 223 | ACI rising edge to ADO valid | $1.5 \times T_C$ | — | 10.0 | ns |

¹ In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of the DSP56367 internal clock frequency. For example, if the DSP56367 is running at 150 MHz internally, the ACI frequency should be less than 75 MHz.



AA1280

Figure 3-36 Digital Audio Transmitter Timing

3.16 Timer Timing

Table 3-21 Timer Timing¹

| No. | Characteristics | Expression | 150 MHz | | Unit |
|-----|-----------------|----------------------|---------|-----|------|
| | | | Min | Max | |
| 480 | TIO Low | $2 \times T_C + 2.0$ | 15.4 | — | ns |
| 481 | TIO High | $2 \times T_C + 2.0$ | 15.4 | — | ns |

¹ $V_{CC} = 1.8 \text{ V} \pm 0.09 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50 \text{ pF}$

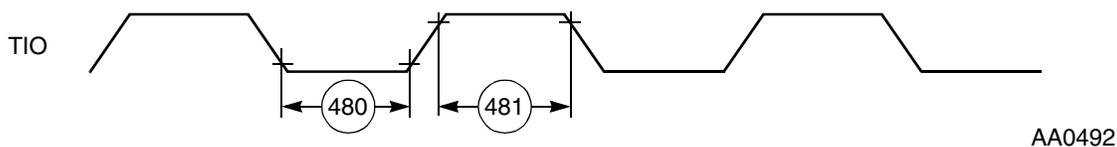


Figure 3-37 TIO Timer Event Input Restrictions

3.17 GPIO Timing

Table 3-22 GPIO Timing

| No. | Characteristics ¹ | Expression | Min | Max | Unit |
|------------------|---|-------------------------|------|------|------|
| 490 ² | EXTAL edge to GPIO out valid (GPIO out delay time) | | — | 32.8 | ns |
| 491 | EXTAL edge to GPIO out not valid (GPIO out hold time) | | 4.8 | — | ns |
| 492 | GPIO In valid to EXTAL edge (GPIO in set-up time) | | 10.2 | — | ns |
| 493 | EXTAL edge to GPIO in not valid (GPIO in hold time) | | 1.8 | — | ns |
| 494 ² | Fetch to EXTAL edge before GPIO change | $6.75 \times T_C - 1.8$ | 43.4 | — | ns |
| 495 | GPIO out rise time | — | — | 13 | ns |
| 496 | GPIO out fall time | — | — | 13 | ns |

¹ $V_{CC} = 1.8 \text{ V} \pm 0.09 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50 \text{ pF}$

² Valid only when PLL enabled with multiplication factor equal to one.

JTAG Timing

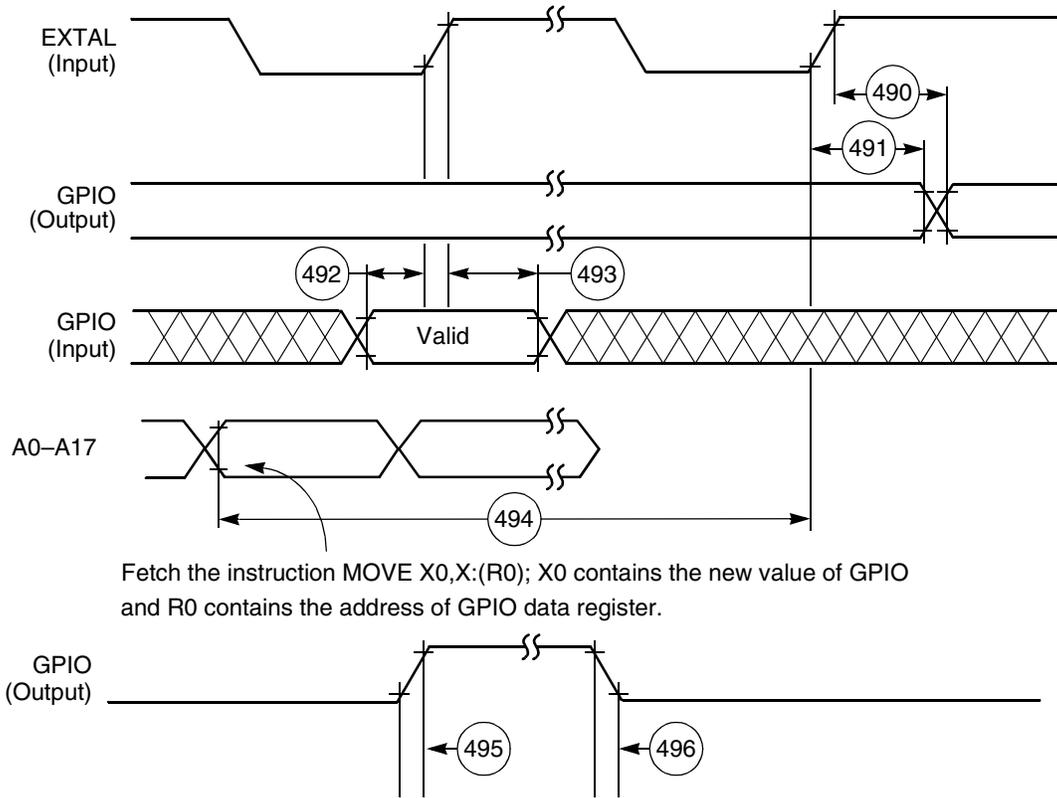


Figure 3-38 GPIO Timing

3.18 JTAG Timing

Table 3-23 JTAG Timing^{1, 2}

| No. | Characteristics | All frequencies | | Unit |
|-----|---|-----------------|------|------|
| | | Min | Max | |
| 500 | TCK frequency of operation ($1/(T_C \times 3)$; maximum 22 MHz) | 0.0 | 22.0 | MHz |
| 501 | TCK cycle time in Crystal mode | 45.0 | — | ns |
| 502 | TCK clock pulse width measured at 1.5 V | 20.0 | — | ns |
| 503 | TCK rise and fall times | 0.0 | 3.0 | ns |
| 504 | Boundary scan input data setup time | 5.0 | — | ns |
| 505 | Boundary scan input data hold time | 24.0 | — | ns |
| 506 | TCK low to output data valid | 0.0 | 40.0 | ns |
| 507 | TCK low to output high impedance | 0.0 | 40.0 | ns |
| 508 | TMS, TDI data setup time | 5.0 | — | ns |

Table 3-23 JTAG Timing^{1, 2} (continued)

| No. | Characteristics | All frequencies | | Unit |
|-----|-------------------------------|-----------------|------|------|
| | | Min | Max | |
| 509 | TMS, TDI data hold time | 25.0 | — | ns |
| 510 | TCK low to TDO data valid | 0.0 | 44.0 | ns |
| 511 | TCK low to TDO high impedance | 0.0 | 44.0 | ns |

¹ $V_{CC} = 1.8\text{ V} \pm 0.09\text{ V}$; $T_J = -40^\circ\text{C}$ to $+95^\circ\text{C}$, $C_L = 50\text{ pF}$

² All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

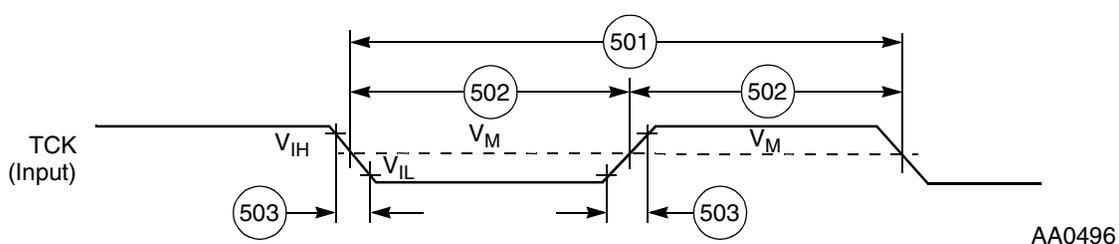


Figure 3-39 Test Clock Input Timing Diagram

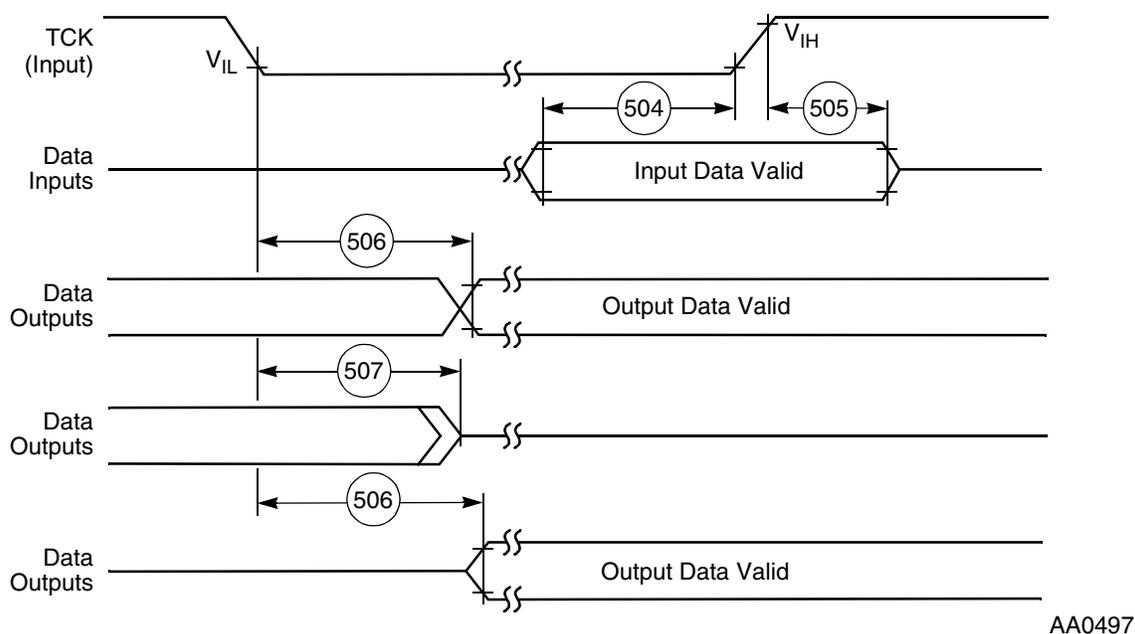


Figure 3-40 Boundary Scan (JTAG) Timing Diagram

JTAG Timing

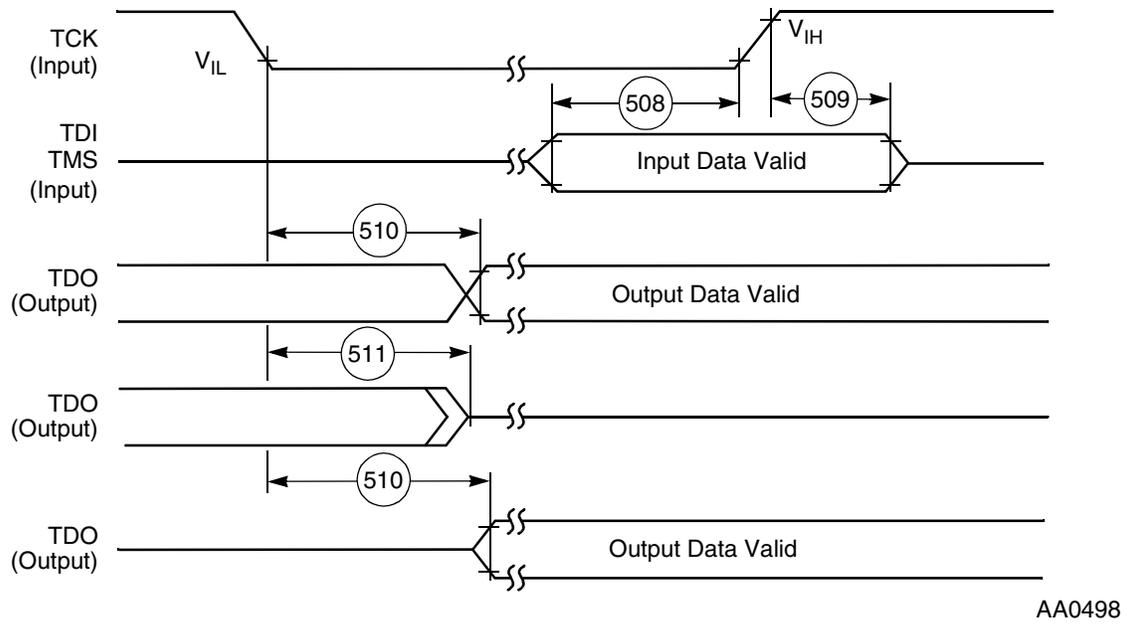


Figure 3-41 Test Access Port Timing Diagram

4 Packaging

4.1 Pin-out and Package Information

This section provides information about the available package for this product, including diagrams of the package pinouts and tables describing how the signals described in **Section 1** are allocated for the package. The DSP56367 is available in a 144-pin LQFP package. [Table 4-1](#) and [Table 4-2](#) show the pin/name assignments for the packages.

4.1.1 LQFP Package Description

Top view of the 144-pin LQFP package is shown in [Figure 4-1](#) with its pin-outs. The package drawing is shown in [Figure 4-2](#).

Pin-out and Package Information

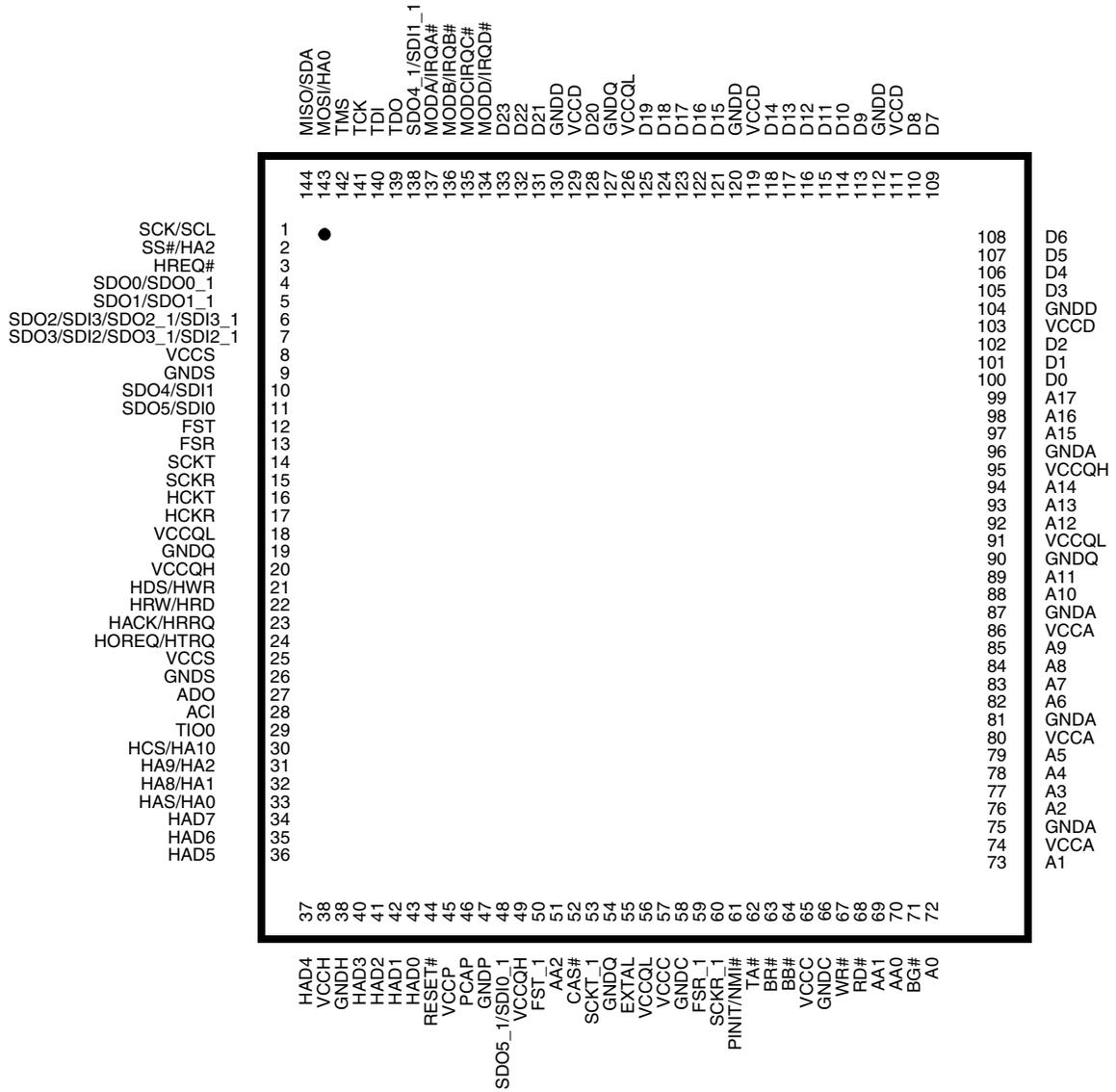


Figure 4-1 144-pin package

Table 4-1 Signal Identification by Name

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|-------------|---------|-------------|---------|-------------|---------|-------------------------|---------|
| A0 | 72 | D9 | 113 | GNDS | 9 | SDO0/SDO0_1 | 4 |
| A1 | 73 | D10 | 114 | GNDS | 26 | SDO1/SDO1_1 | 5 |
| A2 | 76 | D11 | 115 | HA8/HA1 | 32 | SDO2/SDI3/SDO2_1/SDI3_1 | 6 |
| A3 | 77 | D12 | 116 | HA9/HA2 | 31 | SDO3/SDI2/SDO3_1/SDI2_1 | 7 |
| A4 | 78 | D13 | 117 | HACK/HRRQ | 23 | SDO4/SDI1 | 10 |
| A5 | 79 | D14 | 118 | HAD0 | 43 | SDO4_1/SDI1_1 | 138 |
| A6 | 82 | D15 | 121 | HAD1 | 42 | SDO5/SDI0 | 11 |
| A7 | 83 | D16 | 122 | HAD2 | 41 | SDO5_1/SDI0_1 | 48 |
| A8 | 84 | D17 | 123 | HAD3 | 40 | SS#/HA2 | 2 |
| A9 | 85 | D18 | 124 | HAD4 | 37 | TA# | 62 |
| A10 | 88 | D19 | 125 | HAD5 | 36 | TCK | 141 |
| A11 | 89 | D20 | 128 | HAD6 | 35 | TDI | 140 |
| A12 | 92 | D21 | 131 | HAD7 | 34 | TDO | 139 |
| A13 | 93 | D22 | 132 | HAS/HA0 | 33 | TIO0 | 29 |
| A14 | 94 | D23 | 133 | HCKR | 17 | TMS | 142 |
| A15 | 97 | EXTAL | 55 | HCKT | 16 | VCCA | 74 |
| A16 | 98 | FSR | 13 | HCS/HA10 | 30 | VCCA | 80 |
| A17 | 99 | FSR_1 | 59 | HDS/HWR | 21 | VCCA | 86 |
| AA0 | 70 | FST | 12 | HOREQ/HTRQ | 24 | VCCC | 57 |
| AA1 | 69 | FST_1 | 50 | HREQ# | 3 | VCCC | 65 |
| AA2 | 51 | GNDA | 75 | HRW/HRD | 22 | VCCD | 103 |
| ACI | 28 | GNDA | 81 | MODA/IRQA# | 137 | VCCD | 111 |
| ADO | 27 | GNDA | 87 | MODB/IRQB# | 136 | VCCD | 119 |
| BB# | 64 | GNDA | 96 | MODC/IRQC# | 135 | VCCD | 129 |
| BG# | 71 | GNDG | 58 | MODD/IRQD# | 134 | VCCH | 38 |
| BR# | 63 | GNDG | 66 | MISO/SDA | 144 | VCCQH | 20 |
| CAS# | 52 | GNDD | 104 | MOSI/HA0 | 143 | VCCQH | 95 |
| D0 | 100 | GNDD | 112 | PCAP | 46 | VCCQH | 49 |
| D1 | 101 | GNDD | 120 | PINIT/NMI# | 61 | VCCQL | 18 |
| D2 | 102 | GNDD | 130 | RD# | 68 | VCCQL | 56 |
| D3 | 105 | GNDH | 39 | RESET# | 44 | VCCQL | 91 |
| D4 | 106 | GNDP | 47 | SCK/SCL | 1 | VCCQL | 126 |
| D5 | 107 | GNDQ | 19 | SCKR | 15 | VCCP | 45 |
| D6 | 108 | GNDQ | 54 | SCKR_1 | 60 | VCCS | 8 |
| D7 | 109 | GNDQ | 90 | SCKT | 14 | VCCS | 25 |
| D8 | 110 | GNDQ | 127 | SCKT_1 | 53 | WR# | 67 |

Table 4-2 Signal Identification by Pin Number

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|-------------------------|---------|---------------|---------|-------------|---------|---------------|
| 1 | SCK/SCL | 37 | HAD4 | 73 | A1 | 109 | D7 |
| 2 | SS#/HA2 | 38 | VCCH | 74 | VCCA | 110 | D8 |
| 3 | HREQ# | 39 | GNDH | 75 | GNDA | 111 | VCCD |
| 4 | SDO0/SDO0_1 | 40 | HAD3 | 76 | A2 | 112 | GNDD |
| 5 | SDO1/SDO1_1 | 41 | HAD2 | 77 | A3 | 113 | D9 |
| 6 | SDO2/SDI3/SDO2_1/SDI3_1 | 42 | HAD1 | 78 | A4 | 114 | D10 |
| 7 | SDO3/SDI2/SDO3_1/SDI2_1 | 43 | HAD0 | 79 | A5 | 115 | D11 |
| 8 | VCCS | 44 | RESET# | 80 | VCCA | 116 | D12 |
| 9 | GNDS | 45 | VCCP | 81 | GNDA | 117 | D13 |
| 10 | SDO4/SDI1 | 46 | PCAP | 82 | A6 | 118 | D14 |
| 11 | SDO5/SDI0 | 47 | GNDP | 83 | A7 | 119 | VCCD |
| 12 | FST | 48 | SDO5_1/SDI0_1 | 84 | A8 | 120 | GNDD |
| 13 | FSR | 49 | VCCQH | 85 | A9 | 121 | D15 |
| 14 | SCKT | 50 | FST_1 | 86 | VCCA | 122 | D16 |
| 15 | SCKR | 51 | AA2 | 87 | GNDA | 123 | D17 |
| 16 | HCKT | 52 | CAS# | 88 | A10 | 124 | D18 |
| 17 | HCKR | 53 | SCKT_1 | 89 | A11 | 125 | D19 |
| 18 | VCCQL | 54 | GNDQ | 90 | GNDQ | 126 | VCCQL |
| 19 | GNDQ | 55 | EXTAL | 91 | VCCQL | 127 | GNDQ |
| 20 | VCCQH | 56 | VCCQL | 92 | A12 | 128 | D20 |
| 21 | HDS/HWR | 57 | VCCC | 93 | A13 | 129 | VCCD |
| 22 | HRW/HRD | 58 | GNDC | 94 | A14 | 130 | GNDD |
| 23 | HACK/HRRQ | 59 | FSR_1 | 95 | VCCQH | 131 | D21 |
| 24 | HOREQ/HTRQ | 60 | SCKR_1 | 96 | GNDA | 132 | D22 |
| 25 | VCCS | 61 | PINIT/NMI# | 97 | A15 | 133 | D23 |
| 26 | GNDS | 62 | TA# | 98 | A16 | 134 | MODD/IRQD# |
| 27 | ADO | 63 | BR# | 99 | A17 | 135 | MODC/IRQC# |
| 28 | ACI | 64 | BB# | 100 | D0 | 136 | MODB/IRQB# |
| 29 | TIO0 | 65 | VCCC | 101 | D1 | 137 | MODA/IRQA# |
| 30 | HCS/HA10 | 66 | GNDC | 102 | D2 | 138 | SDO4_1/SDI1_1 |
| 31 | HA9/HA2 | 67 | WR# | 103 | VCCD | 139 | TDO |
| 32 | HA8/HA1 | 68 | RD# | 104 | GNDD | 140 | TDI |
| 33 | HAS/HA0 | 69 | AA1 | 105 | D3 | 141 | TCK |
| 34 | HAD7 | 70 | AA0 | 106 | D4 | 142 | TMS |
| 35 | HAD6 | 71 | BG# | 107 | D5 | 143 | MOSI/HA0 |
| 36 | HAD5 | 72 | A0 | 108 | D6 | 144 | MISO/SDA |

4.1.2 LQFP Package Mechanical Drawing

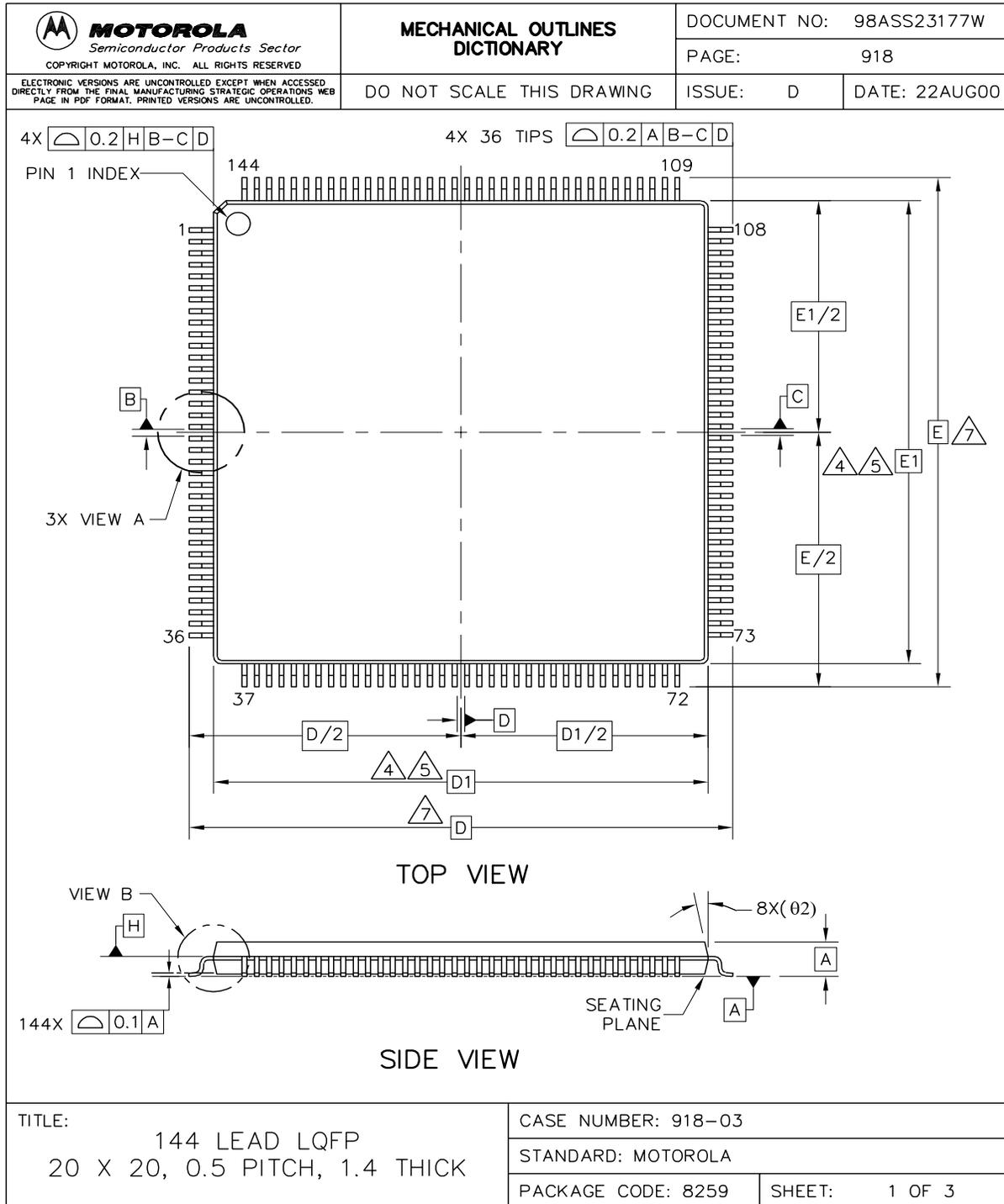


Figure 4-2 DSP56367 144-pin LQFP Package (1 of 3)

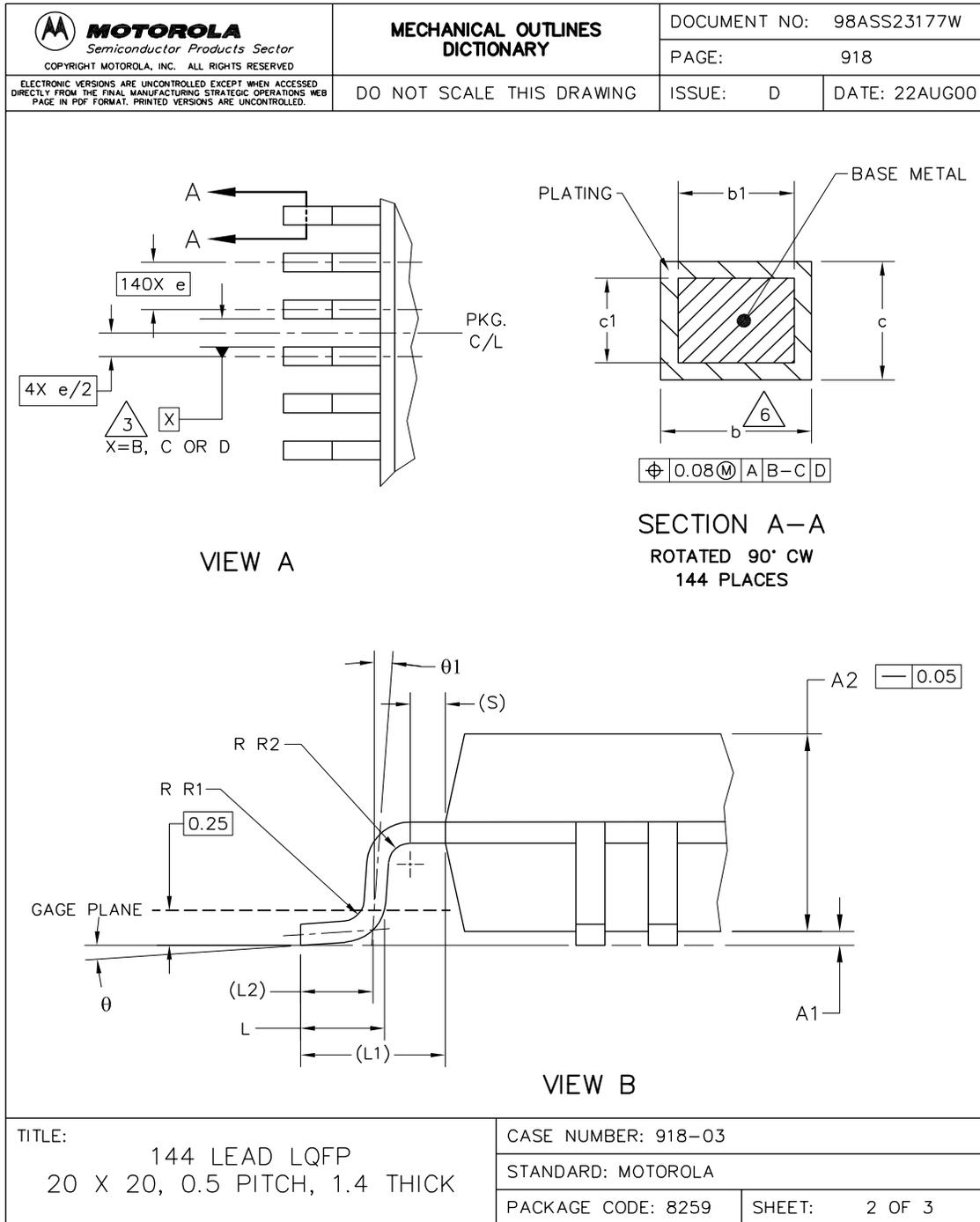


Figure 4-3 DSP56367 144-pin LQFP Package (2 of 3)

| | | | | | | | | | | | |
|---|------|--|-----|--------------------------|---------------|--------------------|-----|--------------------|--|---------------|--|
|  MOTOROLA Semiconductor Products Sector COPYRIGHT MOTOROLA, INC. ALL RIGHTS RESERVED | | MECHANICAL OUTLINES DICTIONARY | | DOCUMENT NO: 98ASS23177W | | | | | | | |
| <small>ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE FINAL MANUFACTURING STRATEGIC OPERATIONS WEB PAGE IN PDF FORMAT. PRINTED VERSIONS ARE UNCONTROLLED.</small> | | DO NOT SCALE THIS DRAWING | | ISSUE: D | DATE: 22AUG00 | | | | | | |
| <p>NOTES:</p> <ol style="list-style-type: none"> 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994. 3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H. 4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm. 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH. 6. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM. 7. DIMENSIONS D AND E ARE DETERMINED AT THE SEATING PLANE, DATUM A. | | | | | | | | | | | |
| DIM | MIN | MAX | DIM | MIN | MAX | DIM | MIN | MAX | | | |
| A | - | - 1.6 | L1 | - 1 REF | - | - | - | - | | | |
| A1 | 0.05 | - 0.15 | L2 | - 0.5 REF | - | - | - | - | | | |
| A2 | 1.35 | - 1.45 | R1 | 0.13 | - 0.2 | - | - | - | | | |
| b | 0.17 | - 0.27 | R2 | 0.13 | - | - | - | - | | | |
| b1 | 0.17 | - 0.23 | S | - 0.25 REF | - | - | - | - | | | |
| c | 0.09 | - 0.20 | θ | 0° | - 7° | - | - | - | | | |
| c1 | 0.09 | - 0.16 | θ1 | 0° | - | - | - | - | | | |
| D | - | 22 BSC | θ2 | - 12° REF | - | - | - | - | | | |
| D1 | - | 20 BSC | - | - | - | - | - | - | | | |
| e | - | 0.5 BSC | - | - | - | - | - | - | | | |
| E | - | 22 BSC | - | - | - | - | - | - | | | |
| E1 | - | 20 BSC | - | - | - | - | - | - | | | |
| L | 0.45 | - 0.75 | - | - | - | - | - | - | | | |
| TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK | | | | CASE NUMBER: 918-03 | | STANDARD: MOTOROLA | | PACKAGE CODE: 8259 | | SHEET: 3 OF 3 | |

Figure 4-4 DSP56367 144-pin LQFP Package (3 of 3)

5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J , in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

- T_A = ambient temperature °C
- $R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
- P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

- $R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
- $R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
- $R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation: $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT} , has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Electrical Design Considerations

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pull-up or pull-down resistor is 10 k ohm.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 μF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQD}}$, and $\overline{\text{TA}}$ pins. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors (TMS, $\overline{\text{TDI}}$, TCK).
- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple DSP56367 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal must be supplied before deassertion of RESET.
- At power-up, ensure that the voltage difference between the 3.3 V tolerant pins and the chip V_{CC} never exceeds a TBD voltage.

5.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

where:

- C = node/pin capacitance
- V = voltage swing
- f = frequency of node/pin toggle

Example 1. Power Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 100 MHz clock, toggling at its maximum possible rate (50 MHz), the current consumption is

$$I = 50 \times 10^{-12} \times 3.3 \times 50 \times 10^6 = 8.25\text{mA}$$

The maximum internal current ($I_{CC1\text{max}}$) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current ($I_{CC1\text{typ}}$) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.

PLL Performance Issues

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in [Appendix A, "Power Consumption Benchmark"](#). Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$I/\text{MIPS} = I/\text{MHz} = (I_{\text{typF2}} - I_{\text{typF1}})/(F2 - F1)$$

where:

I_{typF2} = current at F2

I_{typF1} = current at F1

F2 = high frequency (any specified operating frequency)

F1 = low frequency (any specified operating frequency lower than F2)

NOTE

F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

5.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

5.4.1 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

Appendix A Power Consumption Benchmark

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;*****;*****
;* ;* CHECKS   Typical Power Consumption
;*****

        page      200,55,0,0,0
        nolist

I_VEC EQU $000000    ; Interrupt vectors for program debug only
START EQU $8000      ; MAIN (external) program starting address
INT_PROG EQU $100    ; INTERNAL program memory starting address
INT_XDAT EQU $0      ; INTERNAL X-data memory starting address
INT_YDAT EQU $0      ; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "integu.asm"

        list

        org       P:START

;
        movewp #0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Default: 1 w.s (SRAM)
;
        movewp #0d0000,x:M_PCTL          ; XTAL disable
                                   ; PLL enable
                                   ; CLKOUT disable
;
; Load the program
;
        move     #INT_PROG,r0
        move     #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move     p:(r1)+,x0
        move     x0,p:(r0)+
        nop
PLOAD_LOOP
;
; Load the X-data
;
        move     #INT_XDAT,r0
        move     #XDAT_START,r1
```

```

        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
        clr     b
        move    #$0,x0
        move    #$0,x1
        move    #$0,y0
        move    #$0,y1
        bset    #4,omr           ; ebd
;
sbr      dor     #60,_end
        mac     x0,y0,a    x:(r0)+,x1      y:(r4)+,y1
        mac     x1,y1,a    x:(r0)+,x0      y:(r4)+,y0
        add     a,b
        mac     x0,y0,a    x:(r0)+,x1
        mac     x1,y1,a    y:(r4)+,y0
        move    b1,x:$ff
_end
        bra     sbr
        nop
        nop
        nop
        nop
PROG_END
        nop
        nop

XDAT_START
;
        org     x:0
        dc     $262EB9
        dc     $86F2FE
        dc     $E56A5F
        dc     $616CAC

```

dc \$8FFD75
dc \$9210A
dc \$A06D7B
dc \$CEA798
dc \$8DFBF1
dc \$A063D6
dc \$6C6657
dc \$C2A544
dc \$A3662D
dc \$A4E762
dc \$84F0F3
dc \$E6F1B0
dc \$B3829
dc \$8BF7AE
dc \$63A94F
dc \$EF78DC
dc \$242DE5
dc \$A3E0BA
dc \$EBAB6B
dc \$8726C8
dc \$CA361
dc \$2F6E86
dc \$A57347
dc \$4BE774
dc \$8F349D
dc \$A1ED12
dc \$4BFCE3
dc \$EA26E0
dc \$CD7D99
dc \$4BA85E
dc \$27A43F
dc \$A8B10C
dc \$D3A55
dc \$25EC6A
dc \$2A255B
dc \$A5F1F8
dc \$2426D1
dc \$AE6536
dc \$CBBC37
dc \$6235A4
dc \$37F0D
dc \$63BEC2
dc \$A5E4D3
dc \$8CE810
dc \$3FF09
dc \$60E50E
dc \$CFFB2F
dc \$40753C
dc \$8262C5
dc \$CA641A
dc \$EB3B4B
dc \$2DA928
dc \$AB6641
dc \$28A7E6
dc \$4E2127

```
dc      $482FD4
dc      $7257D
dc      $E53C72
dc      $1A8C3
dc      $E27540
```

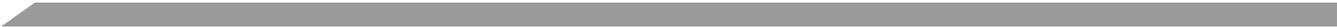
XDAT_END

YDAT_START

```
;      org      y:0
dc      $5B6DA
dc      $C3F70B
dc      $6A39E8
dc      $81E801
dc      $C666A6
dc      $46F8E7
dc      $AAEC94
dc      $24233D
dc      $802732
dc      $2E3C83
dc      $A43E00
dc      $C2B639
dc      $85A47E
dc      $ABFDDF
dc      $F3A2C
dc      $2D7CF5
dc      $E16A8A
dc      $ECB8FB
dc      $4BED18
dc      $43F371
dc      $83A556
dc      $E1E9D7
dc      $ACA2C4
dc      $8135AD
dc      $2CE0E2
dc      $8F2C73
dc      $432730
dc      $A87FA9
dc      $4A292E
dc      $A63CCF
dc      $6BA65C
dc      $E06D65
dc      $1AA3A
dc      $A1B6EB
dc      $48AC48
dc      $EF7AE1
dc      $6E3006
dc      $62F6C7
dc      $6064F4
dc      $87E41D
dc      $CB2692
dc      $2C3863
dc      $C6BC60
dc      $43A519
dc      $6139DE
dc      $ADF7BF
```

dc \$4B3E8C
dc \$6079D5
dc \$E0F5EA
dc \$8230DB
dc \$A3B778
dc \$2BFE51
dc \$E0A6B6
dc \$68FFB7
dc \$28F324
dc \$8F2E8D
dc \$667842
dc \$83E053
dc \$A1FD90
dc \$6B2689
dc \$85B68E
dc \$622EAF
dc \$6162BC
dc \$E4A245

YDAT_END



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