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# FDP2D3N10C / FDPF2D3N10C

## N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 222 A, 2.3 mΩ

### Features

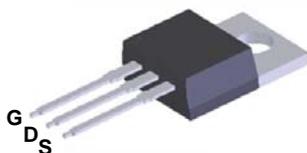
- Max  $r_{DS(on)}$  = 2.3 mΩ at  $V_{GS} = 10$  V,  $I_D = 100$  A
- Extremely Low Reverse Recovery Charge, Qrr
- 100% UIL Tested
- RoHS Compliant

### General Description

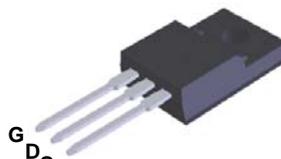
This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Applications

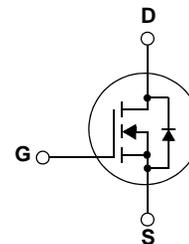
- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



TO-220



TO-220F



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings		Units
		FDP2D3N10C	FDPF2D3N10C	
$V_{DS}$	Drain to Source Voltage	100	100	V
$V_{GS}$	Gate to Source Voltage	±20	±20	V
$I_D$	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 3)	222*	222*	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 3)	157*	157*	
	-Pulsed (Note 1)	888	888	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	1176		mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	214	45	W
	Power Dissipation $T_A = 25^\circ\text{C}$	2.4	2.4	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175		°C

\* Drain current limited by maximum junction temperature. Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	FDP2D3N10C	FDPF2D3N10C	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.7	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

### Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Quantity
FDP2D3N10C	FDP2D3N10C	TO-220	Tube	50 units
FDPF2D3N10C	FDPF2D3N10C	TO-220F	Tube	50 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		70		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 80\text{ V}, T_J = 150\text{ }^\circ\text{C}$			1 500	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 700\text{ }\mu\text{A}$	2.0	3.0	4.0	V
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		2.1	2.3	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 100\text{ A}$		222		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		7980	11180	pF
$C_{oss}$	Output Capacitance			4490	6290	pF
$C_{rss}$	Reverse Transfer Capacitance			40	75	pF
$R_g$	Gate Resistance		0.1	0.8	1.8	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 100\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		42	67	ns
$t_r$	Rise Time			35	56	ns
$t_{d(off)}$	Turn-Off Delay Time			74	118	ns
$t_f$	Fall Time			32	57	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$ $V_{DD} = 50\text{ V},$ $I_D = 100\text{ A}$		108	152	nC
$Q_{gs}$	Gate to Source Gate Charge			36		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			22		nC
$Q_{oss}$	Output Charge	$V_{DD} = 50\text{ V}, V_{GS} = 0\text{ V}$		297		nC

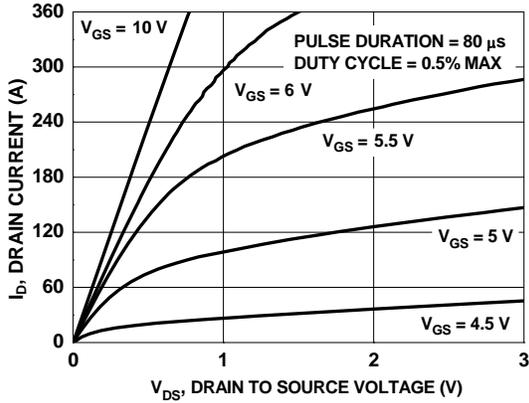
**Drain-Source Diode Characteristic**

$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	222	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	888	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 100\text{ A}$		0.9	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V},$ $I_F = 100\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$		107	172	ns
$Q_{rr}$	Reverse Recovery Charge			191	306	nC
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V},$ $I_F = 100\text{ A}, di_F/dt = 300\text{ A}/\mu\text{s}$		97	155	ns
$Q_{rr}$	Reverse Recovery Charge			492	788	nC

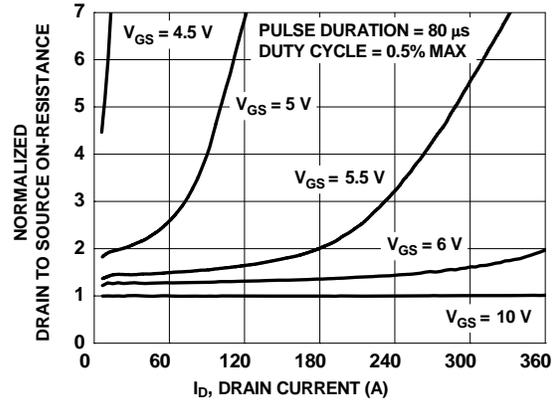
Notes:

1. Pulsed  $I_D$  please refer to Figure.11 and Figure.12 "Forward Bias Safe Operating Area" for more details.
2.  $E_{AS}$  of 1176 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 28\text{ A}$ ,  $V_{DD} = 90\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 89\text{ A}$ .
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

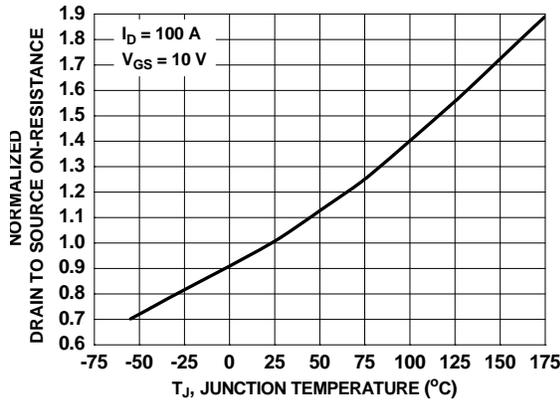
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



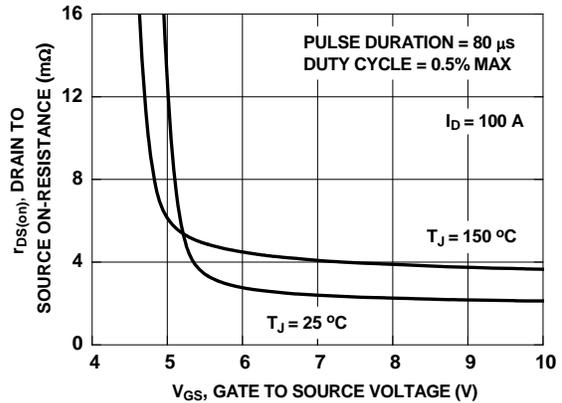
**Figure 1. On-Region Characteristics**



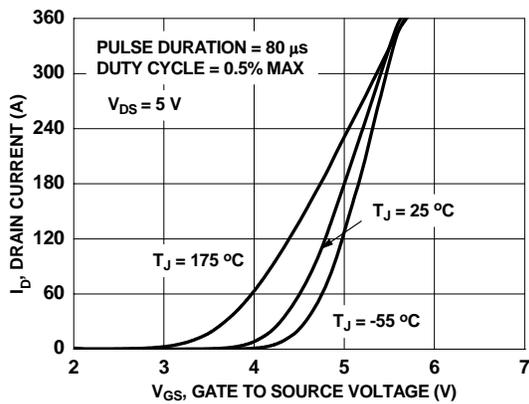
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



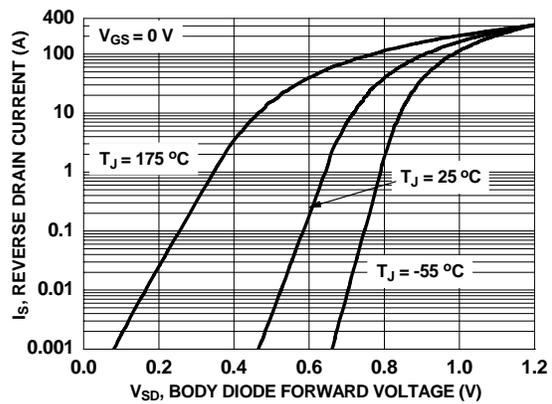
**Figure 3. Normalized On-Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

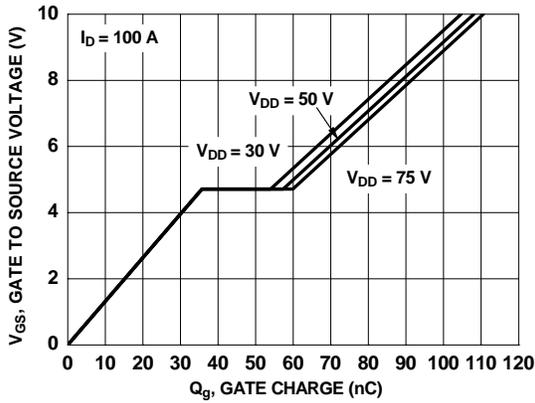


Figure 7. Gate Charge Characteristics

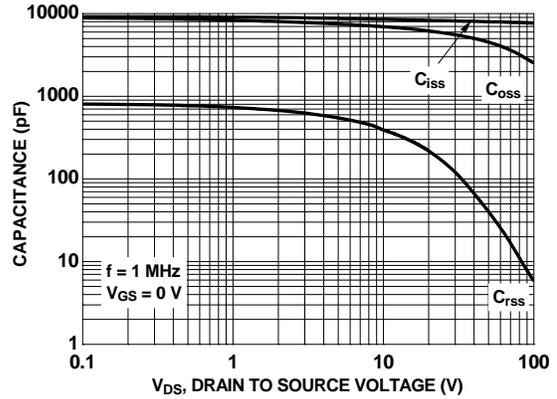


Figure 8. Capacitance vs. Drain to Source Voltage

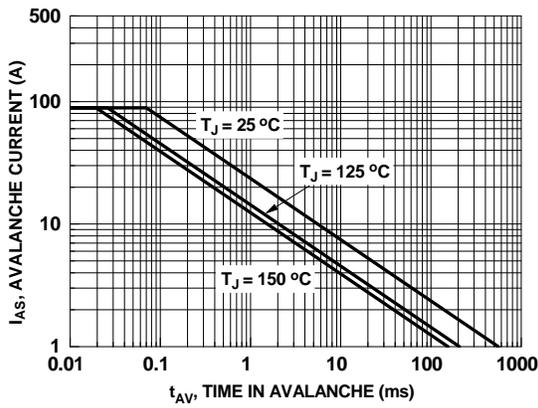


Figure 9. Unclamped Inductive Switching Capability

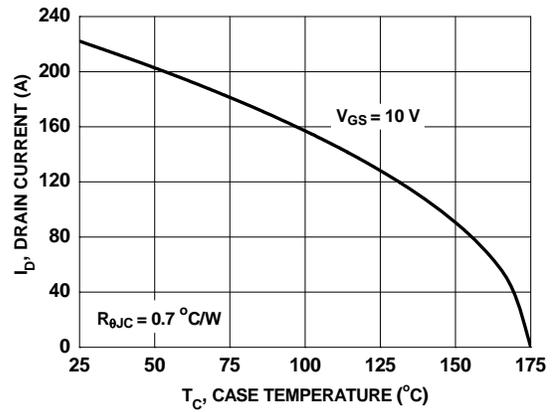


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

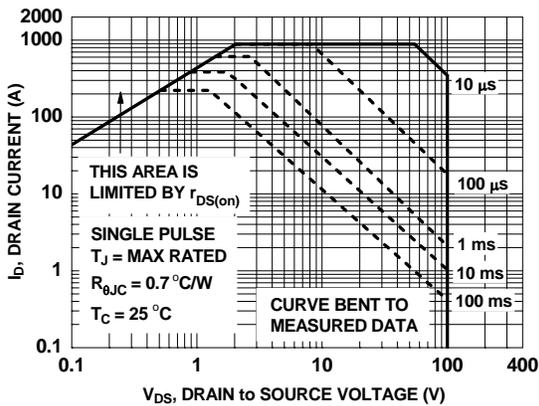


Figure 11. Forward Bias Safe Operating Area for FDP2D3N10C

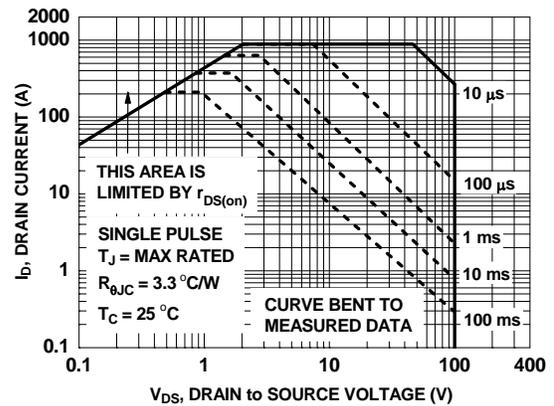
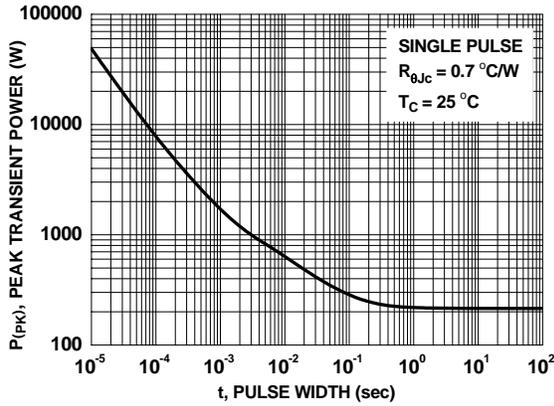
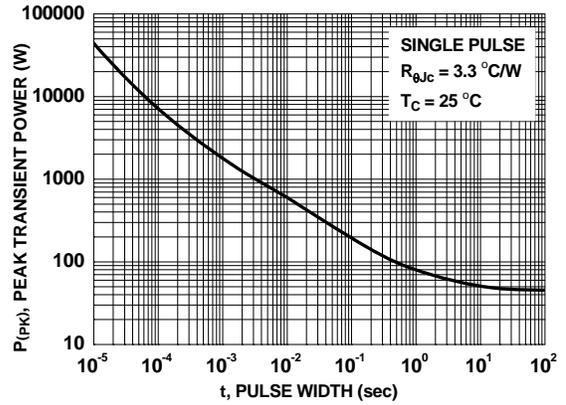


Figure 12. Forward Bias Safe Operating Area for FDPF2D3N10C

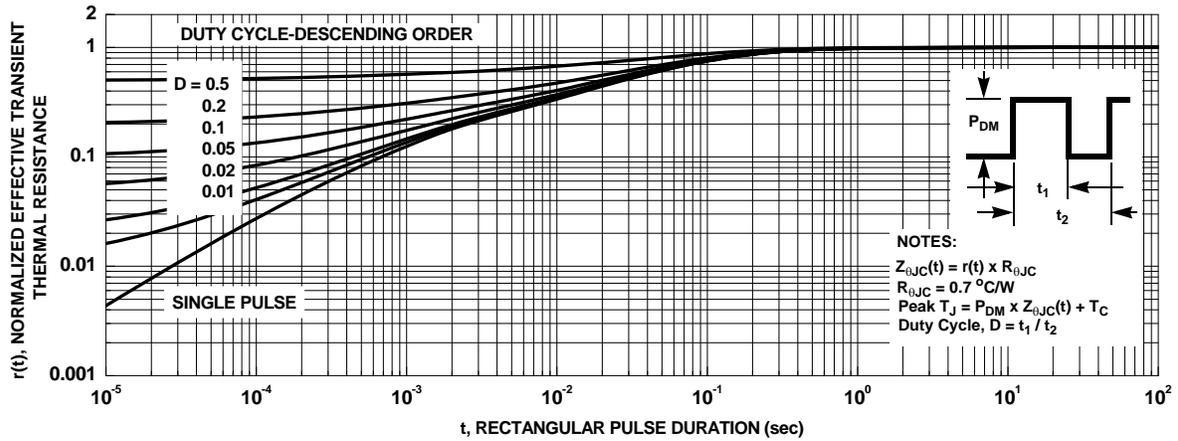
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



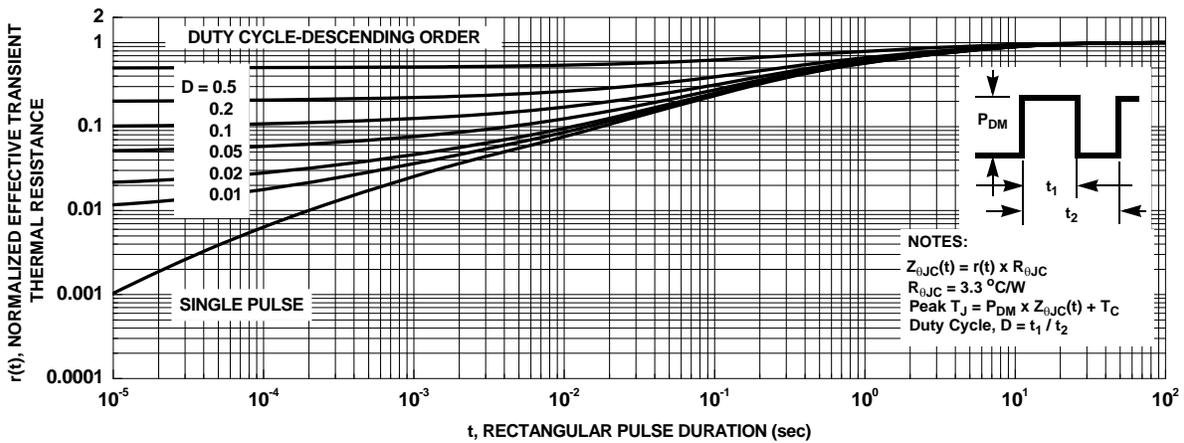
**Figure 13. Single Pulse Maximum Power Dissipation for FDP2D3N10C**



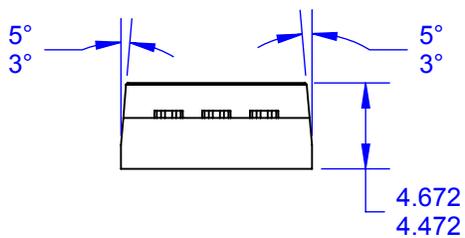
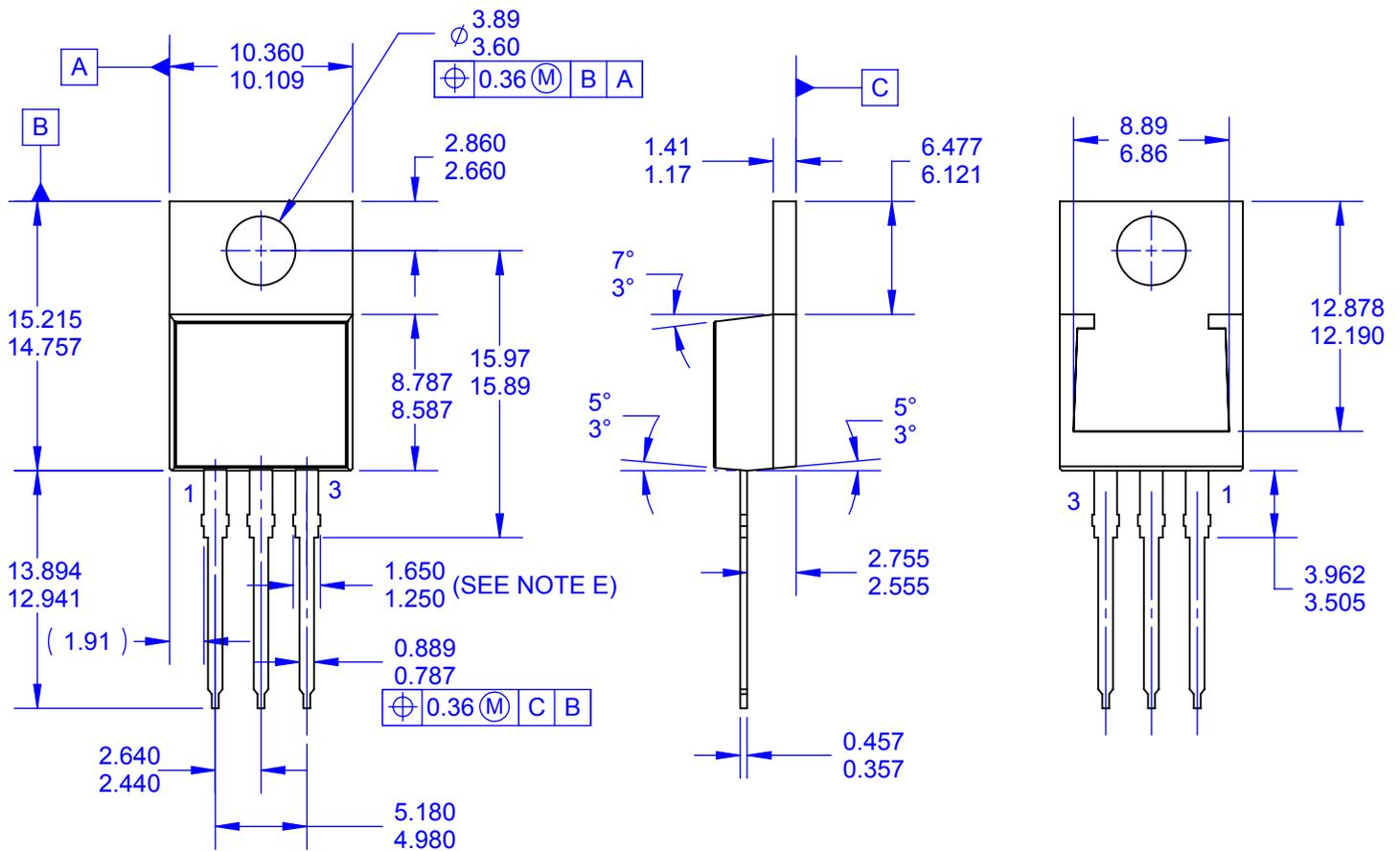
**Figure 14. Single Pulse Maximum Power Dissipation for FDPF2D3N10C**



**Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP2D3N10C**

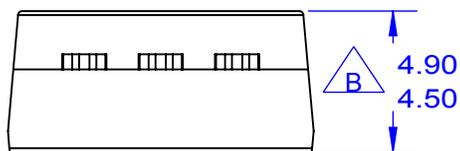
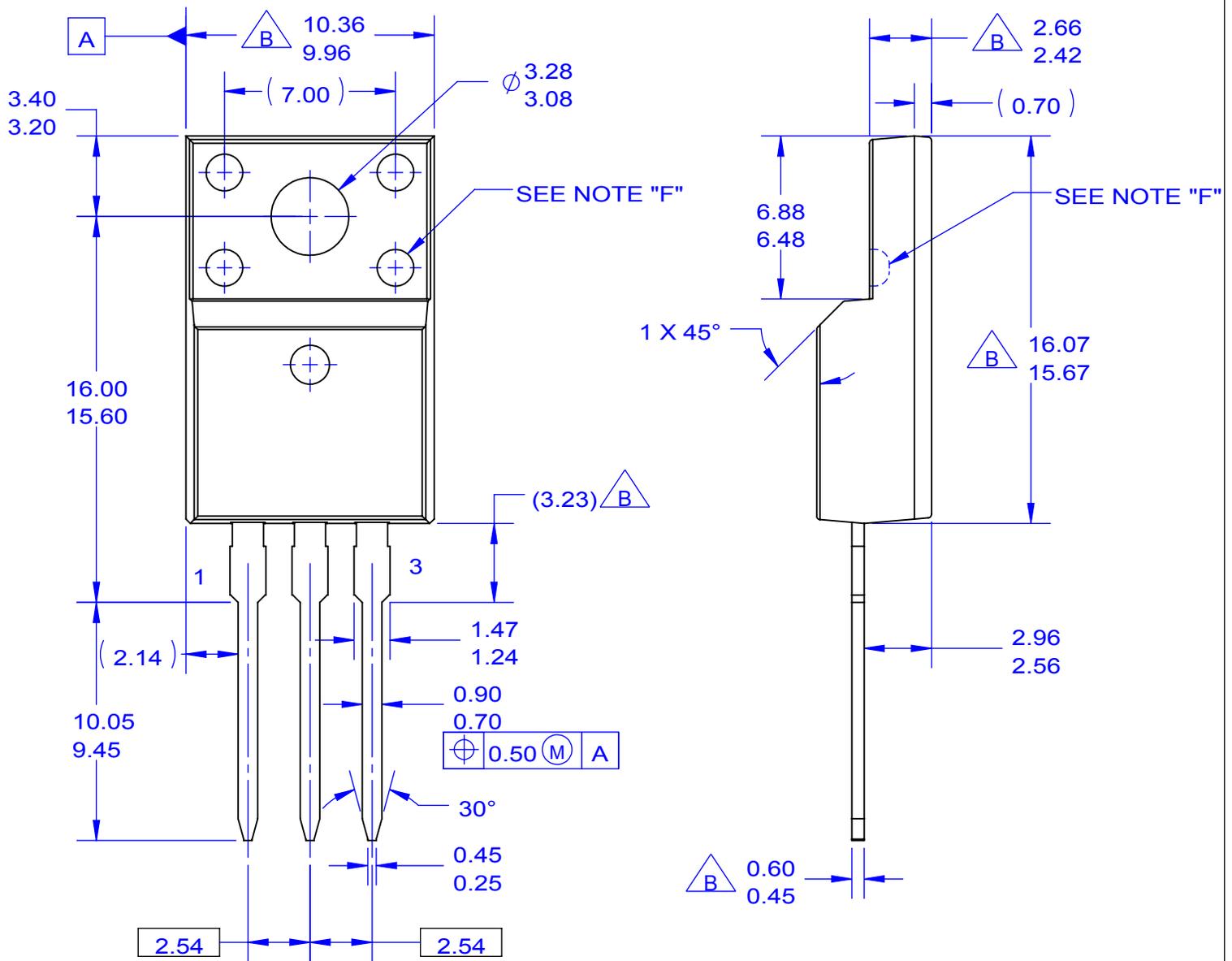


**Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF2D3N10C**



**NOTES:**

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm.
- F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.



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NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV5

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