



ON Semiconductor®

# FDS8449

## 40V N-Channel PowerTrench® MOSFET

### General Description

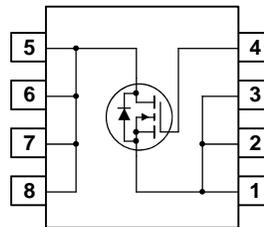
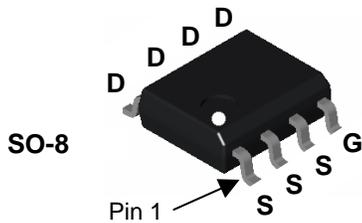
These N-Channel MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

### Application

- Inverter
- Power Supplies

### Features

- 7.6 A, 40V  $R_{DS(on)} = 29m\Omega @ V_{GS} = 10V$   
 $R_{DS(on)} = 36m\Omega @ V_{GS} = 4.5V$
- High power handling capability in a widely used surface mount package
- RoHS compliant



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Rated	Units
V <sub>DSS</sub>	Drain-Source Voltage	40	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	7.6	A
	– Pulsed	50	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b)	2.5	W
		1	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1b)	125	
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	25	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8449	FDS8449	13"	12mm	2500 units

FDS8449 40V N-Channel PowerTrench® MOSFET

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Drain-Source Avalanche Ratings (Note 3)

$E_{AS}$	Drain-Source Avalanche Energy	$V_{DD} = 40\text{ V}, I_D = 7.3\text{ A}, L = 1\text{ mH}$			27	mJ
$I_{AS}$	Drain-Source Avalanche Current			7.3		A

### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		34		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 7.6\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 6.8\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 7.6\text{ A}, T_J = 125^\circ\text{C}$		21 26 29	29 36 43	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 7.6\text{ A}$		21		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V},$		760		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		100		pF
$C_{rss}$	Reverse Transfer Capacitance			60		pF
$R_G$	Gate Resistance	$f = 1.0\text{ MHz}$		1.2		$\Omega$

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}, I_D = 1\text{ A},$		9	18	ns
$t_r$	Turn-On Rise Time	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	17	ns
$t_f$	Turn-Off Fall Time			3	6	ns
$Q_g$	Total Gate Charge	$V_{DS} = 20\text{ V}, I_D = 7.6\text{ A},$		7.7	11	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 5\text{ V}$		2.4		nC
$Q_{gd}$	Gate-Drain Charge			2.8		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.76	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 7.6\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		17		nS
$Q_{rr}$	Diode Reverse Recovery Charge			7		nC

#### Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $50^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



- b)  $125^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2 Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%

3. BV(avalanche) Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

## Typical Characteristics

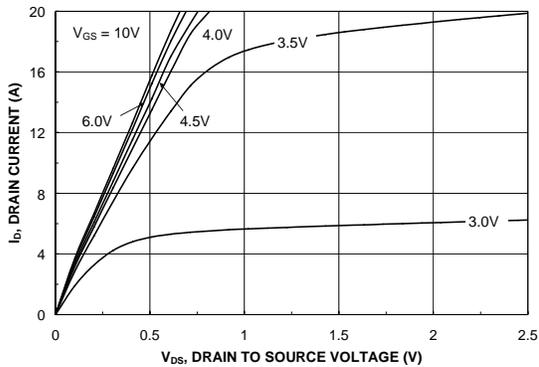


Figure 1. On-Region Characteristics.

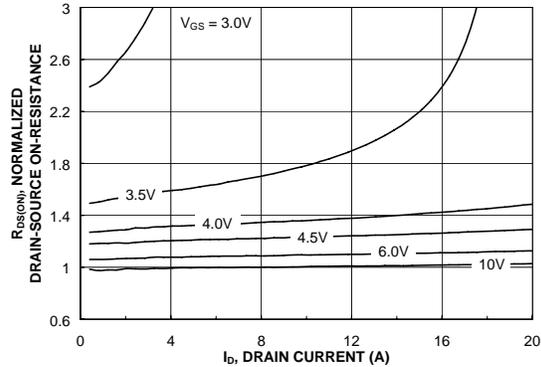


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

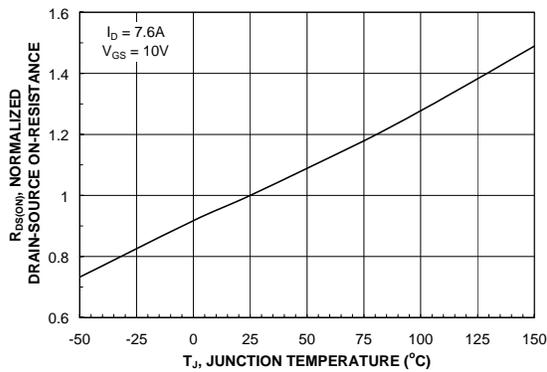


Figure 3. On-Resistance Variation with Temperature.

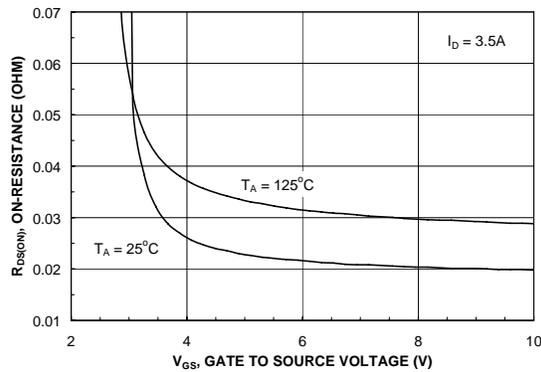


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

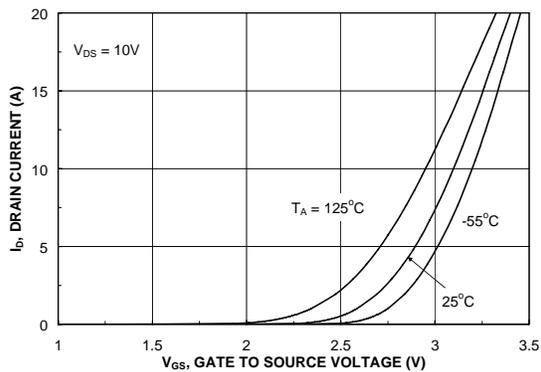


Figure 5. Transfer Characteristics.

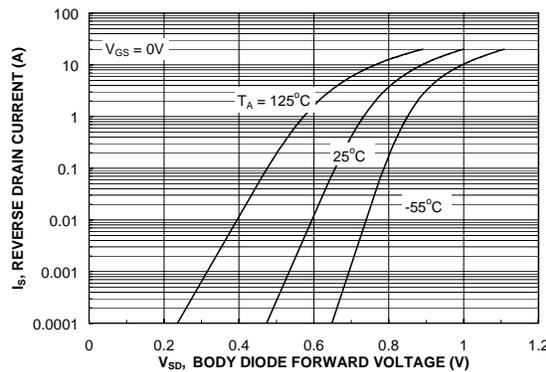


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

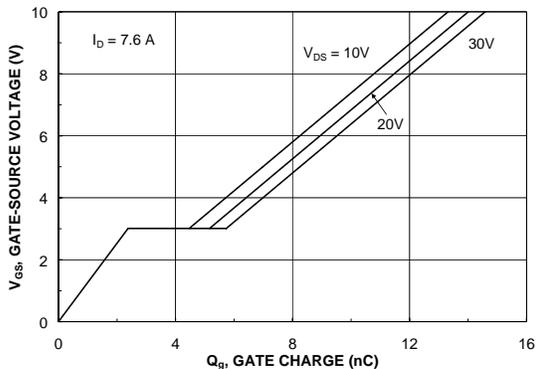


Figure 7. Gate Charge Characteristics.

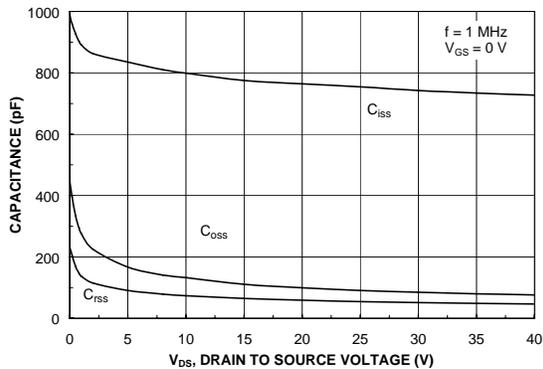


Figure 8. Capacitance Characteristics.

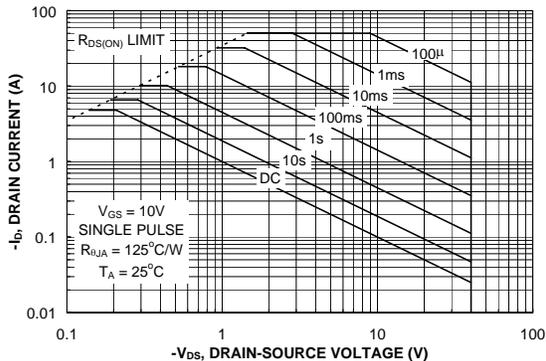


Figure 9. Maximum Safe Operating Area.

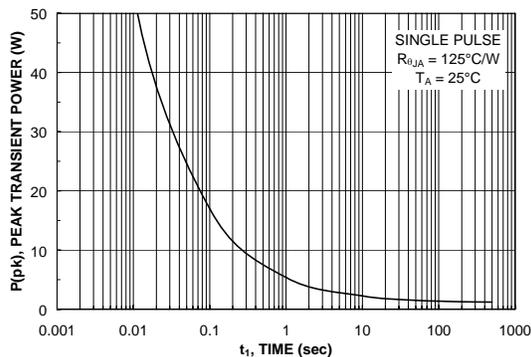


Figure 10. Single Pulse Maximum Power Dissipation.

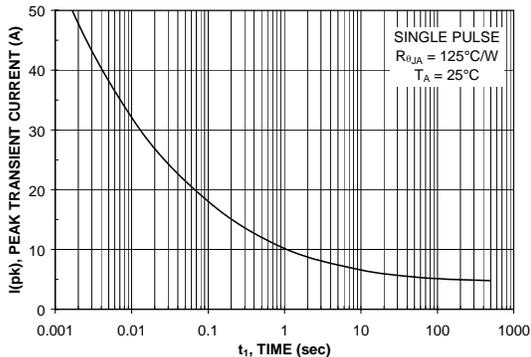


Figure 11. Single Pulse Maximum Peak Current.

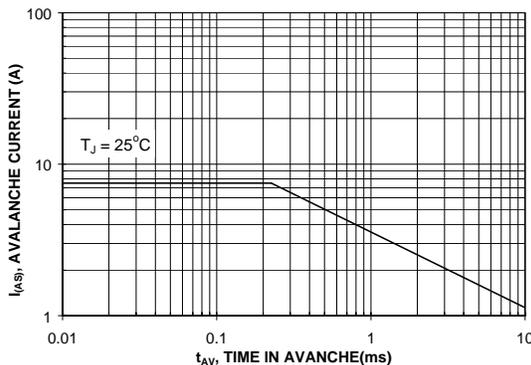
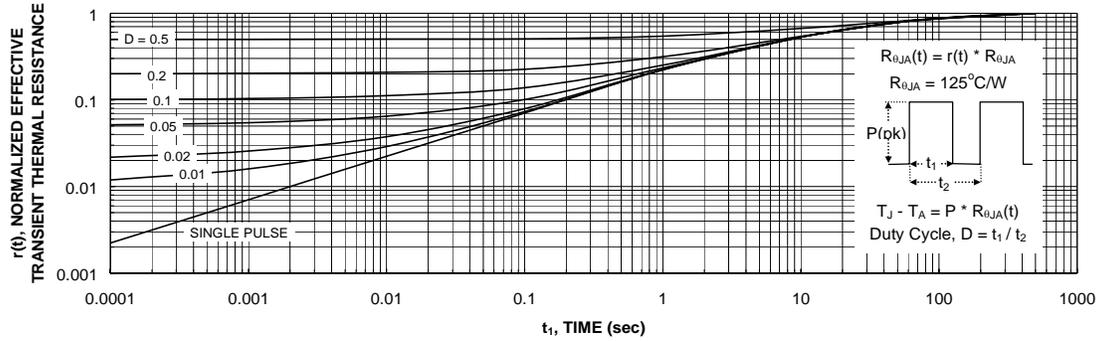


Figure 12. Unclamped Inductive Switching Capability.

## Typical Characteristics



**Figure 25. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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