# MC14022B

# Octal Counter

The MC14022B is a four−stage Johnson octal counter with built−in code converter. High−speed operation and spike−free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive−going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

## Features

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4022B
- Triple Diode Protection on All Inputs
- Pb−Free Packages are Available*

## MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.
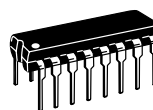
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
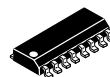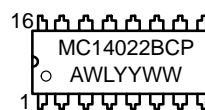
## MARKING DIAGRAMS



PDIP−16
P SUFFIX
CASE 648

MC14022BCP
AWLYYWW

SOIC−16
D SUFFIX
CASE 751B

14022B
AWLYWW

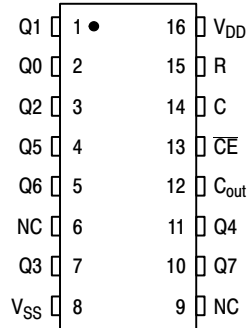| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.
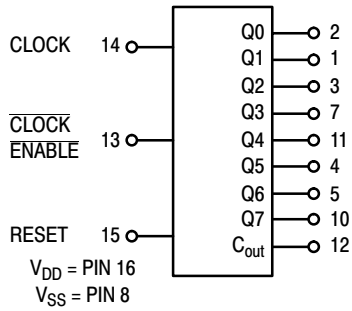
# MC14022B

## PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| Q1 | 1 ● | 16 | $V_{DD}$ |
| Q0 | 2 | 15 | R |
| Q2 | 3 | 14 | C |
| Q5 | 4 | 13 | $\overline{CE}$ |
| Q6 | 5 | 12 | $C_{out}$ |
| NC | 6 | 11 | Q4 |
| Q3 | 7 | 10 | Q7 |
| $V_{SS}$ | 8 | 9 | NC |

NC = NO CONNECTION

## BLOCK DIAGRAM

CLOCK 14 o—

$\overline{CLOCK}$
$\overline{ENABLE}$ 13 o—

RESET 15 o—

Q0 o— 2
Q1 o— 1
Q2 o— 3
Q3 o— 7
Q4 o— 11
Q5 o— 4
Q6 o— 5
Q7 o— 10
$C_{out}$ o— 12

$V_{DD}$ = PIN 16
$V_{SS}$ = PIN 8

NC = PIN 6, 9

## FUNCTIONAL TRUTH TABLE
### (Positive Logic)

| Clock | $\overline{\text{Clock}}$ Enable | Reset | Output=n |
|---|---|---|---|
| 0 | X | 0 | n |
| X | 1 | 0 | n |
| ⌐ | 0 | 0 | n+1 |
| ⌐ | X | 0 | n |
| 1 | ⌐ | 0 | n+1 |
| X | ⌐ | 0 | n |
| X | X | 1 | Q0 |

X = Don't Care. If n < 4 Carry = 1,
Otherwise = 0.

## LOGIC DIAGRAM