1/3.2-Inch System-On-A-Chip (SOC) CMOS Digital Image Sensor

MT9D131C12STC (Color, Pb-Free)

Features

- Micron® DigitalClarity® CMOS imaging technology
- Superior low-light performance
- Ultra-low-power,cost-effective
- Internal master clock generated by on-chip phase-locked loop oscillator (PLL)
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement, including lens shading correction
- Arbitrary image decimation with anti-aliasing
- Integrated real-time JPEG encoder
- Integrated microcontroller for flexibility
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format
  - ITU-R BT.601 (YCbCr)
  - 565RGB
  - 555RGB
  - 444RGB
  - JPEG 4:2:2
  - JPEG 4:2:0
  - Raw 10-bit
- Output FIFO for data rate equalization
- Programmable I/O slew rate

Applications

- Security surveillance cameras
- ePTZ cameras
- Wireless cameras
- Consumer video products
- High-resolution security cameras

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/3.2-inch (4:3)
Active imager size		4.73mm x 3.52mm
Active pixels		1600 x 1200 pixels (UXGA)
Pixel size		2.8µm x 2.8µm
Shutter type		Electronic rolling shutter (ERS)
Maximum frame rate		15 fps at full resolution, 30 fps in preview mode, (800 x 600)
Maximum data rate/ master clock		80 MB/s 6 MHz to 80 MHz
Supply voltage	Analog	2.5–3.1V
	Digital	1.7–1.95V
	I/O	1.7–3.1V
	PLL	2.5–3.1V
ADC resolution		10-bit, on-die
Responsivity		1.0V/lux-sec (550nm)
Dynamic range		71dB
Output gain		16 e-/pix/s at 55°C
Read noise		3.6 e-RMS at 16X
Dark current		30 e-/pix/s at 55°C
SNR_{MAX}		42.3dB
Power consumption		348mW at 15 fps, full resolution
		223mW at 30 fps, preview mode
Operating temperature		–30°C to +70°C
Package		Bare die, 48-pin CLCC

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9D131C12STC ES	48-pin CLCC (Pb-free) ES
MT9D131C12STCD ES	Demo kit
MT9D131C12STCH ES	Demo kit headboard

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

General Description

Micron Imaging MT9D131 is a 1/3.2 inch, 2-megapixel CMOS image sensor with an integrated advanced camera system. The camera system features a microcontroller (MCU) and a sophisticated image flow processor (IFP) with a real-time JPEG encoder.

The sensor core consists of an active pixel array of 1668 x 1248 pixels, programmable timing and control circuitry including a PLL, analog signal chain with automatic offset correction and programmable gain, and two 10-bit A/D converters (ADC). The entire system-on-a-chip (SOC) has ultra-low power requirements and superior low-light performance that is particularly suitable for a wide variety of applications.

Feature Overview

The MT9D131 is a color image sensor with a Bayer color filter arrangement.

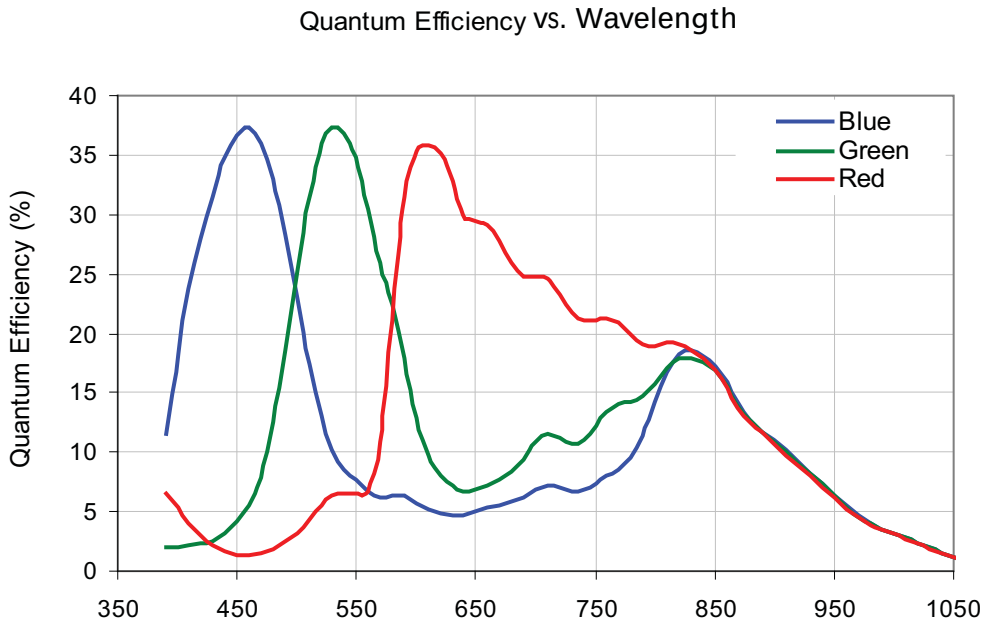
The MT9D131 has an embedded phase-locked loop oscillator (PLL) that can be used with the common wireless system clock. When in use, the PLL adjusts the incoming clock frequency, allowing the MT9D131 to run at almost any resolution and frame rate. To reduce power consumption, the PLL can be bypassed and powered down. The MT9D131 has numerous power conserving features, including an ultra-low power standby mode and the ability to individually shut down unused digital blocks.

Another important consideration for wireless devices is their electromagnetic emission or interference (EMI). The MT9D131 has a programmable I/O slew rate to minimize its EMI and an output FIFO to eliminate output data bursts.

The advanced IFP and flexible programmability of the MT9D131 provide a variety of ways to enhance and optimize the image sensor performance. Built-in optimization algorithms enable the MT9D131 to operate at factory settings as a fully automatic, highly adaptable camera. However, most of its settings are user-programmable by changing register values.

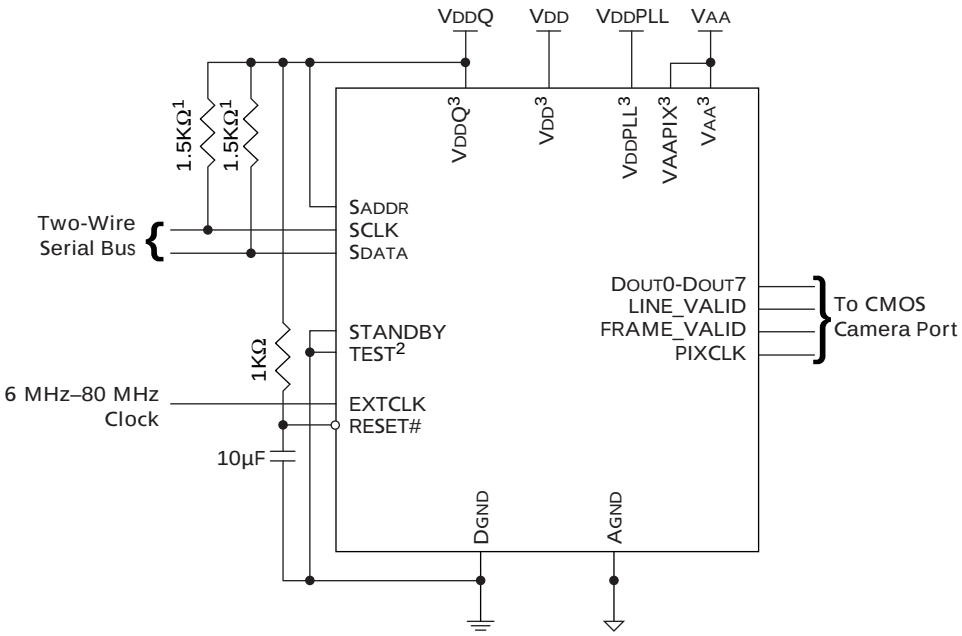
Figure 1 illustrates the MT9D131 quantum efficiency in relation to wavelength.

Figure 1: MT9D131 Quantum Efficiency



Typical Connection

Figure 2: Typical Configuration (Connection)



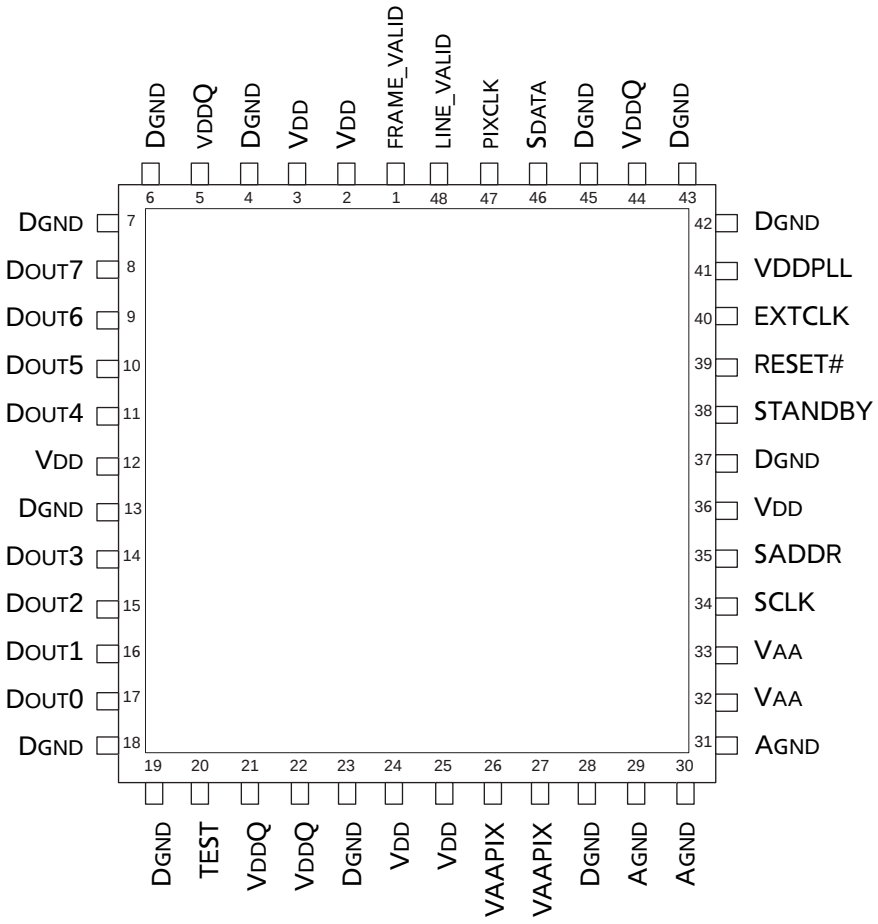
Notes: 1. Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.
2. TEST must be connected to digital ground for normal device operation.
3. All power supply pads must be used.

Signal Description

Table 3: Signal Description

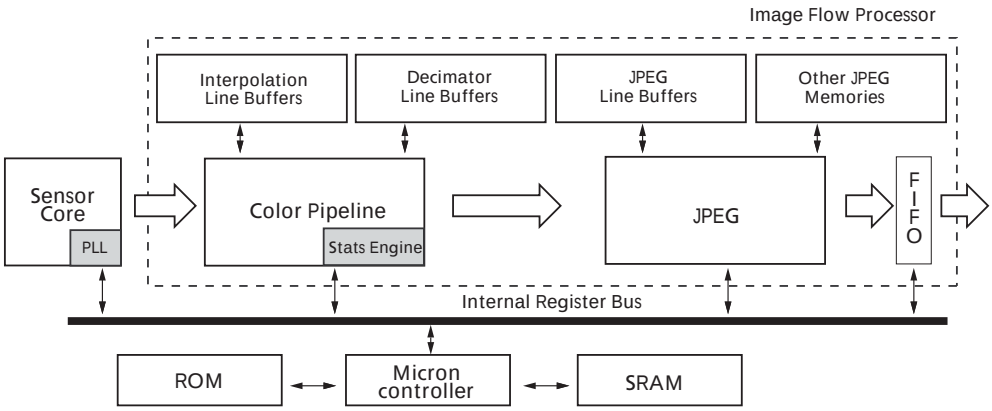
Name	CLCC Pin	Type	Description
EXTCLK	40	Input	Master clock signal (can either drive the on-chip PLL or bypass it).
RESET#	39	Input	Master reset signal, active LOW.
STANDBY	38	Input	Controls sensor's standby mode.
TEST	20	Input	Reserved for factory test. Tie to digital ground during normal operation.
SCLK	34	Input	Two-wire serial interface clock.
SADDR	35	Input	Selects device address for the two-wire serial interface. The address is 0x90 when SADDR is tied LOW, 0xBA if tied HIGH. See also R0x0D:0[10].
DOUT[7:0]	8, 9, 10, 11, 14, 15, 16, 17	Input	Eight-bit image data output or most significant bits (MSB) of 10-bit sensor bypass mode.
FRAME_VALID	1	Input	Identifies rows in the active image.
LINE_VALID	48	Input	Identifies lines in the active image.
PIXCLK	47	Input	Pixel clock. To be used for sampling DOUT, FRAME_VALID, and LINE_VALID.
SDATA	46	I/O	Two-wire serial interface data.
VDD	2, 3, 12, 24, 25, 36	Supply	Digital power (1.8V).
VDDPLL	41	Supply	PLL power (2.8V).
VAA	32, 33	Supply	Analog power (2.8V).
VAAPIX	26, 27	Supply	Pixel array power (2.8V).
VDDQ	21, 22, 44, 5	Supply	I/O power (nominal 1.8V or 2.8V).
AGND	29, 30, 31	Supply	Analog ground.
DGND	4, 6, 7, 13, 18, 19, 23, 28, 37, 42, 43, 45	Supply	Digital, I/O, and PLL ground.

Figure 3: 48-Pin CLCC Pinout



Architecture Overview

Figure 4: Block Diagram

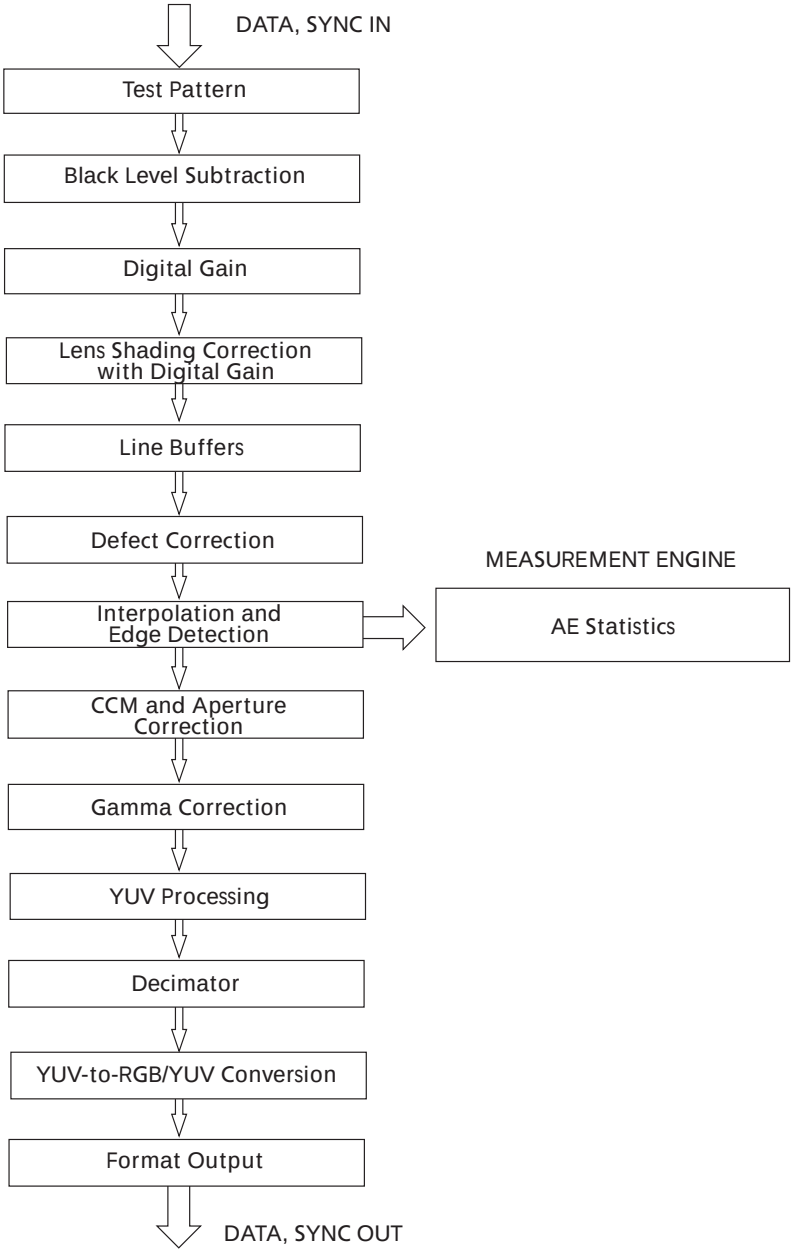


Sensor Core

The MT9D131 sensor core is a 2-megapixel CMOS image sensor with a 2.8µm pixel size designed for an optical format of 1/3.2 inches with a UXGA maximum resolution. The MT9D131 sensor core includes a phase-locked loop oscillator (PLL), to facilitate camera integration and minimize the system cost for wireless and mobile applications. When in use, the PLL generates an internal master clock signal whose frequency can be set higher than the frequency of external clock signal EXTCLK. This allows the MT9D131 to run at any resolution and frame rate up to the specified maximum values, irrespective of the EXTCLK frequency.

Color Pipeline

Figure 5: Color Pipeline



Test Pattern

During normal operation of MT9D131, a stream of raw image data from the sensor core is continuously fed into the color pipeline. For test purposes, this stream can be replaced with a fixed image generated by a special test module in the pipeline. The module provides a selection of test patterns sufficient for basic testing of the pipeline.

Black Level Conditioning and Digital Gain

Image stream processing starts with black level conditioning and multiplication of all pixel values by a programmable digital gain.

Lens Shading Correction

Inexpensive lenses tend to produce images whose brightness is significantly attenuated near the edges. Chromatic aberration in such lenses can cause color variation across the field of view. There are also other factors causing fixed-pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as lens shading. The MT9D131 has an embedded lens shading correction (LC) module that can be programmed to precisely counter the shading effect of a lens on each RGB color signal. The LC module multiplies RGB signals by a 2-dimensional correction function F(x,y), whose profile in both x and y direction is a piecewise quadratic polynomial with coefficients independently programmable for each direction and color.

Line Buffers

Several data processing steps following the lens shading correction require access to pixel values from up to 8 consecutive image lines. For these lines to be simultaneously available for processing, they must be buffered. The IFP includes a number of SRAM line buffers that are used to perform defect correction, color interpolation, image decimation, and JPEG encoding.

Defect Correction

The IFP performs on-the-fly defect correction that can mask pixel array defects such as high-dark-current (“hot”) pixels and pixels that are darker or brighter than their neighbors due to photoresponse nonuniformity. The defect correction algorithm uses several pixel features to distinguish between normal and defective pixels. After identifying the latter, it replaces their actual values with values inferred from the values of nearest same-color neighbors.

Color Interpolation and Edge Detection

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10-bit integer number, which, to make things simple, can be considered proportional to the pixel’s response to a one-color light stimulus—red, green, or blue—depending on the pixel’s position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one-color-per-pixel nature of the data stream, but after the defect correction it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between maintaining the sharpness of the image and filtering out high-frequency noise. The simplest interpolation algorithm is to sort the nearest eight neighbors of every pixel into three sets—red, green, and blue, discard the set of pixels of the same color as the center pixel (if there are any), calculate average pixel values for the remaining two sets, and use the averages instead of the missing color data for the center pixel. Such averaging reduces high-frequency noise, but it also blurs and distorts sharp transitions (edges) in the image. To avoid this problem, the interpolation module performs edge detection in the neighborhood of every processed pixel and, depending on its results, extracts color information from neighboring pixels in a number of different ways. In effect, it does low-pass filtering in flat-field image areas and avoids doing it near edges.

Color Correction and Aperture Correction

To achieve good color fidelity of IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10-bit numbers. Since such sums can have up to 12 significant bits, the bit width of the image data stream is widened to 12 bits per color (36 bits per pixel). The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are independent of the spectral sensitivity and color cross-talk characteristics of the image sensor. The optimal values of color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor.

To increase image sharpness, a programmable aperture correction is applied to color corrected image data, equally to each of the 12-bit R, G, and B color channels.

Gamma Correction

Like the aperture correction, gamma correction is applied equally to each of the 12-bit R, G, and B color channels. Gamma correction curve is implemented as a piecewise linear function with 19 knee points, taking 12-bit arguments and mapping them to 8-bit output. The driver variables include two arrays of knee point ordinates defining two separate gamma curves for sensor operation contexts A and B.

YUV Processing

After the gamma correction, the image data stream undergoes RGB to YUV conversion and optionally further corrective processing. The first step in this processing is removal of highlight coloration, also referred to as “color kill.” It affects only pixels whose brightness exceeds a certain pre-programmed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their brightness and the threshold.

Image Cropping and Decimation

To ensure that the size of images output by MT9D131 can be tailored to the needs of all users, the IFP includes a decimator module. When enabled, this module performs “decimation” of incoming images, that is, shrinks them to arbitrarily selected width and height without reducing the field of view and without discarding any pixel values. The latter point merits underscoring, because the terms “decimator” and “image decimation” suggest image size reduction by deleting columns and/or rows at regular intervals. Despite the terminology, no such deletions take place in the decimator module. Instead, it performs “pixel binning,” that is, divides each input image into rectangular bins corresponding to individual pixels of the desired output image, averages pixel values in these bins,and assembles the output image from the bin averages. Pixels lying on bin boundaries contribute to more than one bin average: their values are added to bin-wide sums of pixel values with fractional weights. The entire procedure preserves all image information that can be included in the downsized output image and filters out high-frequency features that could cause aliasing.

The image decimation in the IFP can be preceded by image cropping and/or image decimation in the sensor core. Image cropping takes place when the sensor core is programmed to output pixel values from a rectangular portion of its pixel array - a window - smaller than the default 1600 x 1200 window. Pixels outside the selected cropping window are not read out, which results in narrower field of view than at the default sensor settings. Irrespective of the size and position of the cropping window, the MT9D131 sensor core can also decimate outgoing images by skipping columns and/or rows of the

pixel array, and/or by binning 2 x 2 groups of pixels of the same color. Since decimation by skipping (that is, deletion) can cause aliasing (even if pixel binning is simultaneously enabled), it is generally better to change image size only by cropping and pixel binning.

The image cropping and decimator module can be used to do digital zoom and pan. If the decimator is programmed to output images smaller than images coming from the sensor core, zoom effect can be produced by cropping the latter from their maximum size down to the size of the output images. The ratio of these two sizes determines the maximum attainable zoom factor. For example, a 1600 x 1200 image rendered on a 160 x 120 display can be zoomed up to 10 times, since 1600/160 = 1200/120 = 10. Panning effect can be achieved by fixing the size of the cropping window and moving it around the pixel array.

YUV-to-RGB/YUV Conversion and Output Formatting

The YUV data stream emerging from the decimator module can either exit the color pipeline as-is or be converted before exit to an alternative YUV or RGB data format.

JPEG Encoder and FIFO

The JPEG compression engine in the MT9D131 is a highly integrated, high-performance solution that can provide sustained data rates of almost 80 MB/s for image sizes up to 1600 x 1200. Additionally, the solution provides for low power consumption and full programmability of JPEG compression parameters for image quality control.

JPEG Encoding Highlights

1. Sequential DCT (baseline) ISO/IEC 10918-1 JPEG-compliant
2. YCbCr 4:2:2 format compression
3. Programmable quantization tables
   - One each for luminance and chrominance (active)
   - Support for three pairs of quantization tables—two pairs serve as a backup for buffer overflow
4. Programmable Huffman Tables
   - 2 AC, 2 DC tables—separate for luminance and chrominance
5. Quality/compression ratio control capability
6. 15 fps MJPEG capability (header processing in external host processor)

Output Interface

Control (Two-Wire Serial Interface)

Camera control and JPEG configuration/control are accomplished using a two-wire serial interface. The interface supports individual access to all camera function registers and JPEG control registers. In particular, all tables located in the JPEG quantization and Huffman memories are accessible using the two-wire interface.

Context and Operational Modes

The MT9D131 can operate in several modes, including preview, still capture (snapshot), and video. All modes of operation are individually configurable and are organized as two contexts—context A and context B. A context is defined by sensor image size, frame rate, resolution and other associated parameters. The user can switch between the two contexts by sending a command through the two-wire serial interface.

Preview

Context A is primarily intended for use in the preview mode. During preview, the sensor usually outputs low resolution images at a relatively high frame rate, and its power consumption is kept to a minimum. Context B can be configured for the still capture or video mode, as required by the user. For still capture configuration, the user typically specifies the desired output image size, if JPEG compression, how many frames to capture, and so on. For video, the user might select a different image size and a fixed frame rate.

Snapshot

To take a snapshot, the user must send a command that changes the context from A to context B. Typical sequence of events after this command is as follows. First, the camera exposure and white balance is automatically adjusted to the changed illumination of the scene. Next, the camera enables JPEG compression and capture one or more frames of desired size. Completing the sequence, the camera automatically returns to context A and resume running preview.

Video

To start video capture, the user has to change relevant context B settings, such as capture mode, image size and frame rate, and again send a context change command. Upon receiving it, the MT9D131 switches to the modified context B settings, while continuing to output YUV-encoded image data. Auto exposure automatically switches to smooth continuous operation. To exit the video capture mode, the user has to send another context change command causing the sensor to switch back to context A.

Auto Exposure

The auto exposure (AE) algorithm performs automatic adjustments of the image brightness by controlling exposure time and analog gains of the sensor core as well as digital gains applied to the image.

Two auto exposure algorithm modes are available:

1. preview
2. scene evaluative

Auto exposure is implemented by means of a firmware driver that analyzes image statistics collected by exposure measurement engine, makes a decision and programs the sensor core and color pipeline to achieve the desired exposure. The measurement engine subdivides the image into 16 windows organized as a 4 x 4 grid.

Preview Mode

This exposure mode is activated during preview or video capture. It relies on the exposure measurement engine that tracks speed and amplitude of the change of the overall luminance in the selected windows of the image.

The backlight compensation is achieved by weighting the luminance in the center of the image higher than the luminance on the periphery. Other algorithm features include the rejection of fast fluctuations in illumination (time averaging), control of speed of response, and control of the sensitivity to the small changes. While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters described above.

Scene Evaluative Algorithm

A scene evaluative AE algorithm is available for use in snapshot mode. The algorithm performs scene analysis and classification with respect to its brightness, contrast and composure and then decides to increase, decrease or keep original exposure target. It makes most difference for backlight and bright outdoor conditions.

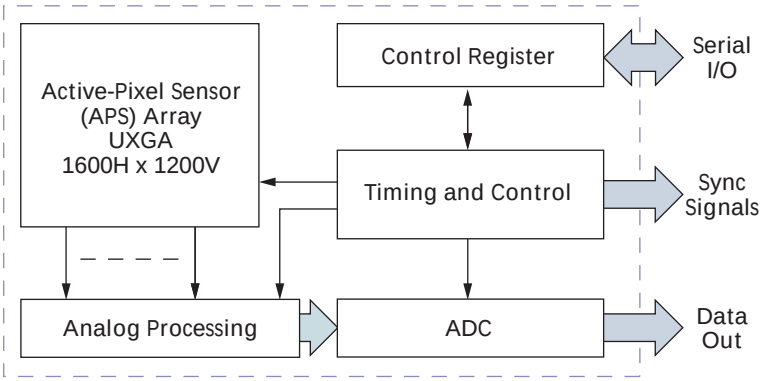
Auto White Balance

The MT9D131 has a built-in auto white balance (AWB) algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. This sophisticated algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a driver performing the selection of the optimal color correction matrix, digital, and sensor core analog gains. While default settings of these algorithms are adequate in most situations, the user can re-program base color correction matrices, place limits on color channel gains, and control the speed of both matrix and gain adjustments. Unlike simple white balancing algorithms found in many PC cameras, the MT9D131 AWB does not require the presence of gray or white elements in the image for good color rendition. The AWB does not attempt to locate "brightest" or "grayest" element of the image but instead performs sophisticated image analysis to differentiate between changes in predominant spectra of illumination and changes in predominant colors of the scene. While defaults are suitable for most applications, a wide range of algorithm parameters can be overwritten by the user using the serial interface.

Flicker Detection

Flicker occurs when the integration time is not an integer multiple of the period of the light intensity. The automatic flicker detection block does not compensate for the flicker, but rather avoids it by detecting the flicker frequency and adjusting the integration time. For integration times below the light intensity period (10ms for 50Hz environment), flicker cannot be avoided.

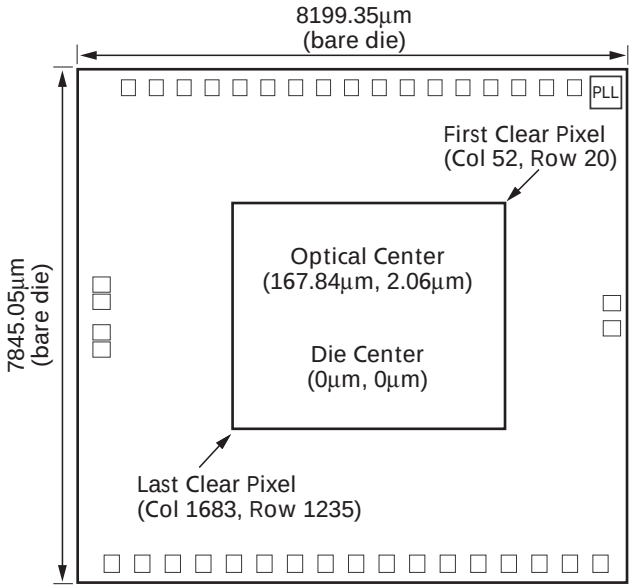
Figure 6: Sensor Core Block Diagram



The core of the sensor is an active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row. In the time interval between resetting a row and reading that row, the pixels in that row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. After a row is read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an ADC. The output from the ADC is a 10-bit value for each pixel in the array. The pixel array contains optically active and light-shielded "black" pixels. The black pixels are used to provide data for on-chip offset correction algorithms (black level control).

Die Outline

Figure 7: Optical Center Offset



Note: Figure not to scale.

Electrical Specifications

Recommended die operating temperature range is from –20° to +55°C. The sensor image quality may degrade above +55°C.

Table 4: AC Electrical Characteristics

Symbol	Definition	Conditions	Min	Type	Max	Units
$f_{EXTCLK1}$	Input clock frequency	PLL enabled (MCLK max = 80 MHz)	6	10	64	MHz
$t_{EXTCLK1}$	Input clock period	PLL enabled (MCLK max = 80 MHz)	15.625	100	166.7	ns
$f_{EXTCLK2}$	Input clock frequency	PLL disabled	6		80	MHz
$t_{EXTCLK2}$	Input clock period	PLL disabled	12.5		166.7	ns
t_R	Input clock rise time		0.5		1	V/ns
t_F	Input clock fall time		0.5		1	V/ns
	Clock duty cycle		40	50	60	%
f_{PIXCLK}	PIXCLK frequency	Default				MHz
t_{PD}	PIXCLK to data valid	Default	–3		3	ns
t_{PFH}	PIXCLK to FV HIGH	Default	–3		3	ns
t_{PLH}	PIXCLK to LV HIGH	Default	–3		3	ns
t_{PFL}	PIXCLK to FV LOW	Default	–3		3	ns
t_{PLL}	PIXCLK to LV LOW	Default	–3		3	ns
C_{IN}	Input pin capacitance			3.5		pF
C_{LOAD}	Load capacitance			15	20	pF

Table 5: AC Setup Conditions

Symbol	Min	Typ	Max	Units
$f_{EXTCLK1}$	6	–	64	MHz
V_{DD}	1.7	1.8	1.95	V
V_{DDQ}	1.7	2.8	3.1	V
V_{AA}	2.5	2.8	3.1	V
VAAPIX	2.5	2.8	3.1	V
V_{DDPLL}	2.5	2.8	3.1	V
Output load	–	15	–	–

Table 6: DC Electrical Definitions and Characteristics

Symbol	Definition	Conditions	Min	Typ	Max	Units	Note
V_{DD}	Core digital voltage		1.7	1.8	1.95	V	
V_{DDQ}	I/O digital voltage		1.7	2.8	3.1	V	
V_{AA}	Analog voltage		2.5	2.8	3.1	V	
VAAPIX	Pixel supply voltage		2.5	2.8	3.1	V	
V_{DDPLL}	PLL supply voltage		2.5	2.8	3.1	V	
V_{IH}	Input high voltage	V_{DDQ} = 2.8V	2.4		V_{DDQ} + 0.3	V	
		V_{DDQ} = 1.8V	1.4		V_{DDQ} + 0.3		
V_{IL}	Input low voltage	V_{DDQ} = 2.8V	GND – 0.3		0.8	V	
		V_{DDQ} = 1.8V	GND – 0.3		0.5		
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DDQ} or D_{GND}	–10	0.5	10	µA	
V_{OH}	Output high voltage	At specified I_{OH}	V_{DDQ} – 0.4			V	
V_{OL}	Output low voltage	At specified I_{OL}			0.4	V	
I_{OH}	Output high current	At specified V_{OH} = V_{DDQ}~400mV at 1.7V V_{DDQ}	–7		x	mA	
I_{OL}	Output low current	At specified V_{OL}~ 400MV at 1.7V V_{DDQ}	7		x	mA	
I_{OZ}	Tri-state output leakage current	V_{IN} = V_{DDQ} or GND	–10	+/-0.5	10	µA	
I_{DD}1	Digital operating current	Context B, 1600 x 1200, JPEG on, MCLK = MAX, PIXCLK = MAX		92	110	mA	
I_{DDQ}1	I/O digital operating current	Context B, 1600 x 1200, JPEG on, MCLK = MAX, PIXCLK = MAX		1.5		mA	1
I_{AA}1	Analog operating current	Context B, 1600 x 1200, JPEG on, MCLK = MAX, PIXCLK = MAX		43	55	mA	
IAAPIX1	Pixel supply current	Context B, 1600 x 1200, JPEG on, MCLK = MAX, PIXCLK = MAX		2.1	3.5	mA	
IDDPLL1	PLL supply current	Context B, 1600 x 1200, JPEG on, MCLK = MAX, PIXCLK = MAX		2.3	3	mA	
I_{DD}2	Digital operating current	Context A, 800 x 600, No JPEG, MCLK = MAX, PIXCLK = MAX		48	60	mA	
I_{DDQ}2	I/O digital operating current	Context A, 800 x 600, No JPEG, MCLK = MAX, PIXCLK = MAX		15		mA	1
IAA2	Analog operating current	Context A, 800 x 600, No JPEG, MCLK = MAX, PIXCLK = MAX		27	35	mA	
IAAPIX2	Pixel supply current	Context A, 800 x 600, No JPEG, MCLK = MAX, PIXCLK = MAX		4	5.5	mA	
IDDPLL2	PLL supply current	Context A, 800 x 600, No JPEG, MCLK = MAX, PIXCLK = MAX		2.3	3	mA	
ISTDBY1	Standby current PLL enabled	PLL enabled (MCLK = 0Hz, held at either V_{IL} or V_{IH})		35	100	µA	
ISTDBY2	Standby current PLL disabled	PLL disabled (MCLK = 0Hz, held at V_{IL} or V_{IH})		35	100	µA	

Notes: 1. Due to the influence of several variables (scene illumination, output load) maximum values are not available.
2. Context B: 1600 x 1200, JPEG on, MCLK = MAX, PIXCLK = MAX.
3. Context A: 800 x 600, No JPEG, MCLK = MAX, PIXCLK = MAX.

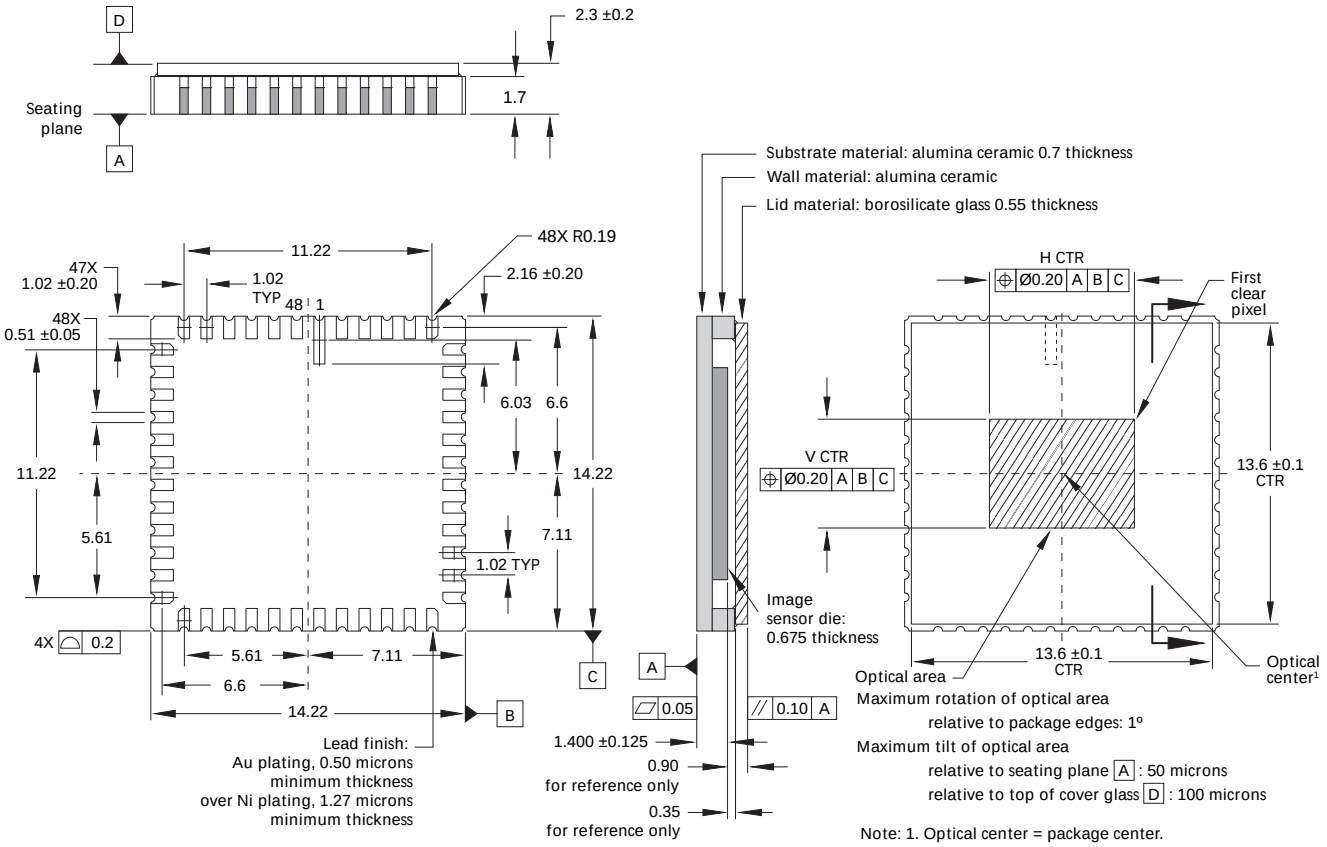
Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Digital power	–0.3	2.4	V
V_{DDQ}	I/O power	–0.3	4.0	V
V_{DDPLL}	PLL power	–0.3	4.0	V
V_{AA}	Analog power (2.8V)	–0.3	4.0	V
VAAPIX	Pixel array power	–0.3	4.0	V
V_{IN}	DC input voltage	–0.3	V_{DDQ} + 0.3	V
V_{OUT}	DC output voltage	–0.3	V_{DDQ} + 0.3	V
T_{OP}	Operation temperature	–30	70	°C
T_{STG}[1]	Storage temperature	–40	85	°C

Note: [1]Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Dimensions

Figure 8: 48-Pin CLCC Package Outline



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Revision History

Rev.B 3/28/2007

- Updated package information