# MC14013B

# Dual Type D Flip-Flop

The MC14013B dual type D flip−flop is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each flip−flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip−flops for counter and toggle applications.

### Features

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge−Clocked Flip−Flop Design
- Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive−going edge of the clock pulse
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4013B
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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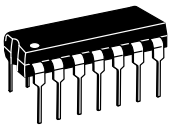
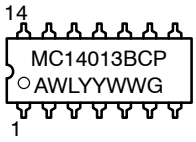
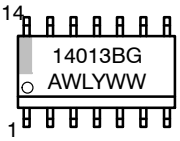
**MARKING DIAGRAMS**



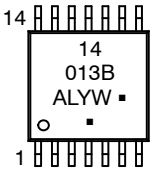
**PDIP−14**
**P SUFFIX**
**CASE 646**

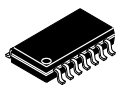



**SOIC−14**
**D SUFFIX**
**CASE 751A**

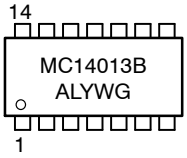



**TSSOP−14**
**DT SUFFIX**
**CASE 948G**



**SOEIAJ−14**
**F SUFFIX**
**CASE 965**




| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

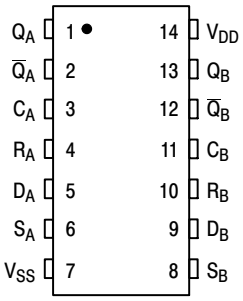
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

### TRUTH TABLE

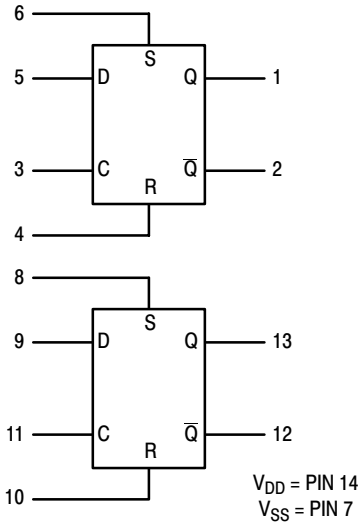
| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| Clock† | Data | Reset | Set | Q | $\overline{Q}$ | |
| ↗ | 0 | 0 | 0 | 0 | 1 | |
| ↗ | 1 | 0 | 0 | 1 | 0 | |
| ↘ | X | 0 | 0 | Q | $\overline{Q}$ | No Change |
| X | X | 1 | 0 | 0 | 1 | |
| X | X | 0 | 1 | 1 | 0 | |
| X | X | 1 | 1 | 1 | 1 | |

X = Don't Care
† = Level Change

### PIN ASSIGNMENT




### BLOCK DIAGRAM




### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14013BCPG | PDIP−14 (Pb−Free) | 25 Units / Rail |
| NLV14013BCPG* | | |
| MC14013BDG | SOIC−14 (Pb−Free) | 55 Units / Rail |
| NLV14013BDG* | | |
| MC14013BDR2G | SOIC−14 (Pb−Free) | 2500 Units / Tape & Reel |
| NLV14013BDR2G* | | |
| MC14013BDTR2G | TSSOP−14 (Pb−Free) | |
| NLV14013BDTR2G* | | |
| MC14013BFG | SOEIAJ−14 (Pb−Free) | 50 Units / Rail |
| MC14013BFELG | | 2000 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | – 55°C Min | – 55°C Max | 25°C Min | 25°C Typ (2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ “1” Level | $V_{OH}$ | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | 5.0<br>10<br>15 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | –<br>–<br>– | Vdc |
| Input Voltage “0” Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 or 0.5 Vdc) | | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| ($V_O$ = 0.5 or 4.5 Vdc) “1” Level | $V_{IH}$ | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | – 3.0 | – | – 2.4 | – 4.2 | – | – 1.7 | – | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | – 0.64 | – | – 0.51 | – 0.88 | – | – 0.36 | – | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | – 1.6 | – | – 1.3 | – 2.25 | – | – 0.9 | – | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | – 4.2 | – | – 3.4 | – 8.8 | – | – 2.4 | – | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | $I_{in}$ | 15 | – | ± 0.1 | — | ±0.00001 | ± 0.1 | – | ± 1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 1.0 | – | 0.002 | 1.0 | – | 30 | μAdc |
| | | 10 | – | 2.0 | – | 0.004 | 2.0 | – | 60 | |
| | | 15 | – | 4.0 | – | 0.006 | 4.0 | – | 120 | |
| Total Supply Current (3) (4) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0<br>10<br>15 | $I_T$ = (0.75 μA/kHz) f + $I_{DD}$<br>$I_T$ = (1.5 μA/kHz) f + $I_{DD}$<br>$I_T$ = (2.3 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

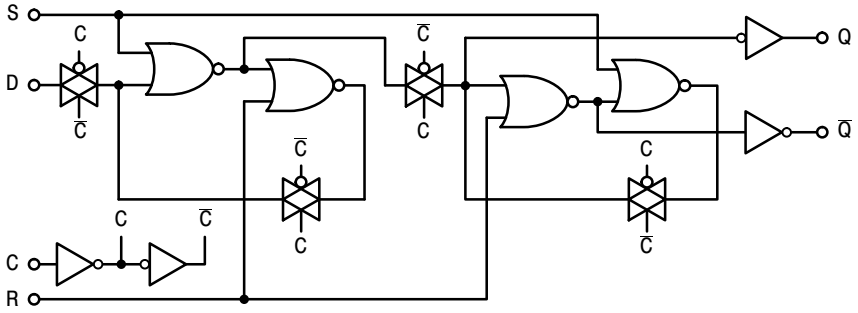
where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.

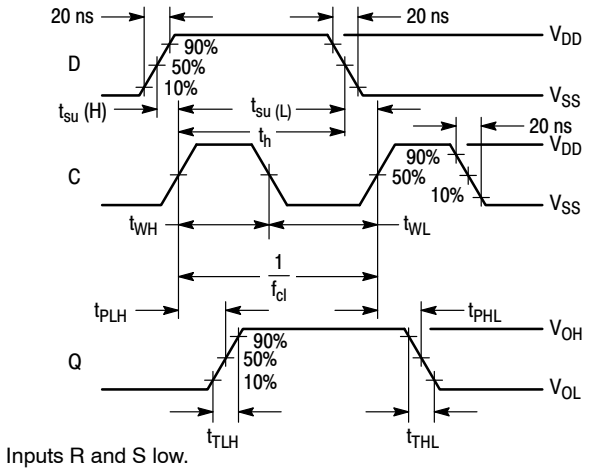
**SWITCHING CHARACTERISTICS** [5] ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ [6] | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | $t_{THL}$ | 5.0 | – | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | – | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$ | | | | | ns |
| Clock to Q, $\overline{Q}$ | $t_{PHL}$ | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 90 ns | | 5.0 | – | 175 | 350 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 42 ns | | 10 | – | 75 | 150 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 25 ns | | 15 | – | 50 | 100 | |
| Set to Q, $\overline{Q}$ | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 90 ns | | 5.0 | – | 175 | 350 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 42 ns | | 10 | – | 75 | 150 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 25 ns | | 15 | – | 50 | 100 | |
| Reset to Q, $\overline{Q}$ | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 265 ns | | 5.0 | – | 225 | 450 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 67 ns | | 10 | – | 100 | 200 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 50 ns | | 15 | – | 75 | 150 | |
| Setup Times [7] | $t_{su}$ | 5.0 | 40 | 20 | – | ns |
| | | 10 | 20 | 10 | – | |
| | | 15 | 15 | 7.5 | – | |
| Hold Times [7] | $t_h$ | 5.0 | 40 | 20 | – | ns |
| | | 10 | 20 | 10 | – | |
| | | 15 | 15 | 7.5 | – | |
| Clock Pulse Width | $t_{WL}$, $t_{WH}$ | 5.0 | 250 | 125 | – | ns |
| | | 10 | 100 | 50 | – | |
| | | 15 | 70 | 35 | – | |
| Clock Pulse Frequency | $f_{cl}$ | 5.0 | – | 4.0 | 2.0 | MHz |
| | | 10 | – | 10 | 5.0 | |
| | | 15 | – | 14 | 7.0 | |
| Clock Pulse Rise and Fall Time | $t_{TLH}$ | 5.0 | – | – | 15 | μs |
| | $t_{THL}$ | 10 | – | – | 5.0 | |
| | | 15 | – | – | 4.0 | |
| Set and Reset Pulse Width | $t_{WL}$, $t_{WH}$ | 5.0 | 250 | 125 | – | ns |
| | | 10 | 100 | 50 | – | |
| | | 15 | 70 | 35 | – | |
| Removal Times | $t_{rem}$ | | | | | ns |
| Set | | 5 | 80 | 0 | – | |
| | | 10 | 45 | 5 | – | |
| | | 15 | 35 | 5 | – | |
| Reset | | 5 | 50 | – 35 | – | |
| | | 10 | 30 | – 10 | – | |
| | | 15 | 25 | – 5 | – | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
7. Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.

**LOGIC DIAGRAM** (1/2 of Device Shown)






Inputs R and S low.

**Figure 1. Dynamic Signal Waveforms (Data, Clock, and Output)**

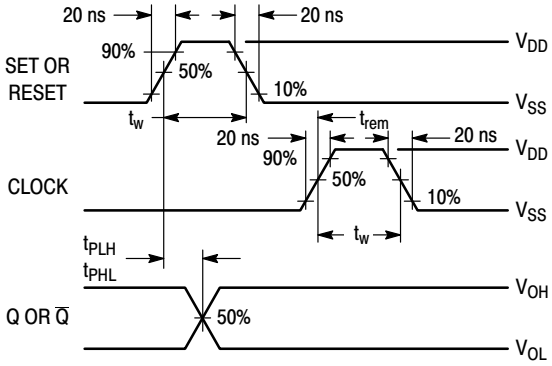
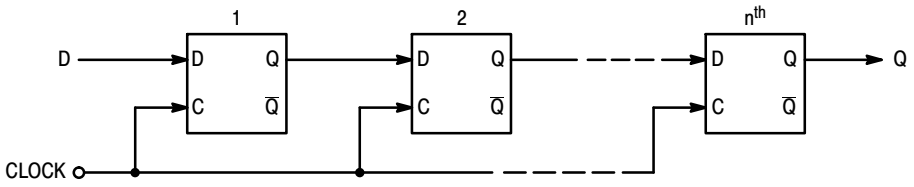


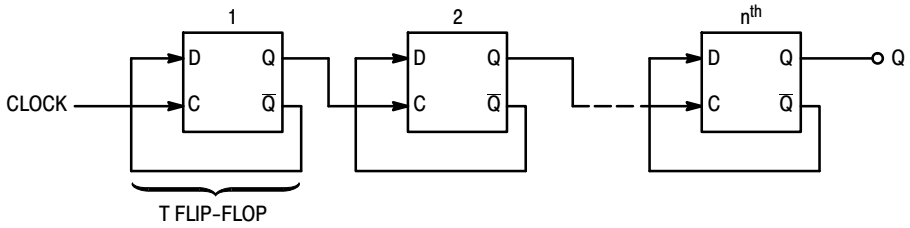

**Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)**

## TYPICAL APPLICATIONS

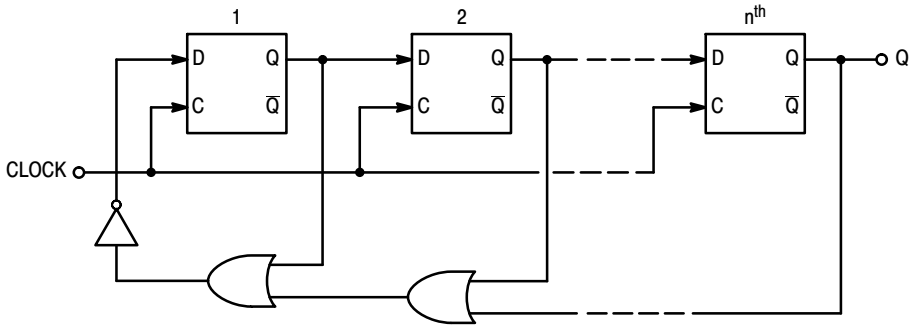
### n–STAGE SHIFT REGISTER




### BINARY RIPPLE UP–COUNTER (Divide–by–$2^n$)

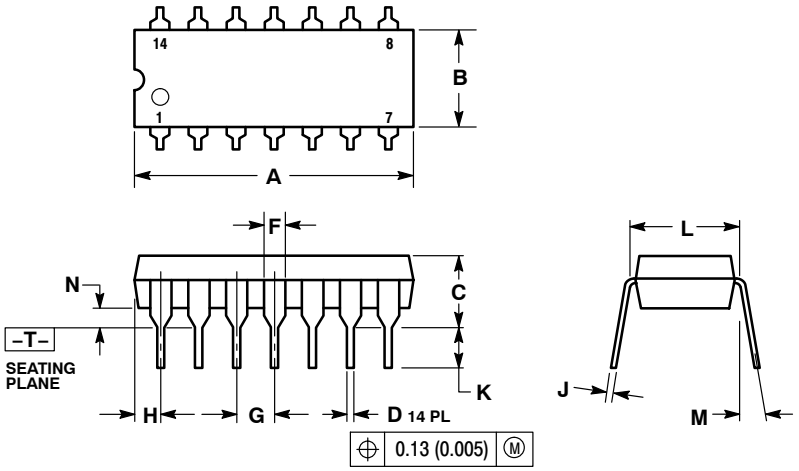



### MODIFIED RING COUNTER (Divide–by–(n+1))



## PACKAGE DIMENSIONS

**PDIP−14**
CASE 646−06
ISSUE P

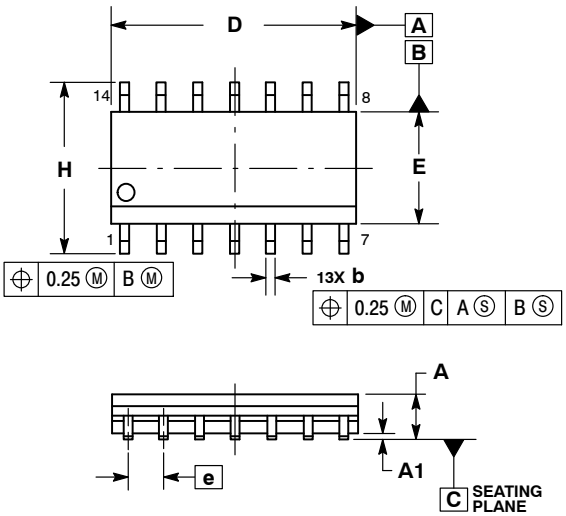


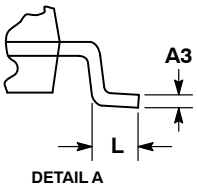

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

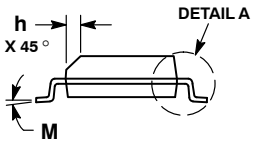
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | −−− | 10 ° | −−− | 10 ° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

## PACKAGE DIMENSIONS

**SOIC−14 NB**
CASE 751A−03
ISSUE K



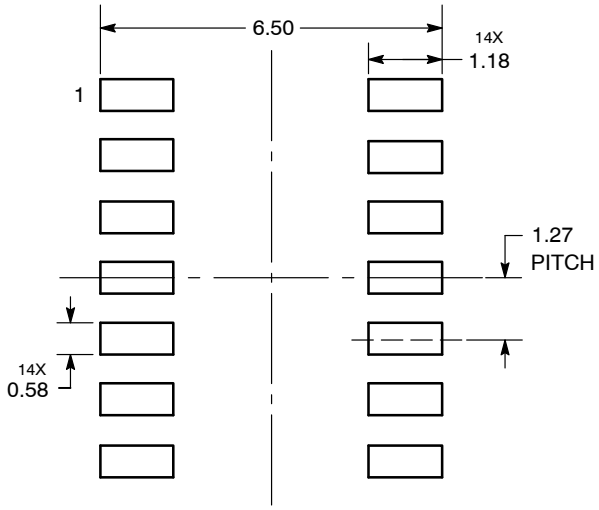




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

### SOLDERING FOOTPRINT*

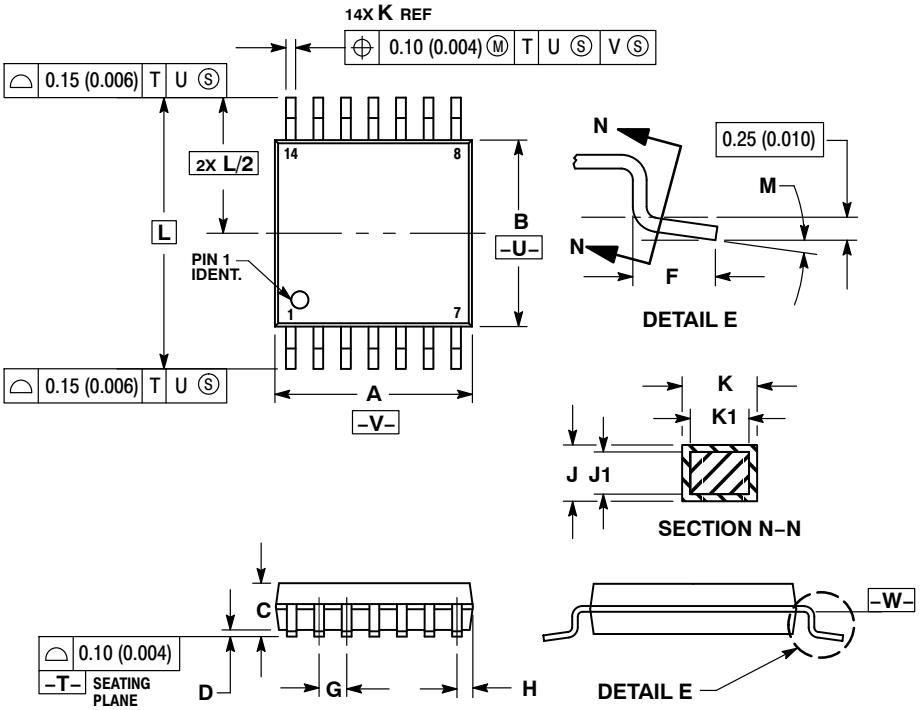



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

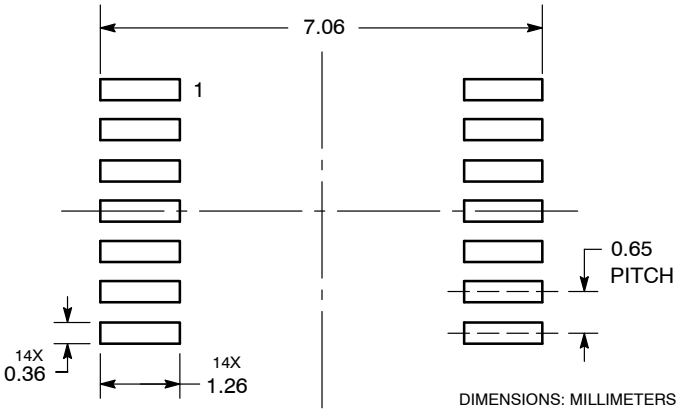
**TSSOP−14**
CASE 948G
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### SOLDERING FOOTPRINT*

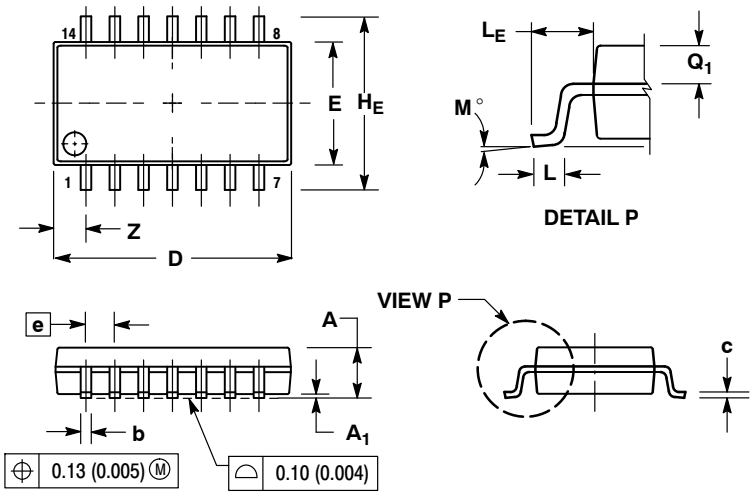



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC14013B

## PACKAGE DIMENSIONS

**SOEIAJ−14**
CASE 965
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.004 | 0.008 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |



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