Quad Array for ESD Protection

This quad monolithic silicon voltage suppressor is designed for applications requiring transient overvoltage protection capability. It is intended for use in voltage and ESD sensitive equipment such as computers, printers, business machines, communication systems, medical equipment, and other applications. Its quad junction common anode design protects four separate lines using only one package. These devices are ideal for situations where board space is at a premium.

Specification Features

- SOT-553 Package Allows Four Separate Unidirectional Configurations
- Low Leakage < 1 µA @ 3 Volt for NZQA5V6XV5T1
- Breakdown Voltage: 5.6 Volt 6.8 Volt @ 1 mA
- ESD Protection Meeting IEC61000-4-2 Level 4

Mechanical Characteristics

- Void Free, Transfer–Molded, Thermosetting Plastic Case
- Corrosion Resistant Finish, Easily Solderable
- Package Designed for Optimal Automated Board Assembly
- Small Package Size for High Density Applications
- 100% Lead Free, MSL1 @ 260°C Reflow Temperature



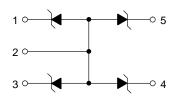
http://onsemi.com



MARKING DIAGRAM



xx = Device MarkingD = One Digit Date Code



ORDERING INFORMATION

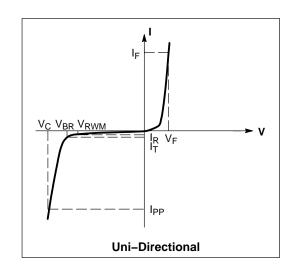
Device	Package	Shipping [†]
NZQA5V6XV5T1	SOT-553	4000/Tape & Reel
NZQA5V6XV5T3	SOT-553	16000/Tape & Reel
NZQA6V2XV5T1	SOT-553	4000/Tape & Reel
NZQA6V8XV5T1	SOT-553	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V_{BR}	Breakdown Voltage @ I _T
I _T	Test Current
ΘV _{BR}	Maximum Temperature Coefficient of V _{BR}
l _F	Forward Current
V _F	Forward Voltage @ I _F
Z _{ZT}	Maximum Zener Impedance @ I _{ZT}
I _{ZK}	Reverse Current
Z _{ZK}	Maximum Zener Impedance @ I _{ZK}



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

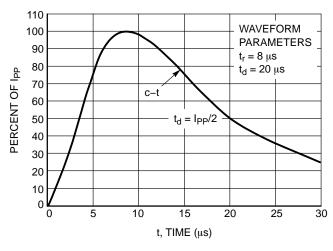
	Characteristic	Symbol	Value	Unit
Peak Power Dissipation	on (8 X 20 μs @ T _A = 25°C) (Note 1)	P _{PK}	100	W
Steady State Power -	1 Diode (Note 2)	P_{D}	300	mW
Thermal Resistance J Above 25°C, Derate		$R_{ hetaJA}$	370 2.7	°C/W mW/°C
Maximum Junction Ter	mperature	T_{Jmax}	150	°C
Operating Junction an	d Storage Temperature Range	T _J T _{stg}	-55 to +150	°C
ESD Discharge	MIL STD 883C – Method 3015–6 IEC1000–4–2, Air Discharge IEC1000–4–2, Contact Discharge	V _{PP}	16 16 9	kV
Lead Solder Temperat	ture (10 seconds duration)	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS $(T_A = 25^{\circ}C)$

	Device		down Vo	-	Leakage Current I _{RM} @ V _{RM} V _C Max @ I _{PI}		х @ І _{РР}	Typ Capacitance @ 0 V Bias (Note 3)	Max V _F @ l _F = 200 mA	
Device	Marking	Min	Nom	Max	V _{RWM}	I _{RWM} (μA)	V _C (V)	I _{PP} (A)	(pF)	(V)
NZQA5V6XV5T1	56	5.32	5.6	5.88	3.0	1.0	10.5	10	90	1.3
NZQA6V2XV5T1	62	5.89	6.2	6.51	4.0	0.5	11.5	9.0	80	1.3
NZQA6V8XV5T1	68	6.46	6.8	7.14	4.3	0.1	12.5	8.0	70	1.3

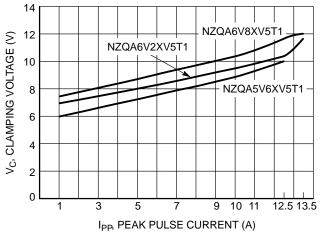
- Non-repetitive current per Figure 1.
 Only 1 diode under power. For all 4 diodes under power, P_D will be 25%. Mounted on FR-4 board with min pad.
 Capacitance of one diode at f = 1 MHz, V_R = 0 V, T_A = 25°C



% OF RATED POWER OR IPP T_A, AMBIENT TEMPERATURE (°C)

Figure 1. Pulse Waveform

Figure 2. Power Derating Curve



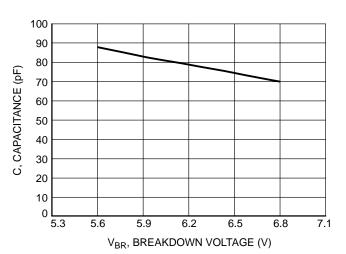
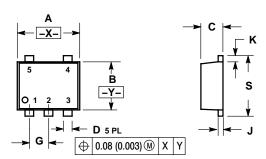


Figure 3. Clamping Voltage versus Peak Pulse Current

Figure 4. Typical Capacitance

PACKAGE DIMENSIONS

SOT-553, 5-LEAD CASE 463B-01 ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
 Y14 5M 1982
- CONTROLLING DIMENSION: MILLIMETERS
 MAXIMUM LEAD THICKNESS INCLUDES LEAD
 FINISH THICKNESS. MINIMUM LEAD THICKNESS
 IS THE MINIMUM THICKNESS OF BASE
 MATERIAL

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	1.50	1.70	0.059	0.067	
В	1.10	1.30	0.043	0.051	
С	0.50	0.60	0.020	0.024	
D	0.17	0.27	0.007	0.011	
G	0.50 BSC		0.020 BSC		
J	0.08	0.18	0.003	0.007	
K	0.10	0.30	0.004	0.012	
S	1.50	1.70	0.059	0.067	

 STYLE 1:
 STYLE 2:

 PIN 1. BASE 1
 PIN 1. CATHODE

 2. EMITTER 1/2
 2. ANODE

 3. BASE 2
 3. CATHODE

 4. COLLECTOR 2
 4. CATHODE

 5. COLLECTOR 1
 5. CATHODE

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082–1312 USA Phone: 480–829–7710 or 800–344–3860 Toll Free USA/Canada Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free LISA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.