REJ09B0241-0100

Everywhere you imagine. RENESAS

16

H8S/2144B,H8S/2134B

Hardware Manual

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer
H8S Family/H8S/2100 Series

H8S/2144B HD64F2144B
H8S/2134B HD64F2134B

Rev.1.00
Revision Date: Jun.24, 2005

Renesas Technology
www.renesas.com

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

     The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index

Preface

The H8S/2144B and H8S/2134B are microcomputers (MCUs) made up of the H8S/2000 CPU employing Renesas Technology's original architecture as their cores, and the peripheral functions required to configure a system.

Target Users: This manual was written for users who will be using the H8S/2144B or H8S/2134B in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the H8S/2144B and H8S/2134B to the target users.
Refer to the H8S/2600 Series, H8S/2000 Series Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions
  Read the H8S/2600 Series, H8S/2000 Series Software Manual.
- In order to understand the details of a register when its name is known
  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bits, and initial values of the registers are summarized in section 19, List of Registers.

Rules:		
	Register name:	The following notation is used for cases when the same or a similar function, e.g. serial communication interface, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB is on the left and the LSB is on the right.
	Number notation:	Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx.
	Signal notation:	An overbar is added to a active-low signal: $\overline{\text{xxxx}}$

Related Manuals: The latest versions of all related manuals are available from our web site.
Please ensure you have the latest versions of all documents you require.
http://www.renesas.com/

H8S/2144B, H8S/2134B manuals:

Manual Title	ADE No.
H8S/2144B, H8S/2134B Hardware Manual	This manual
H8S/2600 Series, H8S/2000 Series Software Manual	REJ09B0139

User's manuals for development tools:

Manual Title	ADE No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	REJ10B0058
Microcomputer Development Environment System H8S, H8/300 Series Simulator/Debugger User's Manual	ADE-702-282
H8S, H8/300 Series High-performance Embedded Workshop 3 Tutorial	REJ10B0024
H8S, H8/300 Series High-performance Embedded Workshop 3 User's Manual	REJ10B0026

Contents

Figures

Section 6 Bus Controller (BSC)

Section 8 14-Bit PWM Timer (PWMX)

Section 9 16-Bit Free-Running Timer (FRT)

Section 10 8-Bit Timer (TMR)

Section 11 Watchdog Timer (WDT)

Section 12 Serial Communication Interface (SCI and IrDA)

Section 13 D/A Converter

Section 14 A/D Converter

Section 16 ROM

Section 17 Clock Pulse Generator

Section 18 Power-Down Modes

Section 20 Electrical Characteristics

Appendix

Tables

Appendix

Section 1 Overview

1.1 Features

- High-speed H8S/2000 central processing unit with an internal 16-bit architecture
  Upward-compatible with H8/300 and H8/300H CPUs on an object level
  Sixteen 16-bit general registers
  65 basic instructions
- Various peripheral functions
  14-bit PWM timer (PWMX)
  16-bit free-running timer (FRT)
  8-bit timer (TMR)
  Watchdog timer (WDT)
  Asynchronous or clock synchronous serial communication interface (SCI, IrDA)
  8-bit D/A converter
  10-bit A/D converter
  Clock pulse generator

- On-chip memory

ROM	Model	ROM	RAM	Remarks
Flash memory version	HD64F2144B	128 kbytes	4 kbytes	
	HD64F2134B	128 kbytes	4 kbytes	

- General I/O ports
  I/O pins: 74 (H8S/2144B) and 58 (H8S/2134B)
  Input-only pins: 8
- Supports various power-down modes
- Compact package

Product	Package	Code	Body Size	Pin Pitch
H8S/2144B	QFP-100B	FP-100B	16.0 × 16.0 mm	0.5 mm
	TQFP-100B	TFP-100B		
H8S/2134B	QFP-80A	FP-80A	17.2 × 17.2 mm	0.65 mm
	TQFP-80C	TFP-80C	14.0 × 14.0 mm	0.5 mm

1.2 Block Diagram

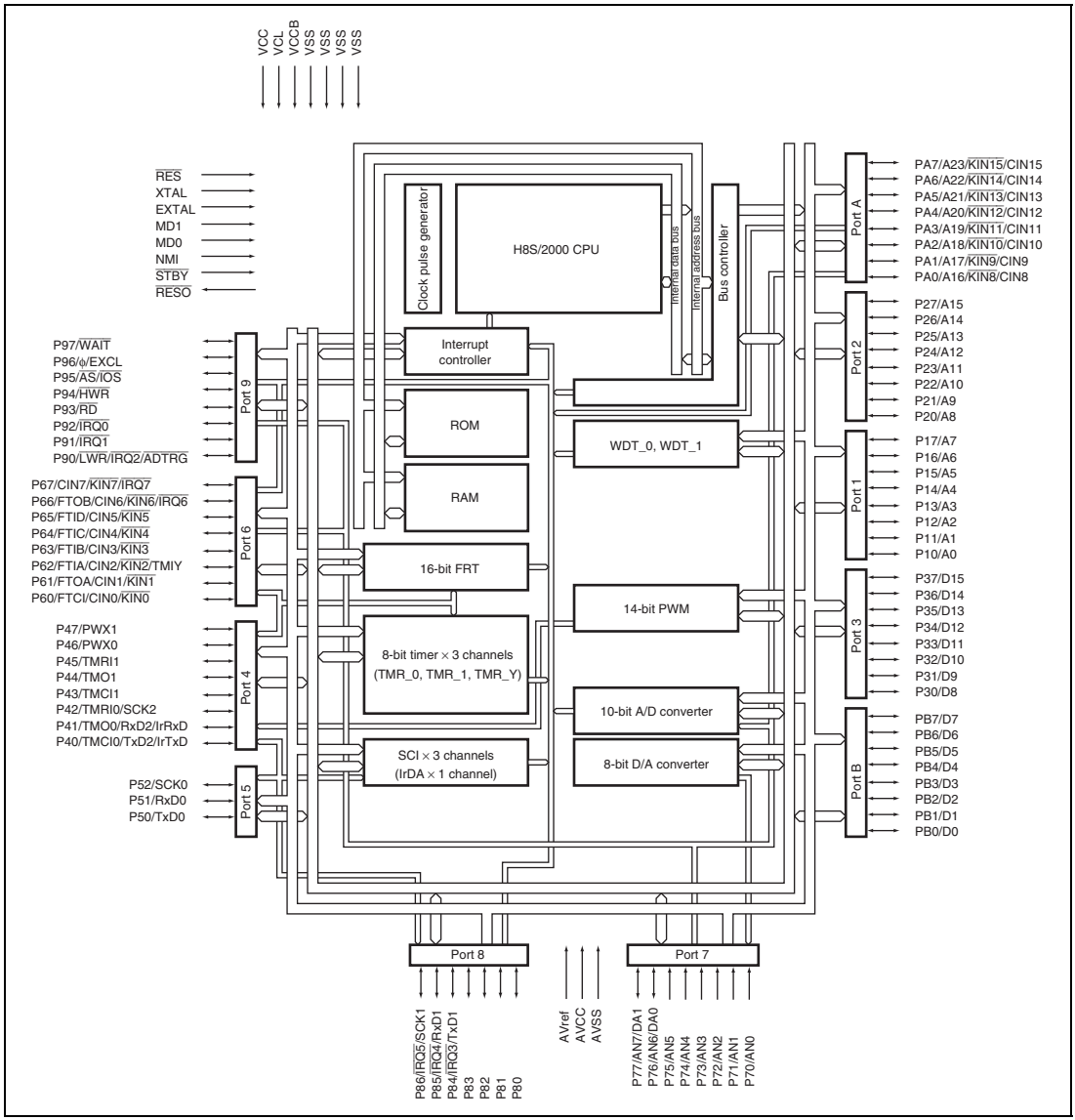


Figure 1.1 Block Diagram of H8S/2144B

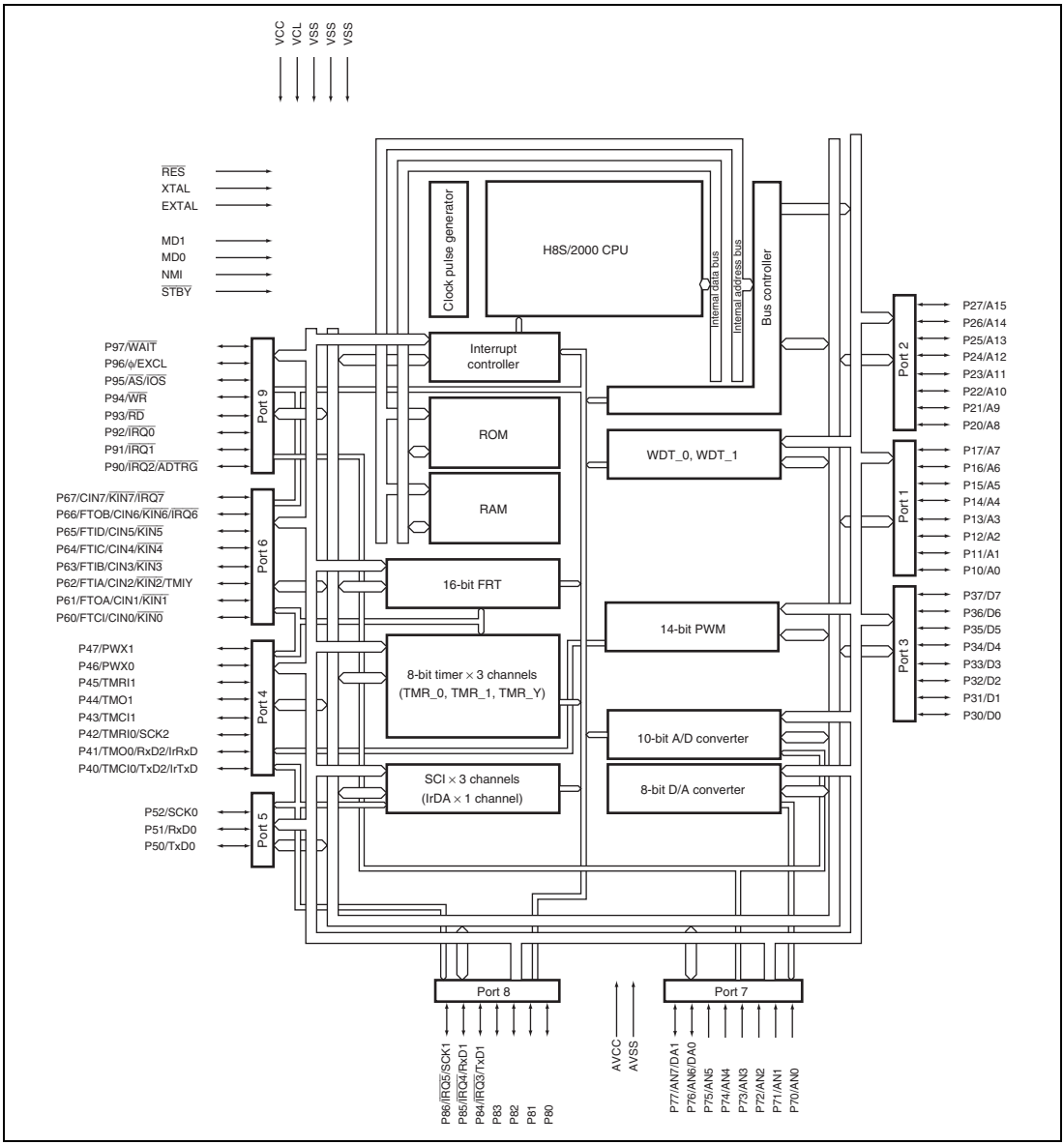


Figure 1.2 Block Diagram of H8S/2134B

1.3 Pin Arrangements and Functions

1.3.1 Pin Arrangements

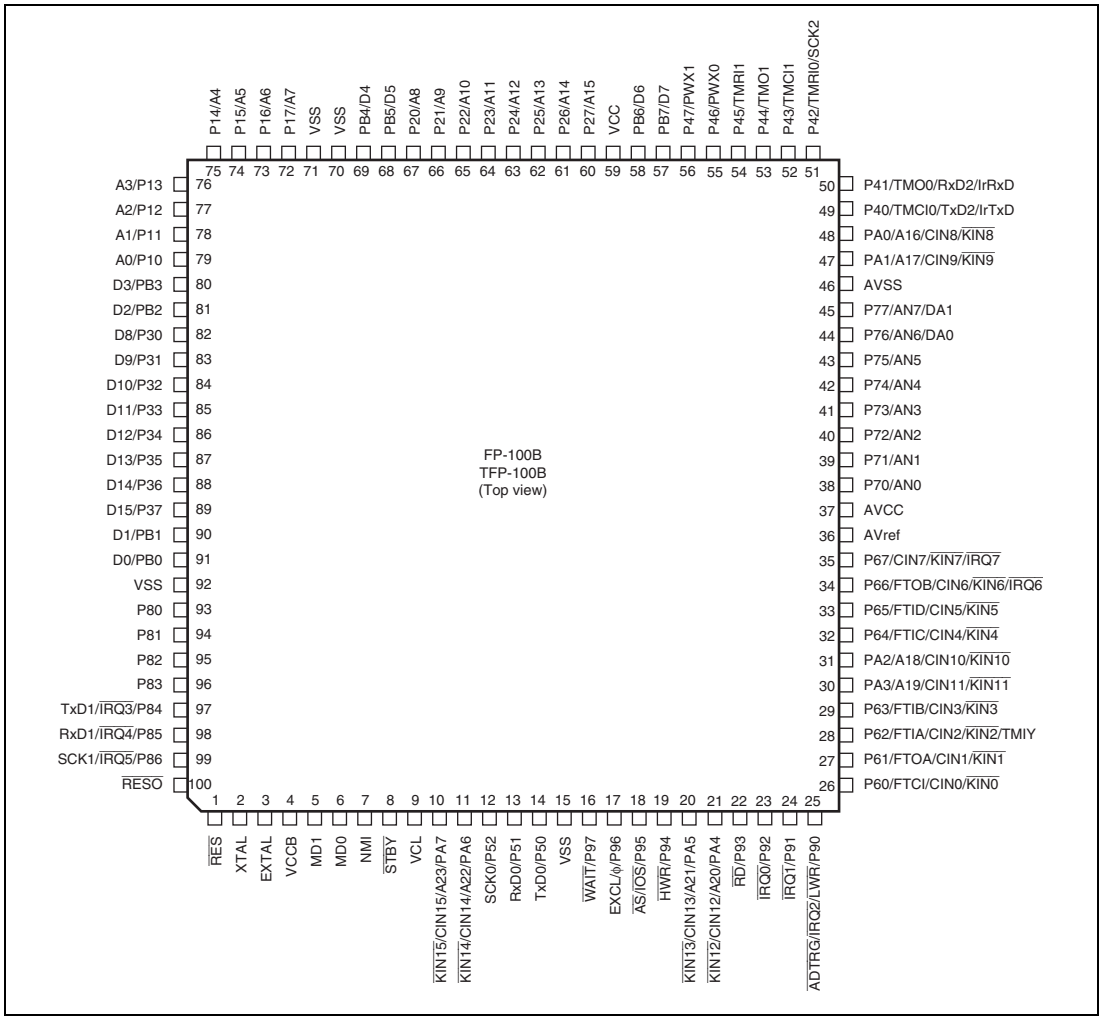


Figure 1.3 Pin Arrangements of H8S/2144B

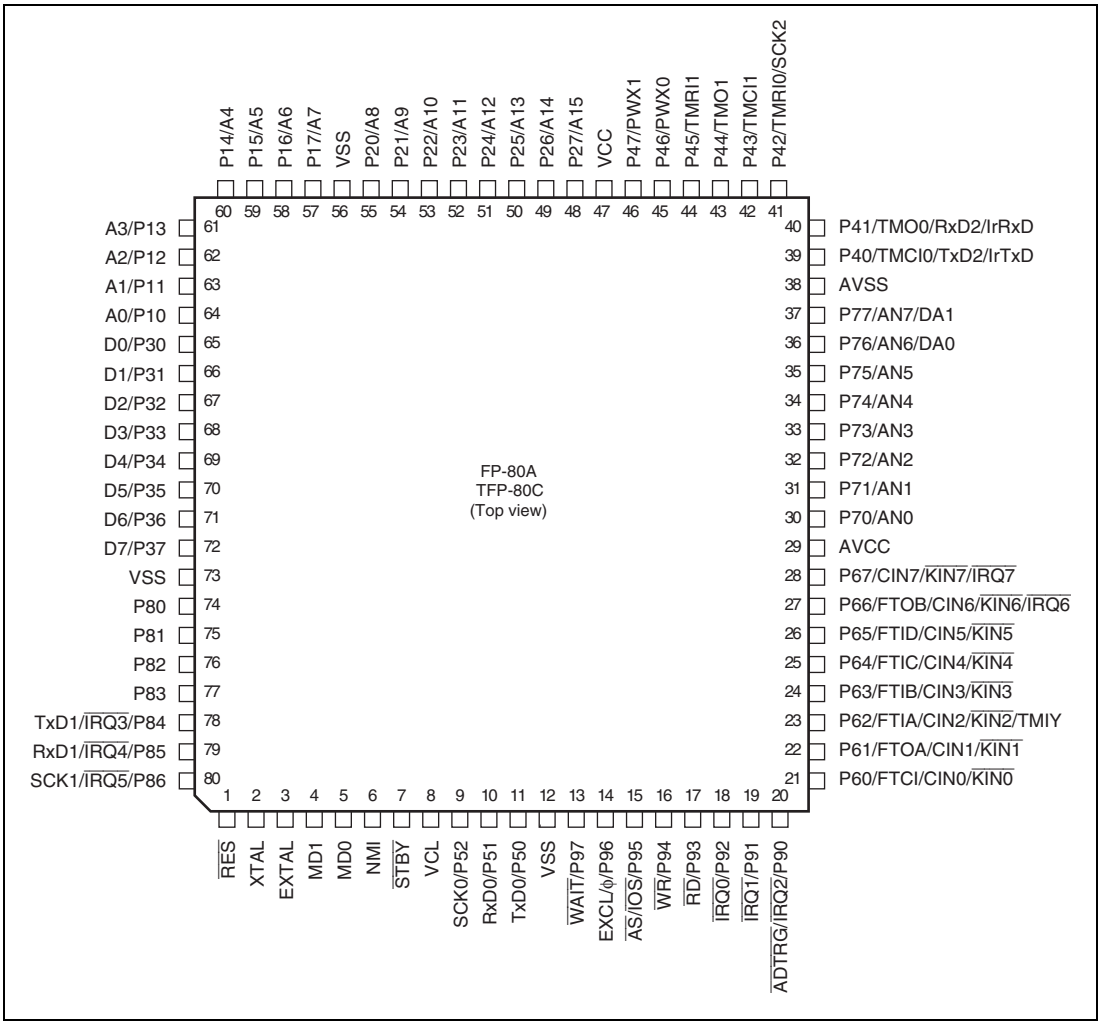


Figure 1.4 Pin Arrangements of H8S/2134B

1.3.2 Pin Functions in Each Operating Mode

Table 1.1 Pin Functions of H8S/2144B in Each Operating Mode

	Pin Name		
Pin No.	**Extended Modes**		**Single-Chip Modes**
FP-100B **TFP-100B**	**Mode 1**	**Mode 2 (EXPE = 1)** **Mode 3 (EXPE = 1)**	**Mode 2 (EXPE = 0)** **Mode 3 (EXPE = 0)**
1	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
2	XTAL	XTAL	XTAL
3	EXTAL	EXTAL	EXTAL
4	VCCB	VCCB	VCCB
5	MD1	MD1	MD1
6	MD0	MD0	MD0
7	NMI	NMI	NMI
8	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$
9	VCL	VCL	VCL
10 (B)	PA7/CIN15/$\overline{\text{KIN15}}$	A23/PA7/CIN15/$\overline{\text{KIN15}}$	PA7/CIN15/$\overline{\text{KIN15}}$
11 (B)	PA6/CIN14/$\overline{\text{KIN14}}$	A22/PA6/CIN14/$\overline{\text{KIN14}}$	PA6/CIN14/$\overline{\text{KIN14}}$
12	P52/SCK0	P52/SCK0	P52/SCK0
13	P51/RxD0	P51/RxD0	P51/RxD0
14	P50/TxD0	P50/TxD0	P50/TxD0
15	VSS	VSS	VSS
16	P97/$\overline{\text{WAIT}}$	P97/$\overline{\text{WAIT}}$	P97
17	ϕ/P96/EXCL	ϕ/P96/EXCL	ϕ/P96/EXCL
18	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	P95
19	$\overline{\text{HWR}}$	$\overline{\text{HWR}}$	P94
20 (B)	PA5/CIN13/$\overline{\text{KIN13}}$	A21/PA5/CIN13/$\overline{\text{KIN13}}$	PA5/CIN13/$\overline{\text{KIN13}}$
21 (B)	PA4/CIN12/$\overline{\text{KIN12}}$	A20/PA4/CIN12/$\overline{\text{KIN12}}$	PA4/CIN12/$\overline{\text{KIN12}}$
22	$\overline{\text{RD}}$	$\overline{\text{RD}}$	P93
23	P92/$\overline{\text{IRQ0}}$	P92/$\overline{\text{IRQ0}}$	P92/$\overline{\text{IRQ0}}$
24	P91/$\overline{\text{IRQ1}}$	P91/$\overline{\text{IRQ1}}$	P91/$\overline{\text{IRQ1}}$
25	$\overline{\text{LWR}}$/P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$	$\overline{\text{LWR}}$/P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$	P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$
26	P60/FTCI/CIN0/$\overline{\text{KIN0}}$	P60/FTCI/CIN0/$\overline{\text{KIN0}}$	P60/FTCI/CIN0/$\overline{\text{KIN0}}$

Pin No.	Pin Name: Extended Modes		Pin Name: Single-Chip Modes
FP-100B TFP-100B	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)
27	P61/FTOA/CIN1/$\overline{\text{KIN1}}$	P61/FTOA/CIN1/$\overline{\text{KIN1}}$	P61/FTOA/CIN1/$\overline{\text{KIN1}}$
28	P62/FTIA/CIN2/$\overline{\text{KIN2}}$/ TMIY	P62/FTIA/CIN2/$\overline{\text{KIN2}}$/ TMIY	P62/FTIA/CIN2/$\overline{\text{KIN2}}$/ TMIY
29	P63/FTIB/CIN3/$\overline{\text{KIN3}}$	P63/FTIB/CIN3/$\overline{\text{KIN3}}$	P63/FTIB/CIN3/$\overline{\text{KIN3}}$
30 (B)	PA3/CIN11/$\overline{\text{KIN11}}$	A19/PA3/CIN11/$\overline{\text{KIN11}}$	PA3/CIN11/$\overline{\text{KIN11}}$
31 (B)	PA2/CIN10/$\overline{\text{KIN10}}$	A18/PA2/CIN10/$\overline{\text{KIN10}}$	PA2/CIN10/$\overline{\text{KIN10}}$
32	P64/FTIC/CIN4/$\overline{\text{KIN4}}$	P64/FTIC/CIN4/$\overline{\text{KIN4}}$	P64/FTIC/CIN4/$\overline{\text{KIN4}}$
33	P65/FTID/CIN5/$\overline{\text{KIN5}}$	P65/FTID/CIN5/$\overline{\text{KIN5}}$	P65/FTID/CIN5/$\overline{\text{KIN5}}$
34	P66/FTOB/CIN6/$\overline{\text{KIN6}}$/ $\overline{\text{IRQ6}}$	P66/FTOB/CIN6/$\overline{\text{KIN6}}$/ $\overline{\text{IRQ6}}$	P66/FTOB/CIN6/$\overline{\text{KIN6}}$/ $\overline{\text{IRQ6}}$
35	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$
36	AVref	AVref	AVref
37	AVCC	AVCC	AVCC
38	P70/AN0	P70/AN0	P70/AN0
39	P71/AN1	P71/AN1	P71/AN1
40	P72/AN2	P72/AN2	P72/AN2
41	P73/AN3	P73/AN3	P73/AN3
42	P74/AN4	P74/AN4	P74/AN4
43	P75/AN5	P75/AN5	P75/AN5
44	P76/AN6/DA0	P76/AN6/DA0	P76/AN6/DA0
45	P77/AN7/DA1	P77/AN7/DA1	P77/AN7/DA1
46	AVSS	AVSS	AVSS
47 (B)	PA1/CIN9/$\overline{\text{KIN9}}$	A17/PA1/CIN9/$\overline{\text{KIN9}}$	PA1/CIN9/$\overline{\text{KIN9}}$
48 (B)	PA0/CIN8/$\overline{\text{KIN8}}$	A16/PA0/CIN8/$\overline{\text{KIN8}}$	PA0/CIN8/$\overline{\text{KIN8}}$
49	P40/TMCI0/TxD2/IrTxD	P40/TMCI0/TxD2/IrTxD	P40/TMCI0/TxD2/IrTxD
50	P41/TMO0/RxD2/IrRxD	P41/TMO0/RxD2/IrRxD	P41/TMO0/RxD2/IrRxD
51	P42/TMRI0/SCK2	P42/TMRI0/SCK2	P42/TMRI0/SCK2
52	P43/TMCI1	P43/TMCI1	P43/TMCI1
53	P44/TMO1	P44/TMO1	P44/TMO1
54	P45/TMRI1	P45/TMRI1	P45/TMRI1

Pin No.	Pin Name: Extended Modes	Pin Name: Single-Chip Modes
FP-100B TFP-100B	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)
55	P46/PWX0	P46/PWX0	P46/PWX0
56	P47/PWX1	P47/PWX1	P47/PWX1
57	PB7/D7	PB7/D7	PB7
58	PB6/D6	PB6/D6	PB6
59	VCC	VCC	VCC
60	A15	A15/P27	P27
61	A14	A14/P26	P26
62	A13	A13/P25	P25
63	A12	A12/P24	P24
64	A11	A11/P23	P23
65	A10	A10/P22	P22
66	A9	A9/P21	P21
67	A8	A8/P20	P20
68	PB5/D5	PB5/D5	PB5
69	PB4/D4	PB4/D4	PB4
70	VSS	VSS	VSS
71	VSS	VSS	VSS
72	A7	A7/P17	P17
73	A6	A6/P16	P16
74	A5	A5/P15	P15
75	A4	A4/P14	P14
76	A3	A3/P13	P13
77	A2	A2/P12	P12
78	A1	A1/P11	P11
79	A0	A0/P10	P10
80	PB3/D3	PB3/D3	PB3
81	PB2/D2	PB2/D2	PB2
82	D8	D8	P30

Pin No.	Pin Name: Extended Modes		Pin Name: Single-Chip Modes
FP-100B TFP-100B	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)
83	D9	D9	P31
84	D10	D10	P32
85	D11	D11	P33
86	D12	D12	P34
87	D13	D13	P35
88	D14	D14	P36
89	D15	D15	P37
90	PB1/D1	PB1/D1	PB1
91	PB0/D0	PB0/D0	PB0
92	VSS	VSS	VSS
93	P80	P80	P80
94	P81	P81	P81
95	P82	P82	P82
96	P83	P83	P83
97	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1
98	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1
99	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1
100	$\overline{\text{RESO}}$	$\overline{\text{RESO}}$	$\overline{\text{RESO}}$

Note: * The (B) in Pin No. means that the VCCB is supplied.

Table 1.2 Pin Functions of H8S/2134B in Each Operating Mode

Pin No.	Pin Name: Extended Modes		Pin Name: Single-Chip Modes
FP-80A TFP-80C	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)
1	$\overline{\text{RES}}$	$\overline{\text{RES}}$	$\overline{\text{RES}}$
2	XTAL	XTAL	XTAL
3	EXTAL	EXTAL	EXTAL
4	MD1	MD1	MD1
5	MD0	MD0	MD0
6	NMI	NMI	NMI
7	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$	$\overline{\text{STBY}}$
8	VCL	VCL	VCL
9	P52/SCK0	P52/SCK0	P52/SCK0
10	P51/RxD0	P51/RxD0	P51/RxD0
11	P50/TxD0	P50/TxD0	P50/TxD0
12	VSS	VSS	VSS
13	P97/$\overline{\text{WAIT}}$	P97/$\overline{\text{WAIT}}$	P97
14	P96/ϕ/EXCL	P96/ϕ/EXCL	P96/ϕ/EXCL
15	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	$\overline{\text{AS}}$/$\overline{\text{IOS}}$	P95
16	$\overline{\text{WR}}$	$\overline{\text{WR}}$	P94
17	$\overline{\text{RD}}$	$\overline{\text{RD}}$	P93
18	P92/$\overline{\text{IRQ0}}$	P92/$\overline{\text{IRQ0}}$	P92/$\overline{\text{IRQ0}}$
19	P91/$\overline{\text{IRQ1}}$	P91/$\overline{\text{IRQ1}}$	P91/$\overline{\text{IRQ1}}$
20	P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$	P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$	P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$
21	P60/FTCI/CIN0/$\overline{\text{KIN0}}$	P60/FTCI/CIN0/$\overline{\text{KIN0}}$	P60/FTCI/CIN0/$\overline{\text{KIN0}}$
22	P61/FTOA/CIN1/$\overline{\text{KIN1}}$	P61/FTOA/CIN1/$\overline{\text{KIN1}}$	P61/FTOA/CIN1/$\overline{\text{KIN1}}$
23	P62/FTIA/CIN2/$\overline{\text{KIN2}}$/ TMIY	P62/FTIA/CIN2/$\overline{\text{KIN2}}$/ TMIY	P62/FTIA/CIN2/$\overline{\text{KIN2}}$/ TMIY
24	P63/FTIB/CIN3/$\overline{\text{KIN3}}$	P63/FTIB/CIN3/$\overline{\text{KIN3}}$	P63/FTIB/CIN3/$\overline{\text{KIN3}}$
25	P64/FTIC/CIN4/$\overline{\text{KIN4}}$	P64/FTIC/CIN4/$\overline{\text{KIN4}}$	P64/FTIC/CIN4/$\overline{\text{KIN4}}$
26	P65/FTID/CIN5/$\overline{\text{KIN5}}$	P65/FTID/CIN5/$\overline{\text{KIN5}}$	P65/FTID/CIN5/$\overline{\text{KIN5}}$

Pin No.	Pin Name: Extended Modes		Pin Name: Single-Chip Modes
FP-80A TFP-80C	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)
27	P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$	P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$	P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$
28	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$
29	AVCC	AVCC	AVCC
30	P70/AN0	P70/AN0	P70/AN0
31	P71/AN1	P71/AN1	P71/AN1
32	P72/AN2	P72/AN2	P72/AN2
33	P73/AN3	P73/AN3	P73/AN3
34	P74/AN4	P74/AN4	P74/AN4
35	P75/AN5	P75/AN5	P75/AN5
36	P76/AN6/DA0	P76/AN6/DA0	P76/AN6/DA0
37	P77/AN7/DA1	P77/AN7/DA1	P77/AN7/DA1
38	AVSS	AVSS	AVSS
39	P40/TMCI0/TxD2/IrTxD	P40/TMCI0/TxD2/IrTxD	P40/TMCI0/TxD2/IrTxD
40	P41/TMO0/RxD2/IrRxD	P41/TMO0/RxD2/IrRxD	P41/TMO0/RxD2/IrRxD
41	P42/TMRI0/SCK2	P42/TMRI0/SCK2	P42/TMRI0/SCK2
42	P43/TMCI1	P43/TMCI1	P43/TMCI1
43	P44/TMO1	P44/TMO1	P44/TMO1
44	P45/TMRI1	P45/TMRI1	P45/TMRI1
45	P46/PWX0	P46/PWX0	P46/PWX0
46	P47/PWX1	P47/PWX1	P47/PWX1
47	VCC	VCC	VCC
48	A15	A15/P27	P27
49	A14	A14/P26	P26
50	A13	A13/P25	P25
51	A12	A12/P24	P24
52	A11	A11/P23	P23
53	A10	A10/P22	P22

Pin No.	Pin Name: Extended Modes		Pin Name: Single-Chip Modes
FP-80A TFP-80C	Mode 1	Mode 2 (EXPE = 1) Mode 3 (EXPE = 1)	Mode 2 (EXPE = 0) Mode 3 (EXPE = 0)
54	A9	A9/P21	P21
55	A8	A8/P20	P20
56	VSS	VSS	VSS
57	A7	A7/P17	P17
58	A6	A6/P16	P16
59	A5	A5/P15	P15
60	A4	A4/P14	P14
61	A3	A3/P13	P13
62	A2	A2/P12	P12
63	A1	A1/P11	P11
64	A0	A0/P10	P10
65	D0	D0	P30
66	D1	D1	P31
67	D2	D2	P32
68	D3	D3	P33
69	D4	D4	P34
70	D5	D5	P35
71	D6	D6	P36
72	D7	D7	P37
73	VSS	VSS	VSS
74	P80	P80	P80
75	P81	P81	P81
76	P82	P82	P82
77	P83	P83	P83
78	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1	P84/$\overline{\text{IRQ3}}$/TxD1
79	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1	P85/$\overline{\text{IRQ4}}$/RxD1
80	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1	P86/$\overline{\text{IRQ5}}$/SCK1

1.3.3 Pin Functions

Table 1.3 Pin Functions

Type	Symbol	Pin No. [H8S/2144B] FP-100B, TFP-100B	Pin No. [H8S/2134B] FP-80A, TFP-80C	I/O	Name and Function
Power	VCC	59	47	I	Power supply pin. Connect this pin to the system power supply.
	VCL	9	8	I	Pin for connecting an external capacitor for the internal step-down circuit. This pin should be connected to the VSS via the external capacitor. Do not connect to the VCC. For details, see section 20, Electrical Characteristics.
	VCCB	4	—	I	The power supply pin for the input/output buffers of port A. Available only for the H8S/2144B.
	VSS	15, 70, 71, 92	12, 56, 73	I	Ground pins. Connect all the pins to the system power supply (0 V).
Clock	XTAL	2	2	I	Pins for connection to a crystal resonator. An external clock can be input on the EXTAL pin. See section 17, Clock Pulse Generator, for typical connection diagrams.
	EXTAL	3	3	I	
	φ	17	14	O	Supplies the system clock to external devices.
	EXCL	17	14	I	Input an external 32.768-kHz clock for the subclock.
Operating mode control	MD1, MD0	5, 6	4, 5	I	These pins set the operating mode. The relationship between these signals and the operating mode is shown below. Signal levels on these pins should not be changed during operation.

MD1	MD0	Operating Mode
0	1	Mode 1
		Normal
		On-chip ROM disabled extended mode
1	0	Mode 2
		Advanced
		On-chip ROM enabled extended mode
		Single-chip mode
1	1	Mode 3
		Normal
		On-chip ROM enabled extended mode
		Single-chip mode

Type	Symbol	Pin No. [H8S/2144B] FP-100B, TFP-100B	Pin No. [H8S/2134B] FP-80A, TFP-80C	I/O	Name and Function
System control	$\overline{\text{RES}}$	1	1	I	Reset pin. When this signal is driven low, this LSI enters the reset state.
	$\overline{\text{RESO}}$	100	—	O	Outputs a reset to external devices. Available only for the H8S/2144B.
	$\overline{\text{STBY}}$	8	7	I	When this signal is driven low, a transition is made to the hardware standby mode.
Address bus	A23 to A16	10, 11, 20, 21, 30, 31, 47, 48	—	O	Address output pins when an 16-bit access space is used. Available only for the H8S/2144B.
	A15 to A0	60 to 67, 72 to 79	48 to 55, 57 to 64	O	Address output pins
Data bus	D15 to D8	89 to 82	—	I/O	Bidirectional bus for data accessed in units of 8 bits or for the upper byte data accessed in units of 16 bits. Available only for the H8S/2144B.
	D7 to D0	57, 58, 68, 69, 80, 81, 90, 91	72 to 65	I/O	Bidirectional bus for the lower byte data accessed in units of 16 bits in the H8S/2144B. Bidirectional bus for data accessed in units of 8 bits in the H8S/2134B.
Bus control	$\overline{\text{WAIT}}$	16	13	I	Requests insertion of a wait in the bus cycle when accessing the external 3-state address space.
	$\overline{\text{RD}}$	22	17	O	When the signal level is low, it indicates that the external address space is being read from.
	$\overline{\text{WR}}$	—	16	O	When the signal level is low, it indicates that the external address space is being written to. Available only for the H8S/2134B.
	$\overline{\text{HWR}}$	19	—	O	When the signal level is low, it indicates that the external address space is being written to. The upper byte of the data bus is valid. Available only for the H8S/2144B.
	$\overline{\text{LWR}}$	25	—	O	When the signal level is low, it indicates that the external address space is being written to. The lower byte of the data bus is valid. Available only for the H8S/2144B.

Type	Symbol	Pin No. [H8S/2144B] FP-100B, TFP-100B	Pin No. [H8S/2134B] FP-80A, TFP-80C	I/O	Name and Function
Bus control	$\overline{AS}$/$\overline{IOS}$	18	15	O	Strobe signal. When the signal level is low, it indicates that address outputs on the address bus is valid or an I/O select signal is output. Set the register to select the function to be used.
Interrupt signals	NMI	7	6	I	Input pin for a nonmaskable interrupt request.
	$\overline{IRQ0}$ to $\overline{IRQ7}$	23 to 25, 97 to 99, 34, 35	18 to 20 78 to 80, 27, 28	I	Input pins for maskable interrupts.
16-bit free-running timer (FRT)	FTCI	26	21	I	The counter clock input pin.
	FTOA	27	22	O	The output compare A output pin.
	FTOB	34	27	O	The output compare B output pin.
	FTIA	28	23	I	The input capture A input pin.
	FTIB	29	24	I	The input capture B input pin.
	FTIC	32	25	I	The input capture C input pin.
	FTID	33	26	I	The input capture D input pin.
8-bit timer (TMR_0, TMR_1, TMR_Y)	TMO0 TMO1	50 53	40 43	O	The waveform output pins for the output compare function.
	TMCI0 TMCI1	49 52	39 42	I	Input pins for the external clock input to counters.
	TMRI0 TMRI1	51 54	41 44	I	The counter reset input pins.
	TMIY	28	23	I	The counter clock input pin or reset input pin.
14-bit PWM timer (PWMX)	PWX0 PWX1	55 56	45 46	O	PWM D/A pulse output pins.
Serial communi-cation interface (SCI_0, SCI_1, SCI_2)	TxD0 TxD1 TxD2	14 97 49	11 78 39	O	Transmit data output pins.
	RxD0 RxD1 RxD2	13 98 50	10 79 40	I	Receive data input pins.
	SCK0 SCK1 SCK2	12 99 51	9 80 41	I/O	Clock input/output pins. The output type is NMOS push-pull.

Type	Symbol	Pin No. [H8S/2144B] FP-100B, TFP-100B	Pin No. [H8S/2134B] FP-80A, TFP-80C	I/O	Name and Function
SCI with IrDA (SCI_2)	IrTxD	49	39	O	Input and output pins for data encoded for IrDA use.
	IrRxD	50	40	I	
Keyboard buffer controller	[H8S/2144B] $\overline{KIN15}$ to $\overline{KIN0}$ [H8S/2134B] $\overline{KIN7}$ to $\overline{KIN0}$	10, 11, 20, 21, 30, 31, 47, 48, 35 to 32, 29 to 26	28 to 21	I	Input pins for a matrix keyboard. Normally, P10 to P17 and P20 to P27 are used for key scanning outputs. Up to 256-key matrix (16 × 16) in the H8S/2144B or up to 128-key matrix (16 × 8) can be configured.
A/D converter	AN7 to AN0	45 to 38	37 to 30	I	Analog input pins for the A/D converter.
	[H8S/2144B] CIN15 to CIN0 [H8S/2134B] CIN7 to CIN0	10, 11, 20, 21, 30, 31, 47, 48, 35 to 32, 29 to 26	28 to 21	I	Extended A/D conversion input pins. Since these pins are also used as digital input/output pins, accuracy will fall.
	$\overline{ADTRG}$	25	20	I	Pin for input of an external trigger to start A/D conversion.
D/A converter	DA0 DA1	44 45	36 37	O	Analog output pins for the D/A converter.
A/D converter D/A converter	AVCC	37	29	I	The analog power supply pin for the A/D converter and D/A converter. When neither the A/D nor D/A converters are used, this pin should be connected to the system power supply (+5 V).
	AVref	36	—	I	The reference voltage pin for the A/D converter and D/A converter. Available only for the H8S/2144B. When neither the A/D nor D/A converters are used, this pin should be connected to the system power supply (+5 V).
	AVSS	46	38	I	The ground pin for the A/D converter and D/A converter. This pin should be connected to the system power supply (0 V).

Type	Symbol	Pin No. [H8S/2144B] FP-100B, TFP-100B	Pin No. [H8S/2134B] FP-80A, TFP-80C	I/O	Name and Function
I/O ports	P17 to P10	72 to 79	57 to 64	I/O	8-bit input/output pins with input pull-up MOSs. These pins can drive LED signals.
	P27 to P20	60 to 67	48 to 55	I/O	8-bit input/output pins with input pull-up MOSs. These pins can drive LED signals.
	P37 to P30	89 to 82	72 to 65	I/O	8-bit input/output pins with input pull-up MOSs. These pins can drive LED signals.
	P47 to P40	56 to 49	46 to 39	I/O	8-bit input/output pins
	P52 to P50	12 to 14	9 to 11	I/O	3-bit input/output pins
	P67 to P60	35 to 32 29 to 26	28 to 21	I/O	8-bit input/output pins with input pull-up MOSs
	P77 to P70	45 to 38	37 to 30	I	8-bit input pins
	P86 to P80	99 to 93	80 to 74	I/O	7-bit input/output pins
	P97 to P90	16 to 19 22 to 25	13 to 20	I/O	8-bit input/output pins
	PA7 to PA0	10, 11, 20, 21, 30, 31, 47, 48	—	I/O	8-bit input/output pins with input pull-up MOSs. The VCCB is supplied to these pins. Available only for the H8S/2144B.
	PB7 to PB0	57, 58, 68, 69, 80, 81, 90, 91	—	I/O	8-bit input/output pins with input pull-up MOSs. Available only for the H8S/2144B.

Section 2 CPU

The H8S/2000 CPU is a high-speed central processing unit with an internal 32-bit architecture that is upward-compatible with the H8/300 and H8/300H CPUs. The H8S/2000 CPU has sixteen 16-bit general registers, can address a 16-Mbyte linear address space, and is ideal for realtime control.

This section describes the H8S/2000 CPU. The usable modes and address spaces differ depending on the product. For details on each product, refer to section 3, MCU Operating Modes.

2.1 Features

- Upward-compatibility with H8/300 and H8/300H CPUs
  Can execute H8/300 CPU and H8/300H CPU object programs
- General-register architecture
  Sixteen 16-bit general registers also usable as sixteen 8-bit registers or eight 32-bit registers
- Sixty-five basic instructions
  8/16/32-bit arithmetic and logic instructions
  Multiply and divide instructions
  Powerful bit-manipulation instructions
- Eight addressing modes
  Register direct [Rn]
  Register indirect [@ERn]
  Register indirect with displacement [@(d:16,ERn) or @(d:32,ERn)]
  Register indirect with post-increment or pre-decrement [@ERn+ or @–ERn]
  Absolute address [@aa:8, @aa:16, @aa:24, or @aa:32]
  Immediate [#xx:8, #xx:16, or #xx:32]
  Program-counter relative [@(d:8,PC) or @(d:16,PC)]
  Memory indirect [@@aa:8]
- 16-Mbyte address space
  Program: 16 Mbytes
  Data: 16 Mbytes
- High-speed operation
  All frequently-used instructions are executed in one or two states
  8/16/32-bit register-register add/subtract: 1 state
  8 × 8-bit register-register multiply: 12 states (MULXU.B), 13 states (MULXS.B)
  16 ÷ 8-bit register-register divide: 12 states (DIVXU.B)

16 × 16-bit register-register multiply: 20 states (MULXU.W), 21 states (MULXS.W)
32 ÷ 16-bit register-register divide: 20 states (DIVXU.W)

- Two CPU operating modes
  Normal mode
  Advanced mode
- Power-down state
  Transition to power-down state by SLEEP instruction
  Selectable CPU clock speed

2.1.1 Differences between H8S/2600 CPU and H8S/2000 CPU

The differences between the H8S/2600 CPU and the H8S/2000 CPU are as shown below.

- Register configuration
  The MAC register is supported only by the H8S/2600 CPU.
- Basic instructions
  The four instructions MAC, CLRMAC, LDMAC, and STMAC are supported only by the H8S/2600 CPU.
- The number of execution states of the MULXU and MULXS instructions

		Execution States	
Instruction	**Mnemonic**	**H8S/2600**	**H8S/2000**
MULXU	MULXU.B Rs, Rd	3	12
	MULXU.W Rs, ERd	4	20
MULXS	MULXS.B Rs, Rd	4	13
	MULXS.W Rs, ERd	5	21

In addition, there are differences in address space, CCR and EXR register functions, power-down modes, etc., depending on the model.

2.1.2 Differences from H8/300 CPU

In comparison to the H8/300 CPU, the H8S/2000 CPU has the following enhancements.

- More general registers and control registers
  Eight 16-bit extended registers and one 8-bit control register have been added.
- Expanded address space

Normal mode supports the same 64-kbyte address space as the H8/300 CPU.
Advanced mode supports a maximum 16-Mbyte address space.

- Enhanced addressing
  The addressing modes have been enhanced to make effective use of the 16-Mbyte address space.
- Enhanced instructions
  Addressing modes of bit-manipulation instructions have been enhanced.
  Signed multiply and divide instructions have been added.
  Two-bit shift and two-bit rotate instructions have been added.
  Instructions for saving and restoring multiple registers have been added.
  A test and set instruction has been added.
- Higher speed
  Basic instructions are executed twice as fast.

2.1.3 Differences from H8/300H CPU

In comparison to the H8/300H CPU, the H8S/2000 CPU has the following enhancements.

- Additional control register
  One 8-bit control register has been added.
- Enhanced instructions
  Addressing modes of bit-manipulation instructions have been enhanced.
  Two-bit shift and two-bit rotate instructions have been added.
  Instructions for saving and restoring multiple registers have been added.
  A test and set instruction has been added.
- Higher speed
  Basic instructions are executed twice as fast.

2.2 CPU Operating Modes

The H8S/2000 CPU has two operating modes: normal and advanced. Normal mode supports a maximum 64-kbyte address space. Advanced mode supports a maximum 16-Mbyte address space. The mode is selected by the LSI's mode pins.

2.2.1 Normal Mode

The exception vector table and stack have the same structure as in the H8/300 CPU in normal mode.

- Address space

  Linear access to a maximum address space of 64 kbytes is possible.
- Extended registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers.

  When extended register En is used as a 16-bit register it can contain any value, even when the corresponding general register (Rn) is used as an address register. (If general register Rn is referenced in the register indirect addressing mode with pre-decrement (@–Rn) or post-increment (@Rn+) and a carry or borrow occurs, the value in the corresponding extended register (En) will be affected.)
- Instruction set

  All instructions and addressing modes can be used. Only the lower 16 bits of effective addresses (EA) are valid.
- Exception vector table and memory indirect branch addresses

  In normal mode, the top area starting at H'0000 is allocated to the exception vector table. One branch address is stored per 16 bits. The exception vector table in normal mode is shown in figure 2.1. For details on the exception vector table, see section 4, Exception Handling.

  The memory indirect addressing mode (@@aa:8) employed in the JMP and JSR instructions uses an 8-bit absolute address included in the instruction code to specify a memory operand that contains a branch address. In normal mode, the operand is a 16-bit (word) operand, providing a 16-bit branch address. Branch addresses can be stored in the top area from H'0000 to H'00FF. Note that this area is also used for the exception vector table.
- Stack structure

  In normal mode, when the program counter (PC) is pushed onto the stack in a subroutine call in normal mode, and the PC and condition-code register (CCR) are pushed onto the stack in exception handling, they are stored as shown in figure 2.2. The extended control register (EXR) is not pushed onto the stack. For details, see section 4, Exception Handling.

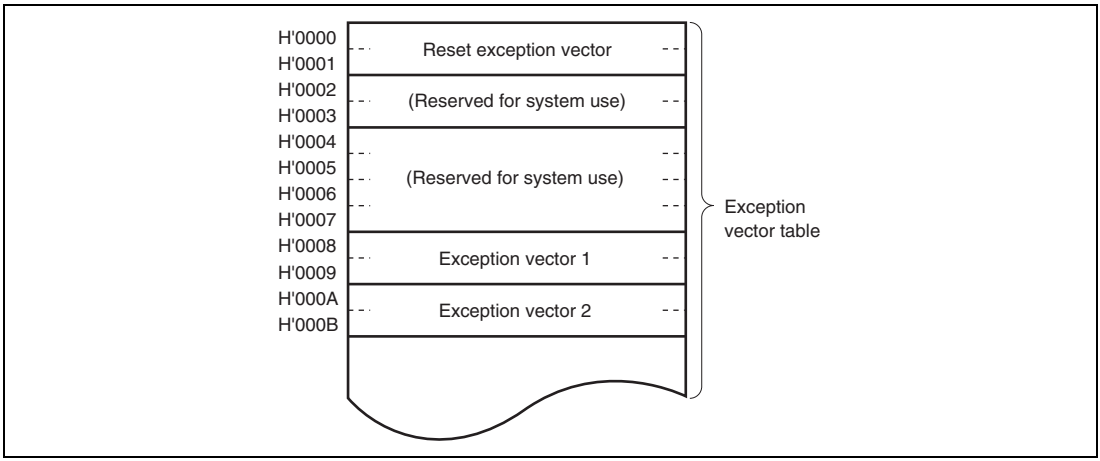


Figure 2.1 Exception Vector Table (Normal Mode)

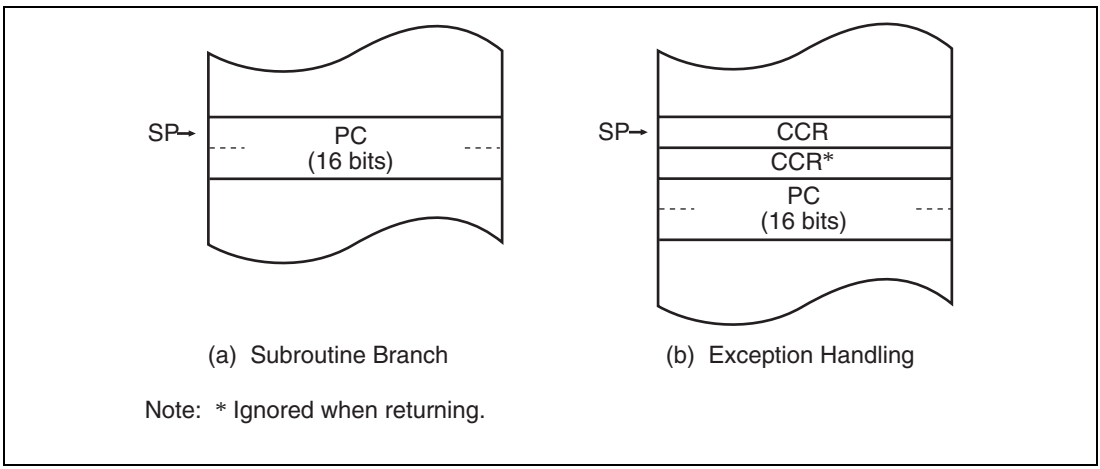


Figure 2.2 Stack Structure in Normal Mode

2.2.2 Advanced Mode

- Address space

  Linear access to a maximum address space of 16 Mbytes is possible.
- Extended registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers. They can also be used as the upper 16-bit segments of 32-bit registers or address registers.
- Instruction set

  All instructions and addressing modes can be used.
- Exception vector table and memory indirect branch addresses

  In advanced mode, the top area starting at H'00000000 is allocated to the exception vector table in 32-bit units. In each 32 bits, the upper 8 bits are ignored and a branch address is stored in the lower 24 bits (see figure 2.3). For details on the exception vector table, see section 4, Exception Handling.

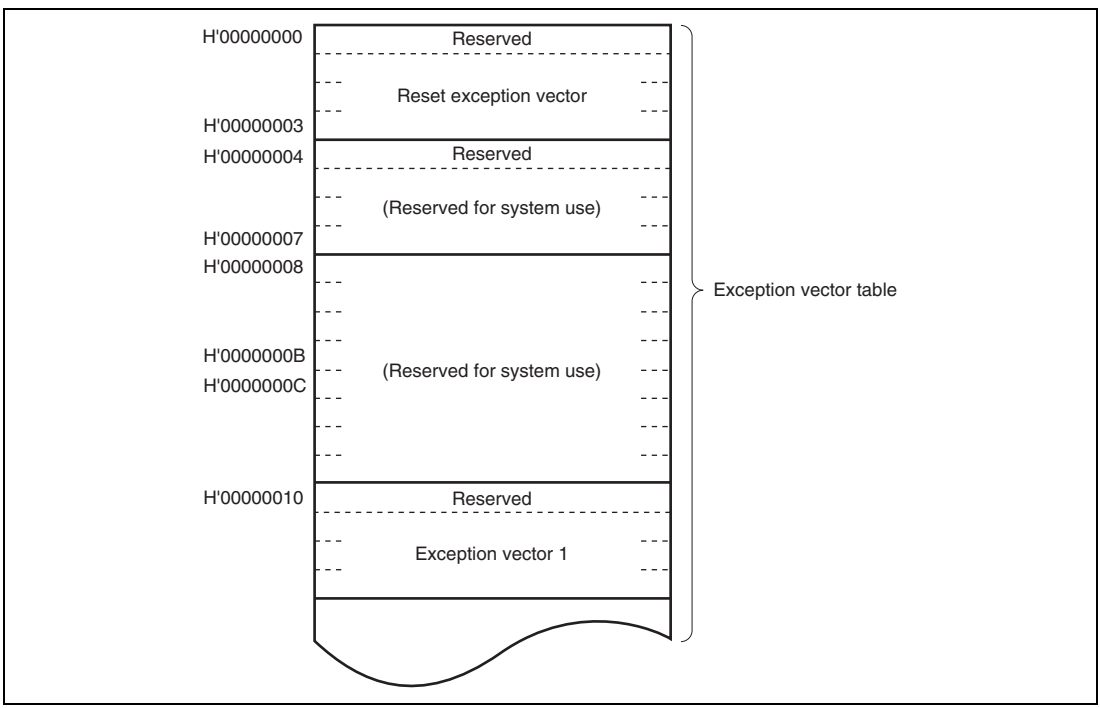


Figure 2.3 Exception Vector Table (Advanced Mode)

The memory indirect addressing mode (@@aa:8) employed in the JMP and JSR instructions uses an 8-bit absolute address included in the instruction code to specify a memory operand that contains a branch address. In advanced mode, the operand is a 32-bit longword operand, providing a 32-bit branch address. The upper 8 bits of these 32 bits are a reserved area that is regarded as H'00. Branch addresses can be stored in the area from H'00000000 to H'000000FF. Note that the top area of this range is also used for the exception vector table.

- Stack structure

  In advanced mode, when the program counter (PC) is pushed onto the stack in a subroutine call, and the PC and condition-code register (CCR) are pushed onto the stack in exception handling, they are stored as shown in figure 2.4. The extended control register (EXR) is not pushed onto the stack. For details, see section 4, Exception Handling.

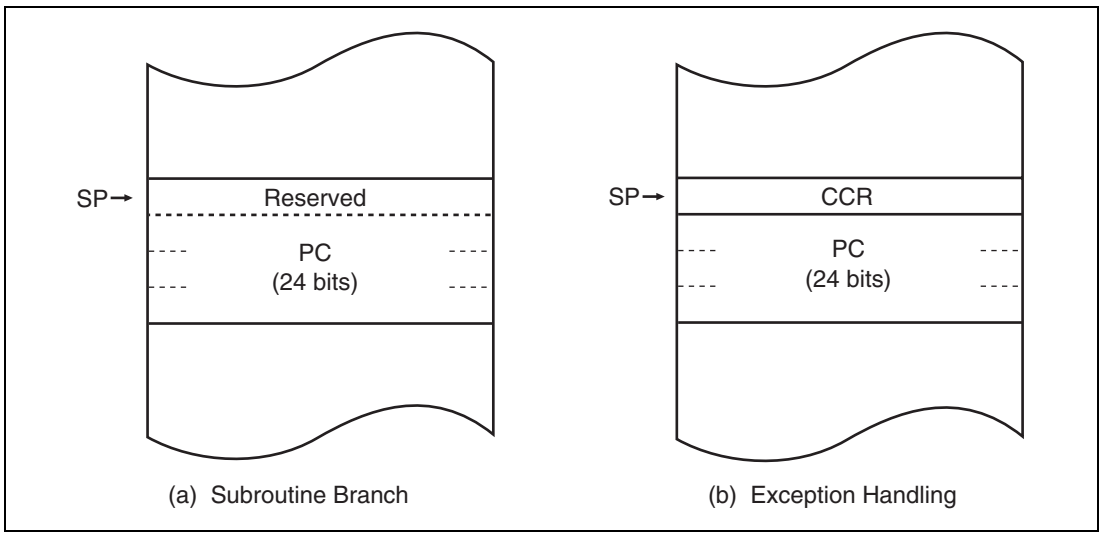


Figure 2.4 Stack Structure in Advanced Mode

2.3 Address Space

Figure 2.5 shows a memory map of the H8S/2000 CPU. The H8S/2000 CPU provides linear access to a maximum 64-kbyte address space in normal mode, and a maximum 16-Mbyte (architecturally 4-Gbyte) address space in advanced mode. The usable modes and address spaces differ depending on the product. For details on each product, refer to section 3, MCU Operating Modes.

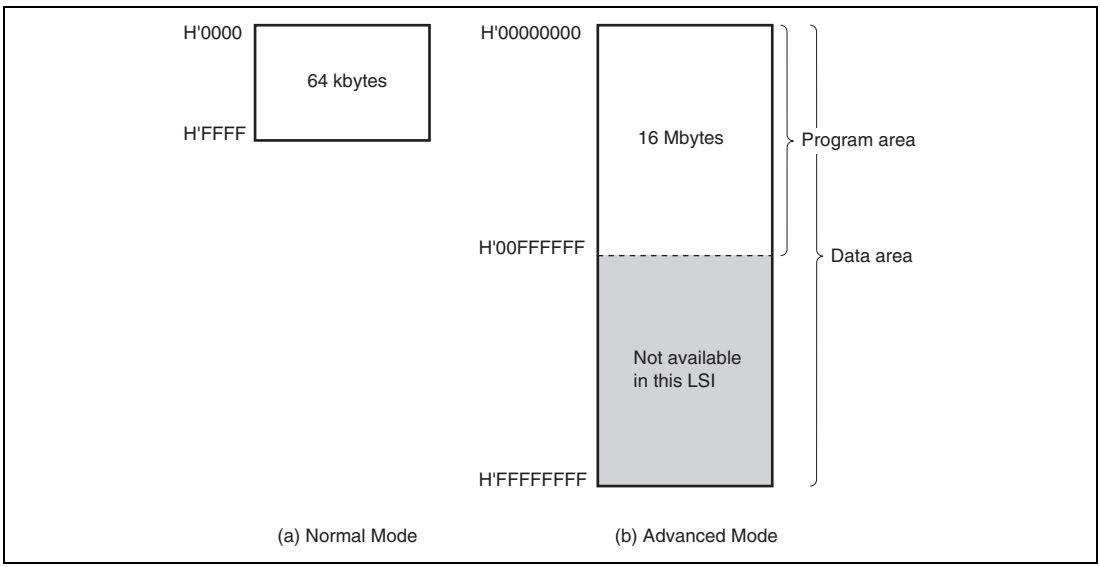


Figure 2.5 Memory Map

2.4 Register Configuration

The H8S/2000 CPU has the internal registers shown in figure 2.6. There are two types of registers: general registers and control registers. Control registers are a 24-bit program counter (PC), an 8-bit extended control register (EXR), and an 8-bit condition code register (CCR).

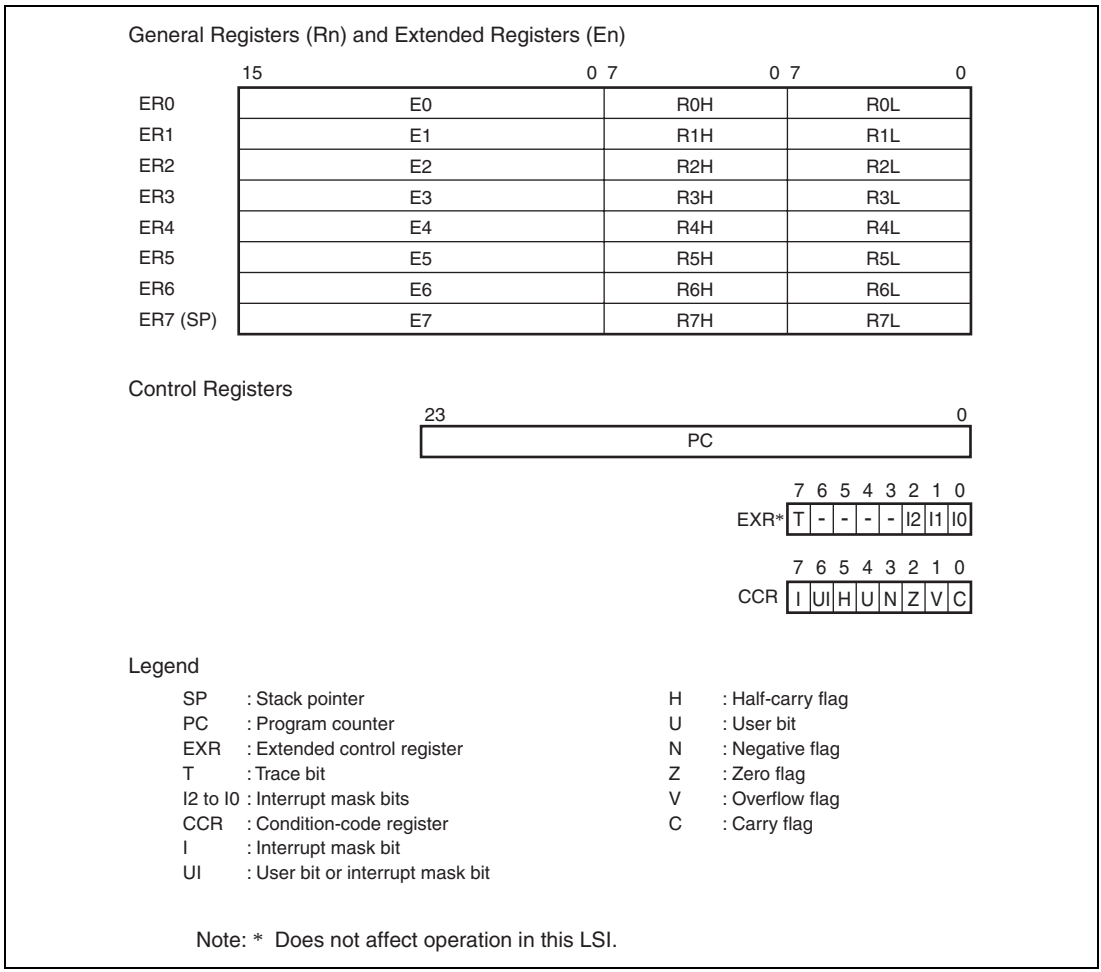


Figure 2.6 CPU Internal Registers

2.4.1 General Registers

The H8S/2000 CPU has eight 32-bit general registers. These general registers are all functionally alike and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.7 illustrates the usage of the general registers.

When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

When the general registers are used as 16-bit registers, the ER registers are divided into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

When the general registers are used as 8-bit registers, the R registers are divided into 8-bit general registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum sixteen 8-bit registers.

The usage of each register can be selected independently.

General register ER7 has the function of the stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.8 shows the stack.

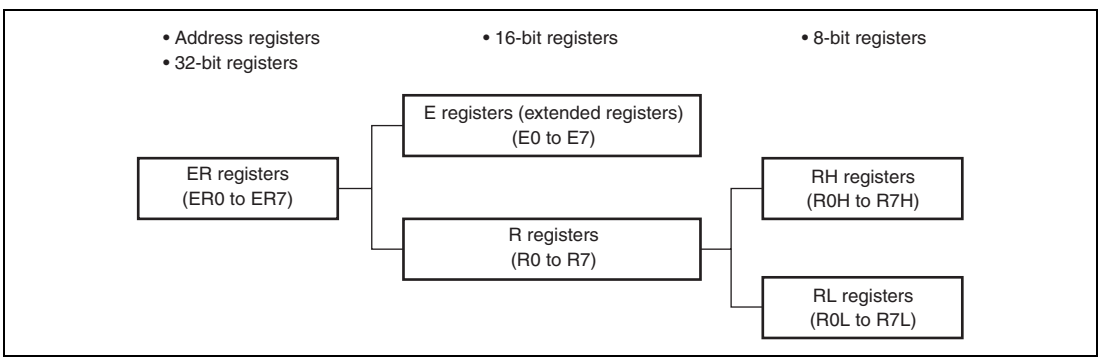


Figure 2.7 Usage of General Registers

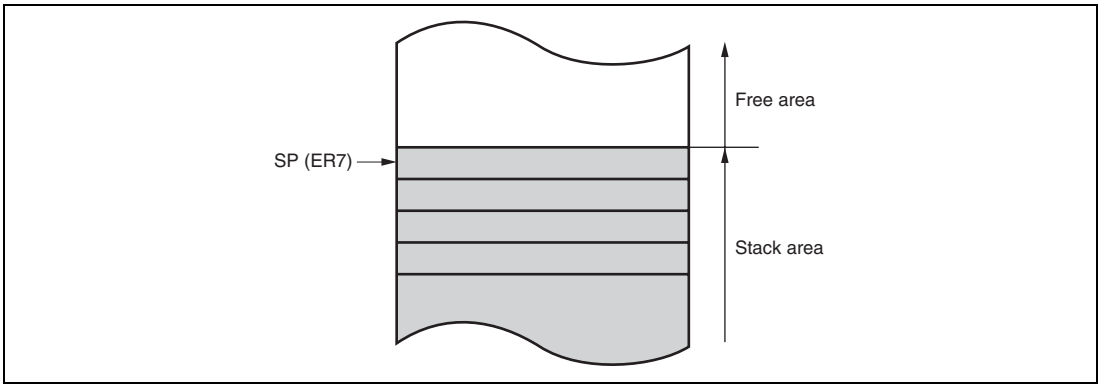


Figure 2.8 Stack

2.4.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched for read, the least significant PC bit is regarded as 0.)

2.4.3 Extended Control Register (EXR)

EXR does not affect operation in this LSI.

Bit	Bit Name	Initial Value	R/W	Description
7	T	0	R/W	Trace Bit Does not affect operation in this LSI.
6 to 3	—	All 1	R	Reserved These bits are always read as 1.
2 to 0	I2 I1 I0	All 1	R/W	Interrupt Mask Bits 2 to 0 Do not affect operation in this LSI.

2.4.4 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. Operations can be performed on the CCR bits by the LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as branching conditions for conditional branch (Bcc) instructions.

Bit	Bit Name	Initial Value	R/W	Description
7	I	1	R/W	Interrupt Mask Bit Masks interrupts other than NMI when set to 1. NMI is accepted regardless of the I bit setting. The I bit is set to 1 at the start of an exception-handling sequence. For details, refer to section 5, Interrupt Controller.
6	UI	Undefined	R/W	User Bit or Interrupt Mask Bit Can be written to and read from by software using the LDC, STC, ANDC, ORC, and XORC instructions.
5	H	Undefined	R/W	Half-Carry Flag When the ADD.B, ADDX.B, SUB.B, SUBX.B, CMP.B or NEG.B instruction is executed, this flag is set to 1 if there is a carry or borrow at bit 3, and cleared to 0 otherwise. When the ADD.W, SUB.W, CMP.W, or NEG.W instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 11, and cleared to 0 otherwise. When the ADD.L, SUB.L, CMP.L, or NEG.L instruction is executed, the H flag is set to 1 if there is a carry or borrow at bit 27, and cleared to 0 otherwise.
4	U	Undefined	R/W	User Bit Can be written to and read from by software using the LDC, STC, ANDC, ORC, and XORC instructions.
3	N	Undefined	R/W	Negative Flag Stores the value of the most significant bit of data as a sign bit.
2	Z	Undefined	R/W	Zero Flag Set to 1 to indicate zero data, and cleared to 0 to indicate non-zero data.
1	V	Undefined	R/W	Overflow Flag Set to 1 when an arithmetic overflow occurs, and cleared to 0 otherwise.
0	C	Undefined	R/W	Carry Flag Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by • Add instructions, to indicate a carry • Subtract instructions, to indicate a borrow • Shift and rotate instructions, to indicate a carry The carry flag is also used as a bit accumulator by bit manipulation instructions.

2.4.5 Initial Register Values

The program counter (PC) among CPU internal registers is initialized when reset exception handling loads a start address from a vector table. The trace (T) bit in EXR is cleared to 0, and the interrupt mask (I) bits in CCR and EXR are set to 1. The other CCR bits and the general registers are not initialized. Note that the stack pointer (ER7) is undefined. The stack pointer should therefore be initialized by an MOV.L instruction executed immediately after a reset.

2.5 Data Formats

The H8S/2000 CPU can process 1-bit, 4-bit BCD, 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.5.1 General Register Data Formats

Figure 2.9 shows the data formats of general registers.

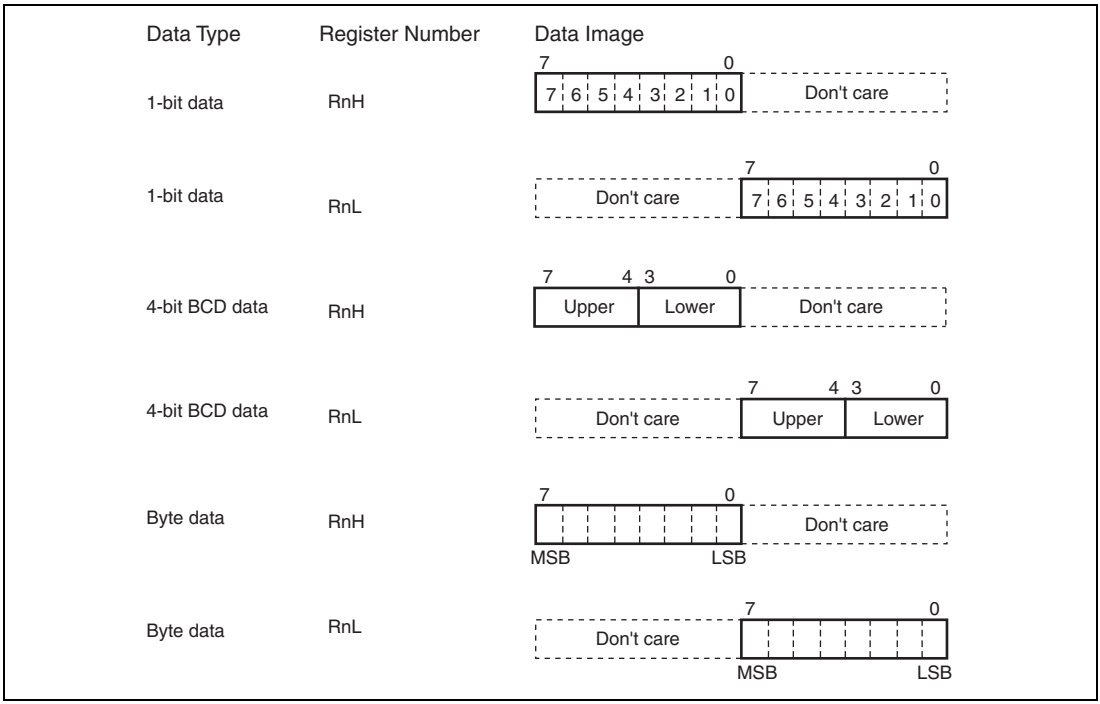


Figure 2.9 General Register Data Formats (1)

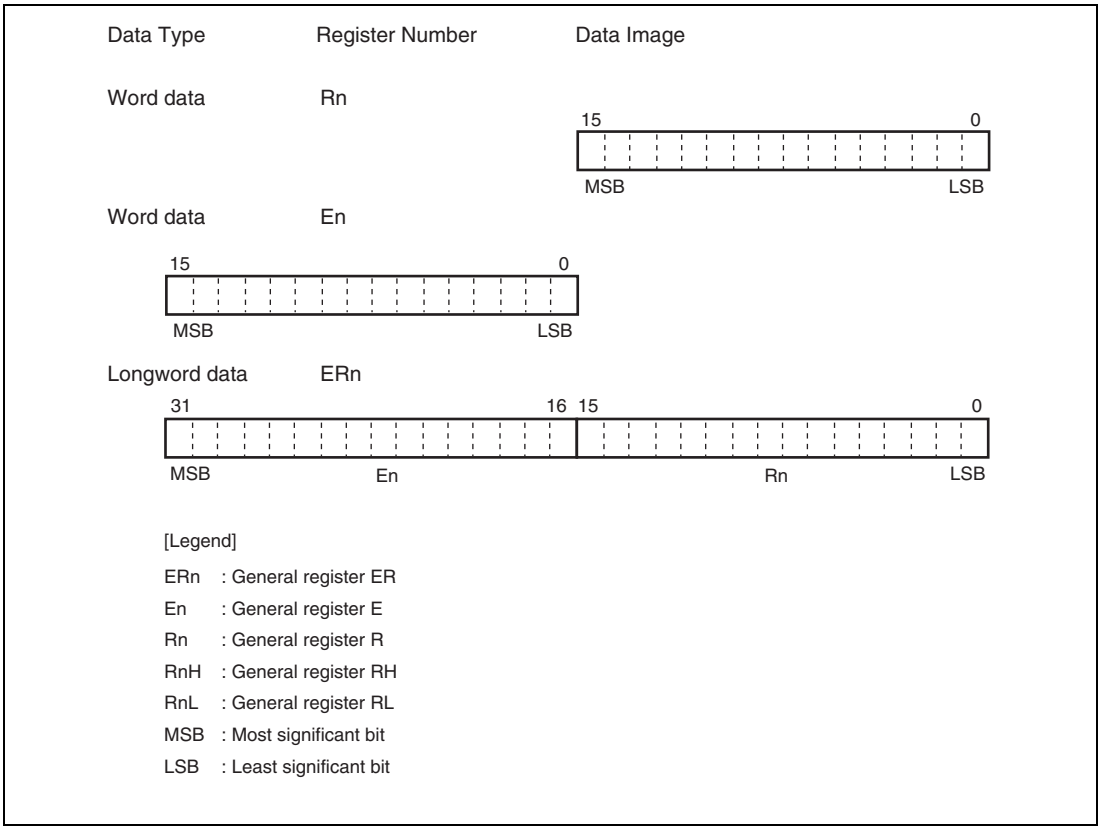


Figure 2.9 General Register Data Formats (2)

2.5.2 Memory Data Formats

Figure 2.10 shows the data formats in memory. The H8S/2000 CPU can access word data and longword data in memory, but word or longword data must begin at an even address. If an attempt is made to access word or longword data at an odd address, no address error occurs but the least significant bit of the address is regarded as 0, so the access starts at the preceding address. This also applies to instruction fetches.

When SP (ER7) is used as an address register to access the stack, the operand size should be word size or longword size.

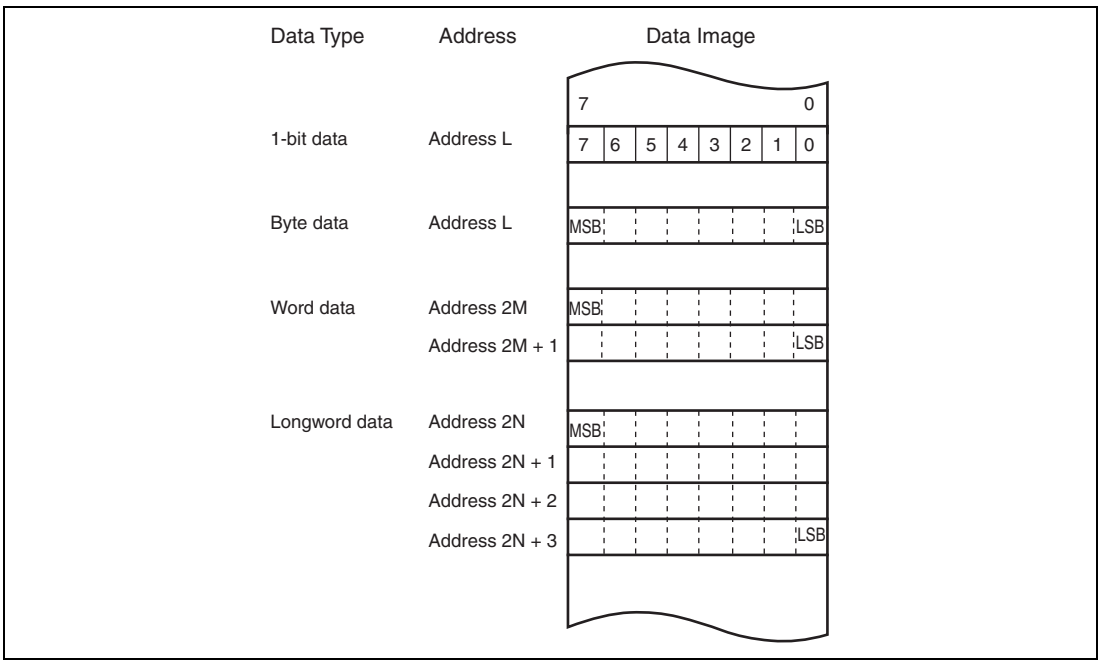


Figure 2.10 Memory Data Formats

2.6 Instruction Set

The H8S/2000 CPU has 65 types of instructions. The instructions are classified by function as shown in table 2.1.

Table 2.1 Instruction Classification

Function	Instructions	Size	Types
Data transfer	MOV	B/W/L	5
	POP*[1], PUSH*[1]	W/L	
	LDM*[5], STM*[5]	L	
	MOVFPE*[3], MOVTPE*[3]	B	
Arithmetic operations	ADD, SUB, CMP, NEG	B/W/L	19
	ADDX, SUBX, DAA, DAS	B	
	INC, DEC	B/W/L	
	ADDS, SUBS	L	
	MULXU, DIVXU, MULXS, DIVXS	B/W	
	EXTU, EXTS	W/L	
	TAS*[4]	B	
Logic operations	AND, OR, XOR, NOT	B/W/L	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	B/W/L	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BLD, BILD, BST, BIST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR	B	14
Branch	B_{CC}*[2], JMP, BSR, JSR, RTS	—	5
System control	TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	—	9
Block data transfer	EEPMOV	—	1
			Total: 65

Notes: B: Byte size; W: Word size; L: Longword size.

1. POP.W Rn and PUSH.W Rn are identical to MOV.W @SP+, Rn and MOV.W Rn, @-SP. POP.L ERn and PUSH.L ERn are identical to MOV.L @SP+, ERn and MOV.L ERn, @-SP.
2. B_{CC} is the general name for conditional branch instructions.
3. Cannot be used in this LSI.
4. When using the TAS instruction, use registers ER0, ER1, ER4, and ER5.
5. ER7 is not used as the register that can be saved (STM)/restored (LDM) when using STM/LDM instruction, because ER7 is the stack pointer.

2.6.1 Table of Instructions Classified by Function

Tables 2.3 to 2.10 summarize the instructions in each functional category. The notation used in tables 2.3 to 2.10 is defined below.

Table 2.2 Operation Notation

Symbol	Description
Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
EXR	Extended control register
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
→	Move
~	NOT (logical complement)
:8/:16/:24/:32	8-, 16-, 24-, or 32-bit length

Note: * General registers include 8-bit registers (R0H to R7H, R0L to R7L), 16-bit registers (R0 to R7, E0 to E7), and 32-bit registers (ER0 to ER7).

Table 2.3 Data Transfer Instructions

Instruction	Size*[1]	Function
MOV	B/W/L	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register.
MOVFPE	B	Cannot be used in this LSI.
MOVTPE	B	Cannot be used in this LSI.
POP	W/L	@SP+ → Rn Pops a general register from the stack. POP.W Rn is identical to MOV.W @SP+, Rn. POP.L ERn is identical to MOV.L @SP+, ERn
PUSH	W/L	Rn → @-SP Pushes a general register onto the stack. PUSH.W Rn is identical to MOV.W Rn, @-SP. PUSH.L ERn is identical to MOV.L ERn, @-SP.
LDM*[2]	L	@SP+ → Rn (register list) Pops two or more general registers from the stack.
STM*[2]	L	Rn (register list) → @-SP Pushes two or more general registers onto the stack.

Notes: 1. Size refers to the operand size.
B: Byte
W: Word
L: Longword
2. ER7 is not used as the register that can be saved (STM)/restored (LDM) when using STM/LDM instruction, because ER7 is the stack pointer.

Table 2.4 Arithmetic Operations Instructions (1)

Instruction	Size*	Function
ADD	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd
SUB		Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register. (Subtraction on immediate data and data in a general register cannot be performed in bytes. Use the SUBX or ADD instruction.)
ADDX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd
SUBX		Performs addition or subtraction with carry on data in two general registers, or on immediate data and data in a general register.
INC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd
DEC		Adds or subtracts the value 1 or 2 to or from data in a general register. (Only the value 1 can be added to or subtracted from byte operands.)
ADDS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd
SUBS		Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA	B	Rd (decimal adjust) → Rd
DAS		Decimal-adjusts an addition or subtraction result in a general register by referring to CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd
		Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd
		Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd
		Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.

Note: * Size refers to the operand size.
B: Byte
W: Word
L: Longword

Table 2.4 Arithmetic Operations Instructions (2)

Instruction	Size*[1]	Function
DIVXS	B/W	Rd ÷ Rs → Rd Performs signed division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.
CMP	B/W/L	Rd – Rs, Rd – #IMM Compares data in a general register with data in another general register or with immediate data, and sets the CCR bits according to the result.
NEG	B/W/L	0 – Rd → Rd Takes the two's complement (arithmetic complement) of data in a general register.
EXTU	W/L	Rd (zero extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by padding with zeros on the left.
EXTS	W/L	Rd (sign extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the lower 16 bits of a 32-bit register to longword size, by extending the sign bit.
TAS*[2]	B	@ERd – 0, 1 → (<bit 7> of @ERd) Tests memory contents, and sets the most significant bit (bit 7) to 1.

Notes: 1. Size refers to the operand size.
B: Byte
W: Word
L: Longword
2. When using the TAS instruction, use registers ER0, ER1, ER4 and ER5.

Table 2.5 Logic Operations Instructions

Instruction	Size*	Function
AND	B/W/L	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B/W/L	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B/W/L	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B/W/L	~ Rd → Rd Takes the one's complement (logical complement) of data in a general register.

Note: * Size refers to the operand size.
B: Byte
W: Word
L: Longword

Table 2.6 Shift Instructions

Instruction	Size*	Function
SHAL	B/W/L	Rd (shift) → Rd
SHAR		Performs an arithmetic shift on data in a general register. 1-bit or 2 bit shift is possible.
SHLL	B/W/L	Rd (shift) → Rd
SHLR		Performs a logical shift on data in a general register. 1-bit or 2 bit shift is possible.
ROTL	B/W/L	Rd (rotate) → Rd
ROTR		Rotates data in a general register. 1-bit or 2 bit rotation is possible.
ROTXL	B/W/L	Rd (rotate) → Rd
ROTXR		Rotates data including the carry flag in a general register. 1-bit or 2 bit rotation is possible.

Note: * Size refers to the operand size.
B: Byte
W: Word
L: Longword

Table 2.7 Bit Manipulation Instructions (1)

Instruction	Size*	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in a general register or memory operand to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in a general register or memory operand to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory operand and sets or clears the Z flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C Logically ANDs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIAND	B	C ∧ (<bit-No.> of <EAd>) → C Logically ANDs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C Logically ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIOR	B	C ∨ (~ <bit-No.> of <EAd>) → C Logically ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

Note: * Size refers to the operand size.
B: Byte

Table 2.7 Bit Manipulation Instructions (2)

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C Logically exclusive-ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIXOR	B	C ⊕ ~ (<bit-No.> of <EAd>) → C Logically exclusive-ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory operand to the carry flag.
BILD	B	~ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand.
BIST	B	~ C → (<bit-No.>. of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.

Note: * Size refers to the operand size.
B: Byte

Table 2.8 Branch Instructions

Instruction	Size	Function
Bcc	—	Branches to a specified address if a specified condition is true. The branching conditions are listed below.

Mnemonic	Description	Condition
BRA (BT)	Always (true)	Always
BRN (BF)	Never (false)	Never
BHI	High	$C \vee Z = 0$
BLS	Low or same	$C \vee Z = 1$
BCC (BHS)	Carry clear (high or same)	$C = 0$
BCS (BLO)	Carry set (low)	$C = 1$
BNE	Not equal	$Z = 0$
BEQ	Equal	$Z = 1$
BVC	Overflow clear	$V = 0$
BVS	Overflow set	$V = 1$
BPL	Plus	$N = 0$
BMI	Minus	$N = 1$
BGE	Greater or equal	$N \oplus V = 0$
BLT	Less than	$N \oplus V = 1$
BGT	Greater than	$Z \vee (N \oplus V) = 0$
BLE	Less or equal	$Z \vee (N \oplus V) = 1$

JMP	—	Branches unconditionally to a specified address.
BSR	—	Branches to a subroutine at a specified address
JSR	—	Branches to a subroutine at a specified address
RTS	—	Returns from a subroutine

Table 2.9 System Control Instructions

Instruction	Size*	Function
TRAPA	—	Starts trap-instruction exception handling.
RTE	—	Returns from an exception-handling routine.
SLEEP	—	Causes a transition to a power-down state.
LDC	B/W	(EAs) → CCR, (EAs) → EXR Moves the memory operand contents or immediate data to CCR or EXR. Although CCR and EXR are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
STC	B/W	CCR → (EAd), EXR → (EAd) Transfers CCR or EXR contents to a general register or memory operand. Although CCR and EXR are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
ANDC	B	CCR ∧ #IMM → CCR, EXR ∧ #IMM → EXR Logically ANDs the CCR or EXR contents with immediate data.
ORC	B	CCR ∨ #IMM → CCR, EXR ∨ #IMM → EXR Logically ORs the CCR or EXR contents with immediate data.
XORC	B	CCR ⊕ #IMM → CCR, EXR ⊕ #IMM → EXR Logically exclusive-ORs the CCR or EXR contents with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

Note: * Size refers to the operand size.
B: Byte
W: Word

Table 2.10 Block Data Transfer Instructions

Instruction	Size	Function
EEPMOV.B	—	if R4L ≠ 0 then Repeat @ER5 + → @ER6+ R4L–1 → R4L Until R4L = 0 else next;
EEPMOV.W	—	if R4 ≠ 0 then Repeat @ER5 + → @ER6+ R4–1 → R4 Until R4 = 0 else next; Transfers a data block. Starting from the address set in ER5, transfers data for the number of bytes set in R4L or R4 to the address location set in ER6. Execution of the next instruction begins as soon as the transfer is completed.

2.6.2 Basic Instruction Formats

The H8S/2000 CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op), a register field (r), an effective address extension (EA), and a condition field (cc).

Figure 2.11 shows examples of instruction formats.

- Operation field

  Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.
- Register field

  Specifies a general register. Address registers are specified by 3 bits, and data registers by 3 bits or 4 bits. Some instructions have two register fields, and some have no register field.
- Effective address extension

  8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement.
- Condition field

  Specifies the branching condition of Bcc instructions.

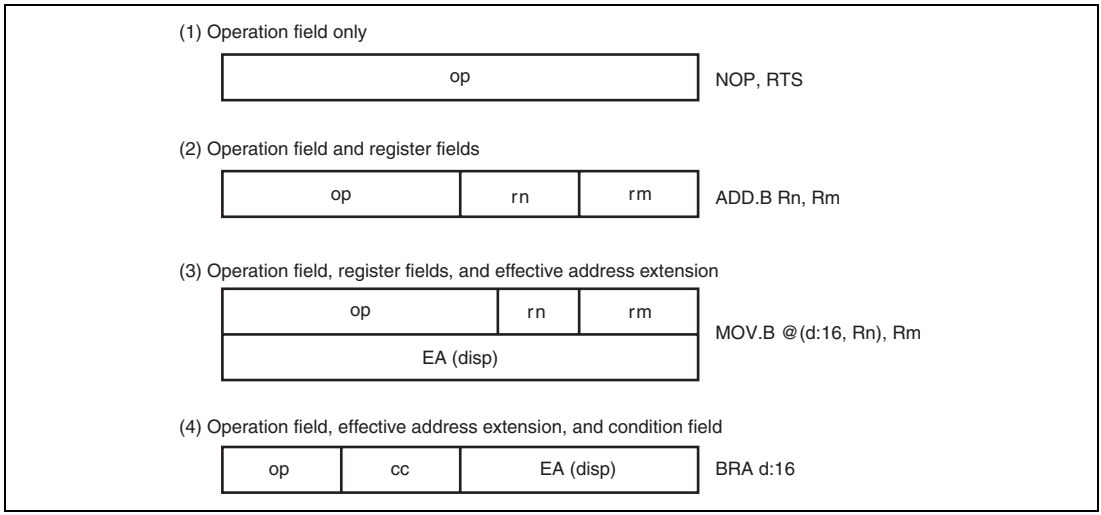


Figure 2.11 Instruction Formats (Examples)

2.7 Addressing Modes and Effective Address Calculation

The H8S/2000 CPU supports the eight addressing modes listed in table 2.11. Each instruction uses a subset of these addressing modes.

Arithmetic and logic operations instructions can use the register direct and immediate addressing modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit manipulation instructions can use register direct, register indirect, or absolute addressing mode to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.11 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:32,ERn)
4	Register indirect with post-increment	@ERn+
	Register indirect with pre-decrement	@–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24/@aa:32
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

2.7.1 Register Direct—Rn

The register field of the instruction code specifies an 8-, 16-, or 32-bit general register which contains the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

2.7.2 Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn) which contains the address of a memory operand. If the address is a program instruction address, the lower 24 bits are valid and the upper 8 bits are all assumed to be 0 (H'00).

2.7.3 Register Indirect with Displacement—@(d:16, ERn) or @(d:32, ERn)

A 16-bit or 32-bit displacement contained in the instruction code is added to an address register (ERn) specified by the register field of the instruction, and the sum gives the address of a memory operand. A 16-bit displacement is sign-extended when added.

2.7.4 Register Indirect with Post-Increment or Pre-Decrement—@ERn+ or @-ERn

Register Indirect with Post-Increment—@ERn+: The register field of the instruction code specifies an address register (ERn) which contains the address of a memory operand. After the operand is accessed, 1, 2, or 4 is added to the address register contents and the sum is stored in the

address register. The value added is 1 for byte access, 2 for word access, and 4 for longword access. For word or longword transfer instructions, the register value should be even.

Register Indirect with Pre-Decrement—@-ERn: The value 1, 2, or 4 is subtracted from an address register (ERn) specified by the register field in the instruction code, and the result becomes the address of a memory operand. The result is also stored in the address register. The value subtracted is 1 for byte access, 2 for word access, and 4 for longword access. For word or longword transfer instructions, the register value should be even.

2.7.5 Absolute Address—@aa:8, @aa:16, @aa:24, or @aa:32

The instruction code contains the absolute address of a memory operand. The absolute address may be 8 bits long (@aa:8), 16 bits long (@aa:16), 24 bits long (@aa:24), or 32 bits long (@aa:32). Table 2.12 indicates the accessible absolute address ranges.

To access data, the absolute address should be 8 bits (@aa:8), 16 bits (@aa:16), or 32 bits (@aa:32) long. For an 8-bit absolute address, the upper 16 bits are all assumed to be 1 (H'FFFF). For a 16-bit absolute address, the upper 16 bits are a sign extension. For a 32-bit absolute address, the entire address space is accessed.

A 24-bit absolute address (@aa:24) indicates the address of a program instruction. The upper 8 bits are all assumed to be 0 (H'00).

Table 2.12 Absolute Address Access Ranges

Absolute Address		Normal Mode	Advanced Mode
Data address	8 bits (@aa:8)	H'FF00 to H'FFFF	H'FFFF00 to H'FFFFFF
	16 bits (@aa:16)	H'0000 to H'FFFF	H'000000 to H'007FFF, H'FF8000 to H'FFFFFF
	32 bits (@aa:32)		H'000000 to H'FFFFFF
Program instruction address	24 bits (@aa:24)		

2.7.6 Immediate—#xx:8, #xx:16, or #xx:32

The 8-bit (#xx:8), 16-bit (#xx:16), or 32-bit (#xx:32) immediate data contained in an instruction code can be used directly as an operand.

The ADDS, SUBS, INC, and DEC instructions implicitly contain immediate data in their instruction codes. Some bit manipulation instructions contain 3-bit immediate data in the instruction code, specifying a bit number. The TRAPA instruction contains 2-bit immediate data in its instruction code, specifying a vector address.

2.7.7 Program-Counter Relative—@(d:8, PC) or @(d:16, PC)

This mode can be used by the Bcc and BSR instructions. An 8-bit or 16-bit displacement contained in the instruction code is sign-extended to 24 bits and added to the 24-bit address indicated by the PC value to generate a 24-bit branch address. Only the lower 24 bits of this branch address are valid; the upper 8 bits are all assumed to be 0 (H'00). The PC value to which the displacement is added is the address of the first byte of the next instruction, so the possible branching range is –126 to +128 bytes (–63 to +64 words) or –32766 to +32768 bytes (–16383 to +16384 words) from the branch instruction. The resulting value should be an even number.

2.7.8 Memory Indirect—@@aa:8

This mode can be used by the JMP and JSR instructions. The instruction code contains an 8-bit absolute address specifying a memory operand which contains a branch address. The upper bits of the 8-bit absolute address are all assumed to be 0, so the address range is 0 to 255 (H'0000 to H'00FF in normal mode, H'000000 to H'0000FF in advanced mode).

In normal mode, the memory operand is a word operand and the branch address is 16 bits long. In advanced mode, the memory operand is a longword operand, the first byte of which is assumed to be 0 (H'00). Note that the top area of the address range in which the branch address is stored is also used for the exception vector area. For further details, refer to section 4, Exception Handling.

If an odd address is specified in word or longword memory access, or as a branch address, the least significant bit is regarded as 0, causing data to be accessed or the instruction code to be fetched at the address preceding the specified address. (For further information, see section 2.5.2, Memory Data Formats.)

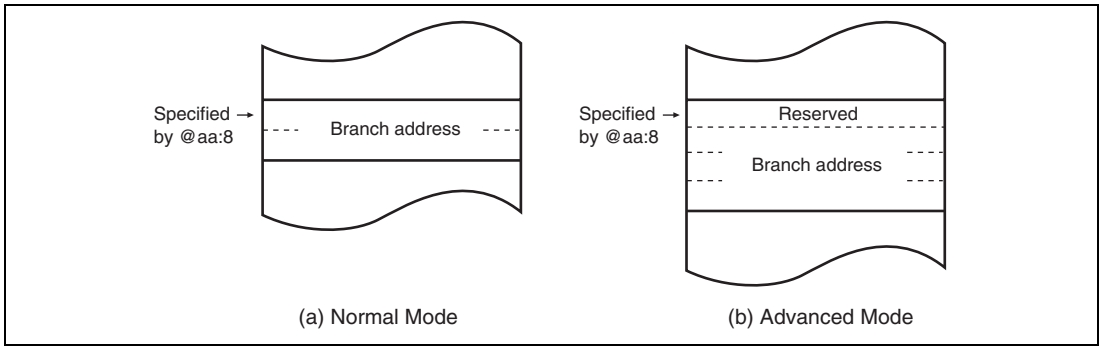


Figure 2.12 Branch Address Specification in Memory Indirect Addressing Mode

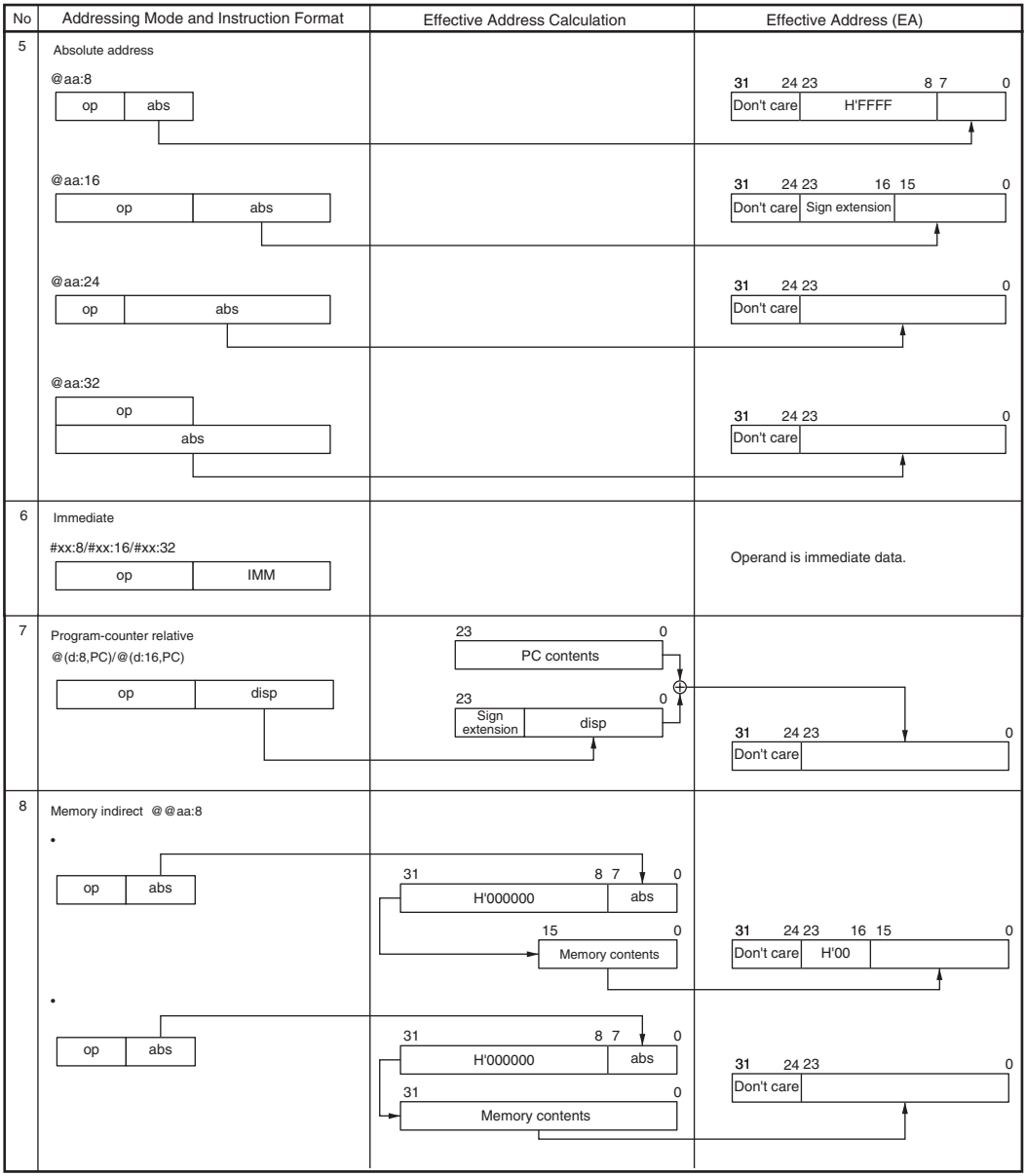
2.7.9 Effective Address Calculation

Table 2.13 indicates how effective addresses are calculated in each addressing mode. In normal mode, the upper 8 bits of the effective address are ignored in order to generate a 16-bit address.

Table 2.13 Effective Address Calculation (1)

No	Addressing Mode and Instruction Format	Effective Address Calculation	Effective Address (EA)
1	Register direct (Rn) op | rm | rn		Operand is general register contents.
2	Register indirect (@ERn) op | r	31 … 0: General register contents	31 … 24 23 … 0: Don't care |
3	Register indirect with displacement @(d:16,ERn) or @(d:32,ERn) op | r | disp	31 … 0: General register contents 31 … 0: Sign extension | disp	31 … 24 23 … 0: Don't care |
4	Register indirect with post-increment or pre-decrement • Register indirect with post-increment @ERn+ op | r • Register indirect with pre-decrement @-ERn op | r	31 … 0: General register contents 1, 2, or 4 Operand Size / Offset: Byte 1; Word 2; Longword 4	31 … 24 23 … 0: Don't care |

Table 2.13 Effective Address Calculation (2)



2.8 Processing States

The H8S/2000 CPU has four main processing states: the reset state, exception handling state, program execution state, and program stop state. Figure 2.13 indicates the state transitions.

- Reset state

  In this state the CPU and on-chip peripheral modules are all initialized and stopped. When the $\overline{\text{RES}}$ input goes low, all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{\text{RES}}$ signal changes from low to high. For details, refer to section 4, Exception Handling.

  The reset state can also be entered by a watchdog timer overflow.

- Exception-handling state

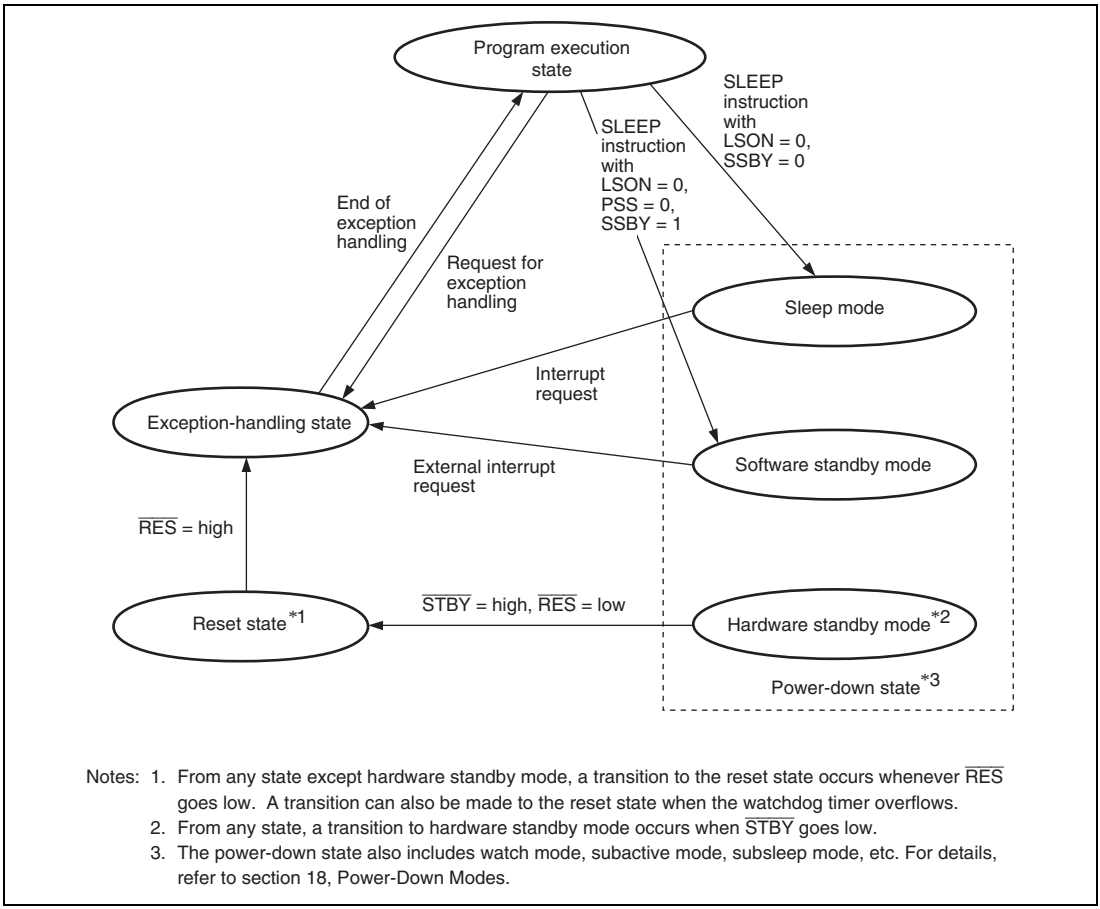
  The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to an exception source, such as, a reset, trace, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address. For further details, refer to section 4, Exception Handling.

- Program execution state

  In this state the CPU executes program instructions in sequence.

- Program stop state

  This is a power-down state in which the CPU stops operating. The program stop state occurs when a SLEEP instruction is executed or the CPU enters hardware standby mode. For details, refer to section 18, Power-Down Modes.



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever $\overline{RES}$ goes low. A transition can also be made to the reset state when the watchdog timer overflows.
2. From any state, a transition to hardware standby mode occurs when $\overline{STBY}$ goes low.
3. The power-down state also includes watch mode, subactive mode, subsleep mode, etc. For details, refer to section 18, Power-Down Modes.

Figure 2.13 State Transitions

2.9 Usage Notes

2.9.1 Note on TAS Instruction Usage

When using the TAS instruction, use registers ER0, ER1, ER4 and ER5.

The TAS instruction is not generated in the H8S, H8/300 Series C/C++ Compiler by Renesas Technology Corp. When the TAS instruction is used as a user-defined intrinsic function, use registers ER0, ER1, ER4 and ER5.

2.9.2 Note on STM/LDM Instruction Usage

ER7 is not used as the register that can be saved (STM)/restored (LDM) when using STM/LDM instruction, because ER7 is the stack pointer. Two, three, or four registers can be saved/restored by one STM/LDM instruction. The following ranges can be specified in the register list.

Two registers: ER0—ER1, ER2—ER3, or ER4—ER5

Three registers: ER0—ER2 or ER4—ER6

Four registers: ER0—ER3

The STM/LDM instruction including ER7 is not generated by the H8S, H8/300 Series C/C++ Compiler by Renesas Technology Corp.

2.9.3 Note on Bit Manipulation Instructions

The BSET, BCLR, BNOT, BST, and BIST instructions read data from the specified address in byte units, manipulate the data of the target bit, and write data to the same address again in byte units. Special care is required when using these instructions in cases where a register containing a write-only bit is used or a bit is directly manipulated for a port, because this may rewrite data of a bit other than the bit to be manipulated.

Example: The BCLR instruction is executed for DDR in port 4.

P47 and P46 are input pins, with a low-level signal input at P47 and a high-level signal input at P46. P45 to P40 are output pins and output low-level signals. The following shows an example in which P40 is set to be an input pin with the BCLR instruction.

Prior to executing BCLR:

	P47	P46	P45	P44	P43	P42	P41	P40
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
DDR	0	0	1	1	1	1	1	1
DR	1	0	0	0	0	0	0	0

BCLR instruction executed:

```
BCLR   #0,    @P4DDR
```

The BCLR instruction is executed for DDR in port 4.

After executing BCLR:

	P47	P46	P45	P44	P43	P42	P41	P40
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
DDR	1	1	1	1	1	1	1	0
DR	1	0	0	0	0	0	0	0

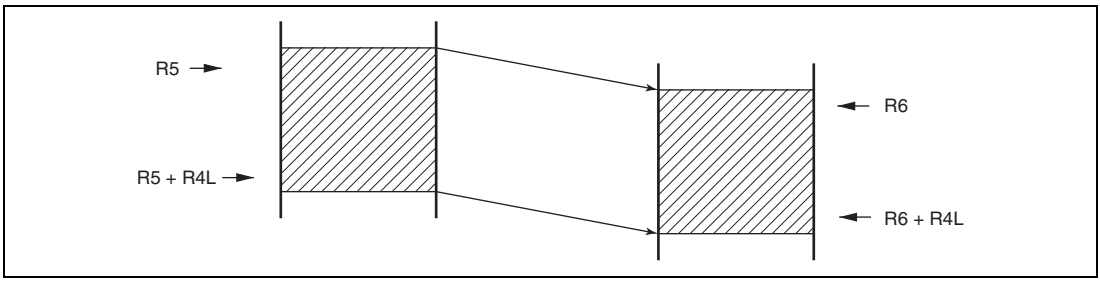
Operation:

1. When the BCLR instruction is executed, first the CPU reads P4DDR.
   Since P4DDR is a write-only register, so the CPU reads H'FF. In this example P4DDR has a value of H'3F, but the value read by the CPU is H'FF.
2. The CPU clears bit 0 of the read data to 0, changing data to H'FE.
3. The CPU writes H'FE to DDR, completing execution of BCLR.

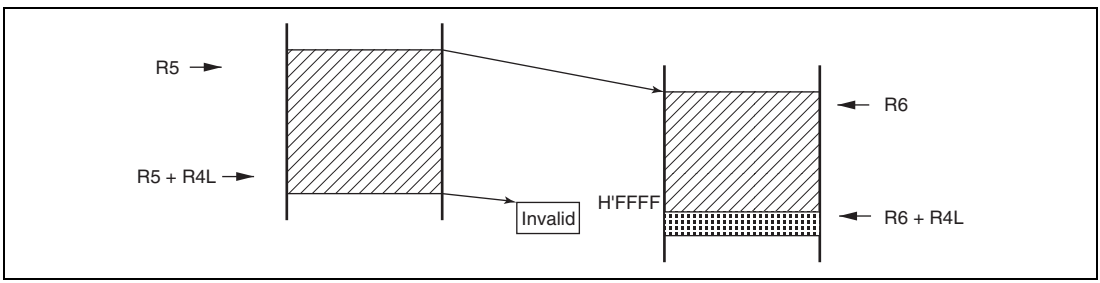
As a result of the BCLR instruction, bit 0 in DDR is set to 0, and P40 becomes an input pin. However, bits 7 and 6 of DDR are modified to 1, therefore P47 and P46 become output pins.

2.9.4 EEPMOV Instruction

1. EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4L, which starts from the address indicated by R5, to the address indicated by R6.



2. Set R4L and R6 so that the end address of the destination address (value of R6 + R4L) does not exceed H'FFFF (the value of R6 must not change from H'FFFF to H'0000 during execution).



Section 3 MCU Operating Modes

3.1 MCU Operating Mode Selection

This LSI has three operating modes (modes 1 to 3). The operating mode is determined by the setting of the mode pins (MD1 and MD0). Table 3.1 shows the MCU operating mode selection.

Table 3.1 lists the MCU operating modes.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD1	MD0	CPU Operating Mode	Description	On-Chip ROM
0	0	0	—	—	—
1		1	Normal	Expanded mode with on-chip ROM disabled	Disabled
2	1	0	Advanced	Expanded mode with on-chip ROM enabled	Enabled
				Single-chip mode	
3		1	Normal	Expanded mode with on-chip ROM enabled	
				Single-chip mode	

Mode 1 is an expanded mode that allows access to external memory and peripheral devices. With modes 2 and 3, operation begins in single-chip mode after reset release, but a transition can be made to external expansion mode by setting the EXPE bit in MDCR to 1.

Mode 0 cannot be used in this LSI. Thus, mode pins should be set to enable mode 1, 2 or 3 in normal program execution state. Mode pins should not be changed during operation.

3.2 Register Descriptions

The following registers are related to the operating mode. For details on the bus control register (BCR), refer to section 6.3.1, Bus Control Register (BCR).

- Mode control register (MDCR)
- System control register (SYSCR)
- Serial timer control register (STCR)

3.2.1 Mode Control Register (MDCR)

MDCR is used to set an operating mode and to monitor the current operating mode.

Bit	Bit Name	Initial Value	R/W	Description
7	EXPE	—*	R/W*	Extended Mode Enable Specifies extended mode. Fixed to 1 and cannot be modified in mode 1. Readable/writable and the initial value is 0 in mode 2 or 3. 0: Single-chip mode 1: Extended mode
6 to 2	—	All 0	R	Reserved These bits are always read as 0. These bits cannot be modified.
1	MDS1	—*	R	Mode Select 1 and 0
0	MDS0	—*	R	These bits indicate the input levels at mode pins (MD1 and MD0) (the current operating mode). Bits MDS1 and MDS0 correspond to MD1 and MD0, respectively. These bits are read-only bits and they cannot be written to. The mode pin (MD1 and MD0) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

Note: * The initial values are determined by the settings of the MD1 and MD0 pins.

3.2.2 System Control Register (SYSCR)

SYSCR selects a system pin function, monitors a reset source, selects the interrupt control mode and the detection edge for NMI, pin location selection, enables or disables register access to the on-chip peripheral modules, and enables or disables on-chip RAM address space.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved Although this bit is readable or writable, do not set to 1.
6	IOSE	0	R/W	IOS Enable Enables or disables $\overline{AS}$/$\overline{IOS}$ pin function in extended mode. 0: $\overline{AS}$ pin Outputs low when an external area is accessed. 1: $\overline{IOS}$ pin Outputs low when a specified address of addresses H'(FF)F000 to H'(FF)F7FF is accessed.
5	INTM1	0	R	Interrupt Control Select Mode 1 and 0
4	INTM0	0	R/W	These bits select the control mode of the interrupt controller. For details on the interrupt control modes and interrupt control select modes 1 and 0, see section 5.6, Interrupt Control Modes and Interrupt Operation. 00: Interrupt control mode 0 01: Interrupt control mode 1 10: Setting prohibited 11: Setting prohibited
3	XRST	1	R	External Reset This bit indicates the reset source. A reset is caused by an external reset input, or when the watchdog timer overflows. 0: A reset is caused when the watchdog timer overflows. 1: A reset is caused by an external reset.

Bit	Bit Name	Initial Value	R/W	Description
2	NMIEG	0	R/W	NMI Edge Select Selects the valid edge of the NMI interrupt input. 0: An interrupt is requested at the falling edge of NMI input 1: An interrupt is requested at the rising edge of NMI input
1	HIE	0	R/W	Host Interface Enable Controls the CPU access to the keyboard matrix interrupt and input pull-up MOS control registers (KMIMR, KMPCR, and KMIMRA), and the 8-bit timer (TMR_Y) registers (TCR_Y, TCSR_Y, TCORA_Y, TCORB_Y, TCNT_Y, and TISR). 0: TMR_Y registers are accessed through an area from H'(FF)FFF0 to H'(FF)FFF7 and an area from H'(FF)FFFC to H'(FF)FFFF 1: Keyboard matrix interrupt and input pull-up MOS control registers are accessed through an area from H'(FF)FFF0 to H'(FF)FFF7 and an area from H'(FF)FFFC to H'(FF)FFFF
0	RAME	1	R/W	RAM Enable Enables or disables on-chip RAM. The RAME bit is initialized when the reset state is released. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

3.2.3 Serial Timer Control Register (STCR)

STCR enables or disables register access and on-chip flash memory, and selects the input clock of the timer counter.

Bit	Bit Name	Initial Value	R/W	Description
7	IICS*	0	R/W	I^2C Extra Buffer Select Specifies bits 7 to 4 of port A as open-drain output buffers. These pins are used to implement an I^2C interface only by software. 0: PA7 to PA4 are normal input/output pins. 1: PA7 to PA4 are input/output pins enabling bus driving.
6, 5	—	All 0	R/W	Reserved These bits should not be changed.
4	IICE	0	R/W	I^2C Master Enable Enables or disables the CPU access to the PWMX registers (DADRAH/DACR, DADRAL, DADRBH/DACNTH, DADRBL/DACNTL), and SCI registers (SMR, BRR, SCMR). 0: SCI_1 registers are accessed through an area from H'(FF)FF88 to H'(FF)FF89 and an area from H'(FF)FF8E to H'(FF)FF8F. SCI_2 registers are accessed through an area from H'(FF)FFA0 to H9'(FF)FFA1 and an area from H'(FF)FFA6 to H'(FF)FFA7. SCI_0 registers are accessed through an area from H'(FF)FFD8 to H'(FF)FFD9 and an area from H'(FF)FFDE to H'(FF)FFDF. 1: No are accessed through an area from H'(FF)FF88 to H'(FF)FF89 and an area from H'(FF)FF8E to H'(FF)FF8F. PWMX registers are accessed through an area from H'(FF)FFA0 to H'(FF)FFA1 and an area from H'(FF)FFA6 to H'(FF)FFA7. No registers are accessed through an area from H'(FF)FFD8 to H'(FF)FFD9 and through an area from H'(FF)FFDE to H'(FF)FFDF.

Bit	Bit Name	Initial Value	R/W	Description
3	FLSHE	0	R/W	Flash Memory Control Register Enable Enables or disables CPU access for flash memory registers (FLMCR1, FLMCR2, EBR1, EBR2), control registers in power-down state (SBYCR, LPWRCR, MSTPCRH, MSTPCRL), and control registers of on-chip peripheral modules (PCSR, SYSCR2). 0: Registers in power-down state and control registers of on-chip peripheral modules are accessed in an area from H'(FF)FF80 to H'(FF)FF87. 1: Control registers of flash memory are accessed in an area from H'(FF)FF80 to H'(FF)FF87.
2	—	0	R/(W)	Reserved The initial value should not be changed.
1	ICKS1	0	R/W	Internal Clock Source Select 1, 0
0	ICKS0	0	R/W	These bits select a clock to be input to the timer counter (TCNT) and a count condition together with bits CKS2 to CKS0 in the timer control register (TCR). For details, refer to section 10.3.4, Timer Control Register (TCR).

Note: * Available only for the H8S/2144B.

3.3 Operating Mode Descriptions

3.3.1 Mode 1

The CPU can access a 64-kbyte address space in normal mode. The on-chip ROM is disabled.

Ports 1 and 2 function as an address bus, port 3 functions as a data bus, and part of port 9 carries bus control signals. Clearing the ABW bit to 0 in the WSCR register makes port B a data bus.

3.3.2 Mode 2

The CPU can access a 16-Mbyte address space in advanced mode. The on-chip ROM is enabled.

After a reset, the LSI is set to single-chip mode. To access an external address space, bit EXPE in MDCR should be set to 1.

When the EXPE bit in MDCR is set to 1, ports 1, 2 and A function as input ports after a reset. Ports 1, 2 and A output an address by setting 1 to the corresponding port data direction register (DDR). Port 3 functions as a data bus, and parts of port 9 carry bus control signals. Port B functions as a data bus when the ABW bit in WSCR is cleared to 0.

3.3.3 Mode 3

The CPU can access a 64-kbyte address space in normal mode. The on-chip ROM is enabled. The CPU can access a 56-kbyte address space in mode 3.

After a reset, the LSI is set to single-chip mode. To access an external address space, bit EXPE in MDCR should be set to 1.

When the EXPE bit in MDCR is set to 1, ports 1 and 2 function as input ports after a reset. Ports 1 and 2 function as an address bus by setting 1 to the corresponding port data direction register (DDR). Port 3 functions as a data bus, and parts of port 9 carry bus control signals. Port B functions as a data bus when the ABW bit in WSCR is cleared to 0.

3.3.4 Pin Functions in Each Operating Mode

Pin functions of ports 1 to 3, 9, A, and B depend on the operating mode. Table 3.2 shows pin functions in each operating mode.

Table 3.2 Pin Functions in Each Mode

Port		Mode 1	Mode 2	Mode 3
Port 1		A	P*[1]/A	P*[1]/A
Port 2		A	P*[1]/A	P*[1]/A
Port A*[2]		P	P*[1]/A	P
Port 3		D	P*[1]/D	P*[1]/D
Port B*[2]		P*[1]/D	P*[1]/D	P*[1]/D
Port 9	P97	P*[1]/C	P*[1]/C	P*[1]/C
	P96	C*[1]/P	P*[1]/C	P*[1]/C
	P95 to P93	C	P*[1]/C	P*[1]/C
	P92 to P91	P	P	P
	P90	P*[1]/C	P*[1]/C	P*[1]/C

[Legend]

P: I/O port

A: Address bus output

D: Data bus I/O

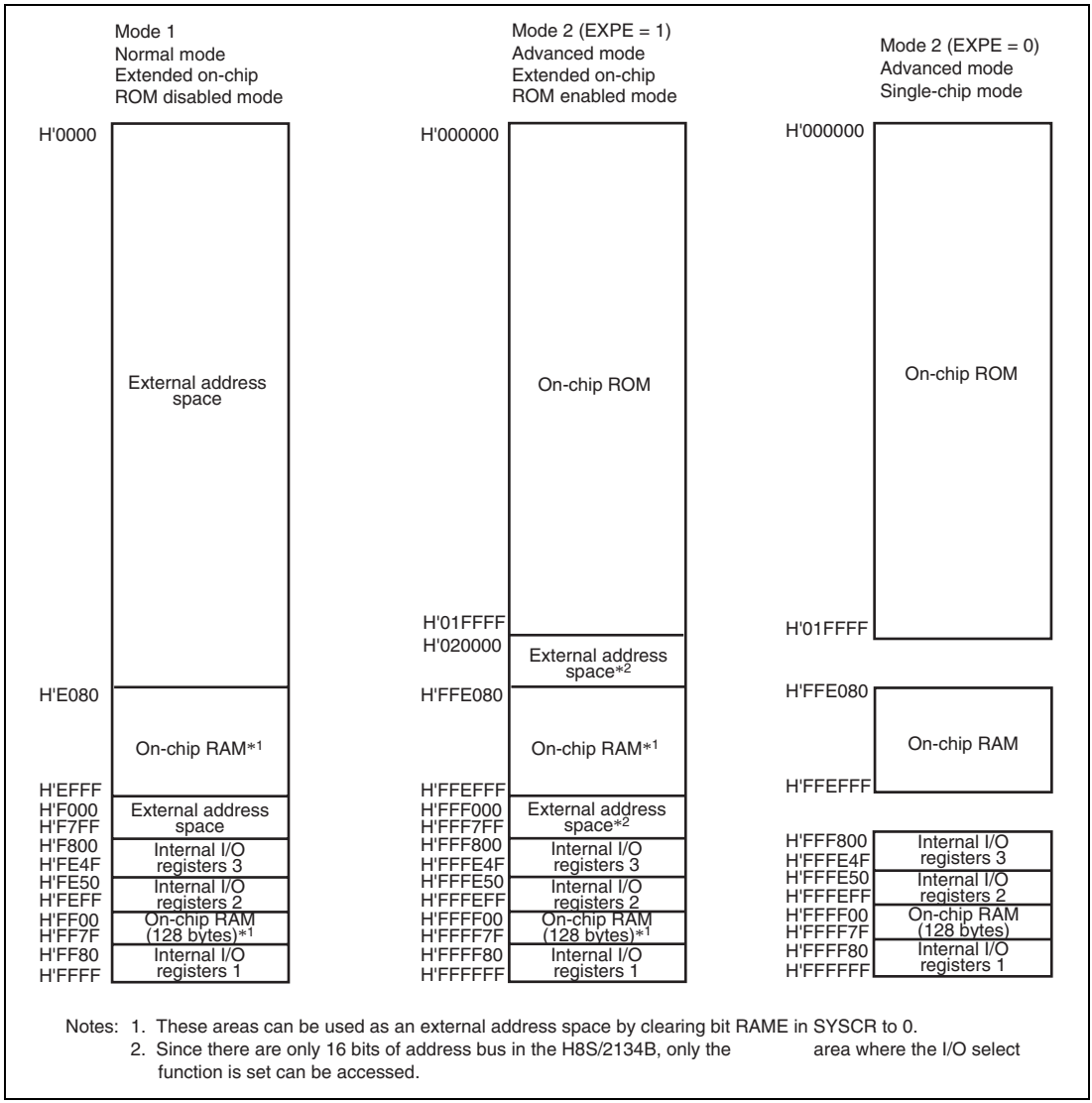
C: Control signals, clock I/O

Notes: 1. Immediately after a reset.

2. Available only for the H8S/2144B.

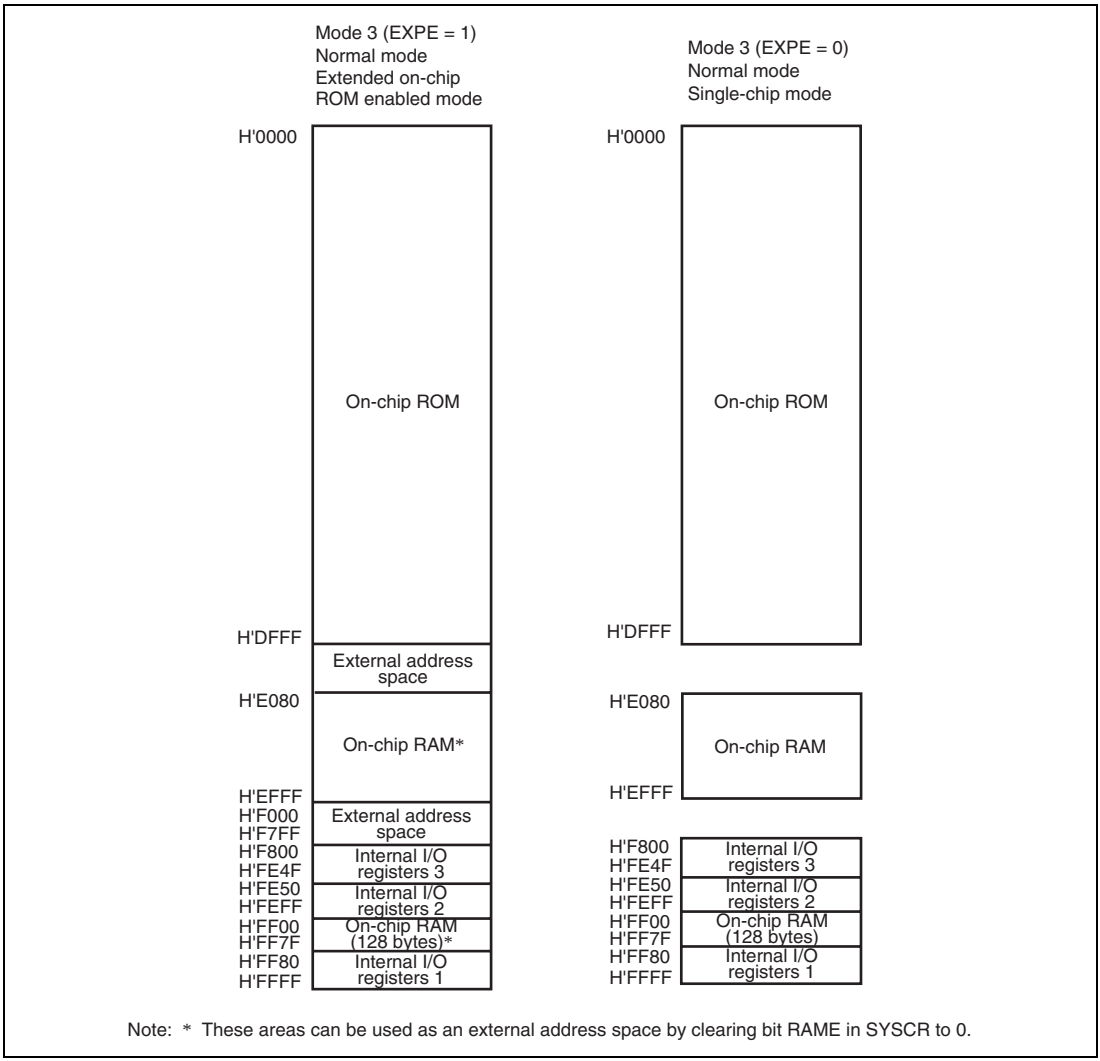
3.4 Address Map in Each Operating Mode

Figures 3.1 and 3.2 show the address map in each operating mode.



Notes: 1. These areas can be used as an external address space by clearing bit RAME in SYSCR to 0.
2. Since there are only 16 bits of address bus in the H8S/2134B, only the area where the I/O select function is set can be accessed.

Figure 3.1 Address Map (1)



Note: * These areas can be used as an external address space by clearing bit RAME in SYSCR to 0.

Figure 3.2 Address Map (2)

Section 4 Exception Handling

4.1 Exception Handling Types and Priority

Exception handling is caused by a reset, interrupt, direct transition, or trap instruction as shown in table 4.1. Exception handling is prioritized as shown in table 4.1. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority.

Table 4.1 Exception Types and Priority

Priority	Exception Type	Start of Exception Handling
High	Reset	Starts immediately after the signal level on the $\overline{\text{RES}}$ pin changes from low to high or when the watchdog timer overflows.
	Interrupt	Starts when execution of the current instruction or exception handling ends, if an interrupt request has been issued. Interrupt detection is not performed on completion of ANDC, ORC, XORC, or LDC instruction execution, or on completion of reset exception handling.
	Direct transition	Starts when a direct transition occurs as the result of SLEEP instruction execution.
	Trap instruction	Started by execution of a trap (TRAPA) instruction. Trap instruction exception handling requests are accepted at all times in program execution state.
Low		

4.2 Exception Sources and Exception Vector Table

Different vector addresses are assigned to different exception sources. Table 4.2 lists the exception sources and their vector addresses.

Table 4.2 Exception Handling Vector Table

Exception Source		Vector Number	Vector Address	
			Normal Mode	Advanced Mode
Reset		0	H'0000 to H'0001	H'000000 to H'000003
Reserved for system use		1 ⋮ 5	H'0002 to H'0003 ⋮ H'000A to H'000B	H'000004 to H'000007 ⋮ H'000014 to H'000017
Direct transition		6	H'000C to H'000D	H'000018 to H'00001B
External interrupt (NMI)		7	H'000E to H'000F	H'00001C to H'00001F
Trap instruction (four sources)		8	H'0010 to H'0011	H'000020 to H'000023
		9	H'0012 to H'0013	H'000024 to H'000027
		10	H'0014 to H'0015	H'000028 to H'00002B
		11	H'0016 to H'0017	H'00002C to H'00002F
Reserved for system use		12 ⋮ 15	H'0018 to H'0019 ⋮ H'001E to H'001F	H'000030 to H'000033 ⋮ H'00003C to H'00003F
External interrupt	IRQ0	16	H'0020 to H'0021	H'000040 to H'000043
	IRQ1	17	H'0022 to H'0023	H'000044 to H'000047
	IRQ2	18	H'0024 to H'0025	H'000048 to H'00004B
	IRQ3	19	H'0026 to H'0027	H'00004C to H'00004F
	IRQ4	20	H'0028 to H'0029	H'000050 to H'000053
	IRQ5	21	H'002A to H'002B	H'000054 to H'000057
	IRQ6	22	H'002C to H'002D	H'000058 to H'00005B
	IRQ7	23	H'002E to H'002F	H'00005C to H'00005F
Internal interrupt*		24 ⋮ 107	H'0030 to H'0031 ⋮ H'00DE to H'00DF	H'000060 to H'000063 ⋮ H'0001BC to H'0001BF

Note: * For details on the internal interrupt vector table, see section 5.5, Interrupt Exception Handling Vector Table.

4.3 Reset

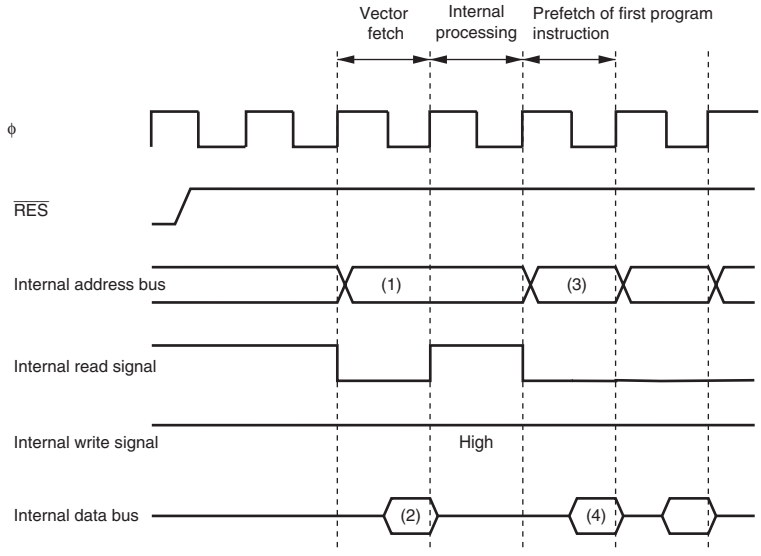
The reset exception handling is given the highest priority. When the $\overline{\text{RES}}$ signal goes low, all processing halts and this LSI enters the reset state. When the power is turned on, hold the $\overline{\text{RES}}$ signal low for at least 20 ms to ensure that this LSI is reset. To reset this LSI during operation, hold the $\overline{\text{RES}}$ signal low for at least 20 cycles. A reset initializes the internal state of the CPU and the registers of on-chip peripheral modules. This LSI can also be reset by an overflow of the watchdog timer. For details, see section 11, Watchdog Timer (WDT).

4.3.1 Reset Exception Handling

When the $\overline{\text{RES}}$ signal goes high after being held low for a given time, this LSI starts the reset exception handling as follows:

1. The internal state of the CPU and the registers of the on-chip peripheral modules are initialized and the I bit is set to 1 in CCR.
2. The vector address of the reset exception handling is read and transferred to the PC, and program execution starts from the address indicated by the PC.

Figure 4.1 shows an example of the reset sequence.



(1) Reset exception handling vector address ((1) = H'0000)
(2) Start address (contents of reset exception handling vector address)
(3) Start address ((3) = (2))
(4) First program instruction

Figure 4.1 Reset Sequence (Mode 3)

4.3.2 Interrupts after Reset

If an interrupt is accepted after a reset and before the stack pointer (SP) is initialized, the PC and CCR will not be saved correctly, leading to a program crash. To prevent this, all interrupt requests, including NMI, are disabled immediately after a reset. Since the first instruction of a program is always executed immediately after the reset state ends, make sure that this instruction initializes the stack pointer (example: MOV.L #xx: 32, SP).

4.3.3 On-Chip Peripheral Modules after Reset is Released

After a reset is released, the module stop control registers (MSTPCR) are initialized, and all modules are in module stop mode. Therefore, the registers of on-chip peripheral modules cannot be read from or written to. To read from and write to these registers, leave the module stop mode.

4.4 Interrupt Exception Handling

Interrupts are controlled by the interrupt controller. The sources to start interrupt exception handling are external interrupt sources (NMI, IRQ7 to IRQ0, and KIN15 to KIN0) and internal interrupt sources from the on-chip peripheral modules. NMI is an interrupt with the highest priority. For details, refer to section 5, Interrupt Controller.

Interrupt exception handling is conducted as follows:

1. The values in the program counter (PC) and condition code register (CCR) are saved to the stack.
2. A vector address corresponding to the interrupt source is generated, the start address is loaded from the vector table to the PC, and program execution begins from that address.

4.5 Trap Instruction Exception Handling

Trap instruction exception handling starts when a TRAPA instruction is executed. Trap instruction exception handling can be executed at all times in the program execution state.

Trap instruction exception handling is conducted as follows:

1. The values in the program counter (PC) and condition code register (CCR) are saved to the stack.
2. A vector address corresponding to the interrupt source is generated, the start address is loaded from the vector table to the PC, and program execution starts from that address.

The TRAPA instruction fetches a start address from a vector table entry corresponding to a vector number from 0 to 3, as specified in the instruction code.

Table 4.3 shows the status of CCR after execution of trap instruction exception handling.

Table 4.3 Status of CCR after Trap Instruction Exception Handling

	CCR	
Interrupt Control Mode	**I**	**UI**
0	1	—
1	1	1

[Legend]
1: Set to 1
—: Retains value prior to execution

4.6 Stack Status after Exception Handling

Figure 4.2 shows the stack after completion of trap instruction exception handling and interrupt exception handling.

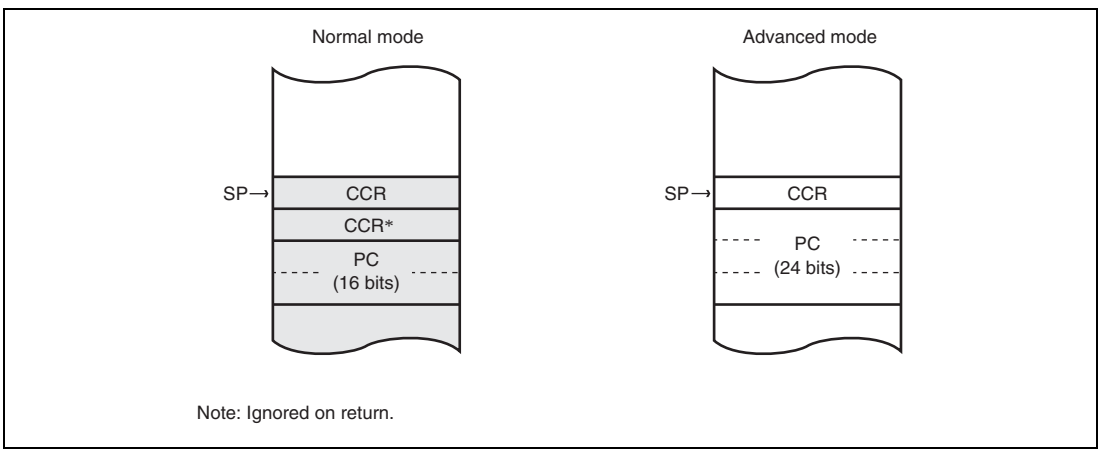


Figure 4.2 Stack Status after Exception Handling

4.7 Usage Note

When accessing word data or longword data, this LSI assumes that the lowest address bit is 0. The stack should always be accessed in words or longwords, and the value of the stack pointer (SP: ER7) should always be kept even.

Use the following instructions to save registers:

```
PUSH.W   Rn    (or MOV.W Rn, @-SP)
PUSH.L   ERn   (or MOV.L ERn, @-SP)
```

Use the following instructions to restore registers:

```
POP.W    Rn    (or MOV.W @SP+, Rn)
POP.L    ERn   (or MOV.L @SP+, ERn)
```

Setting SP to an odd value may lead to a malfunction. Figure 4.3 shows an example of what happens when the SP value is odd.

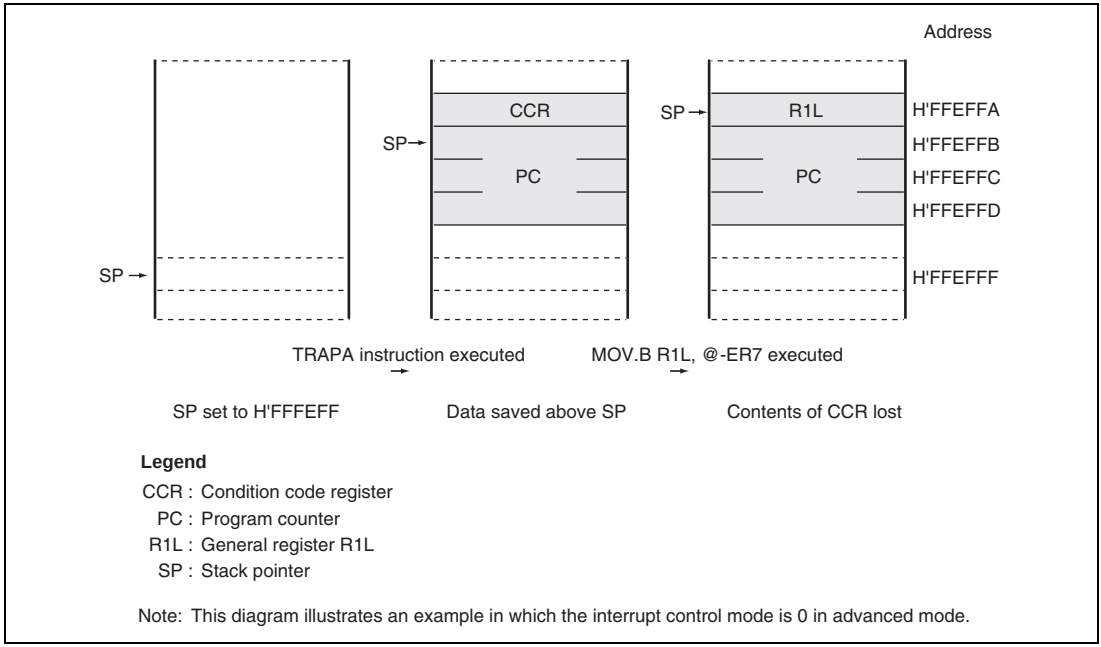


Figure 4.3 Operation when SP Value is Odd

Section 5 Interrupt Controller

5.1 Features

- Two interrupt control modes

  Any of two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the system control register (SYSCR).
- Priorities settable with ICR

  An interrupt control register (ICR) is provided for setting interrupt priorities. Three priority levels can be set for each module for all interrupts except NMI and address break.
- Independent vector addresses

  All interrupt sources are assigned independent vector addresses, making it unnecessary for the source to be identified in the interrupt handling routine.
- 23 external interrupts

  NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge detection can be selected for NMI. Falling-edge, rising-edge, or both-edge detection, or level sensing, can be selected for $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$. The IRQ6 interrupt is shared by the interrupt from the $\overline{\text{IRQ6}}$ pin and eight external interrupt inputs ($\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$), and the IRQ7 interrupt is shared by the interrupt from the $\overline{\text{IRQ7}}$ pin and sixteen external interrupt inputs ($\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$). $\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$ can be masked individually by the user program.

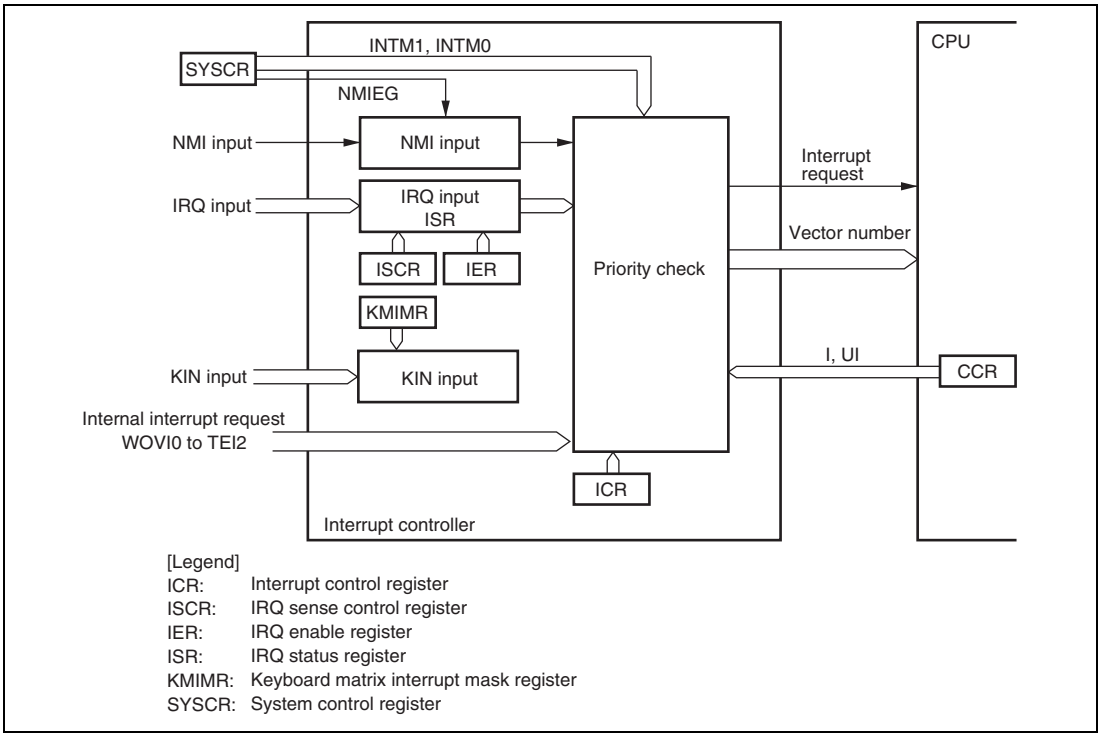


Figure 5.1 Block Diagram of Interrupt Controller

5.2 Input/Output Pins

Table 5.1 summarizes the pins of the interrupt controller.

Table 5.1 Pin Configuration

Symbol	I/O	Function
NMI	Input	Nonmaskable external interrupt Rising edge or falling edge can be selected
$\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$	Input	Maskable external interrupts Rising edge, falling edge, or both edges, or level sensing, can be selected individually for each pin.
$\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$ ($\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$)*	Input	Maskable external interrupts Falling edge or level sensing can be selected.

Note: * H8S/2134B

5.3 Register Descriptions

The interrupt controller has the following registers. For details on the system control register (SYSCR), refer to section 3.2.2, System Control Register (SYSCR).

- Interrupt control registers A to C (ICRA to ICRC)
- Address break control register (ABRKCR)
- Break address registers A to C (BARA to BARC)
- IRQ sense control registers (ISCRH, ISCRL)
- IRQ enable register (IER)
- IRQ status register (ISR)
- Keyboard matrix interrupt mask registers (KMIMRA, KMIMR)

5.3.1 Interrupt Control Registers A to C (ICRA to ICRC)

The ICR registers set interrupt control levels for interrupts other than NMI and address breaks.

The correspondence between interrupt sources and ICRA to ICRC settings is shown in table 5.2.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	ICRn7 to IRCn0	All 0	R/W	Interrupt Control Level 0: Corresponding interrupt source is interrupt control level 0 (no priority) 1: Corresponding interrupt source is interrupt control level 1 (priority)

n: A to C

Table 5.2 Correspondence between Interrupt Source and ICR

		Register		
Bit	**Bit Name**	**ICRA**	**ICRB**	**ICRC**
7	ICRn7	IRQ0	A/D converter	SCI_0
6	ICRn6	IRQ1	FRT	SCI_1
5	ICRn5	IRQ2, IRQ3	—	SCI_2
4	ICRn4	IRQ4, IRQ5	—	—
3	ICRn3	IRQ6, IRQ7	TMR_0	—
2	ICRn2	—	TMR_1	—
1	ICRn1	WDT_0	TMR_Y	—
0	ICRn0	WDT_1	—	—

n: A to C

—: Reserved. The write value should always be 0.

5.3.2 Address Break Control Register (ABRKCR)

ABRKCR controls the address breaks. When both the CMF flag and BIE flag are set to 1, an address break is requested.

Bit	Bit Name	Initial Value	R/W	Description
7	CMF	0	R	Condition Match Flag Address break source flag. Indicates that an address specified by BARA to BARC is prefetched. [Setting condition] When an address specified by BARA to BARC is prefetched while the BIE flag is set to 1. [Clearing condition] When an exception handling is executed for an address break interrupt.
6 to 1	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
0	BIE	0	R/W	Break Interrupt Enable Enables or disables address break. 0: Disabled 1: Enabled

5.3.3 Break Address Registers A to C (BARA to BARC)

The BAR registers specify an address that is to be a break address. An address in which the first byte of an instruction exists should be set as a break address. In normal mode, addresses A23 to A16 are not compared.

- BARA

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	A23 to A16	All 0	R/W	Addresses 23 to 16 The A23 to A16 bits are compared with A23 to A16 in the internal address bus.

- BARB

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	A15 to A8	All 0	R/W	Addresses 15 to 8 The A15 to A8 bits are compared with A15 to A8 in the internal address bus.

- BARC

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	A7 to A1	All 0	R/W	Addresses 7 to 1 The A7 to A1 bits are compared with A7 to A1 in the internal address bus.
0	—	0	R	Reserved This bit is always read as 0 and cannot be modified.

5.3.4 IRQ Sense Control Registers (ISCRH, ISCRL)

The ISCR registers select the source that generates an interrupt request at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.

- ISCRH

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ7SCB	0	R/W	IRQn Sense Control B
6	IRQ7SCA	0	R/W	IRQn Sense Control A
5	IRQ6SCB	0	R/W	00: Interrupt request generated at low level of $\overline{\text{IRQn}}$ input
4	IRQ6SCA	0	R/W	
3	IRQ5SCB	0	R/W	01: Interrupt request generated at falling edge of $\overline{\text{IRQn}}$ input
2	IRQ5SCA	0	R/W	
1	IRQ4SCB	0	R/W	10: Interrupt request generated at rising edge of $\overline{\text{IRQn}}$ input
0	IRQ4SCA	0	R/W	11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQn}}$ input (n = 7 to 4)

- ISCRL

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ3SCB	0	R/W	IRQn Sense Control B
6	IRQ3SCA	0	R/W	IRQn Sense Control A
5	IRQ2SCB	0	R/W	00: Interrupt request generated at low level of $\overline{\text{IRQn}}$ input
4	IRQ2SCA	0	R/W	01: Interrupt request generated at falling edge of $\overline{\text{IRQn}}$ input
3	IRQ1SCB	0	R/W	10: Interrupt request generated at rising edge of $\overline{\text{IRQn}}$ input
2	IRQ1SCA	0	R/W	11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQn}}$ input
1	IRQ0SCB	0	R/W	(n = 3 to 0)
0	IRQ0SCA	0	R/W	

5.3.5 IRQ Enable Register (IER)

IER controls the enabling and disabling of interrupt requests IRQ7 to IRQ0.

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ7E	0	R/W	IRQn Enable (n = 7 to 0)
6	IRQ6E	0	R/W	The IRQn interrupt request is enabled when this bit is 1.
5	IRQ5E	0	R/W	
4	IRQ4E	0	R/W	
3	IRQ3E	0	R/W	
2	IRQ2E	0	R/W	
1	IRQ1E	0	R/W	
0	IRQ0E	0	R/W	

5.3.6 IRQ Status Register (ISR)

The ISR register is a flag register that indicates the status of IRQ7 to IRQ0 interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ7F	0	R/(W)*	[Setting condition] When the interrupt source selected by the ISCR registers occurs [Clearing conditions] • When reading IRQnF flag when IRQnF = 1, then writing 0 to IRQnF flag • When interrupt exception handling is executed when low-level detection is set and $\overline{\text{IRQn}}$ input is high (n = 7 to 0) • When IRQn interrupt exception handling is executed when falling-edge, rising-edge, or both-edge detection is set
6	IRQ6F	0	R/(W)*	
5	IRQ5F	0	R/(W)*	
4	IRQ4F	0	R/(W)*	
3	IRQ3F	0	R/(W)*	
2	IRQ2F	0	R/(W)*	
1	IRQ1F	0	R/(W)*	
0	IRQ0F	0	R/(W)*	

Note: * Only 0 can be written, for flag clearing.

5.3.7 Keyboard Matrix Interrupt Mask Registers (KMIMRA, KMIMR)

KMIMRA and KMIMR mask each key-sensing input ($\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$) interrupt. To make the settings of these registers valid, clear bit MSTP2 in MSTPCRL to 0.

- KMIMRA

Bit	Bit Name	Initial Value	R/W	Description
7	KMIMR15	1	R/W	Keyboard Matrix Interrupt Mask 15 to 8
6	KMIMR14	1	R/W	These bits enable or disable a key-sensing input interrupt request (KIN15 to KIN8).
5	KMIMR13	1	R/W	
4	KMIMR12	1	R/W	0: Enables a key-sensing input interrupt request
3	KMIMR11	1	R/W	1: Disables a key-sensing input interrupt request
2	KMIMR10	1	R/W	
1	KMIMR9	1	R/W	
0	KMIMR8	1	R/W	

Note: Bits KMIMR15 to KMIMR8 should not be cleared to 0 in the H8S/2134B.

- KMIMR

Bit	Bit Name	Initial Value	R/W	Description
7	KMIMR7	1	R/W	Keyboard Matrix Interrupt Mask 7 to 0
6	KMIMR6	0	R/W	These bits enable or disable a key-sensing input interrupt request (KIN7 to KIN0).
5	KMIMR5	1	R/W	
4	KMIMR4	1	R/W	KMIMR6 also performs interrupt request mask control for pin $\overline{\text{IRQ6}}$.
3	KMIMR3	1	R/W	
2	KMIMR2	1	R/W	0: Enables a key-sensing input interrupt request
1	KMIMR1	1	R/W	1: Disables a key-sensing input interrupt request
0	KMIMR0	1	R/W	

Figure 5.2 shows the relationship between interrupts IRQ7 and IRQ6, interrupts KIN15 to KIN0, and KMIMRA and KMIMR.

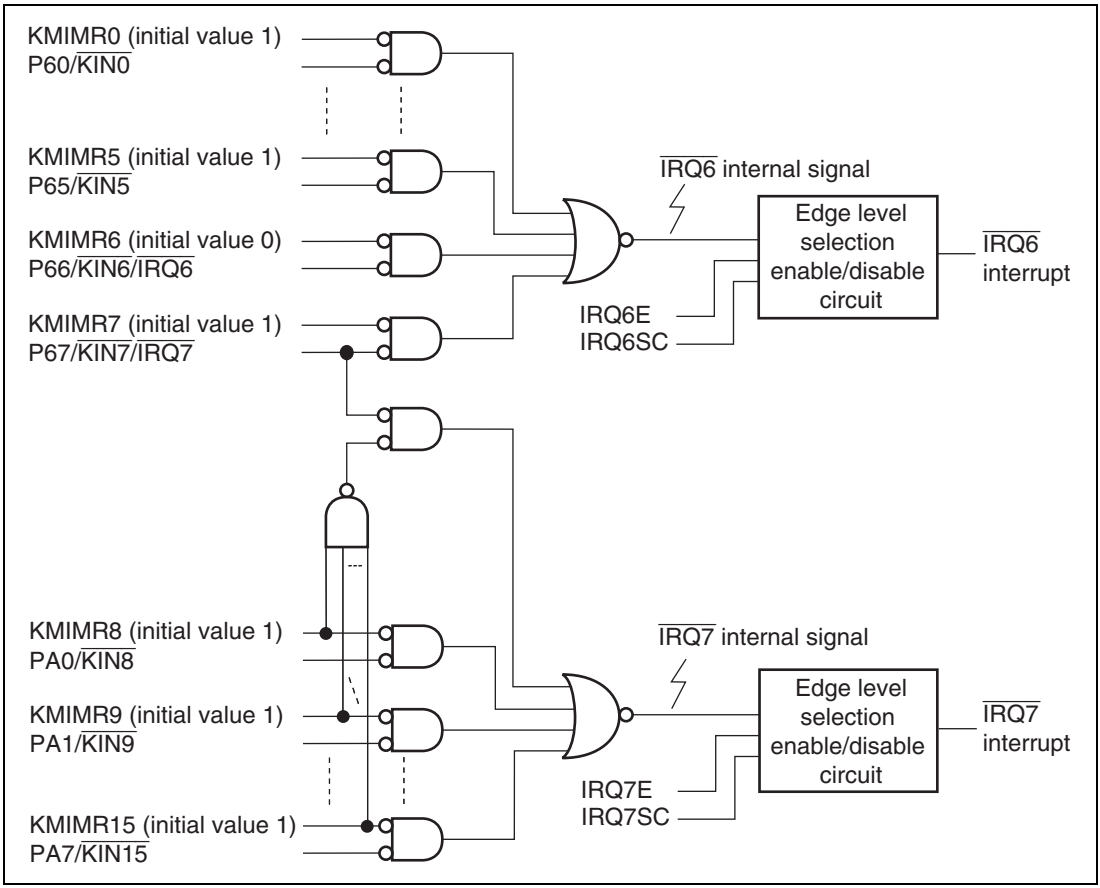


Figure 5.2 Relationship between Interrupts IRQ7 and IRQ6, Interrupts KIN15 to KIN0, and Registers KMIMR and KMIMRA

If any of bits KMIMR15 to KMIMR8 is cleared to 0, an interrupt input from the $\overline{\text{IRQ7}}$ pin will be ignored. When pins $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$ or $\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$ are used as key-sense interrupt input pins, either low-level sensing or falling-edge sensing must be specified as the interrupt sensing condition for the corresponding interrupt source (IRQ6 or IRQ7).

5.4 Interrupt Sources

5.4.1 External Interrupts

There are three types of external interrupts: NMI, IRQ7 to IRQ0 and KIN15 to KIN0. KIN15 to KIN8 share the IRQ7 interrupt source, and KIN7 to KIN0 share the IRQ6 interrupt source. Of these, NMI, IRQ7, IRQ6, and IRQ2 to IRQ0 can be used to restore this LSI from software standby mode.

NMI Interrupt: NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the interrupt control mode or the status of the CPU interrupt mask bits. The NMIEG bit in SYSCR can be used to select whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

IRQ7 to IRQ0 Interrupts: Interrupts IRQ7 to IRQ0 are requested by an input signal at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$. Interrupts IRQ7 to IRQ0 have the following features:

- The interrupt exception handling for interrupt requests IRQ7 to IRQ0 can be started at an independent vector address.
- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at pins $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$.
- Enabling or disabling of interrupt requests IRQ7 to IRQ0 can be selected with IER.
- Interrupt control levels can be specified by the ICR settings.
- The status of interrupt requests IRQ7 to IRQ0 is indicated in ISR. ISR flags can be cleared to 0 by software.

The detection of IRQ7 to IRQ0 interrupts does not depend on whether the relevant pin has been set for input or output. However, when a pin is used as an external interrupt input pin, do not clear the corresponding DDR to 0 to use the pin as an I/O pin for another function.

A block diagram of interrupts IRQ7 to IRQ0 is shown in figure 5.3.

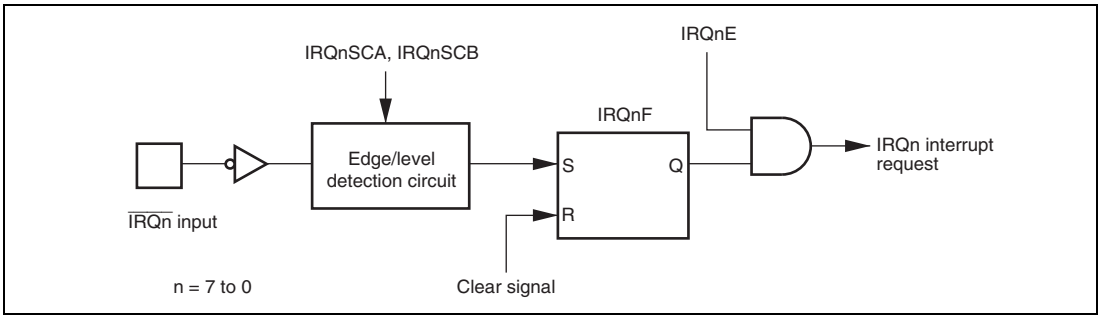


Figure 5.3 Block Diagram of Interrupts IRQ7 to IRQ0

When pin $\overline{\text{IRQ6}}$ is used as an IRQ6 interrupt input pin, clear the KMIMR6 bit to 0.

When pin $\overline{\text{IRQ7}}$ is used as an IRQ7 interrupt pin, set all of bits KMIMR15 to KMIMR8 to 1. If any of these bits is cleared to 0, IRQ7 interrupt input from the $\overline{\text{IRQ7}}$ pin will be ignored.

Since interrupt request flags IRQ7F to IRQ0F are set each time the setting condition is satisfied, regardless of the IER setting, refer to a needed flag only.

KIN15 to KIN0 Interrupts: Interrupts KIN15 to KIN0 are requested by input signals on pins $\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$. When pins $\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$ are used as key-sense inputs, clear a corresponding bit in KMIMR to 0 in order to enable their key-sense input interrupts. Remaining unused bits in KMIMR should be set to 1 in order to disable interrupts. Interrupts KIN15 to KIN8 are requested as an IRQ7 interrupt, and interrupts KIN7 to KIN0 are requested as an IRQ6 interrupt. The pin function, conditions of enabling or disabling interrupts, interrupt sense condition, and interrupt indicating method to generate a key-sense input interrupt depend on those for the IRQ7 or IRQ6 interrupt.

When pins $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$, or $\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$ are used as key-sense interrupt input pins, either low-level sensing or falling-edge sensing must be specified as the interrupt sense condition for the corresponding interrupt source (IRQ6 or IRQ7).

5.4.2 Internal Interrupts

Internal interrupts issued from the on-chip peripheral modules have the following features:

1. For each on-chip peripheral module there are flags that indicate the interrupt request status, and enable bits that individually select enabling or disabling of these interrupts. When the enable bit for a particular interrupt source is set to 1, an interrupt request is sent to the interrupt controller.
2. The priority level for each interrupt can be set by ICR.

5.5 Interrupt Exception Handling Vector Table

Table 5.3 lists interrupt exception handling sources, vector addresses, and interrupt priorities. For default priorities, the lower the vector number, the higher the priority. Modules set at the same priority will conform to their default priorities. Priorities within a module are fixed.

An interrupt control level can be specified for a module to which an ICR bit is assigned. Interrupt requests from modules that are set to control level 1 (priority) by the ICR bit setting and the I and UI bits in CCR are given priority and processed before interrupt requests from modules that are set to control level 0 (no priority).

Table 5.3 Interrupt Sources, Vector Addresses, and Interrupt Priorities

Origin of Interrupt Source	Name	Vector Number	Vector Address: Normal Mode	Vector Address: Advanced Mode	ICR	Priority
External pin	NMI	7	H'000E	H'00001C	—	High
	IRQ0	16	H'0020	H'000040	ICRA7	
	IRQ1	17	H'0022	H'000044	ICRA6	
	IRQ2	18	H'0024	H'000048	ICRA5	
	IRQ3	19	H'0026	H'00004C		
	IRQ4	20	H'0028	H'000050	ICRA4	
	IRQ5	21	H'002A	H'000054		
	IRQ6, KIN7 to KIN0	22	H'002C	H'000058	ICRA3	
	IRQ7, KIN15 to KIN8	23	H'002E	H'00005C		
—	Reserved for system use	24	H'0030	H'000060	—	
WDT_0	WOVI0 (Interval timer)	25	H'0032	H'000064	ICRA1	
WDT_1	WOVI1 (Interval timer)	26	H'0034	H'000068	ICRA0	
—	Address break	27	H'0036	H'00006C	—	
A/D converter	ADI (A/D conversion end)	28	H'0038	H'000070	ICRB7	
—	Reserved for system use	29 to 47	H'003A to H'005E	H'000074 to H'0000BC	—	
FRT	ICIA (Input capture A)	48	H'0060	H'0000C0	ICRB6	
	ICIB (Input capture B)	49	H'0062	H'0000C4		
	ICIC (Input capture C)	50	H'0064	H'0000C8		
	ICID (Input capture D)	51	H'0066	H'0000CC		
	OCIA (Output compare A)	52	H'0068	H'0000D0		
	OCIB (Output compare B)	53	H'006A	H'0000D4		
	FOVI (Overflow)	54	H'006C	H'0000D8		
	Reserved for system use	55	H'006E	H'0000DC		
—	Reserved for system use	56 to 63	H'0070 to H'007E	H'0000E0 to H'0000FC	—	
TMR_0	CMIA0 (Compare match A)	64	H'0080	H'000100	ICRB3	
	CMIB0 (Compare match A)	65	H'0082	H'000104		
	OVI0 (Overflow)	66	H'0084	H'000108		
	Reserved for system use	67	H'0086	H'00010C		Low

Origin of Interrupt Source	Name	Vector Number	Vector Address: Normal Mode	Vector Address: Advanced Mode	ICR	Priority
TMR_1	CMIA1 (Compare match A)	68	H'0088	H'000110	ICRB2	High
	CMIB1 (Compare match B)	69	H'008A	H'000114		
	OVI1 (Overflow)	70	H'008C	H'000118		
	Reserved for system use	71	H'008E	H'00011C		
TMR_Y	CMIAY (Compare match A)	72	H'0090	H'000120	ICRB1	
	CMIBY (Compare match B)	73	H'0092	H'000124		
	OVIY (Overflow)	74	H'0094	H'000128		
	Reserved for system use	75	H'0096	H'00012C		
—	Reserved for system use	76 to 79	H'0098 to H'009E	H'000130 to H'00013C	—	
SCI_0	ERI0 (Reception error 0)	80	H'00A0	H'000140	ICRC7	
	RXI0 (Reception completion 0)	81	H'00A2	H'000144		
	TXI0 (Transmission data empty 0)	82	H'00A4	H'000148		
	TEI0 (Transmission end 0)	83	H'00A6	H'00014C		
SCI_1	ERI1 (Reception error 1)	84	H'00A8	H'000150	ICRC6	
	RXI1 (Reception completion 1)	85	H'00AA	H'000154		
	TXI1 (Transmission data empty 1)	86	H'00AC	H'000158		
	TEI1 (Transmission end 1)	87	H'00AE	H'00015C		
SCI_2	ERI2 (Reception error 2)	88	H'00B0	H'000160	ICRC5	
	RXI2 (Reception completion 2)	89	H'00B2	H'000164		
	TXI2 (Transmission data empty 2)	90	H'00B4	H'000168		
	TEI2 (Transmission end 2)	91	H'00B6	H'00016C		
—	Reserved for system use	92 to 111	H'00B8 to H'00DE	H'000170 to H'0001BC	—	Low

5.6 Interrupt Control Modes and Interrupt Operation

The interrupt controller has two modes: Interrupt control mode 0 and interrupt control mode 1. Interrupt operations differ depending on the interrupt control mode. NMI interrupts and address break interrupts are always accepted except for in reset state or in hardware standby mode. The interrupt control mode is selected by SYSCR. Table 5.4 shows the interrupt control modes.

Table 5.4 Interrupt Control Modes

Interrupt Control Mode	SYSCR		Priority Setting Registers	Interrupt Mask Bits	Description
	INTM1	INTM0			
0	0	0	ICR	I	Interrupt mask control is performed by the I bit. Priority levels can be set with ICR.
1		1	ICR	I, UI	3-level interrupt mask control is performed by the I bit. Priority levels can be set with ICR.

5.6.1 Interrupt Control Mode 0

In interrupt control mode 0, interrupt requests other than NMI and address breaks are masked by ICR and the I bit of the CCR in the CPU. Figure 5.4 shows a flowchart of the interrupt acceptance operation.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. According to the interrupt control level specified in ICR, the interrupt controller only accepts an interrupt request with interrupt control level 1 (priority), and holds pending an interrupt request with interrupt control level 0 (no priority). If several interrupt requests are issued, an interrupt request with the highest priority is accepted according to the priority order, an interrupt handling is requested to the CPU, and other interrupt requests are held pending.
3. If the I bit in CCR is set to 1, only NMI and address break interrupts are accepted by the interrupt controller, and other interrupt requests are held pending. If the I bit is cleared to 0, any interrupt request is accepted.
4. When the CPU accepts an interrupt request, it starts interrupt exception handling after execution of the current instruction has been completed.
5. The PC and CCR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.

6. Next, the I bit in CCR is set to 1. This masks all interrupts except for NMI and address break interrupts.
7. The CPU generates a vector address for the accepted interrupt and starts execution of the interrupt handling routine at the address indicated by the contents of the vector address in the vector table.

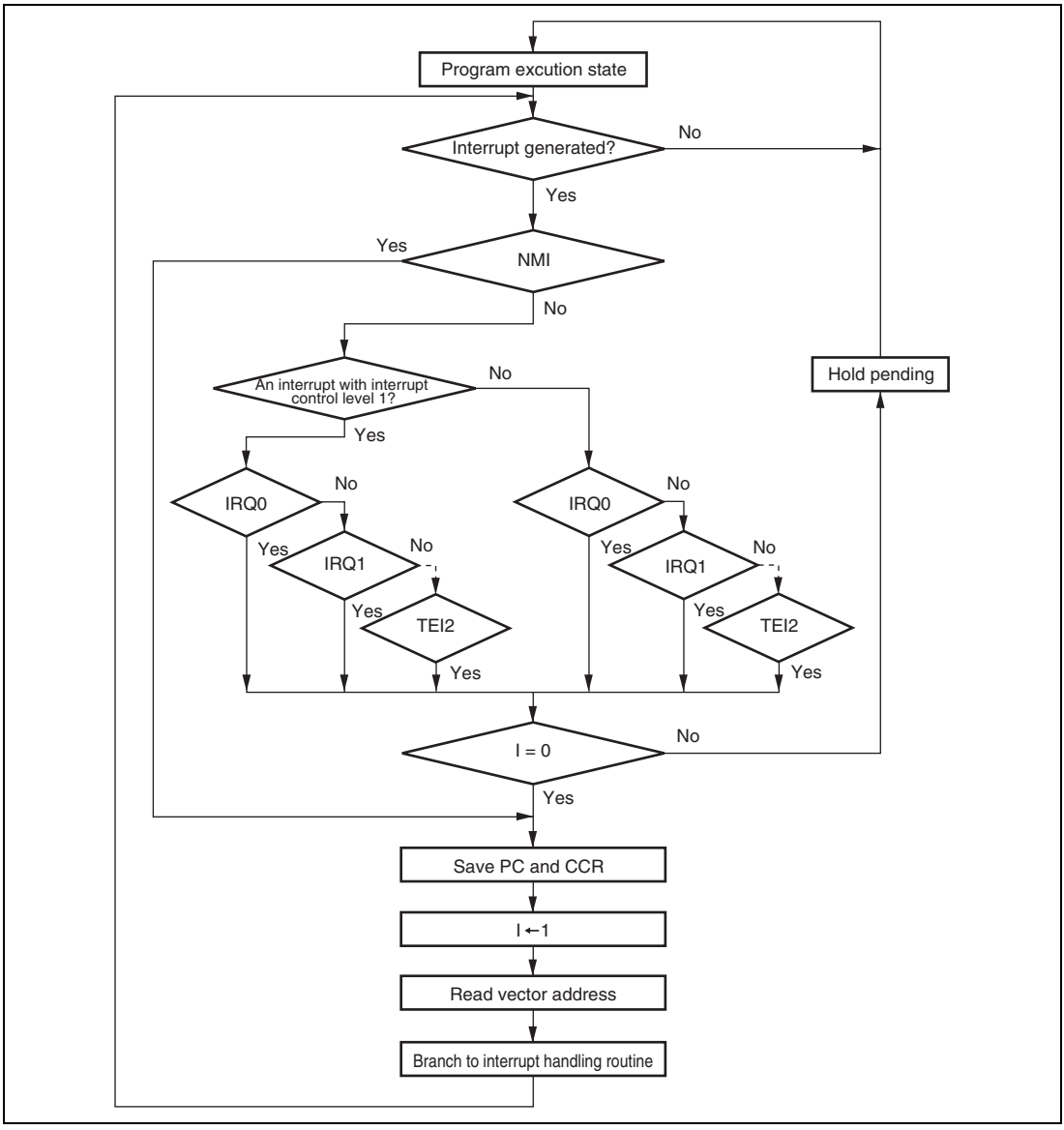


Figure 5.4 Flowchart of Procedure up to Interrupt Acceptance in Interrupt Control Mode 0

5.6.2 Interrupt Control Mode 1

In interrupt control mode 1, mask control is applied to three levels for IRQ and on-chip peripheral module interrupt requests by comparing the I and UI bits in CCR in the CPU, and the ICR setting.

- An interrupt request with interrupt control level 0 is accepted when the I bit in CCR is cleared to 0. When the I bit is set to 1, the interrupt request is held pending
- An interrupt request with interrupt control level 1 is accepted when the I bit or UI bit in CCR is cleared to 0. When both I and UI bits are set to 1, the interrupt request is held pending.

For instance, the state transition when the interrupt enable bit corresponding to each interrupt is set to 1, and ICRA to ICRC are set to H'20, H'00, and H'00, respectively (IRQ2 and IRQ3 interrupts are set to control level 1, and other interrupts are set to control level 0) is shown below. Figure 5.5 shows a state transition diagram.

- All interrupt requests are accepted when I = 0. (Priority order: NMI > IRQ2 > IRQ3 > address break > IRQ0 > IRQ1 …)
- Only NMI, IRQ2, IRQ3 and address break interrupt requests are accepted when I = 1 and UI = 0.
- Only an NMI and address break interrupt request is accepted when I = 1 and UI = 1.

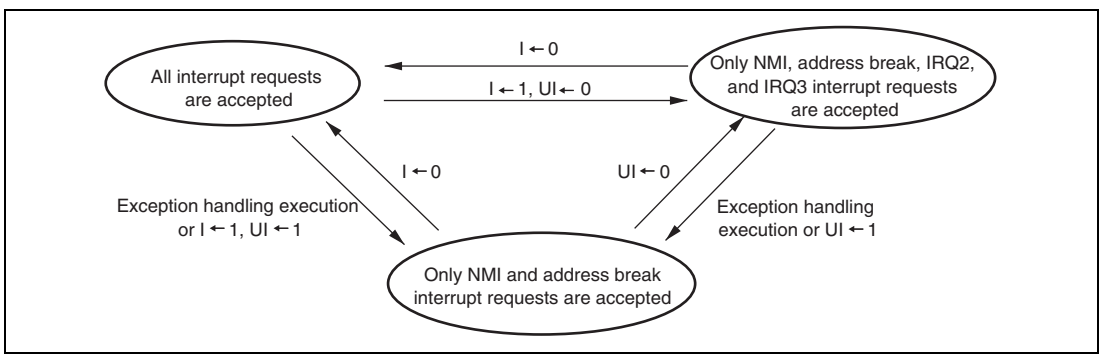


Figure 5.5 State Transition in Interrupt Control Mode 1

Figure 5.6 shows a flowchart of the interrupt acceptance operation.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. According to the interrupt control level specified in ICR, the interrupt controller only accepts an interrupt request with interrupt control level 1 (priority), and holds pending an interrupt request with interrupt control level 0 (no priority). If several interrupt requests are issued, an

interrupt request with the highest priority is accepted according to the priority order, an interrupt handling is requested to the CPU, and other interrupt requests are held pending.

3. An interrupt request with interrupt control level 1 is accepted when the I bit is cleared to 0, or when the I bit is set to 1 while the UI bit is cleared to 0.

   An interrupt request with interrupt control level 0 is accepted when the I bit is cleared to 0. When the I bit is set to 1, only an NMI or address break interrupt request is accepted, and other interrupts are held pending.

   When both the I and UI bits are set to 1, only an NMI or address break interrupt request is accepted, and other interrupts are held pending.

   When the I bit is cleared to 0, the UI bit is not affected.
4. When the CPU accepts an interrupt request, it starts interrupt exception handling after execution of the current instruction has been completed.
5. The PC and CCR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.
6. The I and UI bits in CCR are set to 1. This masks all interrupts except for an NMI or address break interrupt.
7. The CPU generates a vector address for the accepted interrupt and starts execution of the interrupt handling routine at the address indicated by the contents of the vector address in the vector table.

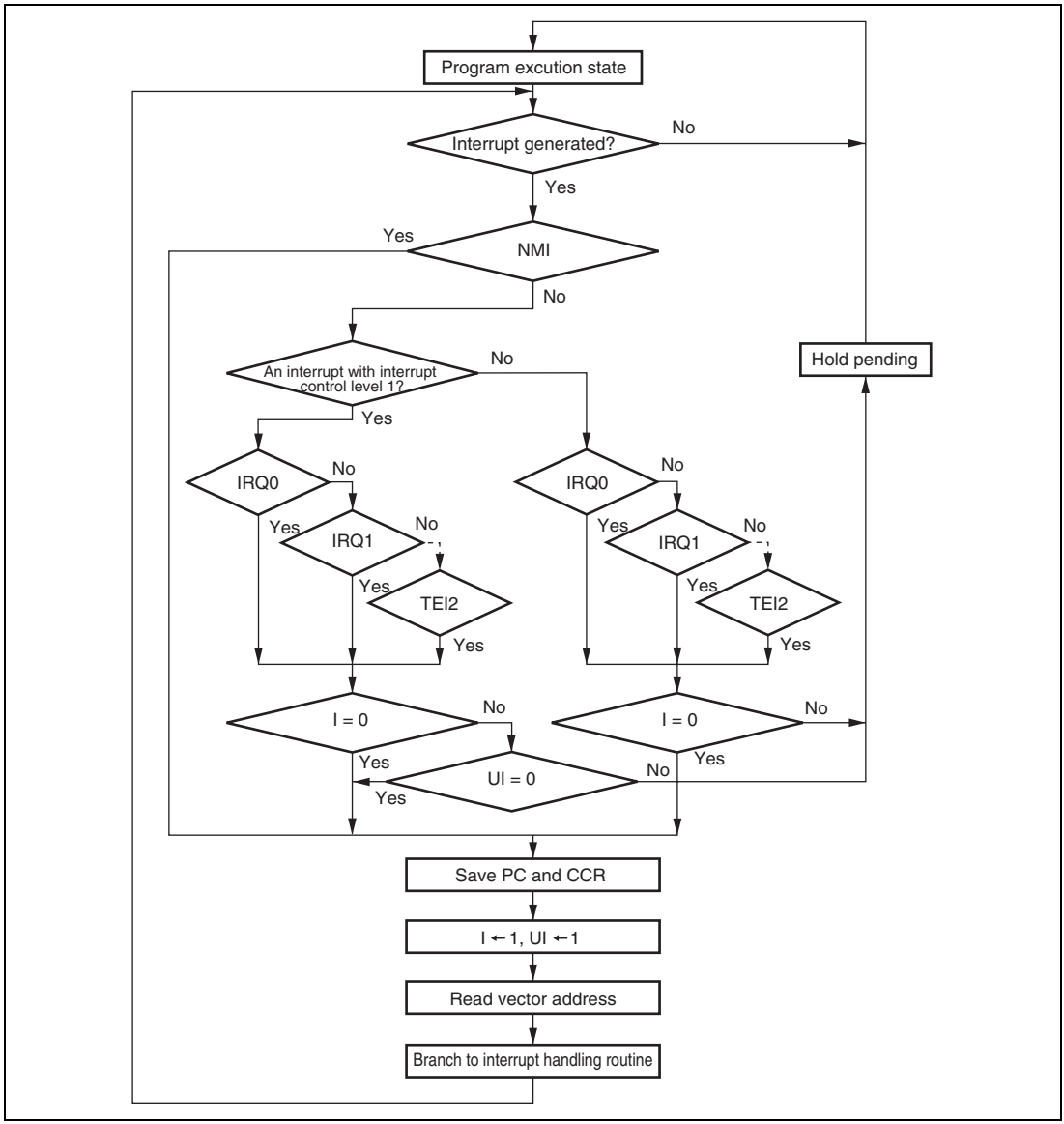


Figure 5.6 Flowchart of Procedure Up to Interrupt Acceptance in Interrupt Control Mode 1

5.6.3 Interrupt Exception Handling Sequence

Figure 5.7 shows the interrupt exception handling sequence. The example shown is for the case where interrupt control mode 0 is set in advanced mode, and the program area and stack area are in on-chip memory.

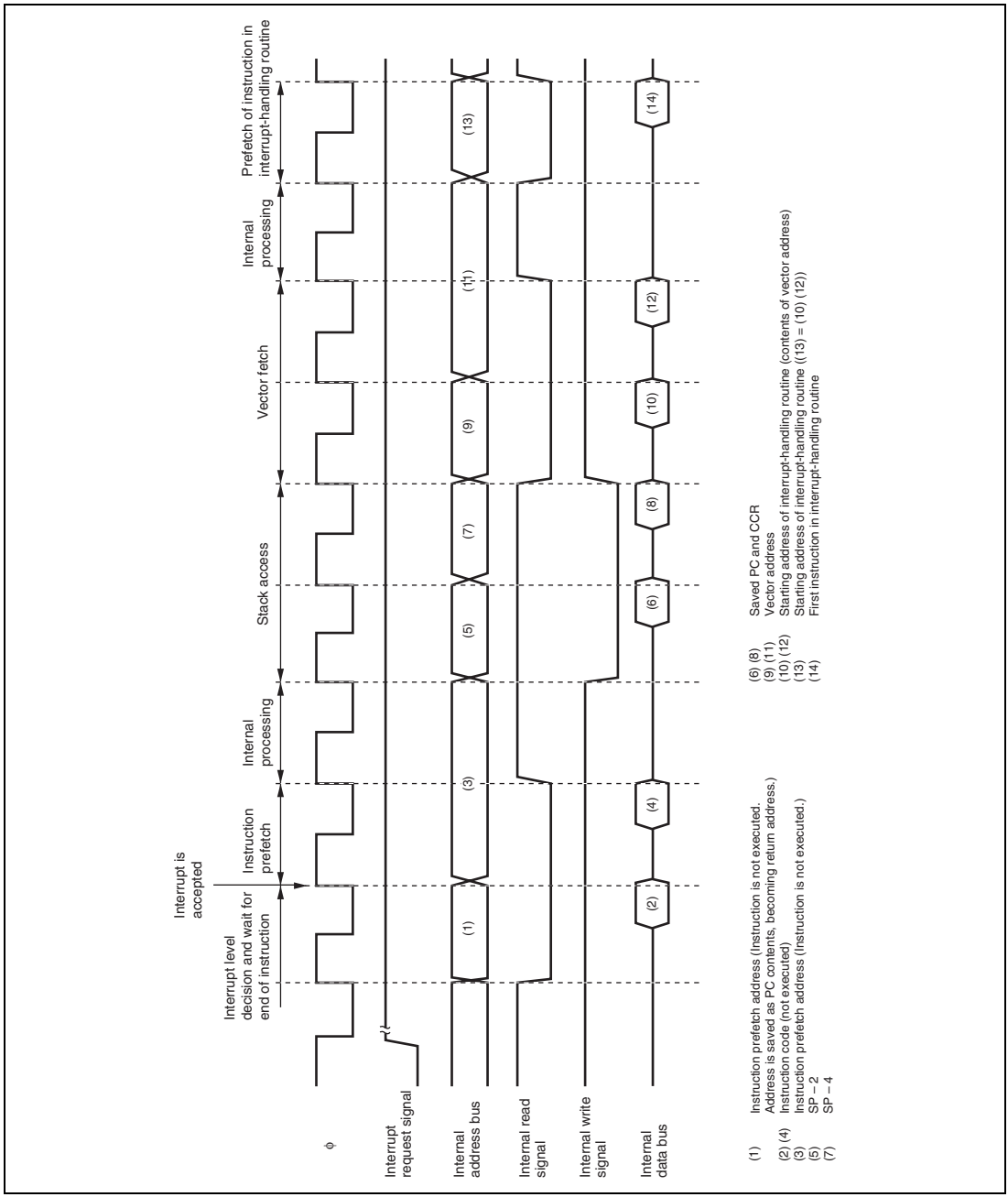


Figure 5.7 Interrupt Exception Handling

5.6.4 Interrupt Response Times

Table 5.5 shows interrupt response times – the intervals between generation of an interrupt request and execution of the first instruction in the interrupt handling routine. The execution status symbols used in table 5.5 are explained in table 5.6.

Table 5.5 Interrupt Response Times

No.	Execution Status	Normal Mode	Advanced Mode
1	Interrupt priority determination*[1]	3	
2	Number of wait states until executing instruction ends*[2]	1 to (19 + 2·S_I)	
3	PC, CCR stack save	2·S_K	2·S_K
4	Vector fetch	S_I	2·S_I
5	Instruction fetch*[3]	2·S_I	
6	Internal processing*[4]	2	
	Total (using on-chip memory)	11 to 31	12 to 32

Notes: 1. Two states in case of internal interrupt.
2. Refers to MULXS and DIVXS instructions.
3. Prefetch after interrupt acceptance and prefetch of interrupt handling routine.
4. Internal processing after interrupt acceptance and internal processing after vector fetch.

Table 5.6 Number of States in Interrupt Handling Routine Execution Status

	Object of Access				
		External Device			
		8-Bit Bus		16-Bit Bus	
Symbol	Internal Memory	2-State Access	3-State Access	2-State Access	3-State Access
Instruction fetch S_I	1	4	6 + 2m	2	3 + m
Branch address read S_J					
Stack manipulation S_K					

[Legend]
m: Number of wait states in external device access

5.7 Address Break

5.7.1 Features

This LSI can determine the specific address prefetch by the CPU to generate an address break interrupt by setting ABRKCR and BAR. If an address break interrupt is generated, the address break interrupt exception handling is performed.

With this function, the execution start point of a program containing a bug is detected and execution is branched to the correcting program.

5.7.2 Block Diagram

Figure 5.8 shows a block diagram of the address break.

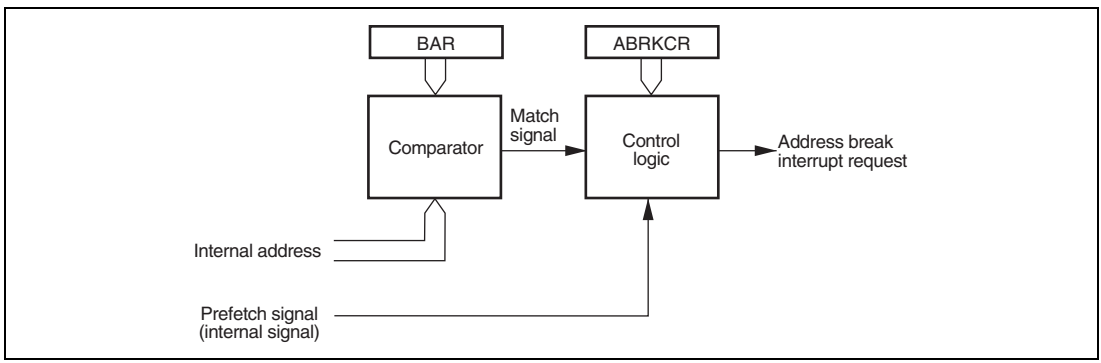


Figure 5.8 Address Break Block Diagram

5.7.3 Operation

If the CPU prefetches an address specified in BAR by setting ABRKCR and BAR, an address break interrupt can be generated. This address break function generates an interrupt request to the interrupt controller at prefetch, and determines the priority by the interrupt controller. When an interrupt is accepted, an interrupt exception handling is activated after the current instruction has been completed. Note that the interrupt mask control according to the I and UI bits in CCR of the CPU is invalid to an address break interrupt.

To use the address break function, set each register as follows:

1. Set a break address in the A23 to A1 bits in BAR.

2. Set the BIE bit in ABRKCR to 1 to enable the address break.
   When the BIE bit is cleared to 0, an address break is not requested.

When the setting conditions are satisfied, the CMF flag in ABRKCR is set to 1 to request an interrupt. The interrupt source should be determined by the interrupt handling routine if necessary.

5.7.4 Usage Notes

1. In an address break, the break address should be an address where the first byte of the instruction exists. Otherwise, a break condition will not be satisfied.
2. In normal mode, addresses A23 to A16 are not compared.
3. When the branch instructions (Bcc, BSR), jump instructions (JMP, JSR), RST instruction, and RTE instruction are placed immediately prior to the address specified by BAR, a prefetch signal to the address may be output to request an address break by executing these instruction. It is necessary to take countermeasures: do not set a break address to an address immediately after these instructions, or determine whether interrupt handling is performed by satisfaction of a normal condition.
4. An address break interrupt is generated by combining the internal prefetch signal and an address. Therefore, the timing to enter the interrupt exception handling differs according to the instructions at the specified and at prior addresses and execution cycles.

Figure 5.9 shows an example of address timing.

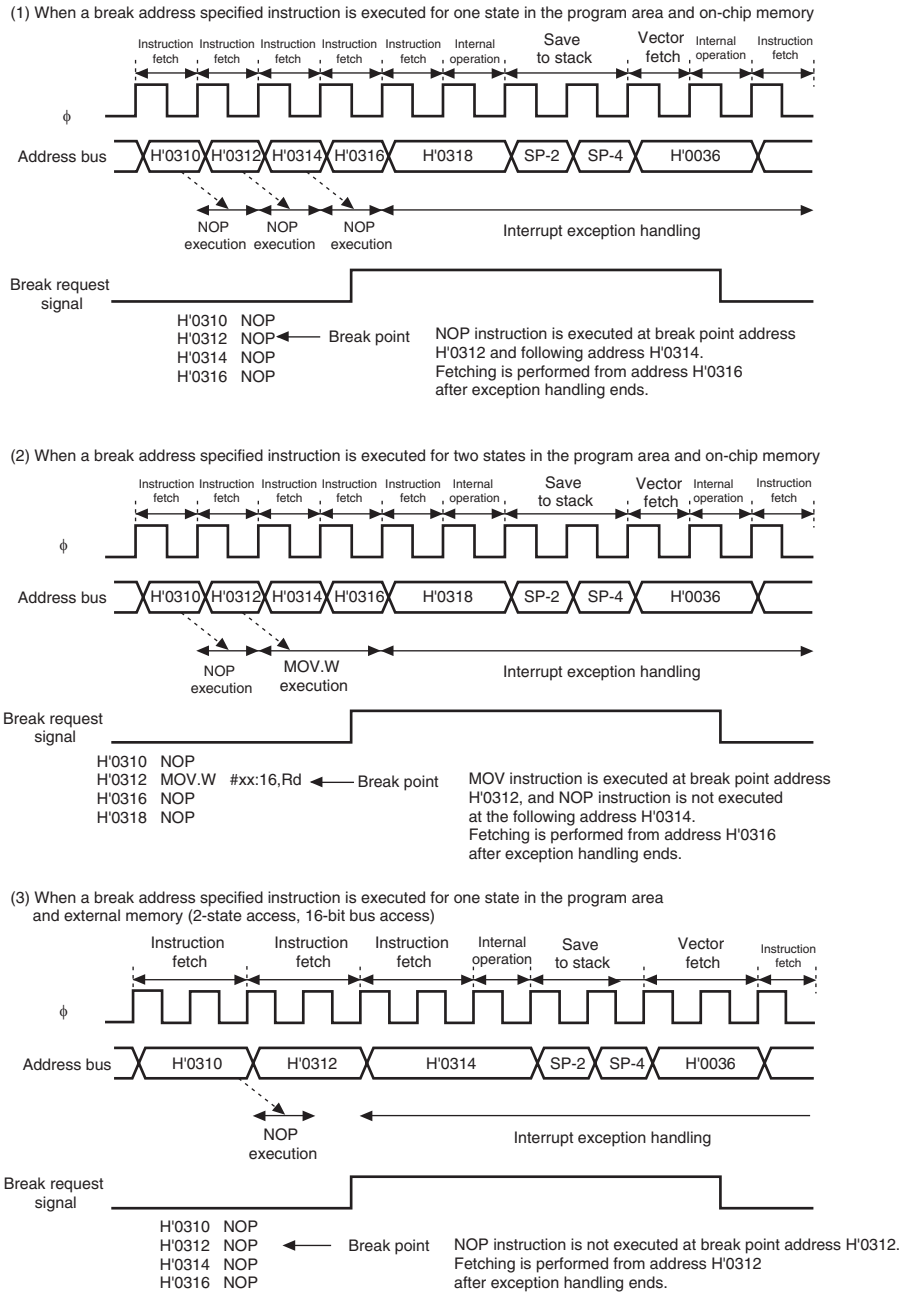


Figure 5.9 Address Break Timing Example

5.8 Usage Notes

5.8.1 Conflict between Interrupt Generation and Disabling

When an interrupt enable bit is cleared to 0 to disable interrupt requests, the disabling becomes effective after execution of the instruction. When an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, and if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request of higher priority than that interrupt, interrupt exception handling will be executed for the higher-priority interrupt, and the lower-priority interrupt will be ignored. The same rule is also applied when an interrupt source flag is cleared to 0. Figure 5.10 shows an example in which the CMIEA bit in the TMR's TCR register is cleared to 0.

The above conflict will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

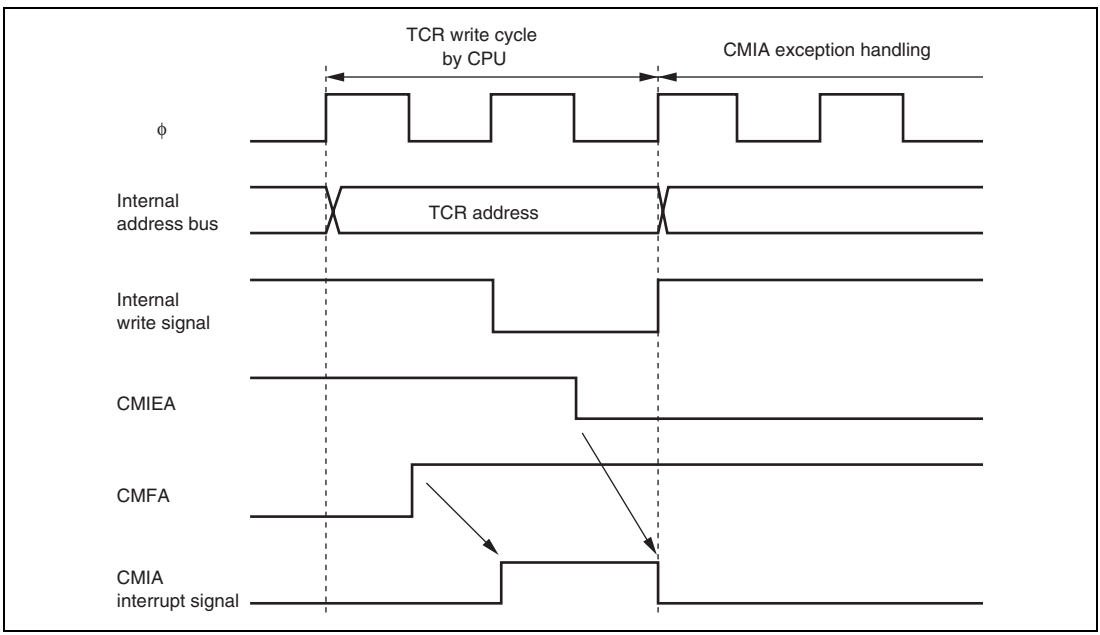


Figure 5.10 Conflict between Interrupt Generation and Disabling

5.8.2 Instructions that Disable Interrupts

The instructions that disable interrupts are LDC, ANDC, ORC, and XORC. After any of these instructions are executed, all interrupts including NMI are disabled and the next instruction is always executed. When the I bit or UI bit is set by one of these instructions, the new value becomes valid two states after execution of the instruction ends.

5.8.3 Interrupts during Execution of EEPMOV Instruction

Interrupt operation differs between the EEPMOV.B instruction and the EEPMOV.W instruction.

With the EEPMOV.B instruction, an interrupt request (including NMI) issued during the transfer is not accepted until the move is completed.

With the EEPMOV.W instruction, if an interrupt request is issued during the transfer, interrupt exception handling starts at a break in the transfer cycle. The PC value saved on the stack in this case is the address of the next instruction. Therefore, if an interrupt is generated during execution of an EEPMOV.W instruction, the following coding should be used.

```
L1:     EEPMOV.W
        MOV.W   R4,R4
        BNE     L1
```

5.8.4 IRQ Status Register (ISR)

According to the pin status after a reset, IRQnF may be set to 1, so ISR should be read after a reset to write 0. (n = 7 to 0)

Section 6 Bus Controller (BSC)

This LSI has an on-chip bus controller (BSC) that can specify the bus settings such as the bus width and the number of access cycles of the external address space.

6.1 Features

- Basic bus interface
  2-state access or 3-state access can be selected for each area
  Program wait cycles can be inserted for each area
- Burst ROM interface
  A burst ROM interface can be set for basic expansion areas
  1-state access or 2-state access can be selected for burst access
- Idle cycle insertion
  An idle cycle can be inserted for external write cycles immediately after external read cycles

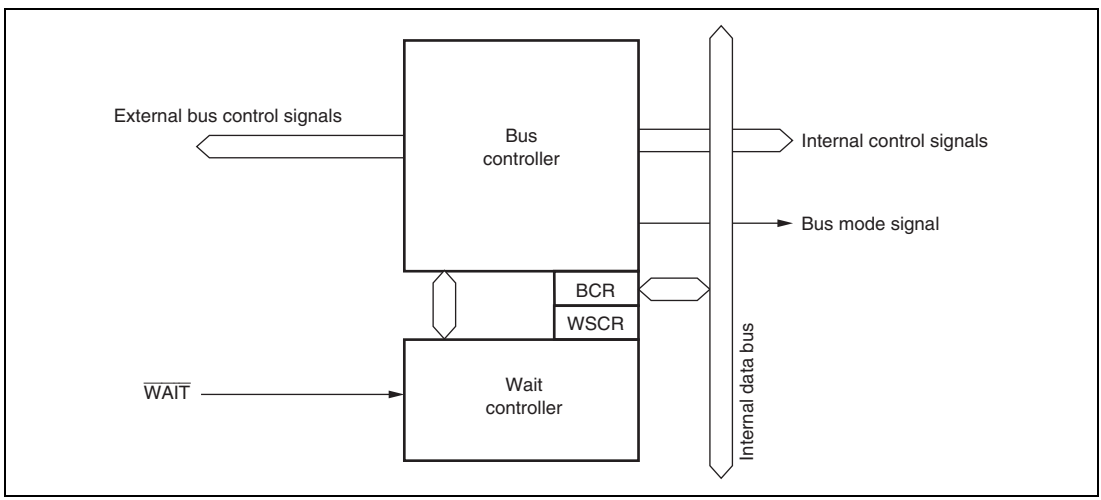


Figure 6.1 Block Diagram of Bus Controller

6.2 Input/Output Pins

Tables 6.1 and 6.2 summarize the pin configuration of the bus controller.

Table 6.1 Pin Configuration of H8S/2144B

Symbol	I/O	Function
$\overline{AS}$	Output	Strobe signal indicating that address output on the address bus is valid (when the IOSE bit in SYSCR is cleared to 0).
$\overline{IOS}$	Output	I/O select signal (when the IOSE bit in SYSCR is set to 1).
$\overline{RD}$	Output	Strobe signal indicating that the external address space is being read.
$\overline{HWR}$	Output	Strobe signal indicating that the external address space is being written to, and the upper byte (D15 to D8) of the data bus is valid.
$\overline{LWR}$	Output	Strobe signal indicating that the external address space is being written to, and the lower byte (D7 to D0) of the data bus is valid.
$\overline{WAIT}$	Input	Wait request signal when accessing the external 3-state access space.

Table 6.2 Pin Configuration of H8S/2134B

Symbol	I/O	Function
$\overline{AS}$	Output	Strobe signal indicating that address output on the address bus is valid (when the IOSE bit in SYSCR is cleared to 0).
$\overline{IOS}$	Output	I/O select signal (when the IOSE bit in SYSCR is set to 1).
$\overline{RD}$	Output	Strobe signal indicating that the external address space is being read.
$\overline{WR}$	Output	Strobe signal indicating that the external address space is being written to, and the data bus (D7 to D0) is valid.
$\overline{WAIT}$	Input	Wait request signal when accessing the external 3-state access space.

6.3 Register Descriptions

The bus controller has the following registers. For details on the system control register, refer to section 3.2.2, System Control Register (SYSCR).

- Bus control register (BCR)
- Wait state control register (WSCR)

6.3.1 Bus Control Register (BCR)

BCR is used to specify the access mode for the external address space or the I/O area range when the $\overline{AS}$/$\overline{IOS}$ pin is specified as an I/O strobe pin.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	R/W	Reserved This bit should not be written by 0.
6	ICIS0	1	R/W	Idle Cycle Insertion Selects whether or not to insert 1-state of the idle cycle between bus cycles when the external write cycle follows the external read cycle. 0: Idle cycle not inserted when the external write cycle follows the external read cycle 1: 1-state idle cycle inserted when the external write cycle follows the external read cycle
5	BRSTRM	0	R/W	Burst ROM Enable Selects the bus interface for the external address space. 0: Basic bus interface 1: Burst ROM interface
4	BRSTS1	1	R/W	Burst Cycle Select 1 Selects the number of cycles in the burst cycle of the burst ROM interface. 0: 1 cycle 1: 2 cycles

Bit	Bit Name	Initial Value	R/W	Description
3	BRSTS0	0	R/W	Burst Cycle Select 0 Selects the number of words that can be accessed by burst access via the burst ROM interface. 0: Max, 4 words 1: Max, 8 words
2	—	0	R/W	Reserved This bit should not be written by 0.
1	IOS1	1	R/W	IOS Select 1, 0
0	IOS0	1	R/W	Select the address range where the $\overline{\text{IOS}}$ signal is output. For details, refer to table 6.4, Address Range for IOS Signal Output.

6.3.2 Wait State Control Register (WSCR)

WSCR is used to specify the data bus width for external address space access, the number of access cycles, the wait mode, and the number of wait cycles for access to external address spaces. The bus width and the number of access cycles for internal memory and internal I/O registers are fixed regardless of the WSCR settings.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved
6	—	0	R/W	These bits should not be written by 1.
5	ABW	1	R/W	Bus Width Control Selects 8 or 16bits for access to the external address space. 0: 16-bit access space* 1: 8-bit access space

Bit	Bit Name	Initial Value	R/W	Description
4	AST	1	R/W	Access State Control Selects 2 or 3 access cycles for access to the external address space. This bit also enables or disables wait-cycle insertion. 0: 2-state access space. Wait cycle insertion disabled in external address space access 1: 3-state access space. Wait cycle insertion enabled in external address space access
3	WMS1	0	R/W	Wait Mode Select 1, 0
2	WMS0	0	R/W	Select the wait mode for access to the external address space when the AST bit is set to 1. 00: Program wait mode 01: Wait disabled mode 10: Pin wait mode 11: Pin auto-wait mode
1	WC1	1	R/W	Wait Count 1, 0
0	WC0	1	R/W	Select the number of program wait cycles to be inserted when the external address space is accessed while the AST bit is set to 1. 00: Program wait cycle is not inserted 01: 1 program wait cycle is inserted 10: 2 program wait cycles are inserted 11: 3 program wait cycles are inserted

Note: * Setting prohibited in the H8S/2134B.

6.4 Bus Control

6.4.1 Bus Specifications

The external address space bus specifications consist of three elements: Bus width, the number of access cycles, and the wait mode and the number of program wait cycles. The bus width and the number of access cycles for on-chip memory and internal I/O registers are fixed, and are not affected by the bus controller settings.

Bus Width: A bus width of 8 or 16 bits can be selected by the ABW bit in WSCR. Note that the 16-bit bus width cannot be set in the H8S/2134B.

Number of Access Cycles: Two or three access cycles can be selected via the AST bit in WSCR. When the 2-state access space is designated, wait-cycle insertion is disabled.

In the burst ROM interface, the number of access cycles is determined regardless of the AST bit setting.

Wait Mode and Number of Program Wait Cycles: When a 3-state access space is designated by the AST bit in WSCR, the wait mode and the number of program wait cycles to be inserted automatically is selected by the WMS1, WMS0, WC1, and WC0 bits in WSCR. From 0 to 3 program wait cycles can be selected.

Table 6.3 shows the bus specifications for the basic bus interface of each area.

Table 6.3 Bus Specifications for Basic Bus Interface

						Bus Specifications		
ABW	AST	WMS1	WMS0	WC1	WC0	Bus Width	Number of Access Cycles	Number of Program Wait Cycles
0	0	—	—	—	—	16	2	0
	1	0	1	—	—	16	3	0
		—*	—*	0	0		3	0
					1			1
				1	0			2
					1			3
1	0	—	—	—	—	8	2	0
	1	0	1	—	—	8	3	0
		—*	—*	0	0		3	0
					1			1
				1	0			2
					1			3

Note: * Other than WMS1 = 0 and WMS0 = 1

6.4.2 Advanced Mode

The external address space is initialized to the basic bus interface and a 3-state access space. In on-chip ROM enabled extended mode, the address space other than on-chip ROM, on-chip RAM, internal I/O registers, and their reserved areas is specified as the external address space. The on-chip RAM and its reserved area are enabled when the RAME bit in SYSCR is set to 1. They are disabled and corresponding addresses are the external address space when the RAME bit is cleared to 0.

In the H8S/2134B, the upper address in advanced mode (A16 to A23) cannot be output since there are only 16 address output pins. However, an area from H'FFF000 to H'FFF7FF can be accessed using the $\overline{AS}/\overline{IOS}$ signal specified as the I/O select signal. Therefore, the area can be accessed even when the H8S/2134B operates in ROM disabled extended and advanced mode.

6.4.3 Normal Mode

The external address space is initialized as the basic bus interface and a 3-state access space. In on-chip ROM disable extended mode, the address space other than on-chip RAM and internal I/O registers is specified as the external address space. In on-chip ROM enable extended mode, the address space other than on-chip ROM, on-chip RAM, internal I/O registers, and their reserved areas is specified as the external address space. The on-chip RAM area is enabled when the RAME bit in SYSCR is set to 1, and disabled and specified as the external address space when the RAME bit is cleared to 0.

6.4.4 I/O Select Signals

The LSI can output I/O select signals ($\overline{IOS}$); the signal is driven low when the corresponding external address space is accessed. Figure 6.2 shows an example of $\overline{IOS}$ signal output timing.

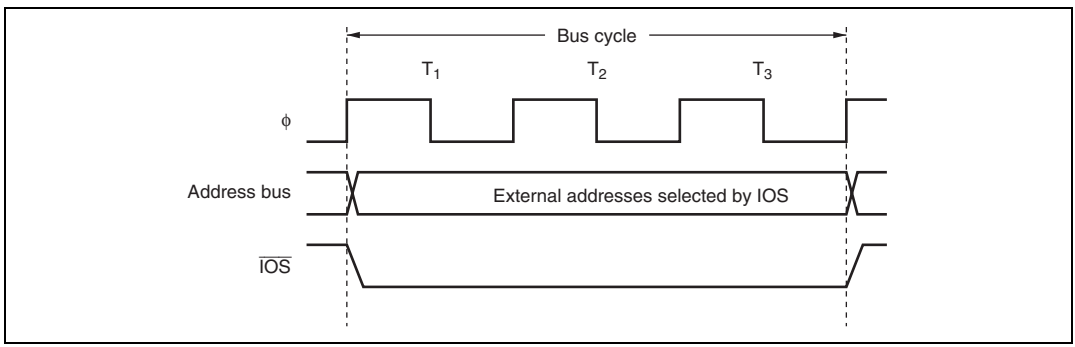


Figure 6.2 $\overline{IOS}$ Signal Output Timing

Enabling or disabling $\overline{IOS}$ signal output is performed by the IOSE bit in SYSCR. In extended mode, the $\overline{IOS}$ pin functions as an $\overline{AS}$ pin by a reset. To use this pin as an $\overline{IOS}$ pin, set the IOSE bit to 1. For details, refer to section 7, I/O Ports.

The address ranges of the $\overline{IOS}$ signal output can be specified by the IOS1 and IOS0 bits in BCR, as shown in table 6.4.

Table 6.4 Address Range for $\overline{IOS}$ Signal Output

IOS1	IOS0	$\overline{IOS}$ Signal Output Range	
0	0	H'(FF)F000 to H'(FF)F03F	
	1	H'(FF)F000 to H'(FF)F0FF	
1	0	H'(FF)F000 to H'(FF)F3FF	
	1	H'(FF)F000 to H'(FF)F7FF	(Initial value)

6.5 Basic Bus Interface

The basic bus interface enables direct connection to ROM and SRAM. For details on selection of the bus specifications when using the basic bus interface, see table 6.3

6.5.1 Data Size and Data Alignment

Data sizes for the CPU and other internal bus masters are byte, word, and longword. The BSC has a data alignment function, and controls whether the upper data bus (D15 to D8) or lower data bus (D7 to D0) is used when the external address space is accessed, according to the bus specifications for the area being accessed (8-bit access space or 16-bit access space) and the data size.

8-Bit Access Space: Figure 6.3 illustrates data alignment control for the 8-bit access space. With the 8-bit access space, the upper data bus (D15 to D8) is always used for accesses. The amount of data that can be accessed at one time is one byte: a word access is performed as two byte accesses, and a longword access, as four byte accesses.

In the H8S/2134B, eight bits of the data bus are available (D7 to D0) and only the 8-bit access space is settable. Therefore, data alignment described in this section is not performed.

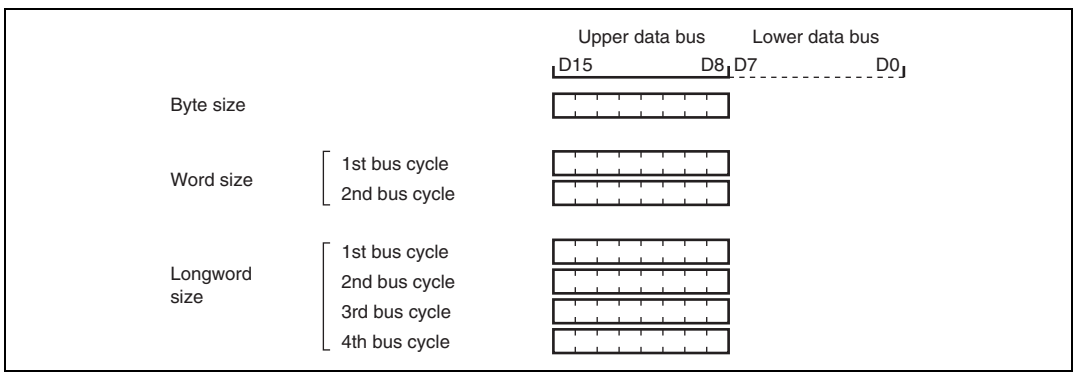


Figure 6.3 Access Sizes and Data Alignment Control (8-Bit Access Space)

16-Bit Access Space (Not available for the H8S/2134B): Figure 6.4 illustrates data alignment control for the 16-bit access space. With the 16-bit access space, the upper data bus (D15 to D8) and lower data bus (D7 to D0) are used for accesses. The amount of data that can be accessed at one time is one byte or one word, and a longword access is executed as two word accesses.

In byte access, whether the upper or lower data bus is used is determined by whether the address is even or odd. The upper data bus is used for an even address, and the lower data bus for an odd address.

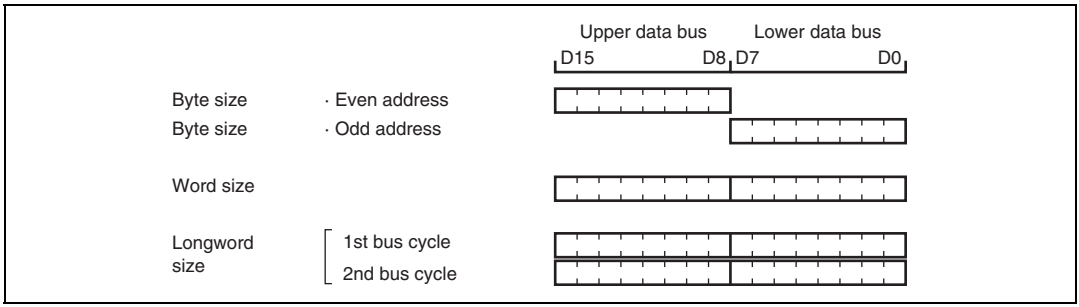


Figure 6.4 Access Sizes and Data Alignment Control (16-bit Access Space)

6.5.2 Valid Strobes

Table 6.5 shows the data buses used and valid strobes for each access space.

In a read, the $\overline{RD}$ signal is valid for both the upper and lower bytes of the data bus. In a write, the $\overline{HWR}$ signal is valid for the upper byte of the data bus, and the $\overline{LWR}$ signal for the lower byte.

In the H8S/2134B, only eight bits of the data bus is valid (D7 to D0). The strobe signals corresponding to the 8-bit data bus are the $\overline{RD}$ and $\overline{WR}$ signal. The $\overline{WR}$ signal in the H8S/2134B is the equivalent of the $\overline{HWR}$ signal in the H8S/2144B.

Table 6.5 Data Buses Used and Valid Strobes

					H8S/2144B		H8S/2134B
Area	**Access Size**	**Read/ Write**	**Address**	**Valid Strobe**	**Upper Data Bus (D15 to D8)**	**Lower Data Bus (D7 to D0)**	**Data Bus (D7 to D0)**
8-bit access space	Byte	Read	—	$\overline{RD}$	Valid	Ports or others	Valid
		Write	—	$\overline{HWR}$ ($\overline{WR}$)		Ports or others	
16-bit access space [H8S/2144B]	Byte	Read	Even	$\overline{RD}$	Valid	Invalid	Valid
			Odd		Invalid	Valid	Invalid
		Write	Even	$\overline{HWR}$	Valid	Undefined	Valid
			Odd	$\overline{LWR}$	Undefined	Valid	Undefined
	Word	Read	—	$\overline{RD}$	Valid	Valid	Valid
		Write	—	$\overline{HWR}$, $\overline{LWR}$	Valid	Valid	Valid

Note: * Undefined: Undefined data is output.
Invalid: Input state with the input value ignored.
Ports or others: Used as ports or I/O pins for on-chip peripheral modules, and are not used as the data bus.

6.5.3 Basic Operation Timing

8-Bit, 2-State Access Space: Figure 6.5 shows the bus timing for an 8-bit, 2-state access space. When an 8-bit access space is accessed, the upper byte (D15 to D8) of the data bus is used in the H8S/2144B. Wait cycles cannot be inserted.

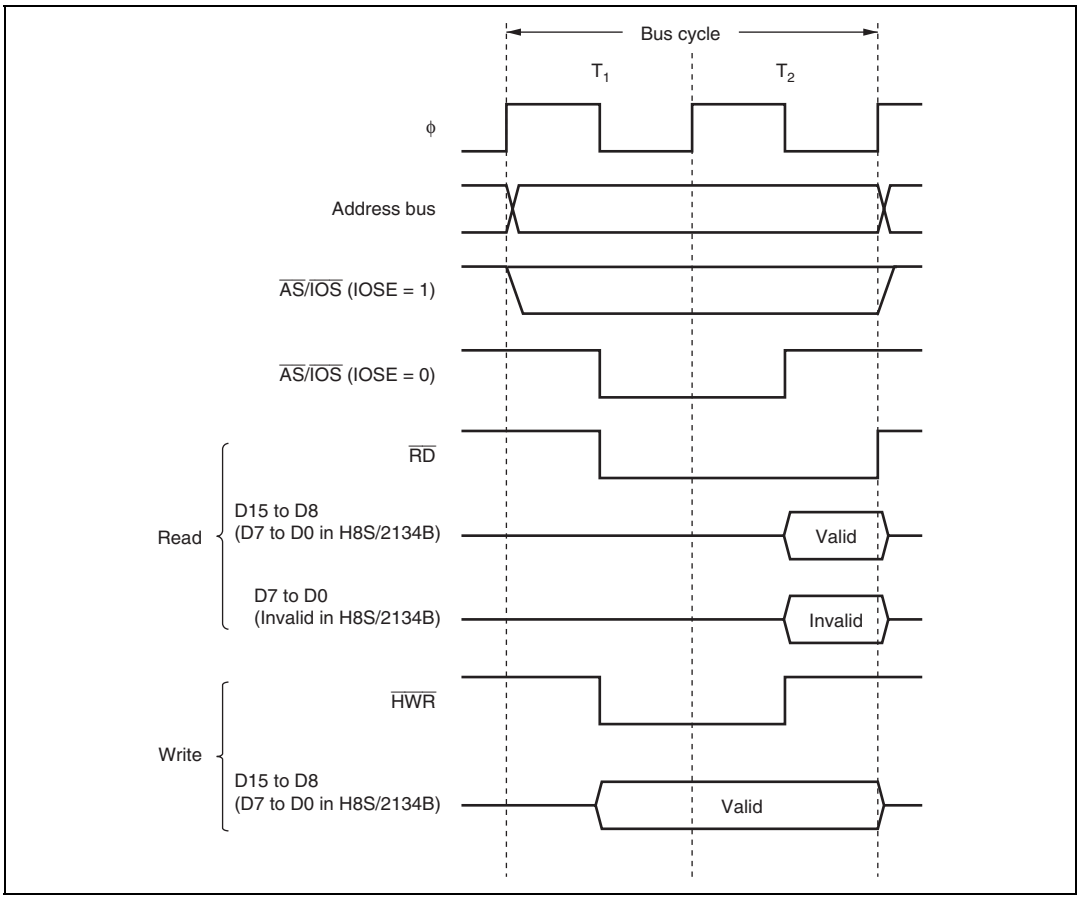


Figure 6.5 Bus Timing for 8-Bit, 2-State Access Space

8-Bit, 3-State Access Space: Figure 6.6 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, the upper byte (D15 to D8) of the data bus is used in the H8S/2144B. Wait cycles can be inserted.

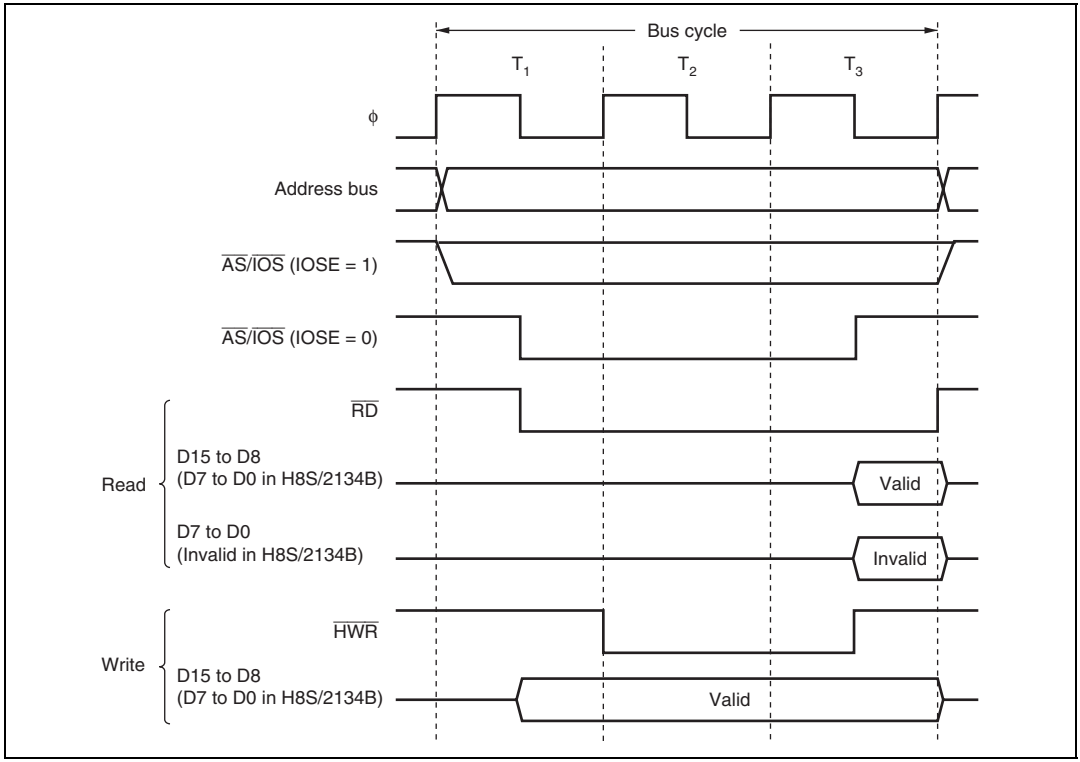


Figure 6.6 Bus Timing for 8-Bit, 3-State Access Space

16-Bit, 2-State Access Space [Available for H8S/2144B]: Figures 6.7 to 6.9 show bus timings for a 16-bit, 2-state access space. When a 16-bit access space is accessed, the upper byte (D15 to D8) of the data bus is used for even addresses, and the lower byte (D7 to D0) for odd addresses. Wait cycles cannot be inserted.

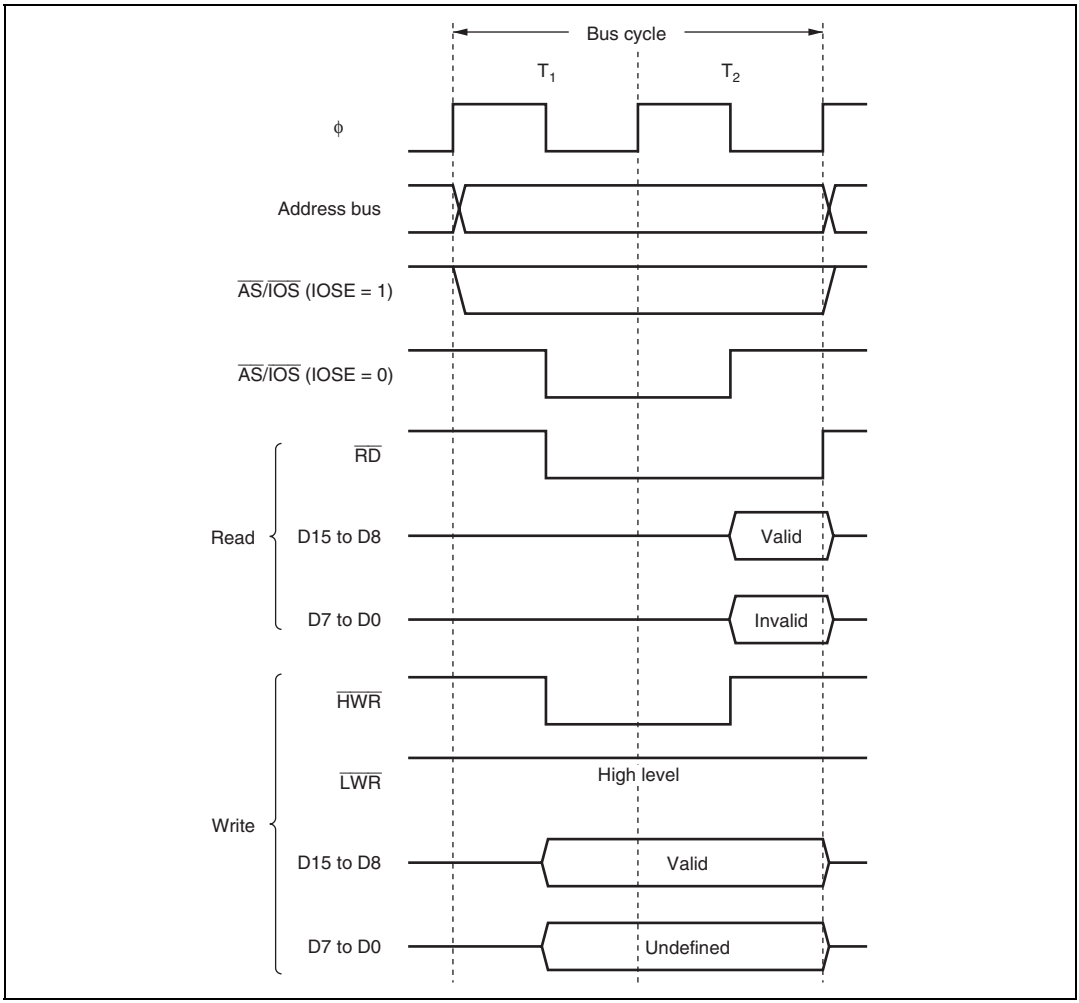


Figure 6.7 Bus Timing for 16-Bit, 2-State Access Space (Even Byte Access)

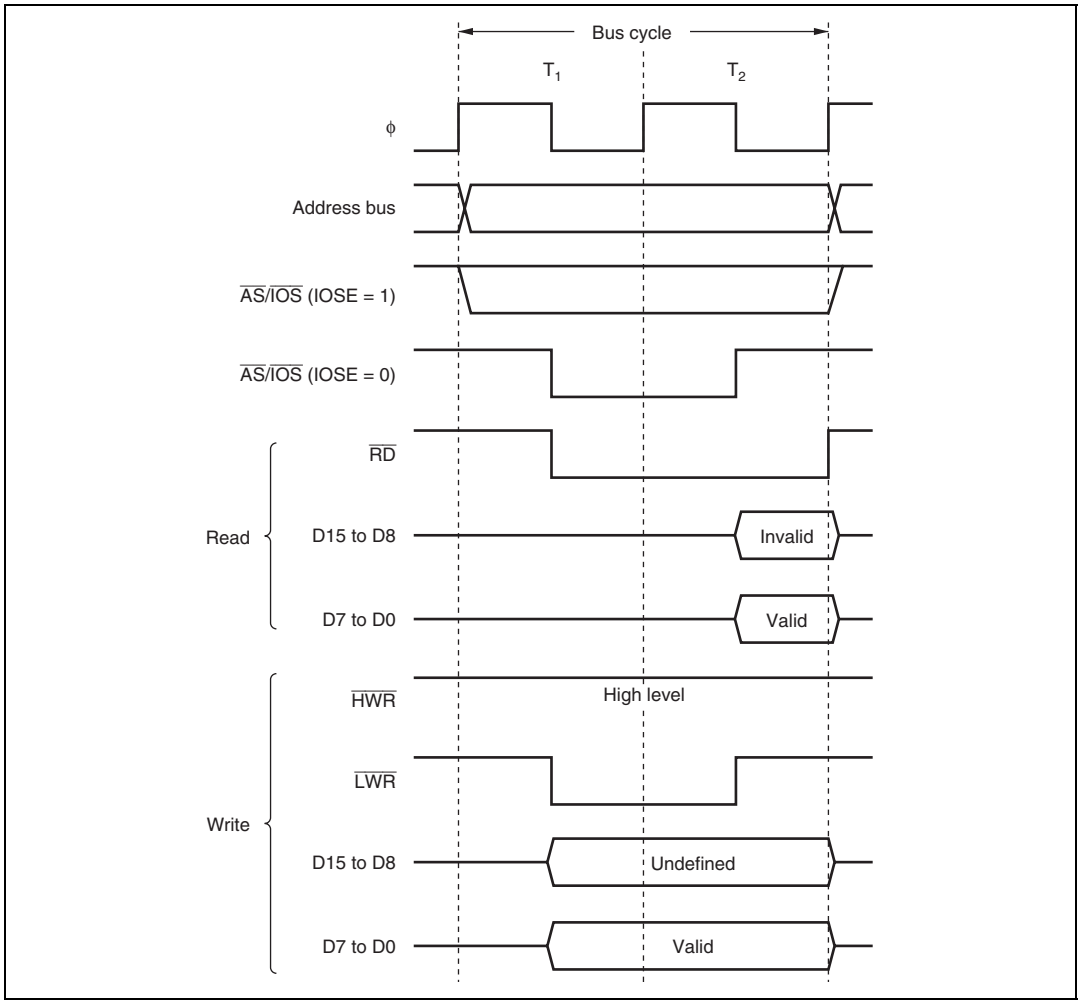


Figure 6.8 Bus Timing for 16-Bit, 2-State Access Space (Odd Byte Access)

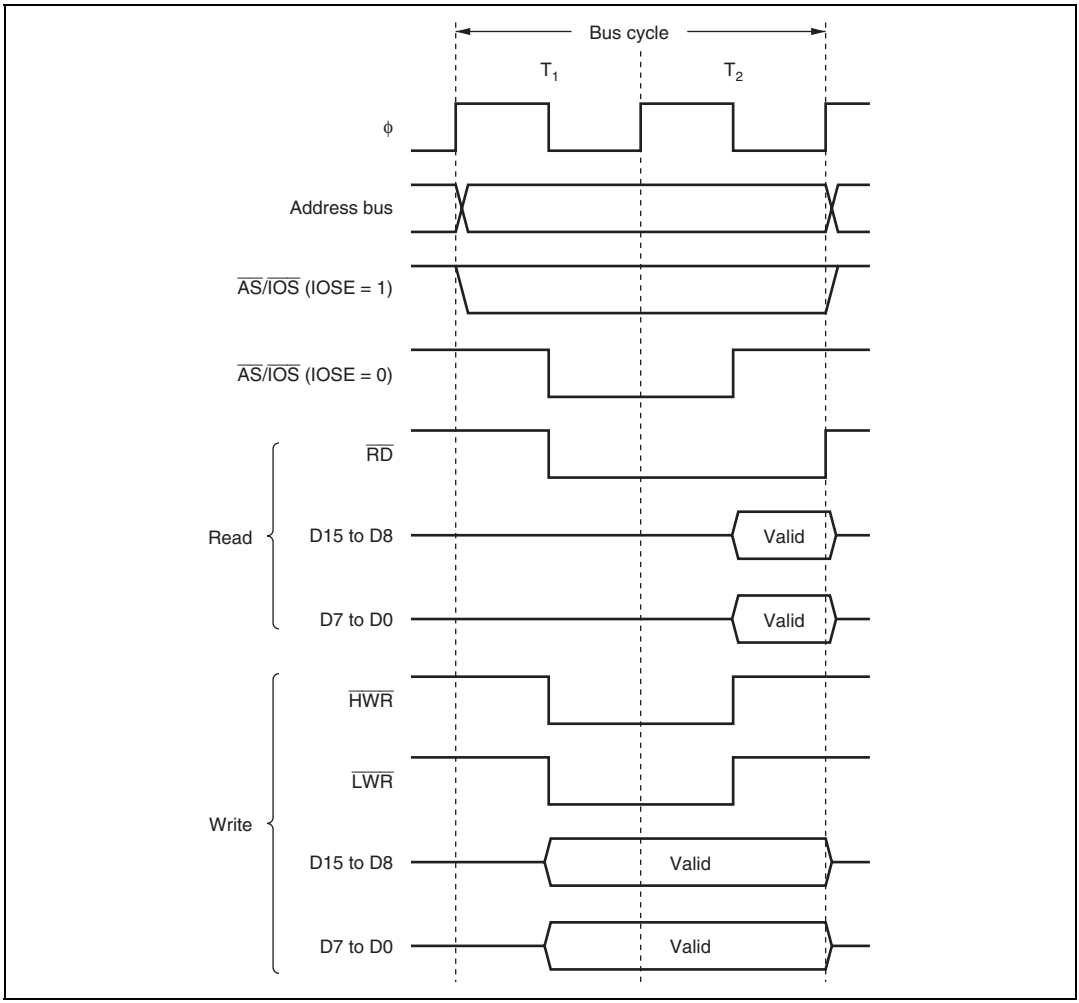


Figure 6.9 Bus Timing for 16-Bit, 2-State Access Space (Word Access)

16-Bit, 3-State Access Space [Available for H8S/2144B]: Figures 6.10 to 6.12 show bus timings for a 16-bit, 3-state access space. When a 16-bit access space is accessed, the upper byte (D15 to D8) of the data bus is used for even addresses, and the lower byte (D7 to D0) for odd addresses. Wait cycles can be inserted.

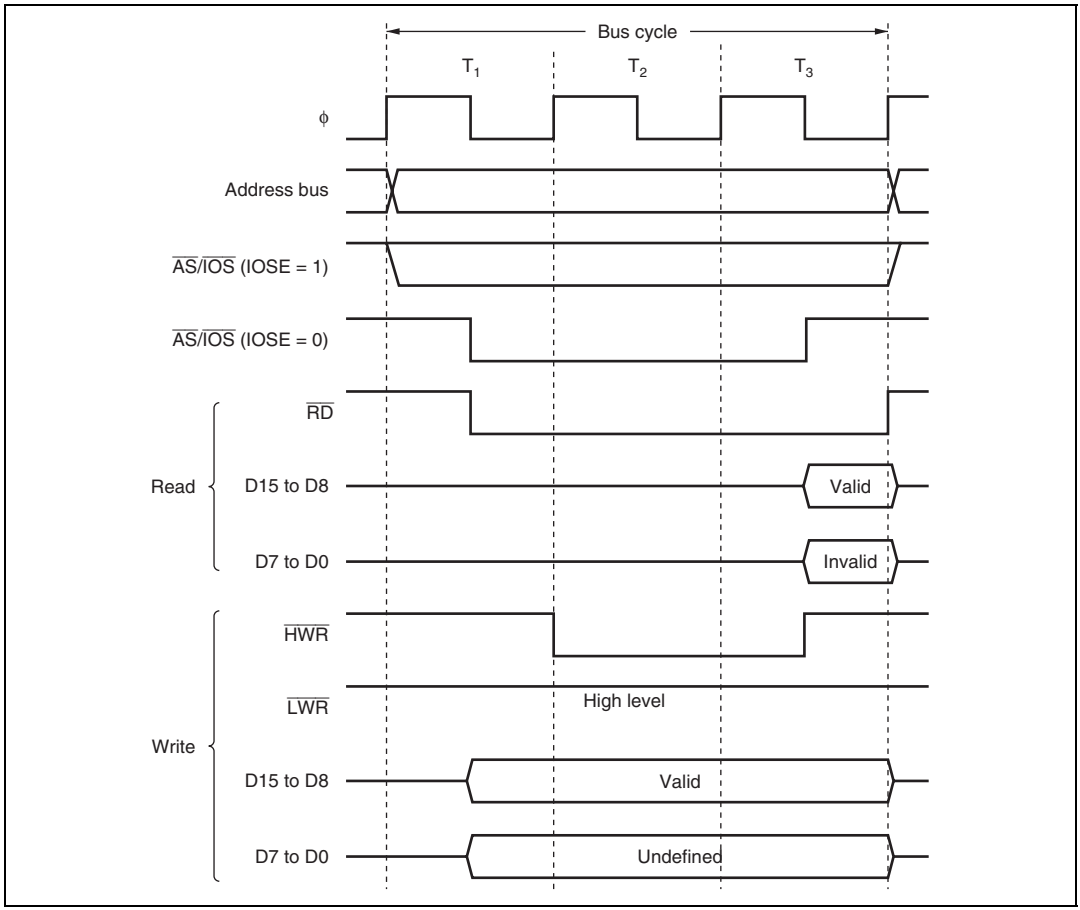


Figure 6.10 Bus Timing for 16-Bit, 3-State Access Space (Even Byte Access)

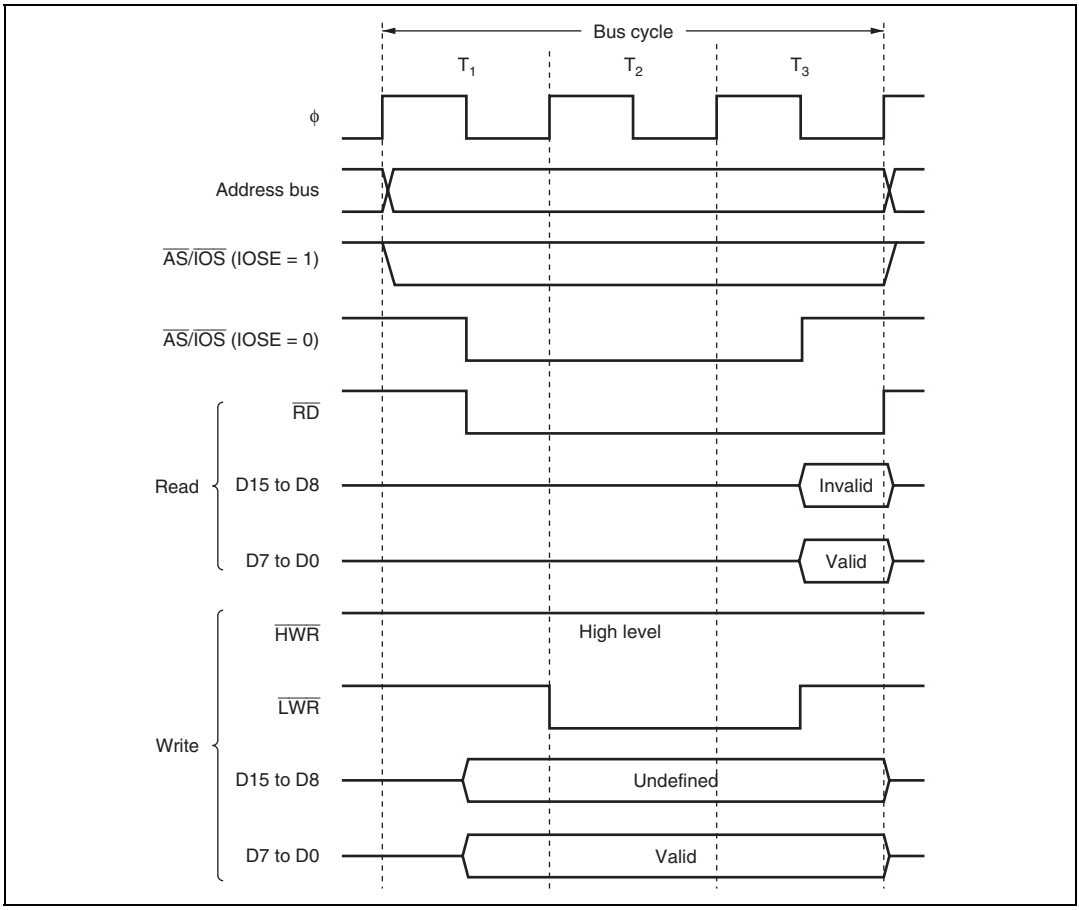


Figure 6.11 Bus Timing for 16-Bit, 3-State Access Space (Odd Byte Access)

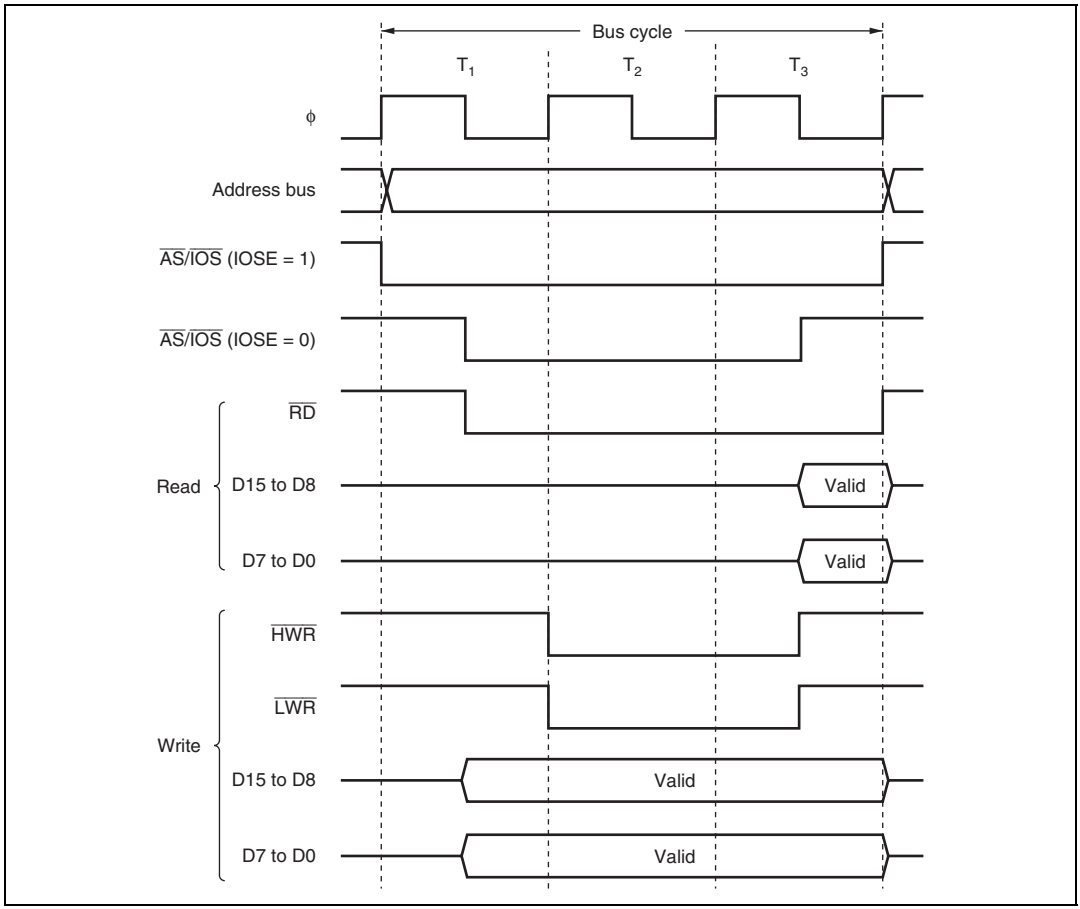


Figure 6.12 Bus Timing for 16-Bit, 3-State Access Space (Word Access)

6.5.4 Wait Control

When accessing the external address space, this LSI can extend the bus cycle by inserting one or more wait cycles (T_W). There are three ways of inserting wait cycles: Program wait insertion, pin wait insertion using the $\overline{\text{WAIT}}$ pin, and the combination of program wait and the $\overline{\text{WAIT}}$ pin.

Program Wait Mode: A specified number of wait cycles T_W can be inserted automatically between the T_2 state and T_3 state when accessing the external address space always according to the settings of the WC1 and WC0 bits in WSCR.

Pin Wait Mode: A specified number of wait cycles T_W can be inserted automatically between the T_2 state and T_3 state when accessing the external address space always according to the settings of the WC1 and WC0 bits. If the $\overline{\text{WAIT}}$ pin is low at the falling edge of ϕ in the last T_2 or T_W state, another T_W state is inserted. If the $\overline{\text{WAIT}}$ pin is held low, T_W states are inserted until it goes high.

This is useful when inserting four or more T_W states, or when changing the number of T_W states to be inserted for each external device.

Pin Auto-Wait Mode: A specified number of wait cycles T_W can be inserted automatically between the T_2 state and T_3 state when accessing the external address space according to the settings of the WC1 and WC0 bits if the $\overline{\text{WAIT}}$ pin is low at the falling edge of ϕ in the last T_2 state. Even if the $\overline{\text{WAIT}}$ pin is held low, T_W states can be inserted only up to the specified number of cycles.

This function enables the low-speed memory interface only by inputting the chip select signal to the $\overline{\text{WAIT}}$ pin.

Figure 6.13 shows an example of wait cycle insertion timing in pin wait mode.

The settings after a reset are: 3-state access, 3 program wait insertion, and $\overline{\text{WAIT}}$ pin input disabled.

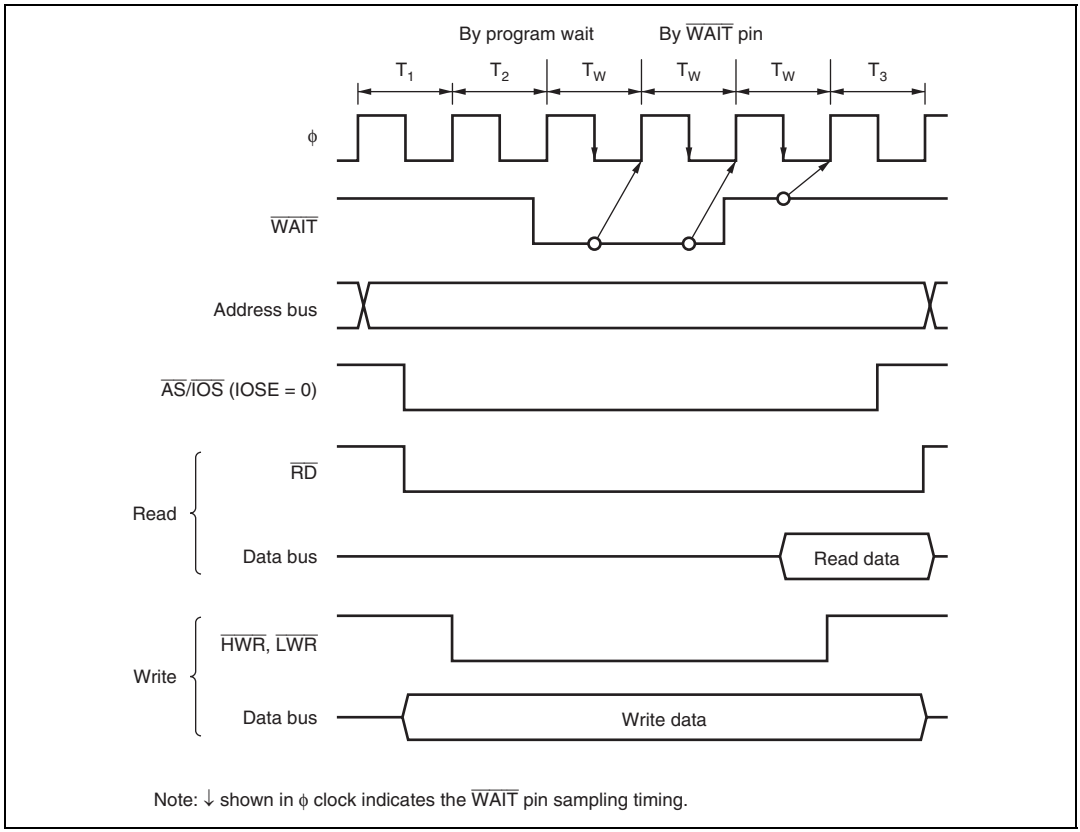


Figure 6.13 Example of Wait Cycle Insertion Timing (Pin Wait Mode)

6.6 Burst ROM Interface

In this LSI, the external address space can be designated as the burst ROM space by setting the BRSTRM bit in BCR to 1, and the burst ROM interface enabled. Consecutive burst accesses of a maximum four or eight words can be performed only during CPU instruction fetch. One or two cycles can be selected for burst ROM access.

6.6.1 Basic Operation Timing

The number of access cycles in the initial cycle (full access) of the burst ROM interface is determined by the AST bit in WSCR. When the AST bit is set to 1, wait cycles can be inserted. One or two cycles can be selected for burst access according to the setting of the BRSTS1 bit in BCR. Wait cycles cannot be inserted in a burst cycle. Burst accesses of a maximum four words is performed when the BRSTS0 bit in BCR is cleared to 0, and burst accesses of a maximum eight words is performed when the BRSTS0 bit in BCR is set to 1.

The basic access timing for the burst ROM space is shown in figures 6.14 and 6.15.

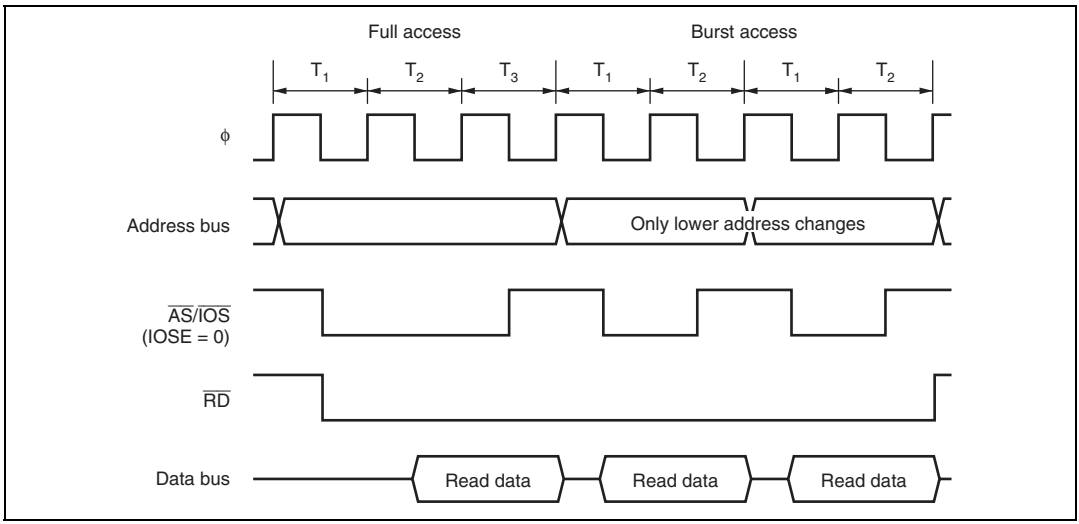


Figure 6.14 Access Timing Example in Burst ROM Space (AST = BRSTS1 = 1)

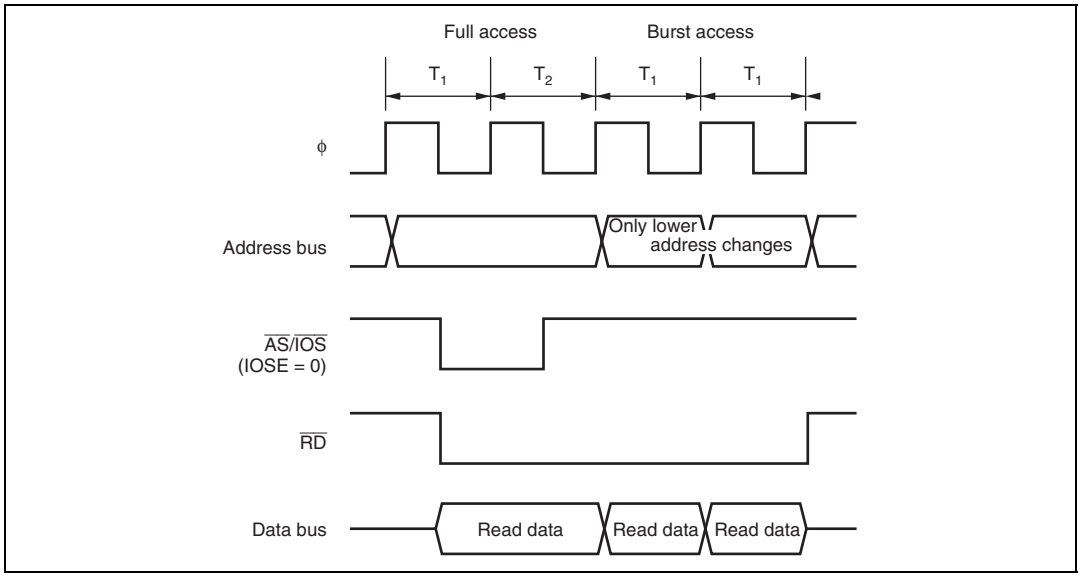


Figure 6.15 Access Timing Example in Burst ROM Space (AST = BRSTS1 = 0)

6.6.2 Wait Control

As with the basic bus interface, program wait insertion or pin wait insertion using the $\overline{\text{WAIT}}$ pin can be used in the initial cycle (full access) of the burst ROM interface. For details, see section 6.5.4, Wait Control. Wait cycles cannot be inserted in a burst cycle.

6.7 Idle Cycle

When this LSI accesses the external address space, it can insert a 1-state idle cycle (T_I) between bus cycles when a write cycle occurs immediately after a read cycle. By inserting an idle cycle it is possible, for example, to avoid data collisions between ROM with a long output floating time, and high-speed memory and I/O interfaces.

If an external write occurs after an external read while the ICIS0 bit is set to 1 in BCR, an idle cycle is inserted at the start of the write cycle.

Figure 6.16 shows examples of idle cycle operation. In these examples, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a CPU write cycle. In figure 6.16 (a), with no idle cycle inserted, a collision occurs in bus cycle B between the read data from ROM and the CPU write data. In figure 6.16 (b), an idle cycle is inserted, thus preventing data collision.

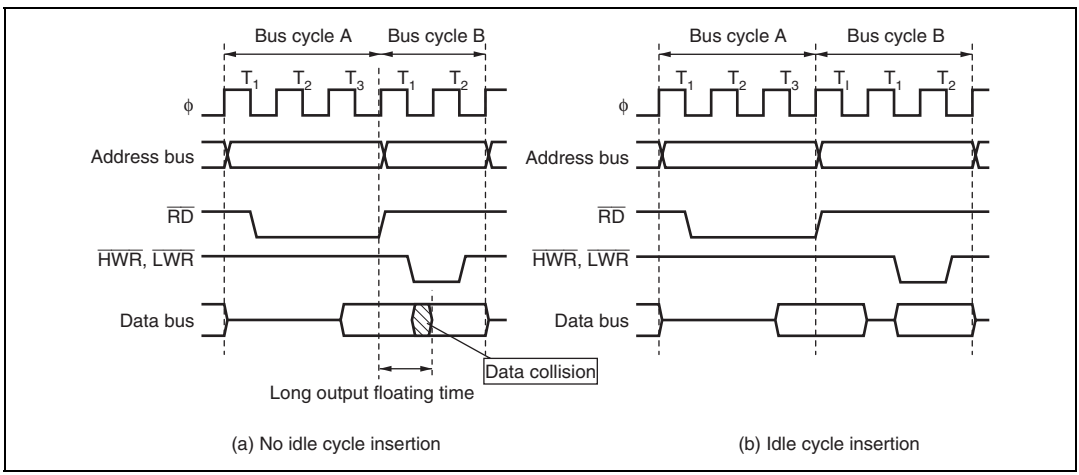


Figure 6.16 Examples of Idle Cycle Operation

Table 6.6 shows the pin states in an idle cycle.

Table 6.6 Pin States in Idle Cycle

Pins (H8S/2144B)	Pins (H8S/2134B)	Pin State
A23 to A0, $\overline{IOS}$	A15 to A0, $\overline{IOS}$	Contents of immediately following bus cycle
D15 to D0	D7 to D0	High impedance
$\overline{AS}$	$\overline{AS}$	High
$\overline{RD}$	$\overline{RD}$	High
$\overline{HWR}$, $\overline{LWR}$	$\overline{WR}$	High

Section 7 I/O Ports

7.1 Overview

In the H8S/2144B, ten I/O ports (ports 1 to 6, 8, 9, A, and B) and one input-only port (port 7) are included. In the H8S/2134B, eight I/O ports (ports 1 to 6, 8, and 9) and one input-only port (port 7) are included.

Table 7.1 is a summary of the port functions. The pins of each port also have other functions.

Each port includes a data direction register (DDR) that controls input/output (not provided for the input-only port) and data registers (DR, ODR) that store output data.

Ports 1 to 3, 6, A, and B have an on-chip input pull-up MOS function. For ports A and B, the on/off status of the input pull-up MOS is controlled by DDR and ODR. Ports 1 to 3 and 6 have an input pull-up MOS control register (PCR), in addition to DDR and DR, to control the on/off status of the input pull-up MOS.

Ports 1 to 6, 8, 9, A, and B can drive a single TTL load and 30 pF capacitive load. All the I/O ports can drive a Darlington transistor when in output mode. Ports 1, 2, and 3 can drive an LED (10 mA sink current).

Port A input and output use by the VccB power supply, which is independent of the V_{CC} power supply. When the VccB voltage is 5V, the pins on port A will be 5-V tolerant.

PA4 to PA7 of port A have the capability to drive bus buffers.

Table 7.1 Port Functions of H8S/2144B

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port 1	General I/O port also functioning as address output pin	A7	A7/P17	P17	On-chip input pull-up MOSs
		A6	A6/P16	P16	
		A5	A5/P15	P15	
		A4	A4/P14	P14	
		A3	A3/P13	P13	
		A2	A2/P12	P12	
		A1	A1/P11	P11	
		A0	A0/P10	P10	
Port 2	General I/O port also functioning as address output pin	A15	A15/P27	P27	On-chip input pull-up MOSs
		A14	A14/P26	P26	
		A13	A13/P25	P25	
		A12	A12/P24	P24	
		A11	A11/P23	P23	
		A10	A10/P22	P22	
		A9	A9/P21	P21	
		A8	A8/P20	P20	
Port 3	General I/O port also functioning as data bus input/output pin	D15		P37	On-chip input pull-up MOSs
		D14		P36	
		D13		P35	
		D12		P34	
		D11		P33	
		D10		P32	
		D9		P31	
		D8		P30	

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port 4	General I/O port also functioning as PWMX output, TMR_0 and TMR_1 input/output, SCI_2 input/output, and IrDA interface input/output pins	P47/PWX1			
		P46/ PWX0			
		P45/TMRI1			
		P44/TMO1			
		P43/TMCI1			
		P42/TMRI0/SCK2			
		P41/TMO0/RxD2/IrRxD			
		P40/TMCI0/TxD2/IrTxD			
Port 5	General I/O port also functioning as SCI_0 input/output pins	P52/SCK0			
		P51/RxD0			
		P50/TxD0			
Port 6	General I/O port also functioning as interrupt input, FRT input/output, TMR_Y input/output, key-sense interrupt input, and extended A/D input pins	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$			On-chip input pull-up MOSs
		P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$			
		P65/FTID/CIN5/$\overline{\text{KIN5}}$			
		P64/FTIC/CIN4/$\overline{\text{KIN4}}$			
		P63/FTIB/CIN3/$\overline{\text{KIN3}}$			
		P62/FTIA/CIN2/$\overline{\text{KIN2}}$/TMIY			
		P61/FTOA/CIN1/$\overline{\text{KIN1}}$			
		P60/FTCI/CIN0/$\overline{\text{KIN0}}$			
Port 7	General input port also functioning as A/D converter analog input and D/A converter analog output pins	P77/AN7/DA1			
		P76/AN6/DA0			
		P75/AN5			
		P74/AN4			
		P73/AN3			
		P72/AN2			
		P71/AN1			
		P70/AN0			

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port 8	General I/O port also functioning as interrupt input and SCI_1 input/output pins	P86/$\overline{\text{IRQ5}}$/SCK1			
		P85/$\overline{\text{IRQ4}}$/RxD1			
		P84/$\overline{\text{IRQ3}}$/TxD1			
		P83			
		P82			
		P81			
		P80			
Port 9	General I/O port also functioning as extended data bus control input/output, subclock input, ϕ output, interrupt input, and A/D converter external trigger input pins	P97/$\overline{\text{WAIT}}$		P97	
		P96/ϕ/EXCL		P96/ϕ/EXCL	
		$\overline{\text{AS}}$/$\overline{\text{IOS}}$		P95	
		$\overline{\text{HWR}}$		P94	
		$\overline{\text{RD}}$		P93	
		P92/$\overline{\text{IRQ0}}$		P92/$\overline{\text{IRQ0}}$	
		P91/$\overline{\text{IRQ1}}$		P91/$\overline{\text{IRQ1}}$	
		P90/$\overline{\text{LWR}}$/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$		P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$	
Port A	General I/O port also functioning as address output, key-sense interrupt input, and extended A/D input pins	PA7/$\overline{\text{KIN15}}$/CIN15	PA7/A23/$\overline{\text{KIN15}}$/CIN15	PA7/$\overline{\text{KIN15}}$/CIN15	On-chip input pull-up MOSs
		PA6/$\overline{\text{KIN14}}$/CIN14	PA6/A22/$\overline{\text{KIN14}}$/CIN14	PA6/$\overline{\text{KIN14}}$/CIN14	
		PA5/$\overline{\text{KIN13}}$/CIN13	PA5/A21/$\overline{\text{KIN13}}$/CIN13	PA5/$\overline{\text{KIN13}}$/CIN13	
		PA4/$\overline{\text{KIN12}}$/CIN12	PA4/A20/$\overline{\text{KIN12}}$/CIN12	PA4/$\overline{\text{KIN12}}$/CIN12	
		PA3/$\overline{\text{KIN11}}$/CIN11	PA3/A19/$\overline{\text{KIN11}}$/CIN11	PA3/$\overline{\text{KIN11}}$/CIN11	
		PA2/$\overline{\text{KIN10}}$/CIN10	PA2/A18/$\overline{\text{KIN10}}$/CIN10	PA2/$\overline{\text{KIN10}}$/CIN10	
		PA1/$\overline{\text{KIN9}}$/CIN9	PA1/A17/$\overline{\text{KIN9}}$/CIN9	PA1/$\overline{\text{KIN9}}$/CIN9	
		PA0/$\overline{\text{KIN8}}$/CIN8	PA0/A16/$\overline{\text{KIN8}}$/CIN8	PA0/$\overline{\text{KIN8}}$/CIN8	

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port B	General I/O port also functioning as data bus input/output pins	PB7/D7		PB7	On-chip input pull-up MOSs
		PB6/D6		PB6	
		PB5/D5		PB5	
		PB4/D4		PB4	
		PB3/D3		PB3	
		PB2/D2		PB2	
		PB1/D1		PB1	
		PB0/D0		PB0	

Table 7.2 Port Functions of H8S/2134B

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port 1	General I/O port also functioning as address output pin	A7	A7/P17	P17	On-chip input pull-up MOSs
		A6	A6/P16	P16	
		A5	A5/P15	P15	
		A4	A4/P14	P14	
		A3	A3/P13	P13	
		A2	A2/P12	P12	
		A1	A1/P11	P11	
		A0	A0/P10	P10	
Port 2	General I/O port also functioning as address output pin	A15	A15/P27	P27	On-chip input pull-up MOSs
		A14	A14/P26	P26	
		A13	A13/P25	P25	
		A12	A12/P24	P24	
		A11	A11/P23	P23	
		A10	A10/P22	P22	
		A9	A9/P21	P21	
		A8	A8/P20	P20	

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port 3	General I/O port also functioning as data bus input/output pin	D7		P37	On-chip input pull-up MOSs
		D6		P36	
		D5		P35	
		D4		P34	
		D3		P33	
		D2		P32	
		D1		P31	
		D0		P30	
Port 4	General I/O port also functioning as PWMX output, TMR_0 and TMR_1 input/output, SCI_2 input/output, and IrDA interface input/output pins	P47/PWX1			
		P46/ PWX0			
		P45/TMRI1			
		P44/TMO1			
		P43/TMCI1			
		P42/TMRI0/SCK2			
		P41/TMO0/RxD2/IrRxD			
		P40/TMCI0/TxD2/IrTxD			
Port 5	General I/O port also functioning as SCI_0 input/output pins	P52/SCK0			
		P51/RxD0			
		P50/TxD0			
Port 6	General I/O port also functioning as interrupt input, FRT input/output, TMR_Y input/output, key-sense interrupt input, and extended A/D input pins	P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$			On-chip input pull-up MOSs
		P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$			
		P65/FTID/CIN5/$\overline{\text{KIN5}}$			
		P64/FTIC/CIN4/$\overline{\text{KIN4}}$			
		P63/FTIB/CIN3/$\overline{\text{KIN3}}$			
		P62/FTIA/CIN2/$\overline{\text{KIN2}}$/TMIY			
		P61/FTOA/CIN1/$\overline{\text{KIN1}}$			
		P60/FTC/CIN0/$\overline{\text{KIN0}}$			

Port	Description	Mode 1	Mode 2 (EXPE = 1)	Mode 3 (EXPE = 0)	I/O Status
Port 7	General input port also functioning as A/D converter analog input and D/A converter analog output pins	P77/AN7/DA1			
		P76/AN6/DA0			
		P75/AN5			
		P74/AN4			
		P73/AN3			
		P72/AN2			
		P71/AN1			
		P70/AN0			
Port 8	General I/O port also functioning as interrupt input and SCI_1 input/output pins	P86/$\overline{\text{IRQ5}}$/SCK1			
		P85/$\overline{\text{IRQ4}}$/RxD1			
		P84/$\overline{\text{IRQ3}}$/TxD1			
		P83			
		P82			
		P81			
		P80			
Port 9	General I/O port also functioning as extended data bus control input/output, subclock input, ϕ output, interrupt input, and A/D converter external trigger input pins	P97/$\overline{\text{WAIT}}$		P97	
		P96/ϕ/EXCL		P96/ϕ/EXCL	
		$\overline{\text{AS}}$/$\overline{\text{IOS}}$		P95	
		$\overline{\text{WR}}$		P94	
		$\overline{\text{RD}}$		P93	
		P92/$\overline{\text{IRQ0}}$		P92/$\overline{\text{IRQ0}}$	
		P91/$\overline{\text{IRQ1}}$		P91/$\overline{\text{IRQ1}}$	
		P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$		P90/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$	

7.2 Port 1

Port 1 is an 8-bit I/O port. Port 1 pins also function as address output pins. Port 1 functions change according to the operating mode. Port 1 has an on-chip input pull-up MOS function that can be controlled by software. Port 1 has the following registers.

- Port 1 data direction register (P1DDR)
- Port 1 data register (P1DR)
- Port 1 pull-up MOS control register (P1PCR)

7.2.1 Port 1 Data Direction Register (P1DDR)

P1DDR specifies input or output for the pins of port 1 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P17DDR	0	W	In mode 1: Each pin of port 1 is address output regardless of the set value of P1DDR. In modes 2 and 3 (EXPE=1): The corresponding port 1 pins are address output ports when P1DDR bits are set to 1, and input ports when cleared to 0. In modes 2 and 3 (EXPE=0): The corresponding port 1 pins are output ports when the P1DDR bits are set to 1, and input ports when cleared to 0.
6	P16DDR	0	W	
5	P15DDR	0	W	
4	P14DDR	0	W	
3	P13DDR	0	W	
2	P12DDR	0	W	
1	P11DDR	0	W	
0	P10DDR	0	W	

7.2.2 Port 1 Data Register (P1DR)

P1DR stores output data for the port 1 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P17DR	0	R/W	If a port 1 read is performed while the P1DDR bits are set to 1, the P1DR values are read. If a port 1 read is performed while the P1DDR bits are cleared to 0, the pin states are read.
6	P16DR	0	R/W	
5	P15DR	0	R/W	
4	P14DR	0	R/W	
3	P13DR	0	R/W	
2	P12DR	0	R/W	
1	P11DR	0	R/W	
0	P10DR	0	R/W	

7.2.3 Port 1 Pull-Up MOS Control Register (P1PCR)

P1PCR controls the on/off status of the port 1 on-chip input pull-up MOSs.

Bit	Bit Name	Initial Value	R/W	Description
7	P17PCR	0	R/W	When the pins are in input state, the corresponding input pull-up MOS is turned on when a P1PCR bit is set to 1.
6	P16PCR	0	R/W	
5	P15PCR	0	R/W	
4	P14PCR	0	R/W	
3	P13PCR	0	R/W	
2	P12PCR	0	R/W	
1	P11PCR	0	R/W	
0	P10PCR	0	R/W	

7.2.4 Pin Functions

- P17/A7, P16/A6, P15/A5, P14/A4, P13/A3, P12/A2, P11/A1, and P10/A0

  Pin functions are switched as shown below according to the combination of the P1nDDR bit and operating mode.

Operating Mode	Mode 1	Mode 2, 3 (EXPE = 1)		Mode 2, 3 (EXPE = 0)	
P1nDDR	—	0	1	0	1
Pin Function	A7 to A0 output pins	P17 to P10 input pins	A7 to A0 output pins	P17 to P10 input pins	P17 to P10 output pins

[Legend]
n = 7 to 0

7.2.5 Port 1 Input Pull-Up MOS

Port 1 has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

Table 7.3 summarizes the input pull-up MOS states.

Table 7.3 Input Pull-Up MOS States (Port 1)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1	Off	Off	Off	Off
2, 3			On/Off	On/Off

[Legend]
Off: Input pull-up MOS is always off.
On/Off: On when the pin is in the input state, P1DDR = 0, and P1PCR = 1; otherwise off.

7.3 Port 2

Port 2 is an 8-bit I/O port. Port 2 pins also function as address bus output pins. Port 2 functions change according to the operating mode. Port 2 has an on-chip input pull-up MOS function that can be controlled by software. Port 2 has the following registers.

- Port 2 data direction register (P2DDR)
- Port 2 data register (P2DR)
- Port 2 pull-up MOS control register (P2PCR)

7.3.1 Port 2 Data Direction Register (P2DDR)

P2DDR specifies input or output for the pins of port 2 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P27DDR	0	W	In Mode 1: The corresponding port 2 pins are address outputs, regardless of the P2DDR setting. Modes 2 and 3 (EXPE = 1): The corresponding port 2 pins are address outputs when P2DDR bits are set to 1, and input ports when cleared to 0. P27 to P24 are switched from address outputs to output ports by setting the IOSE bit to 1. To ensure normal accesses to an external space, port 2 pins should not be set as an on-chip peripheral module output pin when port 2 pins are used as address output pins. Modes 2 and 3 (EXPE = 0): The corresponding port 2 pins are output ports when P2DDR bits are set to 1, and input ports when cleared to 0.
6	P26DDR	0	W	
5	P25DDR	0	W	
4	P24DDR	0	W	
3	P23DDR	0	W	
2	P22DDR	0	W	
1	P21DDR	0	W	
0	P20DDR	0	W	

7.3.2 Port 2 Data Register (P2DR)

P2DR stores output data for port 2.

Bit	Bit Name	Initial Value	R/W	Description
7	P27DR	0	R/W	If a port 2 read is performed while P2DDR bits are set to 1, the P2DR values are read directly, regardless of the actual pin states. If a port 2 read is performed while P2DDR bits are cleared to 0, the pin states are read.
6	P26DR	0	R/W	
5	P25DR	0	R/W	
4	P24DR	0	R/W	
3	P23DR	0	R/W	
2	P22DR	0	R/W	
1	P21DR	0	R/W	
0	P20DR	0	R/W	

7.3.3 Port 2 Pull-Up MOS Control Register (P2PCR)

P2PCR controls the port 2 on-chip input pull-up MOSs.

Bit	Bit Name	Initial Value	R/W	Description
7	P27PCR	0	R/W	In modes 2 and 3, the input pull-up MOS is turned on when a P2PCR bit is set to 1 in the input port state.
6	P26PCR	0	R/W	
5	P25PCR	0	R/W	
4	P24PCR	0	R/W	
3	P23PCR	0	R/W	
2	P22PCR	0	R/W	
1	P21PCR	0	R/W	
0	P20PCR	0	R/W	

7.3.4 Pin Functions

To ensure normal access to external space, P27 should not be set as an on-chip peripheral module output pin when port 2 pins are used as address output pins.

- P27/A15, P26/A14, P25/A13, and P24/A12

  Pin functions are switched as shown below according to the combination of the IOSE bit in SYSCR, P27DDR bit, and operating mode.

Operating Mode	Mode 1	Mode 2, 3 (EXPE = 1)			Mode 2, 3 (EXPE = 0)	
P2nDDR	—	0	1		0	1
IOSE	—	—	0	1	—	—
Pin Function	A15 to A12 output pins	P27 to P24 input pins	A15 to A12 output pins	P27 to P24 input pins	P27 to P24 input pins	P27 to P24 input pins

[Legend]
n = 7 to 4

- P23/A11, P22/A10, P21/A9, and P20/A8

  Pin functions are switched as shown below according to the combination of the P2nDDR bit and operating mode.

Operating Mode	Mode 1	Mode 2, 3 (EXPE = 1)		Mode 2, 3 (EXPE = 0)	
P2nDDR	—	0	1	0	1
Pin Function	A11 to A8 output pins	P23 to P20 input pins	A11 to A8 output pins	P23 to P20 input pins	P23 to P20 input pins

[Legend]
n = 3 to 0

7.3.5 Port 2 Input Pull-Up MOS

Port 2 has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

Table 7.4 summarizes the input pull-up MOS states.

Table 7.4 Input Pull-Up MOS States (Port 2)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1	Off	Off	Off	Off
2, 3			On/Off	On/Off

[Legend]

Off: Input pull-up MOS is always off.

On/Off: On when the pin is in the input state, P2DDR = 0, and P2PCR = 1; otherwise off.

7.4 Port 3

Port 3 is an 8-bit I/O port. Port 3 pins also function as a bidirectional data bus. Port 3 functions change according to the operating mode. Port 3 has the following registers.

- Port 3 data direction register (P3DDR)
- Port 3 data register (P3DR)
- Port 3 pull-up MOS control register (P3PCR)

7.4.1 Port 3 Data Direction Register (P3DDR)

P3DDR specifies input or output for the pins of port 3 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P37DDR	0	W	Modes 1, 2, and 3 (EXPE = 1) The input/output direction specified by P3DDR is ignored, and pins automatically function as data I/O pins. Modes 2 and 3 (EXPE = 0) The corresponding port 3 pins are output ports when P3DDR bits are set to 1, and input ports when cleared to 0.
6	P36DDR	0	W	
5	P35DDR	0	W	
4	P34DDR	0	W	
3	P33DDR	0	W	
2	P32DDR	0	W	
1	P31DDR	0	W	
0	P30DDR	0	W	

7.4.2 Port 3 Data Register (P3DR)

P3DR stores output data of port 3.

Bit	Bit Name	Initial Value	R/W	Description
7	P37DR	0	R/W	If a port 3 read is performed while P3DDR bits are set to 1, the P3DR values are read directly, regardless of the actual pin states. If a port 3 read is performed while P3DDR bits are cleared to 0, the pin states are read.
6	P36DR	0	R/W	
5	P35DR	0	R/W	
4	P34DR	0	R/W	
3	P33DR	0	R/W	
2	P32DR	0	R/W	
1	P31DR	0	R/W	
0	P30DR	0	R/W	

7.4.3 Port 3 Pull-Up MOS Control Register (P3PCR)

P3PCR controls the port 3 on-chip input pull-up MOSs on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P37PCR	0	R/W	In modes 2 and 3 (when EXPE = 0), the input pull-up MOS is turned on when a P3PCR bit is set to 1 in the input port state. The input pull-up MOS function cannot be used when the host interface is enabled.
6	P36PCR	0	R/W	
5	P35PCR	0	R/W	
4	P34PCR	0	R/W	
3	P33PCR	0	R/W	
2	P32PCR	0	R/W	
1	P31PCR	0	R/W	
0	P30PCR	0	R/W	

7.4.4 Pin Functions

- P37/D15*, P36/D14*, P35/D13*, P34/D12*, P33/D11*, P32/D10*, P31/D9*, and P30/D8*
  Pin functions are switched as shown below according to the combination of the P3nDDR bit and operating mode.

Operating Mode	Mode 1, 2, 3 (EXPE = 1)	Mode 2, 3 (EXPE = 0)	
P3nDDR	—	0	1
Pin Function	D15 to D8* input/output pins	P37 to P30 input pins	P37 to P30 output pins

Note: n = 7 to 0
* D7 to D0 in the H8S/2134B are equivalent of D15 to D8 in the H8S/2144B.

7.4.5 Port 3 Input Pull-Up MOS

Port 3 has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

Table 7.5 summarizes the input pull-up MOS states.

Table 7.5 Input Pull-Up MOS States (Port 3)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 3 (EXPE = 1)	Off	Off	Off	Off
2, 3 (EXPE = 0)			On/Off	On/Off

[Legend]

Off: Input pull-up MOS is always off.

On/Off: On when the pin is in the input state, P3DDR = 0, and P3PCR = 1; otherwise off.

7.5 Port 4

Port 4 is an 8-bit I/O port. Port 4 pins also function as PWMX output pins, TMR_0 and TMR_1 I/O pins, SCI_2 I/O pins, and IrDA interface I/O pins. Port 4 pin functions are the same in all operating modes. Port 4 has the following registers.

- Port 4 data direction register (P4DDR)
- Port 4 data register (P4DR)

7.5.1 Port 4 Data Direction Register (P4DDR)

P4DDR specifies input or output for the pins of port 4 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P47DDR	0	W	When a bit in P4DDR is set to 1, the corresponding pin functions as an output port, and when cleared to 0, as an input port. As 14-bit PWM and SCI_2 are initialized in software standby mode, the pin states are determined by the TMR_0, TMR_1, P4DDR, and P4DR specifications.
6	P46DDR	0	W	
5	P45DDR	0	W	
4	P44DDR	0	W	
3	P43DDR	0	W	
2	P42DDR	0	W	
1	P41DDR	0	W	
0	P40DDR	0	W	

7.5.2 Port 4 Data Register (P4DR)

P4DR stores output data for port 4.

Bit	Bit Name	Initial Value	R/W	Description
7	P47DR	0	R/W	If a port 4 read is performed while P4DDR bits are set to 1, the P4DR values are read directly, regardless of the actual pin states. If a port 4 read is performed while P4DDR bits are cleared to 0, the pin states are read.
6	P46DR	0	R/W	
5	P45DR	0	R/W	
4	P44DR	0	R/W	
3	P43DR	0	R/W	
2	P42DR	0	R/W	
1	P41DR	0	R/W	
0	P40DR	0	R/W	

7.5.3 Pin Functions

- P47/PWX1

  Pin functions are switched as shown below according to the combination of the OEB bit in DACR of the 14-bit PWM and the P47DDR bit.

OEB	0		1
P47DDR	0	1	—
Pin Function	P47 input pin	P47 output pin	PWX1 output pin

- P46/PWX0

  Pin functions are switched as shown below according to the combination of the OEA bit in DACR of the 14-bit PWM and the P46DDR bit.

OEA	0		1
P46DDR	0	1	—
Pin Function	P46 input pin	P46 output pin	PWX0 output pin

- P45/TMRI1

  Pin functions are switched as shown below according to the P45DDR bit.

P45DDR	0	1
Pin Function	P45 input pin	P45 output pin
	TMRI1 input pin*	

Note: * When bits CCLR1 and CCLR0 in TCR1 of TMR_1 are set to 1, this pin is used as the TMRI1 input pin.

- P44/TMO1

  Pin functions are switched as shown below according to the combination of the OS3 to OS0 bits in TCSR of TMR_1 and the P44DDR bit.

OS3 to OS0	All 0		Not all 0
P44DDR	0	1	—
Pin Function	P44 input pin	P44 output pin	TMO1 output pin

- P43/TMCI1

  Pin functions are switched as shown below according to the P43DDR bit.

P43DDR	0	1
Pin Function	P43 input pin	P43 output pin
	TMCI1 input pin*	

Note: * When the external clock is selected by bits CKS2 to CKS0 in TCR1 of TMR_1, this pin is used as the TMCI1 input pin.

- P42/TMRI0/SCK2

  Pin functions are switched as shown below according to the combination of the CKE1 and CKE0 bits in SCR of SCI_2, the C/$\overline{A}$ bit in SMR of SCI_2, and the P42DDR bit.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P42DDR	0	1	—	—	—
Pin Function	P42 input pin	P42 output pin	SCK2 output pin	SCK2 output pin	SCK2 input pin
	TMRI0 input pin*				

Note: * When bits CCLR1 and CCLR0 in TCR0 of TMR_0 are set to 1, this pin is used as the TMRI0 input pin.

- P41/TMO0/RxD2/IrRxD

  Pin functions are switched as shown below according to the combination of the OS3 to OS0 bits in TCSR of TMR0, the RE bit in SCR of SCI_2 and the P41DDR bit.

OS3 to OS0	All 0			Not all 0
RE	0		1	0
P41DDR	0	1	—	—
Pin Function	P41 input pin	P41 output pin	RxD2/IrRxD input pin	TMO0 output pin

Note: * When this pin is used as the TMO0 output pin, bit RE in SCR of SCI_2 must be cleared to 0.

- P40/TMCI0/TxD2/IrTxD

  Pin functions are switched as shown below according to the combination of the TE bit in SCR of SCI_2 and the P40DDR bit.

TE	0		1
P40DDR	0	1	—
Pin Function	P40 input pin	P40 output pin	TxD2/IrTxD output pin
	TMCI0 input pin*		

Note: * When an external clock is selected with bits CKS2 to CKS0 in TCR0 of TMR_0, this pin is used as the TMCI0 input pin.

7.6 Port 5

Port 5 is a 3-bit I/O port. Port 5 pins also function as SCI_0 I/O pins. Port 5 has the following registers.

- Port 5 data direction register (P5DDR)
- Port 5 data register (P5DR)

7.6.1 Port 5 Data Direction Register (P5DDR)

P5DDR specifies input or output for the pins of port 5 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved The initial value must not be changed.
2	P52DDR	0	W	The corresponding port 5 pins are output ports when P5DDR bits are set to 1, and input ports when cleared to 0. As SCI_0 is initialized in software standby mode, the pin states are determined by the P5DDR and P5DR specifications.
1	P51DDR	0	W	
0	P50DDR	0	W	

7.6.2 Port 5 Data Register (P5DR) P3PCR

P5DR stores output data for port 5 pins.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved The initial value must not be changed.
2	P52DR	0	R/W	If a port 5 read is performed while P5DDR bits are set to 1, the P5DR values are read directly, regardless of the actual pin states. If a port 5 read is performed while P5DDR bits are cleared to 0, the pin states are read.
1	P51DR	0	R/W	
0	P50DR	0	R/W	

7.6.3 Pin Functions

- P52/SCK0

  Pin functions are switched as shown below according to the combination of the CKE1 and CKE0 bits in SCR of SCI_0, the C/$\overline{A}$ bit in SMR of SCI_0, the ICE bit in ICCR of IIC_0, and the P52DDR bit.

CKE1	0				1
C/$\overline{A}$	0			1	—
CKE0	0		1	—	—
P52DDR	0	1	—	—	—
Pin Function	P52 input pin	P52 output pin	SCK0 output pin	SCK0 output pin	SCK0 input pin

- P51/RxD0

  Pin functions are switched as shown below according to the combination of the RE bit in SCR of SCI_0 and the P51DDR bit.

RE	0		1
P51DDR	0	1	—
Pin Function	P51 input pin	P51 output pin	RxD0 input pin

- P50/TxD0

  Pin functions are switched as shown below according to the combination of the TE bit in SCR of SCI_0 and the P50DDR bit.

TE	0		1
P50DDR	0	1	—
Pin Function	P50 input pin	P50 output pin	TxD0 output pin

7.7 Port 6

Port 6 is an 8-bit I/O port. Port 6 pins also function as the FRT I/O pins, the TMR_Y input pin, key-sense interrupt input pins, extended A/D converter input pins, and external interrupt input pins. The port 6 input level can be switched in four stages. Port 6 pin functions are the same in all operating modes. Port 6 has the following registers.

- Port 6 data direction register (P6DDR)
- Port 6 data register (P6DR)
- Port 6 pull-up MOS control register (KMPCR6)
- System control register 2 (SYSCR2)

7.7.1 Port 6 Data Direction Register (P6DDR)

P6DDR specifies input or output for the pins of port 6 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P67DDR	0	W	The corresponding port 6 pins are output ports when P6DDR bits are set to 1, and input ports when cleared to 0.
6	P66DDR	0	W	
5	P65DDR	0	W	
4	P64DDR	0	W	
3	P63DDR	0	W	
2	P62DDR	0	W	
1	P61DDR	0	W	
0	P60DDR	0	W	

7.7.2 Port 6 Data Register (P6DR)

P6DR stores output data for port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	P67DR	0	R/W	If a port 6 read is performed while P6DDR bits are set to 1, the P6DR values are read directly, regardless of the actual pin states. If a port 6 read is performed while P6DDR bits are cleared to 0, the pin states are read.
6	P66DR	0	R/W	
5	P65DR	0	R/W	
4	P64DR	0	R/W	
3	P63DR	0	R/W	
2	P62DR	0	R/W	
1	P61DR	0	R/W	
0	P60DR	0	R/W	

7.7.3 Port 6 Pull-Up MOS Control Register (KMPCR)

KMPCR controls the port 6 on-chip input pull-up MOSs on a bit-by-bit basis. To make the settings of this register valid, clear bit MSTP2 in MSTPCRL to 0.

Bit	Bit Name	Initial Value	R/W	Description
7	KM7PCR	0	R/W	The input pull-up MOS is turned on when a KMPCR bit is set to 1 while the corresponding P6DDR bit is cleared to 0 (input port setting).
6	KM6PCR	0	R/W	
5	KM5PCR	0	R/W	
4	KM4PCR	0	R/W	
3	KM3PCR	0	R/W	
2	KM2PCR	0	R/W	
1	KM1PCR	0	R/W	
0	KM0PCR	0	R/W	

7.7.4 System Control Register 2 (SYSCR2)

SYSCR2 controls the signal levels input on port 6 and current specifications.

Bit	Bit Name	Initial Value	R/W	Description
7	KWUL1	0	R/W	Key Wakeup Level 1 and 0
6	KWUL0	0	R/W	Selects the input level of port 6. The input levels of other functions of the multiplexed pin are also decided by these bits. 00: Normal input level 01: Input level 1 10: Input level 2 11: Input level 3
5	P6PUE	0	R/W	Port 6 Input Pull-Up MOS Extra Selects the specification of the input pull-up MOS in current driving ability. 0: Normal current specification 1: Limited current specification
4	—	0	—	Reserved Do not write 1 to this bit.
3 to 0	—	All 0	R/W	Reserved Do not write 1 to this bit

7.7.5 Pin Functions

- P67/CIN7/$\overline{\text{KIN7}}$/$\overline{\text{IRQ7}}$

  Pin functions are switched as shown below according to the P67DDR bit.

P67DDR	0	1
Pin Function	P67 input pin	P67 output pin
	$\overline{\text{IRQ7}}$ input pin, $\overline{\text{KIN7}}$ input pin, CIN7 input pin*	

Note: * This pin is used as the $\overline{\text{IRQ7}}$ input pin when bit IRQ7E is set to 1 in IER. It can always be used as the $\overline{\text{KIN7}}$ or CIN7 input pin.

- P66/FTOB/CIN6/$\overline{\text{KIN6}}$/$\overline{\text{IRQ6}}$

  Pin functions are switched as shown below according to the combination of the OEB bit in TOCR of the FRT and the P66DDR bit.

OEB	0	1	
P66DDR	0	1	—
Pin Function	P66 input pin	P66 output pin	FTOB output pin
	$\overline{\text{IRQ6}}$ input pin, $\overline{\text{KIN6}}$ input pin, CIN6 input pin*		

Note: * This pin is used as the $\overline{\text{IRQ6}}$ input pin when bit IRQ6E is set to 1 in IER while the KMIMR6 bit in KMIMR is 0. It can always be used as the $\overline{\text{KIN6}}$ or CIN6 input pin.

- P65/FTID/CIN5/$\overline{\text{KIN5}}$

P65DDR	0	1
Pin Function	P65 input pin	P65 output pin
	FTID input pin, $\overline{\text{KIN5}}$ input pin, CIN5 input pin*	

Note: * This pin can always be used as the FTID, $\overline{\text{KIN5}}$, or CIN5 input pin.

- P64/FTIC/CIN4/$\overline{\text{KIN4}}$

  Pin functions are switched as shown below according to the P64DDR bit.

P64DDR	0	1
Pin Function	P64 input pin	P64 output pin
	FTIC input pin, $\overline{\text{KIN4}}$ input pin, CIN4 input pin*	

Note: * This pin can always be used as the FTIC, $\overline{\text{KIN4}}$, or CIN4 input pin.

- P63/FTIB/CIN3/$\overline{\text{KIN3}}$

P63DDR	0	1
Pin Function	P63 input pin	P63 output pin
	FTIB input pin, $\overline{\text{KIN3}}$ input pin, CIN3 input pin*	

Note: * This pin can always be used as the FTIB, $\overline{\text{KIN3}}$, or CIN3 input pin.

- P62/FTIA/CIN2/$\overline{\text{KIN2}}$/TMIY

P62DDR	0	1
Pin Function	P62 input pin	P62 output pin
	FTIA input pin, TMIY input pin, $\overline{\text{KIN2}}$ input pin, CIN2 input pin*	

Note: * This pin can always be used as the FTIA, TMIY, $\overline{\text{KIN2}}$, or CIN2 input pin.

- P61/FTOA/CIN1/$\overline{\text{KIN1}}$

  Pin functions are switched as shown below according to the combination of the OEA bit in TOCR of the FRT and the P61DDR bit.

OEA	0		1
P61DDR	0	1	—
Pin Function	P61 input pin	P61 output pin	FTOA output pin
	$\overline{\text{KIN1}}$ input pin, CIN1 input pin*		

Note: * This pin can always be used as the $\overline{\text{KIN1}}$ or CIN1 input pin.

- P60/FTCI/CIN0/$\overline{\text{KIN0}}$

P60DDR	0	1
Pin Function	P60 input pin	P60 output pin
	FTCI input pin, $\overline{\text{KIN0}}$ input pin, CIN0 input pin*	

Note: * This pin is used as the FTCI input pin when an external clock is selected with bits CKS1 and CKS0 in TCR of the FRT. It can always be used as the $\overline{\text{KIN0}}$ or CIN0 input pin.

7.7.6 Port 6 Input Pull-Up MOS

Port 6 has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

The input pull-up MOS current specification can be changed by means of the P6PUE bit. When a pin is designated as an on-chip peripheral module output pin, the input pull-up MOS is always off.

Table 7.6 summarizes the input pull-up MOS states.

Table 7.6 Input Pull-Up MOS States (Port 6)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 3	Off	Off	On/Off	On/Off

[Legend]

Off: Input pull-up MOS is always off.

On/Off: On when the pin is in the input state, P6DDR = 0, and KMPCR = 1; otherwise off.

7.8 Port 7

Port 7 is an 8-bit input only port. Port 7 pins also function as the A/D converter analog input pins and D/A converter analog output pins. Port 7 functions are the same in all operating modes. Port 7 has the following register.

- Port 7 input data register (P7PIN)

7.8.1 Port 7 Input Data Register (P7PIN)

P7PIN reflects the pin states of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	P77PIN	Undefined*	R	When a P7PIN read is performed, the pin states are always read. P7PIN has the same address as PBDDR; if a write is performed, data will be written into PBDDR and the port B setting will be changed.
6	P76PIN	Undefined*	R	
5	P75PIN	Undefined*	R	
4	P74PIN	Undefined*	R	
3	P73PIN	Undefined*	R	
2	P72PIN	Undefined*	R	
1	P71PIN	Undefined*	R	
0	P70PIN	Undefined*	R	

Note: * Determined by the pin states of P77 to P70.

7.8.2 Pin Functions

- P77/AN7/DA1

  Pin functions are switched as shown below according to the combination of the DAE bit in DACR of the D/A converter and the DAOE1 bit.

DAOE1	0		1
DAE	0	1	—
Pin Function	P77 input pin	DA1 input pin	DA1 output pin
	AN7 input pin*		

Note: * This pin can always be used as the AN7 input pin.

- P76/AN6/DA0

  Pin functions are switched as shown below according to the combination of the DAE bit in DACR of the D/A converter and the DAOE0 bit.

DAOE0	0		1
DAE	0	1	—
Pin Function	P76 input pin	DA0 output pin	DA0 output pin
	AN6 input pin*		

Note: * This pin can always be used as the AN6 input pin.

- P75/AN5, P74/AN4, P73/AN3, P72/AN2, P71/AN1, P70/AN0

Pin Function	P75 to P70 input pins
	AN5 to AN0 input pin*

Note: * This pin can always be used as the AN5 to AN0 input pins.

7.9 Port 8

Port 8 is an 8-bit I/O port. Port 8 pins also function as SCI_1 I/O pins and interrupt input pins. Port 8 pin functions are the same in all operating modes. Port 8 has the following registers.

- Port 8 data direction register (P8DDR)
- Port 8 data register (P8DR)

7.9.1 Port 8 Data Direction Register (P8DDR)

P8DDR specifies input or output for the pins of port 8 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved The initial value must not be changed.
6	P86DDR	0	W	P8DDR has the same address as PBPIN, and if read, the port B state will be returned. (Available only in the H8S/2144B.) The corresponding port 8 pins are output ports when P8DDR bits are set to 1, and input ports when cleared to 0.
5	P85DDR	0	W	
4	P84DDR	0	W	
3	P83DDR	0	W	
2	P82DDR	0	W	
1	P81DDR	0	W	
0	P80DDR	0	W	

7.9.2 Port 8 Data Register (P8DR)

P8DR stores output data for the port 8 pins (P86 to P80).

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved The initial value must not be changed.
6	P86DR	0	R/W	If a port 8 read is performed while P8DDR bits are set to 1, the P8DR values are read directly, regardless of the actual pin states. If a port 8 read is performed while P8DDR bits are cleared to 0, the pin states are read.
5	P85DR	0	R/W	
4	P84DR	0	R/W	
3	P83DR	0	R/W	
2	P82DR	0	R/W	
1	P81DR	0	R/W	
0	P80DR	0	R/W	

7.9.3 Pin Functions

- P86/$\overline{\text{IRQ5}}$/ SCK1

  Pin functions are switched as shown below according to the combination of the CKE1 and CKE0 bits in SCR of SCI_1, the C/$\overline{\text{A}}$ bit in SMR of SCI_1, and the P86DDR bit.

CKE1	0				1
C/$\overline{\text{A}}$	0			1	—
CKE0	0		1	—	—
P86DDR	0	1	—	—	—
Pin Function	P86 input pin	P86 output pin	SCK1 output pin	SCK1 output pin	SCK1 input pin
	$\overline{\text{IRQ5}}$ input pin*				

Note: * When the IRQ5E bit in IER is set to 1, this pin is used as the $\overline{\text{IRQ5}}$ input pin.

- P85/$\overline{\text{IRQ4}}$/RxD1

  Pin functions are switched as shown below according to the combination of the RE bit in SCR of SCI_1 and the P85DDR bit.

RE	0		1
P85DDR	0	1	—
Pin Function	P85 input pin	P85 output pin	RxD1 input pin
	$\overline{\text{IRQ4}}$ input pin*		

Note: * When the IRQ4E bit in IER is set to 1, this pin is used as the $\overline{\text{IRQ4}}$ input pin.

- P84/$\overline{\text{IRQ3}}$/TxD1

  Pin functions are switched as shown below according to the combination of the TE bit in SCR of SCI_1 and the P84DDR bit.

TE	0		1
P84DDR	0	1	—
Pin Function	P84 input pin	P84 output pin	TxD1 output pin
	$\overline{\text{IRQ3}}$ input pin*		

Note: * When the IRQ3E bit in IER is set to 1, this pin is used as the $\overline{\text{IRQ3}}$ input pin.

- P83

  Pin functions are switched as shown below according to the P83DDR bit.

P83DDR	0	1
Pin Function	P83 input pin	P83 output pin

- P82

  Pin functions are switched as shown below according to the P82DDR bit.

P82DDR	0	1
Pin Function	P82 input pin	P82 output pin

- P81

  Pin functions are switched as shown below according to the P81DDR bit.

P81DDR	0	1
Pin Function	P81 input pin	P81 output pin

- P80

  Pin functions are switched as shown below according to the P80DDR bit.

P80DDR	0	1
Pin Function	P80 input pin	P80 output pin

7.10 Port 9

Port 9 is an 8-bit I/O port. Port 9 pins also function as external interrupt input pins, the A/D converter input pin, the subclock input pin, bus control signal I/O pins, and the system clock (φ) output pin. Port 9 has the following registers.

- Port 9 data direction register (P9DDR)
- Port 9 data register (P9DR)

7.10.1 Port 9 Data Direction Register (P9DDR)

P9DDR specifies input or output for the pins of port 9 on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	P97DDR	0	W	P9DDR is initialized to H'40 (mode 1) or H'00 (modes 2 and 3). Modes 1, 2, and 3 (EXPE = 1): Pin P97 functions as a bus control input ($\overline{\text{WAIT}}$) or an I/O port according to the wait mode setting. When P97 functions as an I/O port, it becomes an output port when P97DDR is set to 1, and an input port when P97DDR is cleared to 0. Pin P96 functions as the ϕ output pin when P96DDR is set to 1, and as the subclock input (EXCL) or an input port when P96DDR is cleared to 0. Pins P95 to P93 automatically become bus control outputs ($\overline{\text{AS}}$/$\overline{\text{IOS}}$, $\overline{\text{HWR}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$), regardless of the input/output direction indicated by P95DDR to P93DDR. Pins P92 and P91 become output ports when P92DDR and P91DDR are set to 1, and input ports when P92DDR and P91DDR are cleared to 0. When the ABW bit in WSCR is cleared to 0 (clearing to 0 is prohibited in the H8S/2134B), pin P90 becomes a bus control output ($\overline{\text{LWR}}$), regardless of the input/output direction indicated by P90DDR. When the ABW bit is 1, pin P90 becomes an output port if P90DDR is set to 1, and an input port if P90DDR is cleared to 0. Modes 2 and 3 (EXPE = 0): When the corresponding P9DDR bits are set to 1, pin P96 functions as the ϕ output pin and pins P97 and P95 to P90 become output ports. When P9DDR bits are cleared to 0, the corresponding pins become input ports.
6	P96DDR	1/0*	W	
5	P95DDR	0	W	
4	P94DDR	0	W	
3	P93DDR	0	W	
2	P92DDR	0	W	
1	P91DDR	0	W	
0	P90DDR	0	W	

Note: * The initial value of P96DDR is 1 (mode 1) or 0 (modes 2 and 3).

7.10.2 Port 9 Data Register (P9DR)

P9DR stores output data for the port 9 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P97DR	0	R/W	With the exception of P96, if a port 9 read is performed while P9DDR bits are set to 1, the P9DR values are read directly, regardless of the actual pin states. If a port 9 read is performed while P9DDR bits are cleared to 0, the pin states are read. For P96, the pin state is always read.
6	P96DR	Undefined*	R	
5	P95DR	0	R/W	
4	P94DR	0	R/W	
3	P93DR	0	R/W	
2	P92DR	0	R/W	
1	P91DR	0	R/W	
0	P90DR	0	R/W	

Note: * The initial value of bit 6 is determined according to the P96 pin state.

7.10.3 Pin Functions

- P97/$\overline{\text{WAIT}}$

  Pin functions are switched as shown below according to the combination of operating mode, the WMS1 bit in WSCR, and the P97DDR bit.

Operating Mode	Modes 1, 2, 3 (EXPE = 1)			Modes 2, 3 (EXPE = 0)	
WMS1	0		1	—	
P97DDR	0	1	—	0	1
Pin Function	P97 input pin	P97 output pin	$\overline{\text{WAIT}}$ input pin	P97 input pin	P97 output pin

- P96/ϕ/EXCL

  Pin functions are switched as shown below according to the combination of the EXCLE bit in LPWRCR and the P96DDR bit.

P96DDR	0		1
EXCLE	0	1	0
Pin Function	P96 input pin	EXCL input pin	ϕ output pin

Note: * When this pin is used as the EXCL input pin, P96DDR should be cleared to 0.

- P95/$\overline{AS}$/$\overline{IOS}$

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the P95DDR bit.

Operating Mode	Modes 1, 2, 3 (EXPE = 1)		Modes 2, 3 (EXPE = 0)	
P95DDR	—		0	1
IOSE	0	1	—	—
Pin Function	$\overline{AS}$ output pin	$\overline{IOS}$ output pin	P95 input pin	P95 output pin

- P94/$\overline{HWR}$*

  Pin functions are switched as shown below according to the combination of operating mode and the P94DDR bit.

Operating Mode	Modes 1, 2, 3 (EXPE = 1)	Modes 2, 3 (EXPE = 0)	
P94DDR	—	0	1
Pin Function	$\overline{HWR}$* output pin	P94 input pin	P94 output pin

Note: * The WR pin in the H8S/2134B

- P93/$\overline{RD}$

  Pin functions are switched as shown below according to the combination of operating mode and the P93DDR bit.

Operating Mode	Modes 1, 2, 3 (EXPE = 1)	Modes 2, 3 (EXPE = 0)	
P93DDR	—	0	1
Pin Function	$\overline{RD}$ output pin	P93 input pin	P93 output pin

- P92/$\overline{IRQ0}$

P92DDR	0	1
Pin Function	P92 input pin	P92 output pin
	$\overline{IRQ0}$ input pin*	

Note: * When bit IRQ0E in IER is set to 1, this pin is used as the $\overline{IRQ0}$ input pin.

- P91/$\overline{\text{IRQ1}}$

P91DDR	0	1
Pin Function	P91 input pin	P91 output pin
	$\overline{\text{IRQ1}}$ input pin*	

Note: * When bit IRQ1E in IER is set to 1, this pin is used as the $\overline{\text{IRQ1}}$ input pin.

- P90/$\overline{\text{LWR}}$*[2]/$\overline{\text{IRQ2}}$/$\overline{\text{ADTRG}}$

  Pin functions are switched as shown below according to the combination of operating mode, the ABW bit in WSCR, and the P90DDR bit.

Operating Mode	Modes 1, 2, 3 (EXPE = 1)			Modes 2, 3 (EXPE = 0)	
ABW	0	1		—	
P90DDR	—	0	1	0	1
Pin Function	$\overline{\text{LWR}}$*[2] output pin	P90 input pin	P90 output pin	P90 input pin	P90 output pin
		$\overline{\text{IRQ2}}$ input pin, $\overline{\text{ADTRG}}$ input pin*[1]			

Note: 1. When the ABW bit in WSCR is set to 1 in mode 1, 2, or 3 (EXPE = 1), or the IRQ2E bit in IER is set to 1 in mode 2 or 3 (EXPE = 0), this pin is used as the $\overline{\text{IRQ2}}$ input pin. When TRGS1 and TRGS0 in ADCR of the A/D converter are both set to 1, this pin is used as the $\overline{\text{ADTRG}}$ input pin.

2. The $\overline{\text{LWR}}$ pin is not available in the H8S/2134B. Do not clear the ABW bit in WSCR to 0.

7.11 Port A (Only for H8S/2144B)

Port A is an 8-bit I/O port. Port A pins also function as key-sense interrupt input pins, extended A/D converter input pins, and address output pins. Port A pin functions change according to the operating mode. Port A input/output operates by VccB power independent from the Vcc power. Up to 5 V can be applied to port A pins if VccB power is 5 V. Port A has the following registers. PADDR and PAPIN have the same address.

- Port A data direction register (PADDR)
- Port A output data register (PAODR)
- Port A input data register (PAPIN)

7.11.1 Port A Data Direction Register (PADDR)

PADDR specifies input or output for the pins of port A on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7DDR	0	W	In mode 1, 2 (EXPE = 0), or 3: The corresponding port A pins are output ports when PADDR bits are set to 1, and input ports when cleared to 0. In mode 2 (EXPE = 1): The corresponding port A pins are address output when PADDR bits are set to 1, and input ports when cleared to 0. The port A pins changes from the address I/O ports to output ports by setting the IOSE bit to 1. PADDR has the same address as PAPIN, if read, port A status is returned.
6	PA6DDR	0	W	
5	PA5DDR	0	W	
4	PA4DDR	0	W	
3	PA3DDR	0	W	
2	PA2DDR	0	W	
1	PA1DDR	0	W	
0	PA0DDR	0	W	

7.11.2 Port A Output Data Register (PAODR)

PAODR stores output data for port A.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7ODR	0	R/W	PAODR can always be read or written to, regardless of the contents of PADDR.
6	PA6ODR	0	R/W	
5	PA5ODR	0	R/W	
4	PA4ODR	0	R/W	
3	PA3ODR	0	R/W	
2	PA2ODR	0	R/W	
1	PA1ODR	0	R/W	
0	PA0ODR	0	R/W	

7.11.3 Port A Input Data Register (PAPIN)

PAPIN indicates the port A state.

Bit	Bit Name	Initial Value	R/W	Description
7	PA7PIN	Undefined*	R	Reading PAPIN always returns the pin states. PAPIN has the same address as PADDR. If a write is performed, the port A settings will change.
6	PA6PIN	Undefined*	R	
5	PA5PIN	Undefined*	R	
4	PA4PIN	Undefined*	R	
3	PA3PIN	Undefined*	R	
2	PA2PIN	Undefined*	R	
1	PA1PIN	Undefined*	R	
0	PA0PIN	Undefined*	R	

Note: * The initial value is determined according to the PA7 to PA0 pin states.

7.11.4 Pin Functions

- PA7/A23/$\overline{\text{KIN15}}$/CIN15

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the PA7DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA7DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA7 input pin	PA7 output pin	PA7 input pin	A23 output pin	PA7 output pin
	$\overline{\text{KIN15}}$ input pin, CIN15 input pin*				

Note: * When the IICS bit in STCR is set to 1, this pin is an NMOS open-drain output, and has direct bus drive capability. This pin can always be used as the $\overline{\text{KIN15}}$ or CIN15 input pin.

- PA6/A22/$\overline{\text{KIN14}}$/CIN14

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the PA6DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA6DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA6 input pin	PA6 output pin	PA6 input pin	A22 output pin	PA6 output pin
	$\overline{\text{KIN14}}$ input pin, CIN14 input pin*				

Note: * When the IICS bit in STCR is set to 1, this pin is an NMOS open-drain output, and has direct bus drive capability. This pin can always be used as the $\overline{\text{KIN14}}$ or CIN14 input pin.

- PA5/A21/$\overline{\text{KIN13}}$/CIN13

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the PA5DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA5DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA5 input pin	PA5 output pin	PA5 input pin	A21 output pin	PA5 output pin
	$\overline{\text{KIN13}}$ input pin, CIN13 input pin*				

Note: * When the IICS bit in STCR is set to 1, this pin is an NMOS open-drain output, and has direct bus drive capability. This pin can always be used as the $\overline{\text{KIN13}}$, or CIN13 input pin.

- PA4/A20/$\overline{\text{KIN12}}$/CIN12

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the PA4DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA4DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA4 input pin	PA4 output pin	PA4 input pin	A20 output pin	PA4 output pin
	$\overline{\text{KIN12}}$ input pin, CIN12 input pin*				

Note: * When the IICS bit in STCR is set to 1, this pin is an NMOS open-drain output, and has direct bus drive capability. This pin can always be used as the $\overline{\text{KIN12}}$ or CIN12 input pin.

- PA3/A19/$\overline{\text{KIN11}}$/CIN11

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the PA3DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA3DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA3 input pin	PA3 output pin	PA3 input pin	A19 output pin	PA3 output pin
	$\overline{\text{KIN11}}$ input pin, CIN11 input pin*				

Note: * This pin can always be used as the $\overline{\text{KIN11}}$ or CIN11 input pin.

- PA2/A18/$\overline{\text{KIN10}}$/CIN10

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR, and the PA2DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA2DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA2 input pin	PA2 output pin	PA2 input pin	A18 output pin	PA2 output pin
	$\overline{\text{KIN10}}$ input pin, CIN10 input pin*				

Note: * This pin can always be used as the $\overline{\text{KIN10}}$ or CIN10 input pin.

- PA1/A17/$\overline{\text{KIN9}}$/CIN9

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR and the PA1DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA1DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA1 input pin	PA1 output pin	PA1 input pin	A17 output pin	PA1 output pin
	$\overline{\text{KIN9}}$ input pin, CIN9 input pin*				

Note: * This pin can always be used as the $\overline{\text{KIN9}}$ or CIN9 input pin.

- PA0/A16/ $\overline{\text{KIN8}}$/CIN8

  Pin functions are switched as shown below according to the combination of operating mode, the IOSE bit in SYSCR and the PA0DDR bit.

Operating Mode	Modes 1, 2 (EXPE = 0), 3		Mode 2 (EXPE = 1)		
PA0DDR	0	1	0	1	
IOSE	—	—	—	0	1
Pin Function	PA0 input pin	PA0 output pin	PA0 input pin	A16 output pin	PA0 output pin
	$\overline{\text{KIN8}}$ input pin, CIN8 input pin*				

Note: * This pin can always be used as the $\overline{\text{KIN8}}$ or CIN8 input pin.

7.11.5 Port A Input Pull-Up MOS

Port A has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

The input pull-up MOS for pins PA7 to PA4 is always off when IICS is set to 1.

Table 7.7 summarizes the input pull-up MOS states.

Table 7.7 Input Pull-Up MOS States (Port A)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 3	Off	Off	On/Off	On/Off

[Legend]

Off: Input pull-up MOS is always off.

On/Off: On when the pin is in the input state, PADDR = 0, and PAODR = 1; otherwise off.

7.12 Port B (Only for H8S/2144B)

Port B is an 8-bit I/O port. Port B pins also have a data bus input/output function. The pin functions depend on the operating mode. Port B has the following registers.

- Port B data direction register (PBDDR)
- Port B output data register (PBODR)
- Port B input data register (PBPIN)

7.12.1 Port B Data Direction Register (PBDDR)

PBDDR specifies input or output for the pins of port B on a bit-by-bit basis.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7DDR	0	W	PBDDR has the same address as P7PIN, and if read, the port 7 pin states will be returned. • Modes 1, 2, and 3 (EXPE = 1) When the ABW bit in WSCR is cleared to 0, port B pins automatically become data I/O pins (D7 to D0), regardless of the input/output direction indicated by PBDDR. When the ABW bit is 1, a port B pin becomes an output port if the corresponding PBDDR bit is set to 1, and an input port if the bit is cleared to 0. • Modes 2 and 3 (EXPE = 0) A port B pin becomes an output port if the corresponding PBDDR bit is set to 1, and an input port if the bit is cleared to 0.
6	PB6DDR	0	W	
5	PB5DDR	0	W	
4	PB4DDR	0	W	
3	PB3DDR	0	W	
2	PB2DDR	0	W	
1	PB1DDR	0	W	
0	PB0DDR	0	W	

7.12.2 Port B Output Data Register (PBODR)

PBODR stores output data for port B.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7ODR	0	R/W	PBODR can always be read or written to, regardless of the contents of PBDDR.
6	PB6ODR	0	R/W	
5	PB5ODR	0	R/W	
4	PB4ODR	0	R/W	
3	PB3ODR	0	R/W	
2	PB2ODR	0	R/W	
1	PB1ODR	0	R/W	
0	PB0ODR	0	R/W	

7.12.3 Port B Input Data Register (PBPIN)

PBPIN indicates the port B state.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7PIN	Undefined*	R	Reading PBPIN always returns the pin states. PBPIN has the same address as P8DDR. If a write is performed, data will be written to P8DDR and the port 8 settings will change.
6	PB6PIN	Undefined*	R	
5	PB5PIN	Undefined*	R	
4	PB4PIN	Undefined*	R	
3	PB3PIN	Undefined*	R	
2	PB2PIN	Undefined*	R	
1	PB1PIN	Undefined*	R	
0	PB0PIN	Undefined*	R	

Note: * The initial value is determined according to the PB7 to PB0 pin states.

7.12.4 Pin Functions

- PB7/D7, PB6/D6, PB5/D5, PB4/D4, PB3/D3, PB2/D2, PB1/D1, and PB0/D0

  Pin functions are switched as shown below according to the combination of the operating mode, the PBnDDR bit, and the ABW bit in WSCR.

Operating Mode	Mode 1 and Modes 2, 3 (EXPE = 1)			Modes 2, 3 (EXPE = 0)	
ABW	0	1		—	
PBnDDR	—	0	1	0	1
Pin Function	Dn I/O pin	PBn input pin	PBn output pin	PBn input pin	PBn output pin

Note: n =7 to 0

7.12.5 Port B Input Pull-Up MOS

Port B has an on-chip input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be specified as on or off on a bit-by-bit basis.

When a pin is specified as an output pin, the input pull-up MOS is always off.

Table 7.8 summarizes the input pull-up MOS states.

Table 7.8 Input Pull-Up MOS States (Port B)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 3 (EXPE = 1) with ABW in WSCR = 0	Off	Off	Off	Off
1, 2, 3 (EXPE = 1) with ABW in WSCR = 1, or 2, 3 (EXPE = 0)			On/Off	On/Off

[Legend]

Off: Input pull-up MOS is always off.

On/Off: On when the pin is in the input state, PBDDR = 0, and PBODR = 1; otherwise off.

Section 8 14-Bit PWM Timer (PWMX)

This LSI has an on-chip 14-bit pulse-width modulator (PWM) timer with two output channels. It can be connected to an external low-pass filter to operate as a 14-bit D/A converter.

8.1 Features

- Division of pulse into multiple base cycles to reduce ripple
- Two resolution settings
  The resolution can be set equal to one or two system clock cycles.
- Two base cycle settings
  The base cycle can be set equal to T × 64 or T × 256, where T is the resolution.
- Four operating speeds
- Four operation clocks (by combination of two resolution settings and two base cycle settings)

Figure 8.1 shows a block diagram of the PWM (D/A) module.

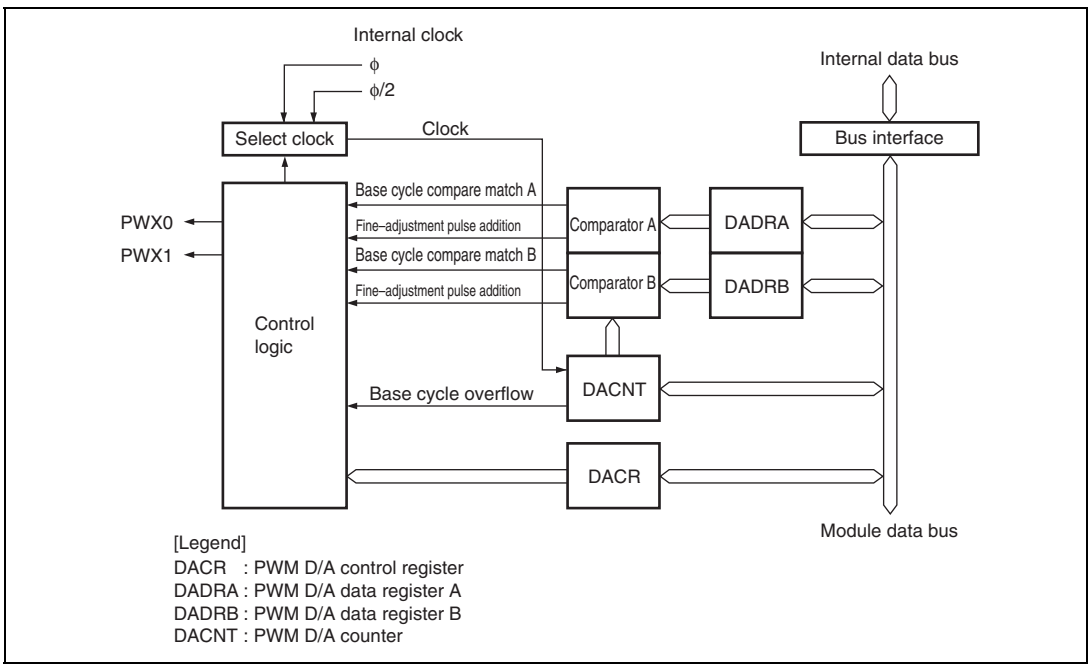


Figure 8.1 PWM (D/A) Block Diagram

8.2 Input/Output Pins

Table 8.1 lists the PWM (D/A) module input and output pins.

Table 8.1 Pin Configuration

Name	Abbreviation	I/O	Function
PWM output pin X0	PWX0	Output	PWM output of PWMX channel A
PWM output pin X1	PWX1	Output	PWM output of PWMX channel B

8.3 Register Descriptions

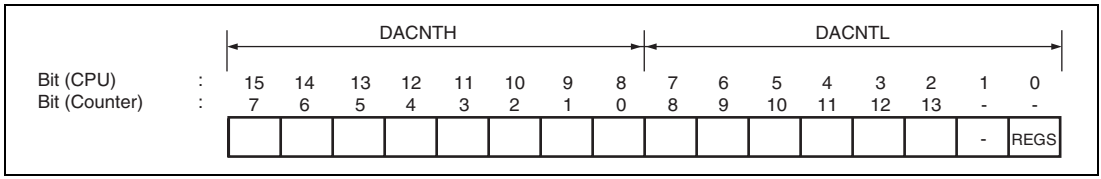
The PWM (D/A) module has the following registers. The PWM (D/A) registers are assigned to the same addresses with other registers. The registers are selected by the IICE bit in the serial timer control register (STCR). For details on STCR, see section 3.2.3, Serial Timer Control Register (STCR).

- PWM (D/A) counter H (DACNTH)
- PWM (D/A) counter L (DACNTL)
- PWM (D/A) data register AH (DADRAH)
- PWM (D/A) data register AL (DADRAL)
- PWM (D/A) data register BH (DADRBH)
- PWM (D/A) data register BL (DADRBL)
- PWM (D/A) control register (DACR)

Note: The same addresses are shared by DADRA and DACR, and by DADRB and DACNT. Switching is performed by the REGS bit in DACNT or DADRB.

8.3.1 PWM (D/A) Counters H and L (DACNTH, DACNTL)

DACNT is a 14-bit readable/writable up-counter. The input clock is selected by the clock select bit (CKS) in DACR. DACNT functions as the time base for both PWM (D/A) channels. When a channel operates with 14-bit precision, it uses all DACNT bits. When a channel operates with 12-bit precision, it uses the lower 12 bits and ignores the upper two bits. Since DACNT consists of 16-bit data, DACNT transfers data to the CPU via the temporary register (TEMP). For details, refer to section 8.4, Bus Master Interface.



- DACNTH

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	UC7 to UC0	All 0	R/W	Upper Up-Counter

- DACNTL

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	UC8 to UC13	All 0	R/W	Lower Up-Counter
1	—	1	R	Reserved This bit is always read as 1 and cannot be modified.
0	REGS	1	R/W	Register Select DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. 0: DADRA and DADRB can be accessed 1: DACR and DACNT can be accessed

8.3.2 PWM (D/A) Data Registers A and B (DADRA, DADRB)

DADRA corresponds to PWM (D/A) channel A, and DADRB to PWM (D/A) channel B. Since DADR consists of 16-bit data, DADR transfers data to the CPU via the temporary register (TEMP). For details, refer to section 8.4, Bus Master Interface.

- DADRA

Bit	Bit Name	Initial Value	R/W	Description
15	DA13	1	R/W	D/A Data 13 to 0 These bits set a digital value to be converted to an analog value. In each base cycle, the DACNT value is continually compared with the DADR value to determine the duty cycle of the output waveform, and to decide whether to output a fine-adjustment pulse equal in width to the resolution. To enable this operation, this register must be set within a range that depends on the CFS bit. If the DADR value is outside this range, the PWM output is held constant. A channel can be operated with 12-bit precision by keeping the two lowest data bits (DA1 and DA0) cleared to 0. The two lowest data bits correspond to the two highest bits in DACNT.
14	DA12	1	R/W	
13	DA11	1	R/W	
12	DA10	1	R/W	
11	DA9	1	R/W	
10	DA8	1	R/W	
9	DA7	1	R/W	
8	DA6	1	R/W	
7	DA5	1	R/W	
6	DA4	1	R/W	
5	DA3	1	R/W	
4	DA2	1	R/W	
3	DA1	1	R/W	
2	DA0	1	R/W	
1	CFS	1	R/W	Carrier Frequency Select 0: Base cycle = resolution (T) × 64 DADR range = H'0401 to H'FFFD 1: Base cycle = resolution (T) × 256 DADR range = H'0103 to H'FFFF
0	—	1	R	Reserved This bit is always read as 1 and cannot be modified.

- DADRB

Bit	Bit Name	Initial Value	R/W	Description
15	DA13	1	R/W	D/A Data 13 to 0 These bits set a digital value to be converted to an analog value. In each base cycle, the DACNT value is continually compared with the DADR value to determine the duty cycle of the output waveform, and to decide whether to output a fine-adjustment pulse equal in width to the resolution. To enable this operation, this register must be set within a range that depends on the CFS bit. If the DADR value is outside this range, the PWM output is held constant. A channel can be operated with 12-bit precision by keeping the two lowest data bits (DA1 and DA0) cleared to 0. The two lowest data bits correspond to the two highest bits in DACNT.
14	DA12	1	R/W	
13	DA11	1	R/W	
12	DA10	1	R/W	
11	DA9	1	R/W	
10	DA8	1	R/W	
9	DA7	1	R/W	
8	DA6	1	R/W	
7	DA5	1	R/W	
6	DA4	1	R/W	
5	DA3	1	R/W	
4	DA2	1	R/W	
3	DA1	1	R/W	
2	DA0	1	R/W	
1	CFS	1	R/W	Carrier Frequency Select 0: Base cycle = resolution (T) × 64 DADR range = H'0401 to H'FFFD 1: Base cycle = resolution (T) × 256 DADR range = H'0103 to H'FFFF
0	REGS	1	R/W	Register Select DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. 0: DADRA and DADRB can be accessed 1: DACR and DACNT can be accessed

8.3.3 PWM (D/A) Control Register (DACR)

DACR selects test mode, enables the PWM outputs, and selects the output phase and operating speed.

Bit	Bit Name	Initial Value	R/W	Description
7	TEST	0	R/W	Test Mode Selects test mode, which is used in testing this LSI. Normally this bit should be cleared to 0. 0: PWM (D/A) in user state: Normal operation 1: PWM (D/A) in test state: Correct conversion results unobtainable
6	PWME	0	R/W	PWM Enable Starts or stops the PWM D/A counter (DACNT). 0: DACNT operates as a 14-bit up-counter 1: DACNT halts at H'0003
5	—	1	R	Reserved
4	—	1	R	These bits are always read as 1 and cannot be modified.
3	OEB	0	R/W	Output Enable B Enables or disables output on PWM (D/A) channel B. 0: PWM (D/A) channel B output (at the PWX1 pin) is disabled 1: PWM (D/A) channel B output (at the PWX1 pin) is enabled
2	OEA	0	R/W	Output Enable A Enables or disables output on PWM (D/A) channel A. 0: PWM (D/A) channel A output (at the PWX0 pin) is disabled 1: PWM (D/A) channel A output (at the PWX0 pin) is enabled
1	OS	0	R/W	Output Select Selects the phase of the PWM (D/A) output. 0: Direct PWM (D/A) output 1: Inverted PWM (D/A) output

Bit	Bit Name	Initial Value	R/W	Description
0	CKS	0	R/W	Clock Select Selects the PWM (D/A) resolution. If the system clock (φ) frequency is 10 MHz, resolutions of 100 ns and 200 ns, can be selected. 0: Operates at resolution (T) = system clock cycle time (t_{cyc}) 1: Operates at resolution (T) = system clock cycle time (t_{cyc}) × 2

8.4 Bus Master Interface

DACNT, DADRA, and DADRB are 16-bit registers. The data bus linking the bus master and the on-chip peripheral modules, however, is only 8 bits wide. When the bus master accesses these registers, it therefore uses an 8-bit temporary register (TEMP).

These registers are written to and read from as follows.

Write: When the upper byte is written to, the upper-byte write data is stored in TEMP. Next, when the lower byte is written to, the lower-byte write data and TEMP value are combined, and the combined 16-bit value is written in the register.

Read: When the upper byte is read from, the upper-byte value is transferred to the CPU and the lower-byte value is transferred to TEMP. Next, when the lower byte is read from, the lower-byte value in TEMP is transferred to the CPU.

These registers should always be accessed 16 bits at a time with a MOV instruction, and the upper byte should always be accessed before the lower byte. Correct data will not be transferred if only the upper byte or only the lower byte is accessed. Also note that a bit manipulation instruction cannot be used to access these registers.

Example 1: Write to DACNT

```
MOV.W R0, @DACNT      ; Write R0 contents to DACNT
```

Example 2: Read DADRA

```
MOV.W @DADRA, R0      ; Copy contents of DADRA to R0
```

Table 8.2 Read and Write Access Methods for 16-Bit Registers

	Read		Write	
Register Name	**Word**	**Byte**	**Word**	**Byte**
DADRA and DADRB	Yes	Yes	Yes	×
DACNT	Yes	×	Yes	×

[Legend]

Yes: Permitted type of access. Word access includes successive byte accesses to the upper byte (first) and lower byte (second).

×: This type of access may give incorrect results.

8.5 Operation

A PWM waveform like the one shown in figure 8.2 is output from the PWMX pin. The value in DADR corresponds to the total width (T_L) of the low (0) pulses output in one conversion cycle (256 pulses when CFS = 0, 64 pulses when CFS = 1). When OS = 0, this waveform is directly output. When OS = 1, the output waveform is inverted, and the DADR value corresponds to the total width (T_H) of the high (1) output pulses. Figures 8.3 and 8.4 show the types of waveform output available.

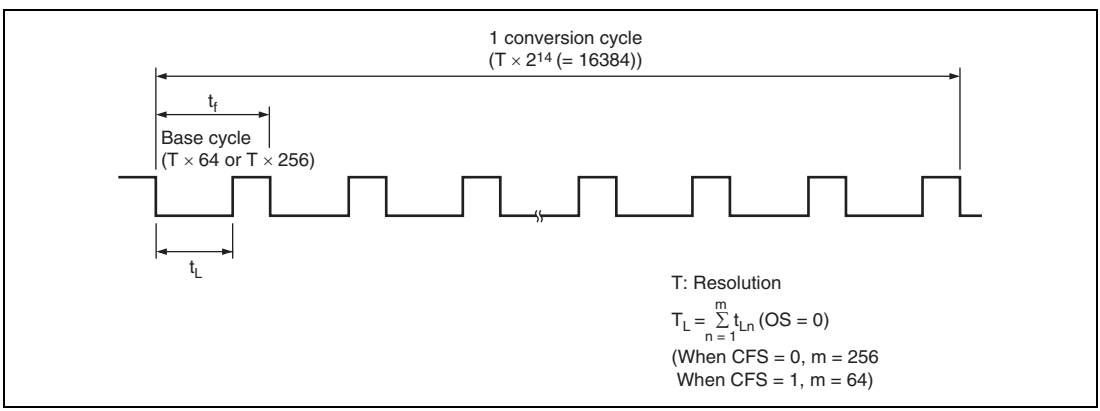


Figure 8.2 PWM D/A Operation

Table 8.3 summarizes the relationships between the CKS, CFS, and OS bit settings and the resolution, base cycle, and conversion cycle. The PWM output remains fixed unless DADR contains at least a certain minimum value.

Table 8.3 Settings and Operation (Examples when ϕ = 10 MHz)

						Fixed DADR Bits					
						Pre-cision	Bit Data				
CKS	Resolu-tion T (µs)	CFS	Base Cycle (µs)	Conversion Cycle (µs)	T_L (if OS = 0) T_H (if OS = 1)	(Bits)	3	2	1	0	Conversion Cycle* (µs)
0	0.1	0	6.4	1638.4	1. Always low (or high)	14					1638.4
					(DADR = H'0001 to H'03FD)	12			0	0	409.6
					2. (Data value) × T (DADR = H'0401 to H'FFFD)	10	0	0	0	0	102.4
		1	25.6		1. Always low (or high)	14					1638.4
					(DADR = H'0003 to H'00FF)	12			0	0	409.6
					2. (Data value) × T (DADR = H'0103 to H'FFFF)	10	0	0	0	0	102.4
1	0.2	0	12.8	3276.8	1. Always low (or high)	14					3276.8
					(DADR = H'0001 to H'03FD)	12			0	0	819.2
					2. (Data value) × T (DADR = H'0401 to H'FFFD)	10	0	0	0	0	204.8
		1	51.2		1. Always low (or high)	14					3276.8
					(DADR = H'0003 to H'00FF)	12			0	0	819.2
					2. (Data value) × T (DADR = H'0103 to H'FFFF)	10	0	0	0	0	204.8

Note: * This column indicates the conversion cycle when specific DADR bits are fixed.

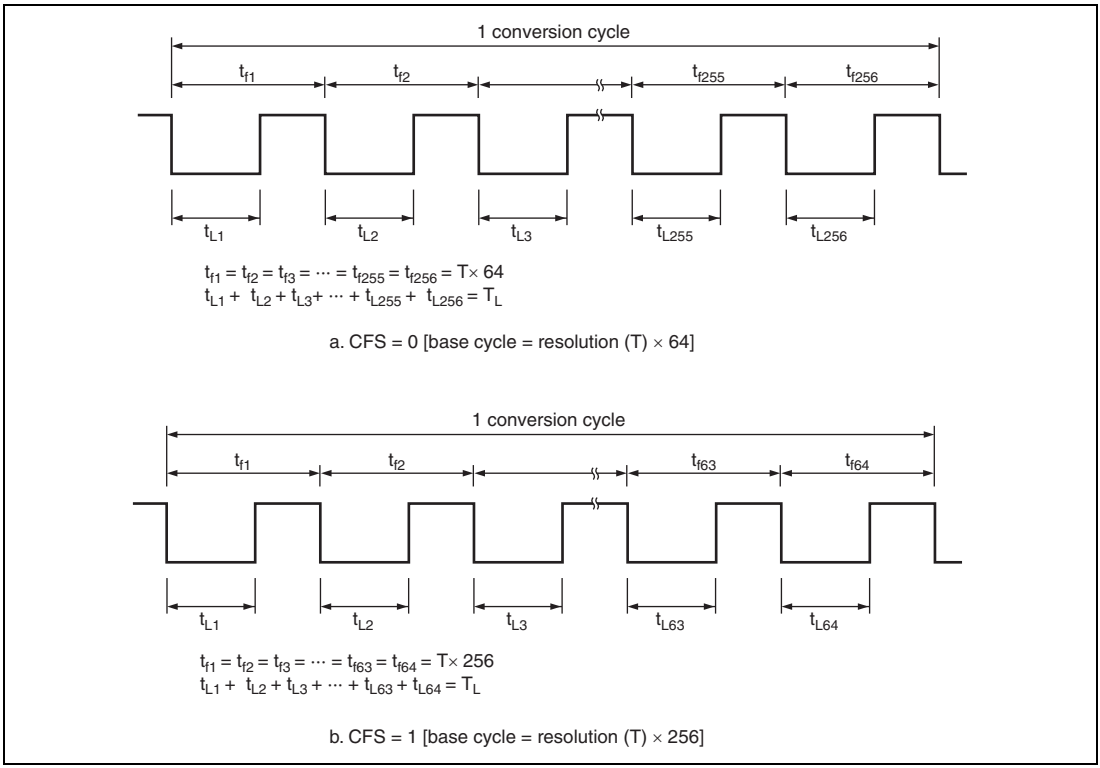


Figure 8.3 Output Waveform (OS = 0, DADR corresponds to T_L)

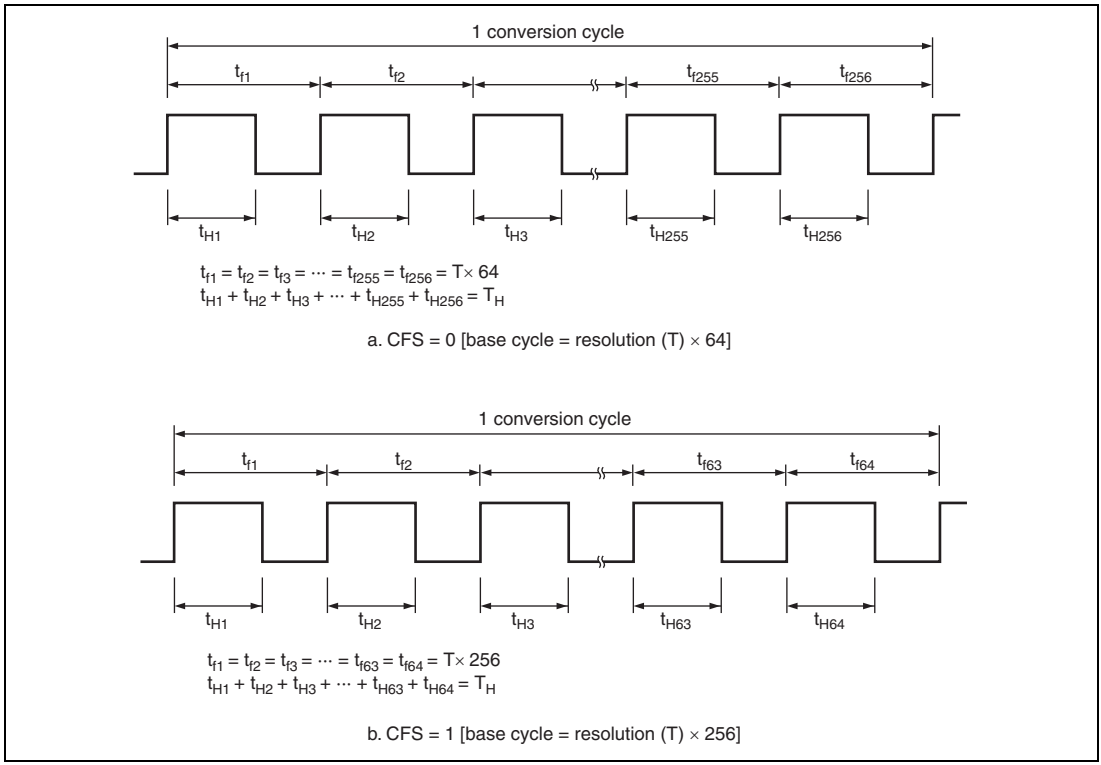


Figure 8.4 Output Waveform (OS = 1, DADR corresponds to T_H)

An example of setting CFS to 1 (basic cycle = resolution (T) × 256) and OS to 1 (PWMX inverted output) is shown as an additional pulse. When CFS is set to 1, the duty ratio of the basic pulse is determined by the upper eight bits (DA13 to DA6) in DADR, and the position of the additional pulse is determined by the following six bits (DA5 to DA0) as shown in figure 8.5.

Table 8.4 shows the position of the additional pulse.

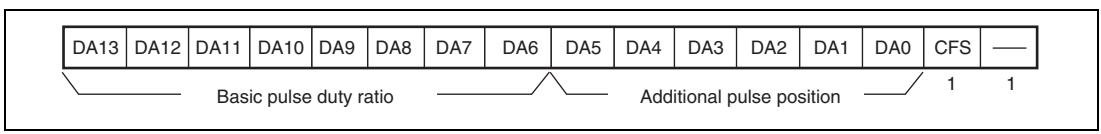


Figure 8.5 D/A Data Register Configuration when CFS = 1

Here, the case of DADR = H'0207 (B'0000 0010 0000 0111) is considered. Figure 8.6 shows an output waveform. Because CFS = 1 and the value of upper eight bits is B'0000 0010, the duty ratio of the basic pulse is 2/256 × (T) of high width.

Since the value of the following six bits is B'0000 01, the additional pulse is output at the position of basic pulse No. 63 as shown in table 8.4. Only 1/256 × (T) of the additional pulse is added to the basic pulse.

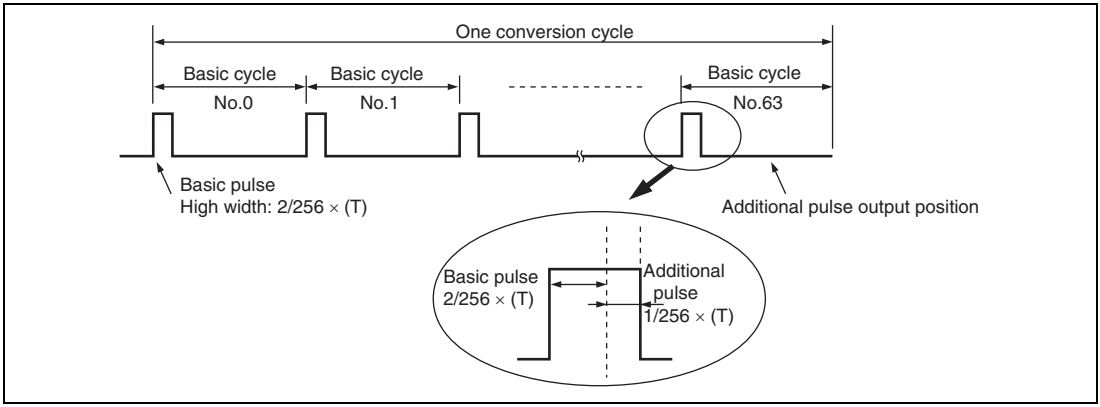
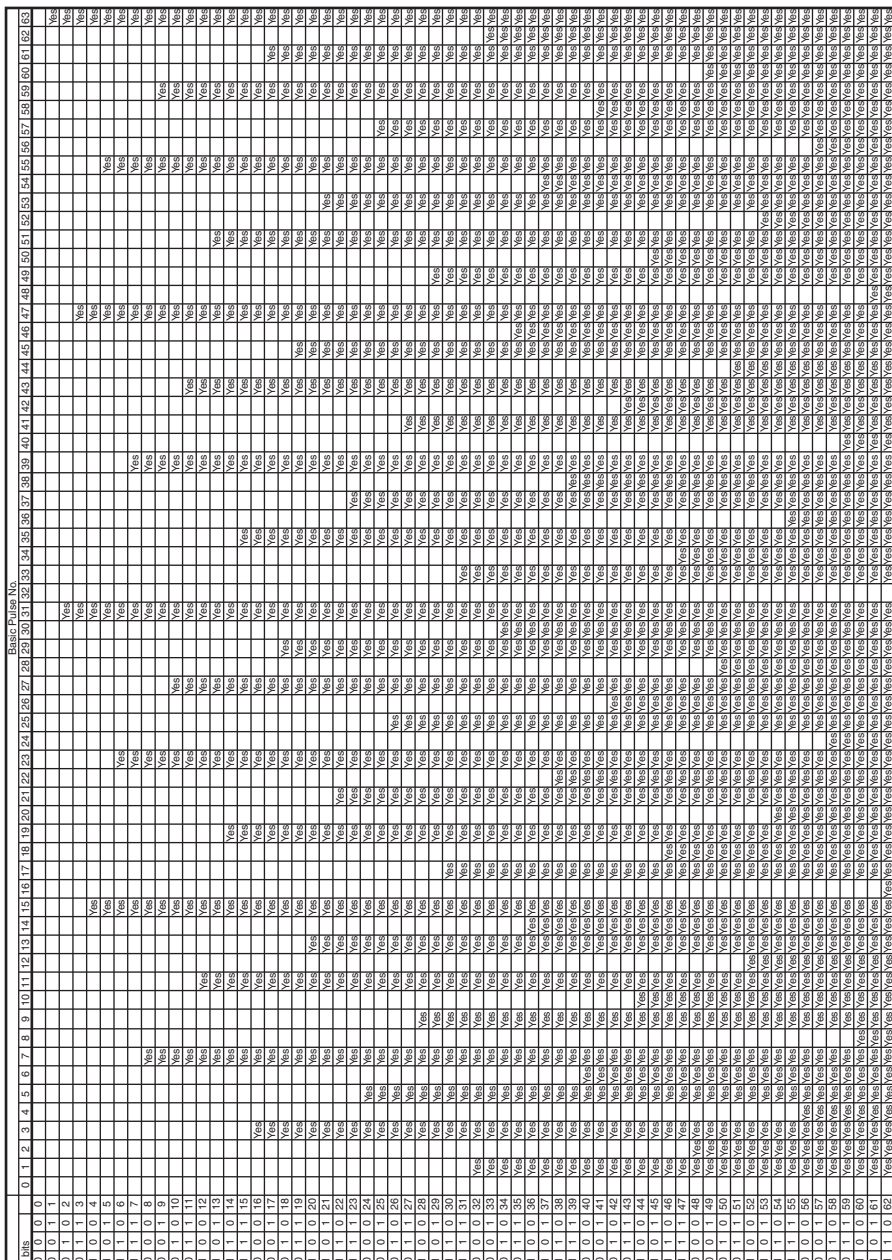


Figure 8.6 Output Waveform when DADR = H'0207 (OS = 1)

Note that the case of CFS = 0 (basic cycle = resolution (T) × 64) is similar other than the duty ratio of the basic pulse is determined by the upper six bits, and the position of the additional pulse is determined by the following eight bits.

Table 8.4 Position of Pulse to be Added to Basic Pulse (CFS = 1)



8.6 Usage Note

8.6.1 Module Stop Mode Setting

PWMX operation can be enabled or disabled using the module stop control register. The initial setting is for PWMX operation to be halted. Register access is enabled by canceling the module stop mode. For details, refer to section 18, Power-Down Modes.

Section 9 16-Bit Free-Running Timer (FRT)

This LSI has an on-chip 16-bit free-running timer (FRT). The FRT operates on the basis of the 16-bit free-running counter (FRC), and outputs two independent waveforms, and measures the input pulse width and external clock periods.

9.1 Features

- Selection of four clock sources

  One of the three internal clocks (ϕ/2, ϕ/8, or ϕ/32), or an external clock input can be selected (enabling use as an external event counter).
- Two independent comparators

  Two independent waveforms can be output.
- Four independent input capture channels

  The rising or falling edge can be selected.

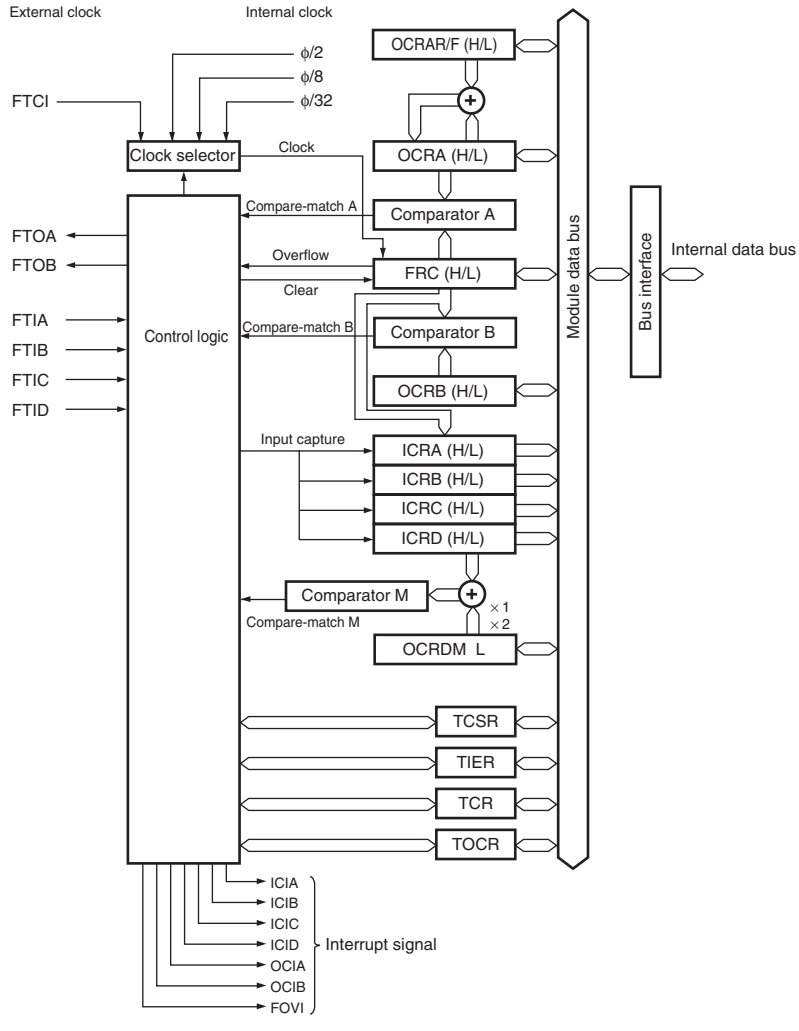
  Buffer modes can be specified.
- Counter clearing

  The free-running counters can be cleared on compare-match A.
- Seven independent interrupts

  Two compare-match interrupts, four input capture interrupts, and one overflow interrupt can be requested independently.
- Special functions provided by automatic addition function

  The contents of OCRAR and OCRAF can be added to the contents of OCRA automatically, enabling a periodic waveform to be generated without software intervention. The contents of ICRD can be added automatically to the contents of OCRDM × 2, enabling input capture operations in this interval to be restricted.

Figure 9.1 shows a block diagram of the FRT.



[Legend]

OCRA, OCRB:	Output compare register A, B (16-bit)
OCRAR, OCRAF:	Output compare register AR, AF (16-bit)
OCRDM:	Output compare register DM (16-bit)
FRC:	Free-running counter (16-bit)
ICRA to D:	Input capture registers A to D (16-bit)
TCSR:	Timer control/status register (8-bit)
TIER:	Timer interrupt enable register (8-bit)
TCR:	Timer control register (8-bit)
TOCR:	Timer output compare control register (8-bit)

Figure 9.1 Block Diagram of 16-Bit Free-Running Timer

9.2 Input/Output Pins

Table 9.1 lists the FRT input and output pins.

Table 9.1 Pin Configuration

Name	Abbreviation	I/O	Function
Counter clock input pin	FTCI	Input	FRC counter clock input
Output compare A output pin	FTOA	Output	Output compare A output
Output compare B output pin	FTOB	Output	Output compare B output
Input capture A input pin	FTIA	Input	Input capture A input
Input capture B input pin	FTIB	Input	Input capture B input
Input capture C input pin	FTIC	Input	Input capture C input
Input capture D input pin	FTID	Input	Input capture D input

9.3 Register Descriptions

The FRT has the following registers.

- Free-running counter (FRC)
- Output compare register A (OCRA)
- Output compare register B (OCRB)
- Input capture register A (ICRA)
- Input capture register B (ICRB)
- Input capture register C (ICRC)
- Input capture register D (ICRD)
- Output compare register AR (OCRAR)
- Output compare register AF (OCRAF)
- Output compare register DM (OCRDM)
- Timer interrupt enable register (TIER)
- Timer control/status register (TCSR)
- Timer control register (TCR)
- Timer output compare control register (TOCR)

Note: OCRA and OCRB share the same address. Register selection is controlled by the OCRS bit in TOCR. ICRA, ICRB, and ICRC share the same addresses with OCRAR, OCRAF, and OCRDM. Register selection is controlled by the ICRS bit in TOCR.

9.3.1 Free-Running Counter (FRC)

FRC is a 16-bit readable/writable up-counter. The clock source is selected by bits CKS1 and CKS0 in TCR. FRC can be cleared by compare-match A. When FRC overflows from H'FFFF to H'0000, the overflow flag bit (OVF) in TCSR is set to 1. FRC should always be accessed in 16-bit units; cannot be accessed in 8-bit units. FRC is initialized to H'0000.

9.3.2 Output Compare Registers A and B (OCRA, OCRB)

The FRT has two output compare registers, OCRA and OCRB, each of which is a 16-bit readable/writable register whose contents are continually compared with the value in FRC. When a match is detected (compare-match), the corresponding output compare flag (OCFA or OCFB) is set to 1 in TCSR. If the OEA or OEB bit in TOCR is set to 1, when the OCR and FRC values match, the output level selected by the OLVLA or OLVLB bit in TOCR is output at the output compare output pin (FTOA or FTOB). Following a reset, the FTOA and FTOB output levels are 0 until the first compare-match. OCR should always be accessed in 16-bit units; cannot be accessed in 8-bit units. OCR is initialized to H'FFFF.

9.3.3 Input Capture Registers A to D (ICRA to ICRD)

The FRT has four input capture registers, ICRA to ICRD, each of which is a 16-bit read-only register. When the rising or falling edge of the signal at an input capture input pin (FTIA to FTID) is detected, the current FRC value is transferred to the corresponding input capture register (ICRA to ICRD). At the same time, the corresponding input capture flag (ICFA to ICFD) in TCSR is set to 1. The FRC contents are transferred to ICR regardless of the value of ICF. The input capture edge is selected by the input edge select bits (IEDGA to IEDGD) in TCR.

ICRC and ICRD can be used as ICRA and ICRB buffer registers, respectively, by means of buffer enable bits A and B (BUFEA and BUFEB) in TCR. For example, if an input capture occurs when ICRC is specified as the ICRA buffer register, the FRC contents are transferred to ICRA, and then transferred to the buffer register ICRC.

To ensure input capture, the input capture pulse width should be at least 1.5 system clocks (ϕ) for a single edge. When triggering is enabled on both edges, the input capture pulse width should be at least 2.5 system clocks (ϕ).

ICRA to ICRD should always be accessed in 16-bit units; cannot be accessed in 8-bit units. ICR is initialized to H'0000.

9.3.4 Output Compare Registers AR and AF (OCRAR, OCRAF)

OCRAR and OCRAF are 16-bit readable/writable registers. When the OCRAMS bit in TOCR is set to 1, the operation of OCRA is changed to include the use of OCRAR and OCRAF. The contents of OCRAR and OCRAF are automatically added alternately to OCRA, and the result is written to OCRA. The write operation is performed on the occurrence of compare-match A. In the 1st compare-match A after setting the OCRAMS bit to 1, OCRAF is added. The operation due to compare-match A varies according to whether the compare-match follows addition of OCRAR or OCRAF. The value of the OLVLA bit in TOCR is ignored, and 1 is output on a compare-match A following addition of OCRAF, while 0 is output on a compare-match A following addition of OCRAR.

When using the OCRA automatic addition function, do not select internal clock $\phi/2$ as the FRC input clock together with a set value of H'0001 or less for OCRAR (or OCRAF).

OCRAR and OCRAF should always be accessed in 16-bit units; cannot be accessed in 8-bit units. OCRAR and OCRAF are initialized to H'FFFF.

9.3.5 Output Compare Register DM (OCRDM)

OCRDM is a 16-bit readable/writable register in which the upper 8 bits are fixed at H'00. When the ICRDMS bit in TOCR is set to 1 and the contents of OCRDM are other than H'0000, the operation of ICRD is changed to include the use of OCRDM. The point at which input capture D occurs is taken as the start of a mask interval. Next, twice the contents of OCRDM is added to the contents of ICRD, and the result is compared with the FRC value. The point at which the values match is taken as the end of the mask interval. New input capture D events are disabled during the mask interval. A mask interval is not generated when the contents of OCRDM are H'0000 while the ICRDMS bit is set to 1.

OCRDM should always be accessed in 16-bit units; cannot be accessed in 8-bit units. OCRDM is initialized to H'0000.

9.3.6 Timer Interrupt Enable Register (TIER)

TIER enables and disables interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	ICIAE	0	R/W	Input Capture Interrupt A Enable Selects whether to enable input capture interrupt A request (ICIA) when input capture flag A (ICFA) in TCSR is set to 1. 0: ICIA requested by ICFA is disabled 1: ICIA requested by ICFA is enabled
6	ICIBE	0	R/W	Input Capture Interrupt B Enable Selects whether to enable input capture interrupt B request (ICIB) when input capture flag B (ICFB) in TCSR is set to 1. 0: ICIB requested by ICFB is disabled 1: ICIB requested by ICFB is enabled
5	ICICE	0	R/W	Input Capture Interrupt C Enable Selects whether to enable input capture interrupt C request (ICIC) when input capture flag C (ICFC) in TCSR is set to 1. 0: ICIC requested by ICFC is disabled 1: ICIC requested by ICFC is enabled
4	ICIDE	0	R/W	Input Capture Interrupt D Enable Selects whether to enable input capture interrupt D request (ICID) when input capture flag D (ICFD) in TCSR is set to 1. 0: ICID requested by ICFD is disabled 1: ICID requested by ICFD is enabled
3	OCIAE	0	R/W	Output Compare Interrupt A Enable Selects whether to enable output compare interrupt A request (OCIA) when output compare flag A (OCFA) in TCSR is set to 1. 0: OCIA requested by OCFA is disabled 1: OCIA requested by OCFA is enabled

Bit	Bit Name	Initial Value	R/W	Description
2	OCIBE	0	R/W	Output Compare Interrupt B Enable Selects whether to enable output compare interrupt B request (OCIB) when output compare flag B (OCFB) in TCSR is set to 1. 0: OCIB requested by OCFB is disabled 1: OCIB requested by OCFB is enabled
1	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether to enable a free-running timer overflow request interrupt (FOVI) when the timer overflow flag (OVF) in TCSR is set to 1. 0: FOVI requested by OVF is disabled 1: FOVI requested by OVF is enabled
0	—	0	R	Reserved This bit is always read as 1 and cannot be modified.

9.3.7 Timer Control/Status Register (TCSR)

TCSR is used for counter clear selection and control of interrupt request signals.

Bit	Bit Name	Initial Value	R/W	Description
7	ICFA	0	R/(W)*	Input Capture Flag A This status flag indicates that the FRC value has been transferred to ICRA by means of an input capture signal. When BUFEA = 1, ICFA indicates that the old ICRA value has been moved into ICRC and the new FRC value has been transferred to ICRA. Only 0 can be written to this bit to clear the flag. [Setting condition] When an input capture signal causes the FRC value to be transferred to ICRA [Clearing condition] Read ICFA when ICFA = 1, then write 0 to ICFA

Bit	Bit Name	Initial Value	R/W	Description
6	ICFB	0	R/(W)*	Input Capture Flag B This status flag indicates that the FRC value has been transferred to ICRB by means of an input capture signal. When BUFEB = 1, ICFB indicates that the old ICRB value has been moved into ICRD and the new FRC value has been transferred to ICRB. Only 0 can be written to this bit to clear the flag. [Setting condition] When an input capture signal causes the FRC value to be transferred to ICRB [Clearing condition] Read ICFB when ICFB = 1, then write 0 to ICFB
5	ICFC	0	R/(W)*	Input Capture Flag C This status flag indicates that the FRC value has been transferred to ICRC by means of an input capture signal. When BUFEA = 1, on occurrence of an input capture signal specified by the IEDGC bit at the FTIC input pin, ICFC is set but data is not transferred to ICRC. In buffer operation, ICFC can be used as an external interrupt signal by setting the ICICE bit to 1. Only 0 can be written to this bit to clear the flag. [Setting condition] When an input capture signal is received [Clearing condition] Read ICFC when ICFC = 1, then write 0 to ICFC
4	ICFD	0	R/(W)*	Input Capture Flag D This status flag indicates that the FRC value has been transferred to ICRD by means of an input capture signal. When BUFEB = 1, on occurrence of an input capture signal specified by the IEDGD bit at the FTID input pin, ICFD is set but data is not transferred to ICRD. In buffer operation, ICFD can be used as an external interrupt signal by setting the ICIDE bit to 1. Only 0 can be written to this bit to clear the flag. [Setting condition] When an input capture signal is received [Clearing condition] Read ICFD when ICFD = 1, then write 0 to ICFD

Bit	Bit Name	Initial Value	R/W	Description
3	OCFA	0	R/(W)*	Output Compare Flag A This status flag indicates that the FRC value matches the OCRA value. Only 0 can be written to this bit to clear the flag. [Setting condition] When FRC = OCRA [Clearing condition] Read OCFA when OCFA = 1, then write 0 to OCFA
2	OCFB	0	R/(W)*	Output Compare Flag B This status flag indicates that the FRC value matches the OCRB value. Only 0 can be written to this bit to clear the flag. [Setting condition] When FRC = OCRB [Clearing condition] Read OCFB when OCFB = 1, then write 0 to OCFB
1	OVF	0	R/(W)*	Timer Overflow This status flag indicates that the FRC has overflowed. Only 0 can be written to this bit to clear the flag. [Setting condition] When FRC overflows (changes from H'FFFF to H'0000) [Clearing condition] Read OVF when OVF = 1, then write 0 to OVF
0	CCLRA	0	R/W	Counter Clear A This bit selects whether the FRC is to be cleared at compare-match A (when the FRC and OCRA values match). 0: FRC clearing is disabled 1: FRC is cleared at compare-match A

Note * Only 0 can be written to clear the flag.

9.3.8 Timer Control Register (TCR)

TCR selects the rising or falling edge of the input capture signals, enables the input capture buffer mode, and selects the FRC clock source.

Bit	Bit Name	Initial Value	R/W	Description
7	IEDGA	0	R/W	Input Edge Select A Selects the rising or falling edge of the input capture A signal (FTIA). 0: Capture on the falling edge of FTIA 1: Capture on the rising edge of FTIA
6	IEDGB	0	R/W	Input Edge Select B Selects the rising or falling edge of the input capture B signal (FTIB). 0: Capture on the falling edge of FTIB 1: Capture on the rising edge of FTIB
5	IEDGC	0	R/W	Input Edge Select C Selects the rising or falling edge of the input capture C signal (FTIC). 0: Capture on the falling edge of FTIC 1: Capture on the rising edge of FTIC
4	IEDGD	0	R/W	Input Edge Select D Selects the rising or falling edge of the input capture D signal (FTID). 0: Capture on the falling edge of FTID 1: Capture on the rising edge of FTID
3	BUFEA	0	R/W	Buffer Enable A Selects whether ICRC is to be used as a buffer register for ICRA. 0: ICRC is not used as a buffer register for ICRA 1: ICRC is used as a buffer register for ICRA
2	BUFEB	0	R/W	Buffer Enable B Selects whether ICRD is to be used as a buffer register for ICRB. 0: ICRD is not used as a buffer register for ICRB 1: ICRD is used as a buffer register for ICRB

Bit	Bit Name	Initial Value	R/W	Description
1	CKS1	0	R/W	Clock Select 1, 0
0	CKS0	0		Select clock source for FRC.
				00: φ/2 internal clock source
				01: φ/8 internal clock source
				10: φ/32 internal clock source
				11: External clock source (counting at FTCI rising edge)

9.3.9 Timer Output Compare Control Register (TOCR)

TOCR enables output from the output compare pins, selects the output levels, switches access between output compare registers A and B, controls the ICRD and OCRA operating modes, and switches access to input capture registers A, B, and C.

Bit	Bit Name	Initial Value	R/W	Description
7	ICRDMS	0	R/W	Input Capture D Mode Select
				Specifies whether ICRD is used in the normal operating mode or in the operating mode using OCRDM.
				0: The normal operating mode is specified for ICRD
				1: The operating mode using OCRDM is specified for ICRD
6	OCRAMS	0	R/W	Output Compare A Mode Select
				Specifies whether OCRA is used in the normal operating mode or in the operating mode using OCRAR and OCRAF.
				0: The normal operating mode is specified for OCRA
				1: The operating mode using OCRAR and OCRAF is specified for OCRA
5	ICRS	0	R/W	Input Capture Register Select
				The same addresses are shared by ICRA and OCRAR, by ICRB and OCRAF, and by ICRC and OCRDM. The ICRS bit determines which registers are selected when the shared addresses are read from or written to. The operation of ICRA, ICRB, and ICRC is not affected.
				0: ICRA, ICRB, and ICRC are selected
				1: OCRAR, OCRAF, and OCRDM are selected

Bit	Bit Name	Initial Value	R/W	Description
4	OCRS	0	R/W	Output Compare Register Select OCRA and OCRB share the same address. When this address is accessed, the OCRS bit selects which register is accessed. The operation of OCRA or OCRB is not affected. 0: OCRA is selected 1: OCRB is selected
3	OEA	0	R/W	Output Enable A Enables or disables output of the output compare A output pin (FTOA). 0: Output compare A output is disabled 1: Output compare A output is enabled
2	OEB	0	R/W	Output Enable B Enables or disables output of the output compare B output pin (FTOB). 0: Output compare B output is disabled 1: Output compare B output is enabled
1	OLVLA	0	R/W	Output Level A Selects the level to be output at the output compare A output pin (FTOA) in response to compare-match A (signal indicating a match between the FRC and OCRA values). When the OCRAMS bit is 1, this bit is ignored. 0: 0 is output at compare-match A 1: 1 is output at compare-match A
0	OLVLB	0	R/W	Output Level B Selects the level to be output at the output compare B output pin (FTOB) in response to compare-match B (signal indicating a match between the FRC and OCRB values). 0: 0 is output at compare-match B 1: 1 is output at compare-match B

9.4 Operation

9.4.1 Pulse Output

Figure 9.2 shows an example of 50%-duty pulses output with an arbitrary phase difference. When a compare match occurs while the CCLRA bit in TCSR is set to 1, the OLVLA and OLVLB bits are inverted by software.

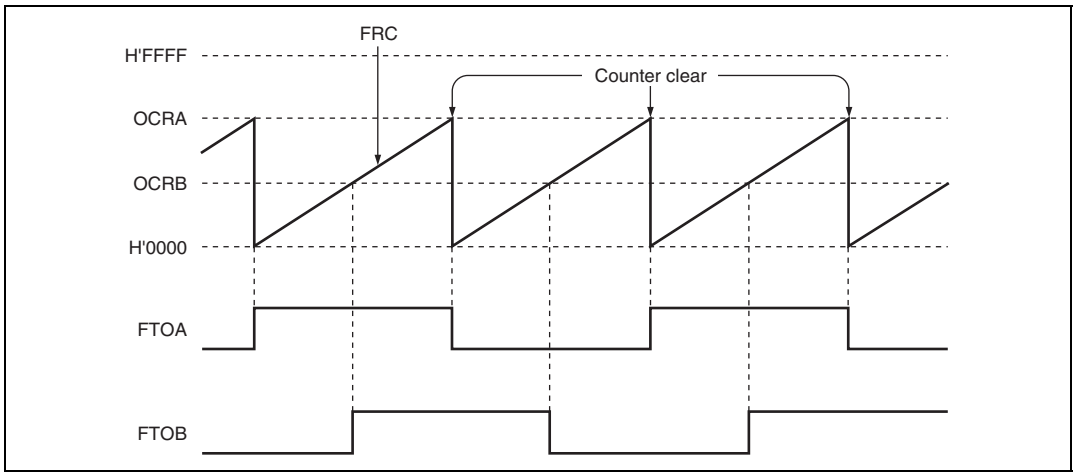


Figure 9.2 Example of Pulse Output

9.5 Operation Timing

9.5.1 FRC Increment Timing

Figure 9.3 shows the FRC increment timing with an internal clock source. Figure 9.4 shows the increment timing with an external clock source. The pulse width of the external clock signal must be at least 1.5 system clocks (ϕ). The counter will not increment correctly if the pulse width is shorter than 1.5 system clocks (ϕ).

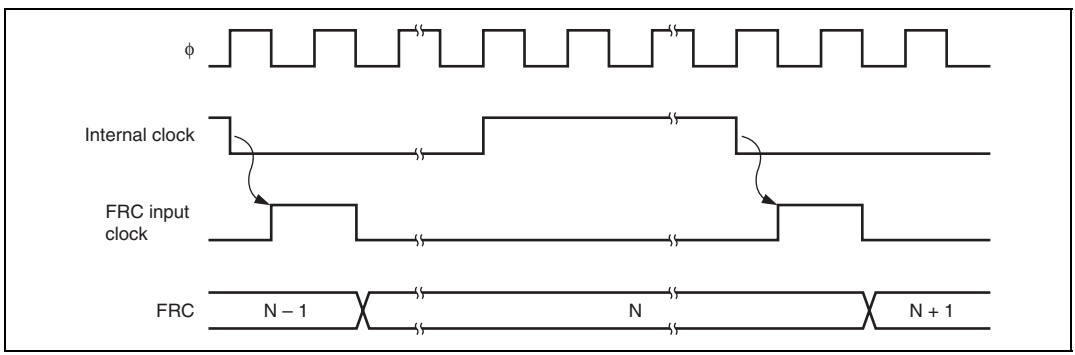


Figure 9.3 Increment Timing with Internal Clock Source

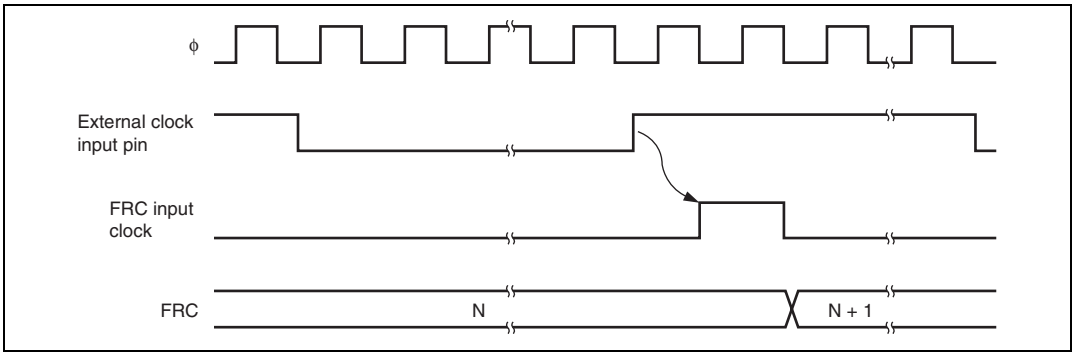


Figure 9.4 Increment Timing with External Clock Source

9.5.2 Output Compare Output Timing

A compare-match signal occurs at the last state when the FRC and OCR values match (at the timing when the FRC updates the counter value). When a compare-match signal occurs, the level selected by the OLVL bit in TOCR is output at the output compare pin (FTOA or FTOB). Figure 9.5 shows the timing of this operation for compare-match A.

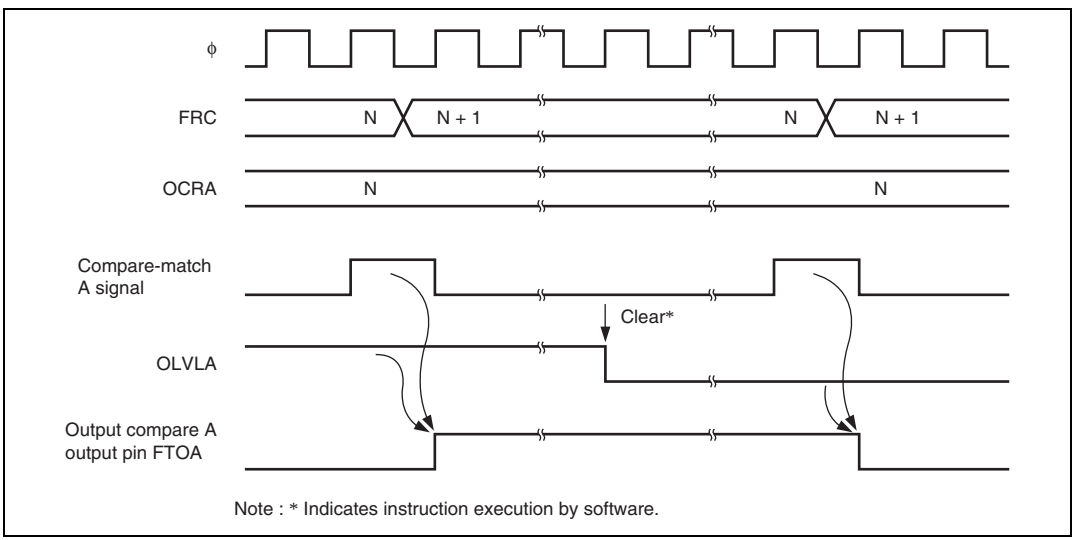


Figure 9.5 Timing of Output Compare A Output

9.5.3 FRC Clear Timing

FRC can be cleared when compare-match A occurs. Figure 9.6 shows the timing of this operation.

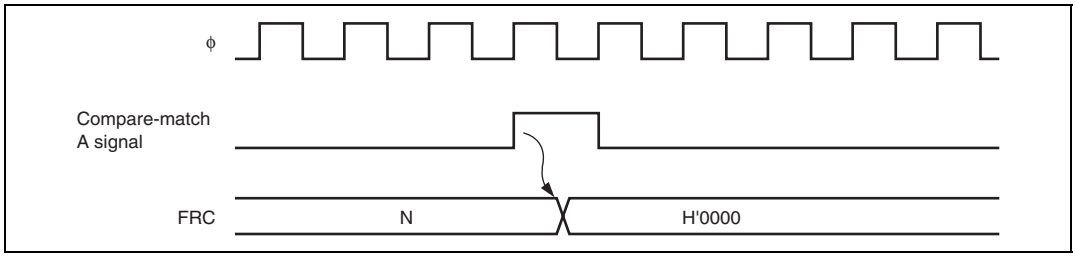


Figure 9.6 Clearing of FRC by Compare-Match A Signal

9.5.4 Input Capture Input Timing

The rising or falling edge can be selected for the input capture input timing by the IEDGA to IEDGD bits in TCR. Figure 9.7 shows the usual input capture timing when the rising edge is selected.

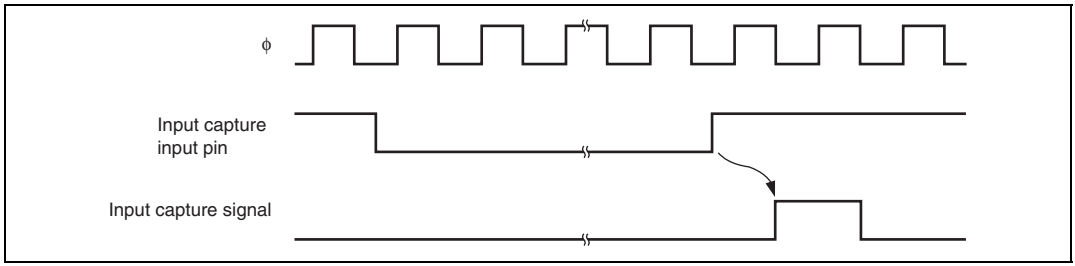


Figure 9.7 Input Capture Input Signal Timing (Usual Case)

If ICRA to ICRAD are read when the corresponding input capture signal arrives, the internal input capture signal is delayed by one system clock (ϕ). Figure 9.8 shows the timing for this case.

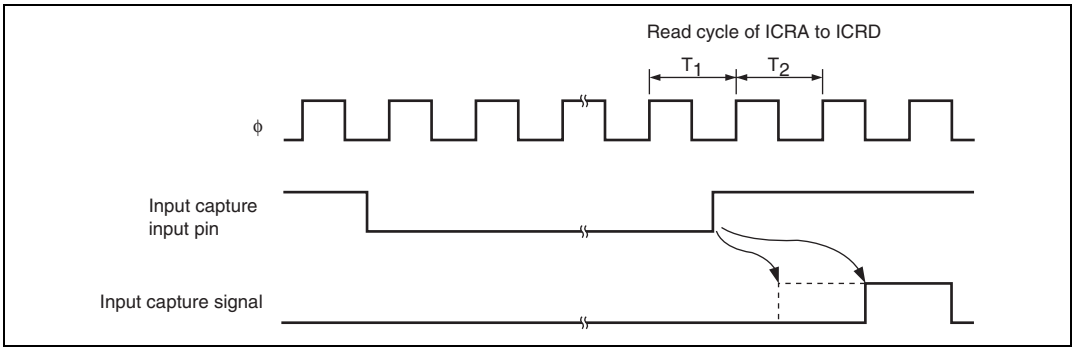


Figure 9.8 Input Capture Input Signal Timing (When ICRA to ICRD are Read)

9.5.5 Buffered Input Capture Input Timing

ICRC and ICRD can operate as buffers for ICRA and ICRB, respectively. Figure 9.9 shows how input capture operates when ICRC is used as ICRA's buffer register (BUFEA = 1) and IEDGA and IEDGC are set to different values (IEDGA = 0 and IEDGC = 1, or IEDGA = 1 and IEDGC = 0), so that input capture is performed on both the rising and falling edges of FTIA.

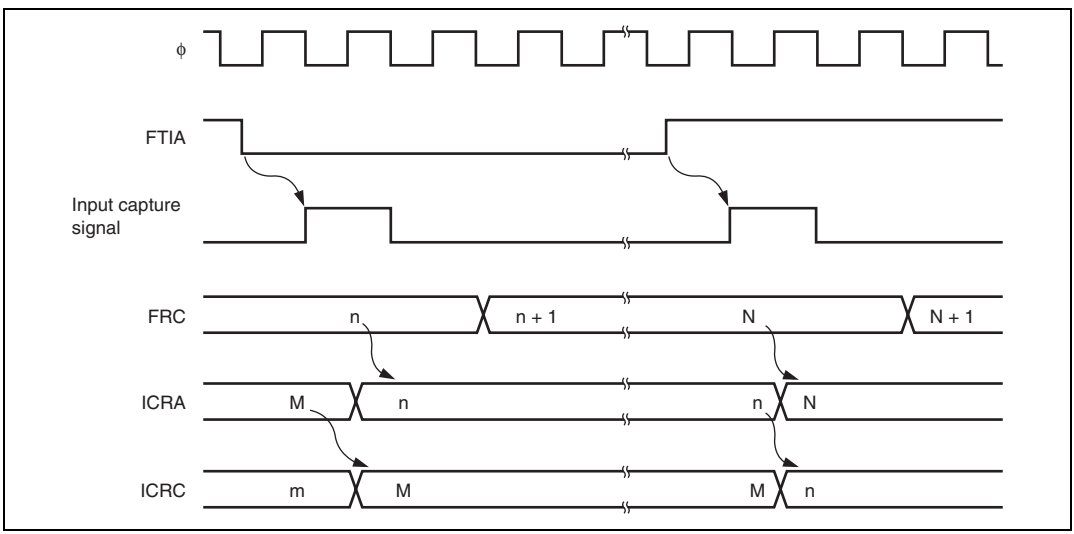


Figure 9.9 Buffered Input Capture Timing

Even when ICRC or ICRD is used as a buffer register, its input capture flag is set by the selected transition of its input capture signal. For example, if ICRC is used to buffer ICRA, when the edge transition selected by the IEDGC bit occurs on the FTIC input capture line, ICFC will be set, and if the ICICE bit is set at this time, an interrupt will be requested. The FRC value will not be transferred to ICRC, however. In buffered input capture, if either set of two registers to which data will be transferred (ICRA and ICRC, or ICRB and ICRD) is being read when the input capture input signal arrives, input capture is delayed by one system clock (ϕ). Figure 9.10 shows the timing when BUFEA = 1.

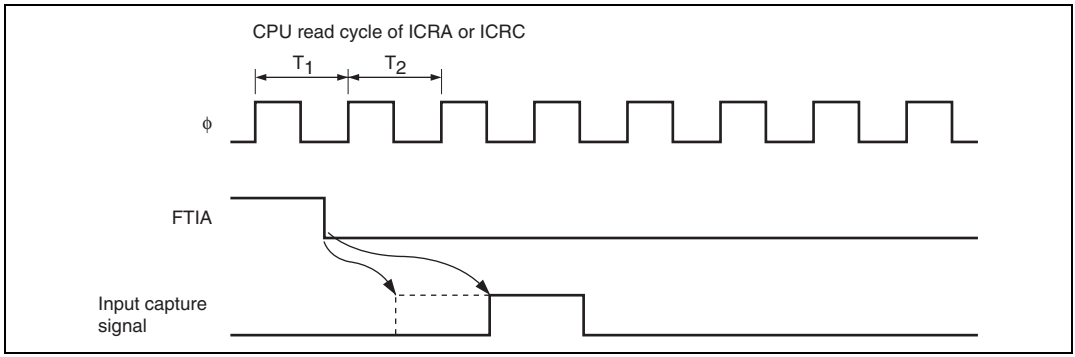


Figure 9.10 Buffered Input Capture Timing (BUFEA = 1)

9.5.6 Timing of Input Capture Flag (ICF) Setting

The input capture flag, ICFA, ICFB, ICFC, or ICFD, is set to 1 by the input capture signal. The FRC value is simultaneously transferred to the corresponding input capture register (ICRA, ICRB, ICRC, or ICRD). Figure 9.11 shows the timing of setting the ICFA to ICFD flag.

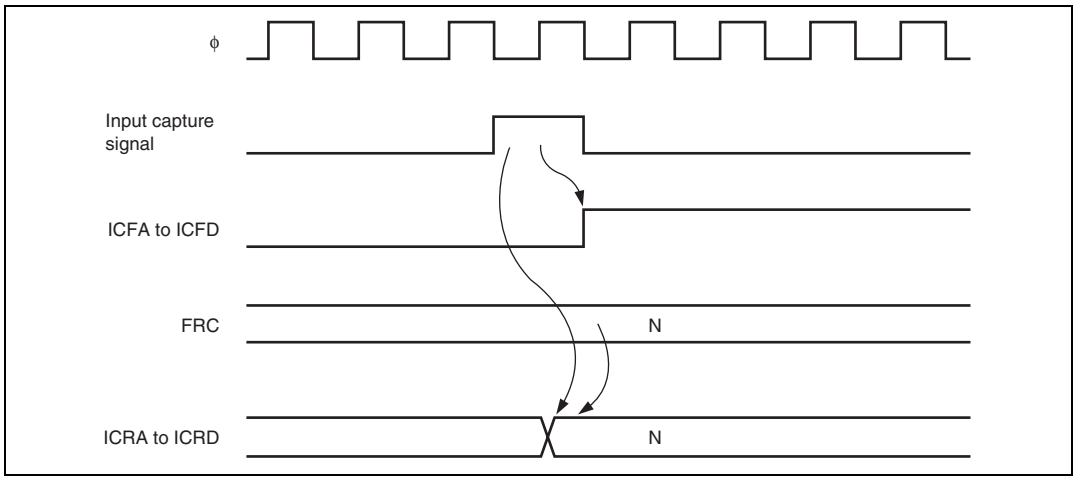


Figure 9.11 Timing of Input Capture Flag (ICFA, ICFB, ICFC, or ICFD) Setting

9.5.7 Timing of Output Compare Flag (OCF) setting

The output compare flag, OCFA or OCFB, is set to 1 by a compare-match signal generated when the FRC value matches the OCRA or OCRB value. This compare-match signal is generated at the last state in which the two values match, just before FRC increments to a new value. When the FRC and OCRA or OCRB value match, the compare-match signal is not generated until the next cycle of the clock source. Figure 9.12 shows the timing of setting the OCFA or OCFB flag.

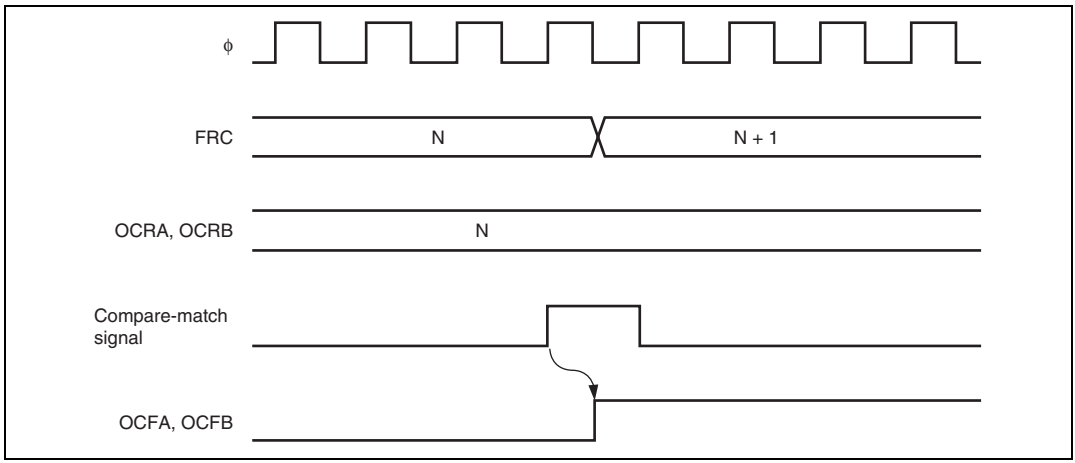


Figure 9.12 Timing of Output Compare Flag (OCFA or OCFB) Setting

9.5.8 Timing of FRC Overflow Flag Setting

The FRC overflow flag (OVF) is set to 1 when FRC overflows (changes from H'FFFF to H'0000). Figure 9.13 shows the timing of setting the OVF flag.

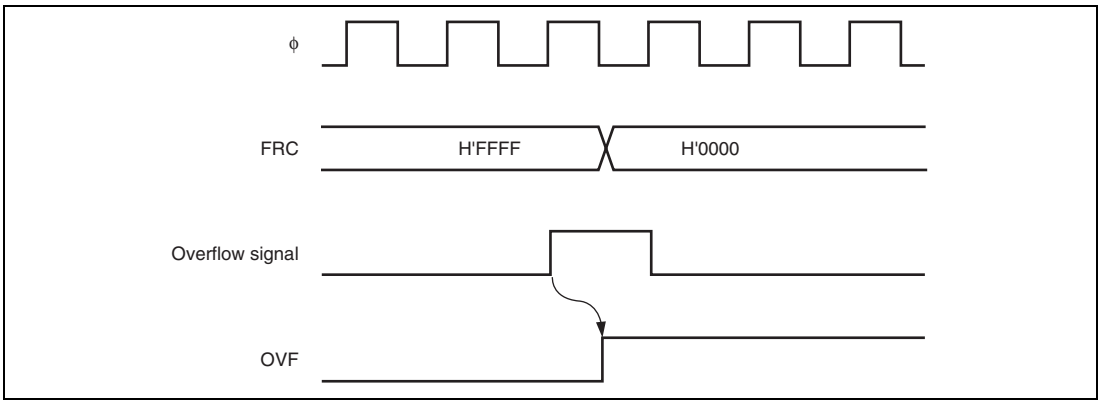


Figure 9.13 Timing of Overflow Flag (OVF) Setting

9.5.9 Automatic Addition Timing

When the OCRAMS bit in TOCR is set to 1, the contents of OCRAR and OCRAF are automatically added to OCRA alternately, and when an OCRA compare-match occurs a write to OCRA is performed. Figure 9.14 shows the OCRA write timing.

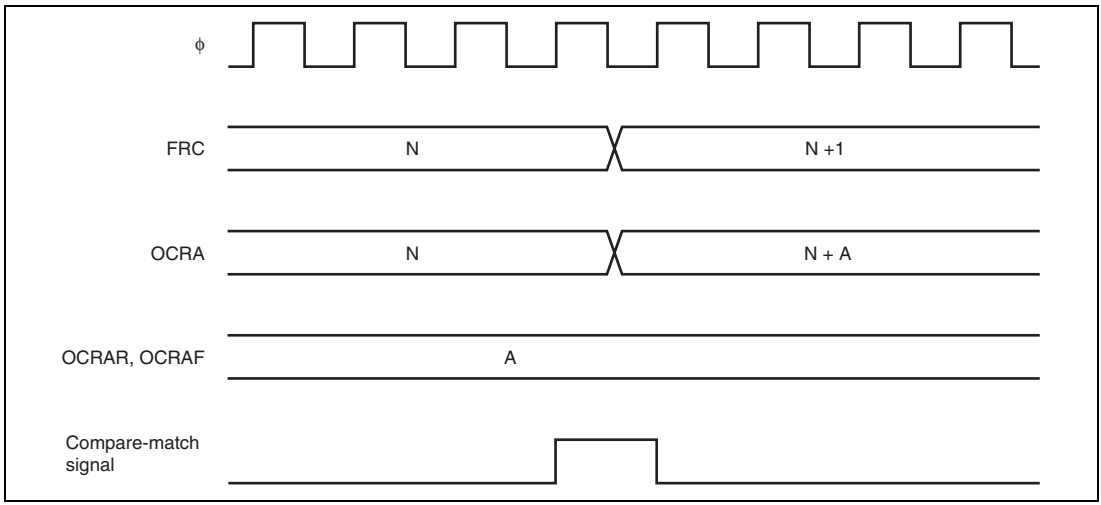


Figure 9.14 OCRA Automatic Addition Timing

9.5.10 Mask Signal Generation Timing

When the ICRDMS bit in TOCR is set to 1 and the contents of OCRDM are other than H'0000, a signal that masks the ICRD input capture signal is generated. The mask signal is set by the input capture signal. The mask signal is cleared by the sum of the ICRD contents and twice the OCRDM contents, and an FRC compare-match. Figure 9.15 shows the timing of setting the mask signal. Figure 9.16 shows the timing of clearing the mask signal.

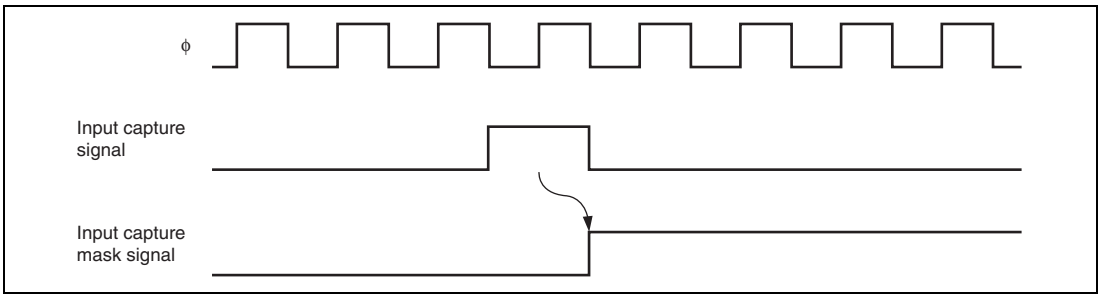


Figure 9.15 Timing of Input Capture Mask Signal Setting

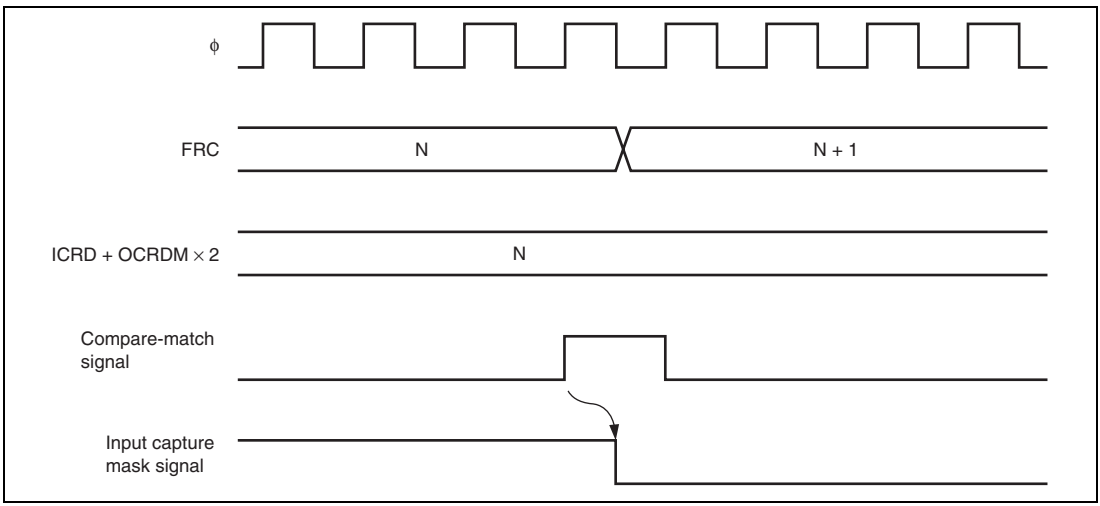


Figure 9.16 Timing of Input Capture Mask Signal Clearing

9.6 Interrupt Sources

The free-running timer can request seven interrupts: ICIA to ICID, OCIA, OCIB, and FOVI. Each interrupt can be enabled or disabled by an enable bit in TIER. Independent signals are sent to the interrupt controller for each interrupt. Table 9.2 lists the sources and priorities of these interrupts.

Table 9.2 FRT Interrupt Sources

Interrupt	Interrupt Source	Interrupt Flag	Priority
ICIA	Input capture of ICRA	ICFA	High
ICIB	Input capture of ICRB	ICFB	
ICIC	Input capture of ICRC	ICFC	
ICID	Input capture of ICRD	ICFD	
OCIA	Compare match of OCRA	OCFA	
OCIB	Compare match of OCRB	OCFB	
FOVI	Overflow of FRC	OVF	Low

9.7 Usage Notes

9.7.1 Conflict between FRC Write and Clear

If an internal counter clear signal is generated during the state after an FRC write cycle, the clear signal takes priority and the write is not performed. Figure 9.17 shows the timing for this type of conflict.

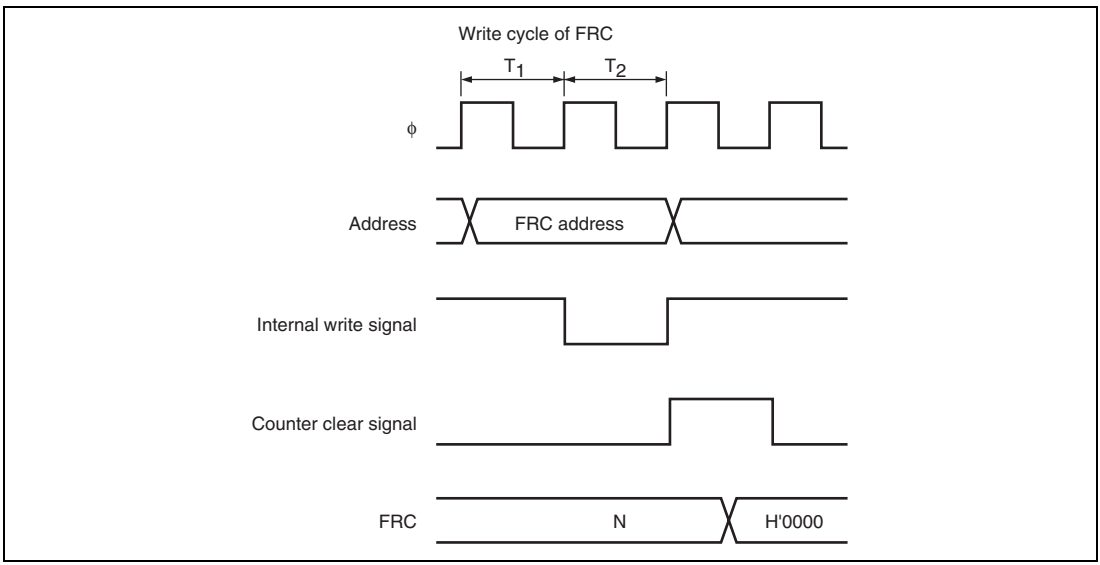


Figure 9.17 FRC Write-Clear Conflict

9.7.2 Conflict between FRC Write and Increment

If an FRC increment pulse is generated during the state after an FRC write cycle, the write takes priority and FRC is not incremented. Figure 9.18 shows the timing for this type of conflict.

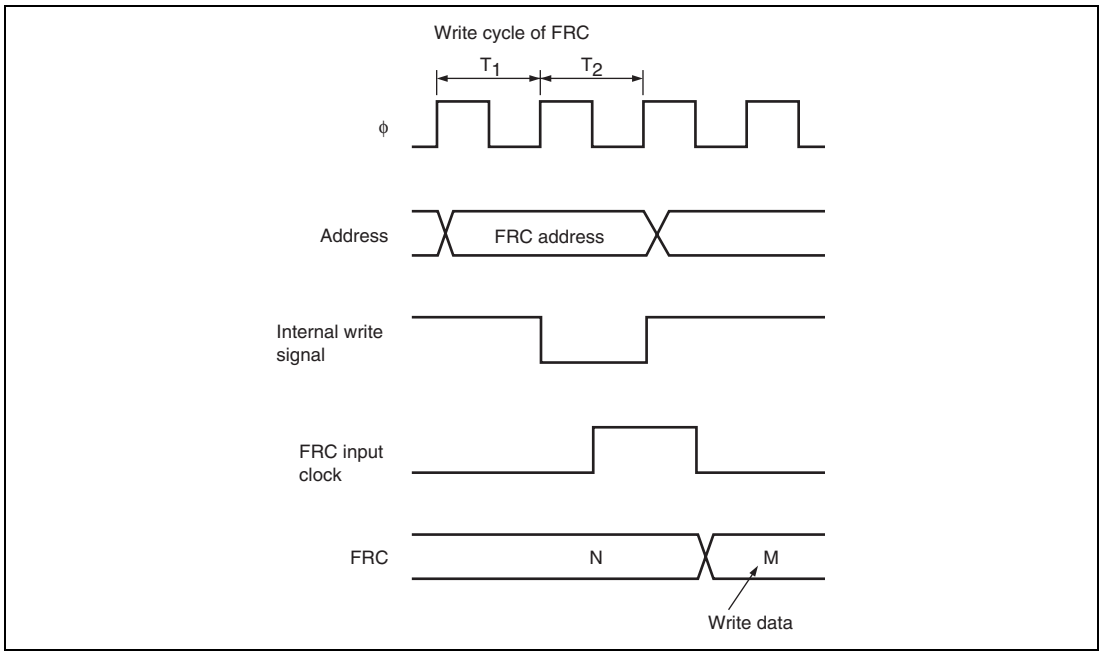


Figure 9.18 FRC Write-Increment Conflict

9.7.3 Conflict between OCR Write and Compare-Match

If a compare-match occurs during the state after an OCRA or OCRB write cycle, the write takes priority and the compare-match signal is disabled. Figure 9.19 shows the timing for this type of conflict.

If automatic addition of OCRAR and OCRAF to OCRA is selected, and a compare-match occurs in the cycle following the OCRA, OCRAR, and OCRAF write cycle, the OCRA, OCRAR and OCRAF write takes priority and the compare-match signal is disabled. Consequently, the result of the automatic addition is not written to OCRA. Figure 9.20 shows the timing for this type of conflict.

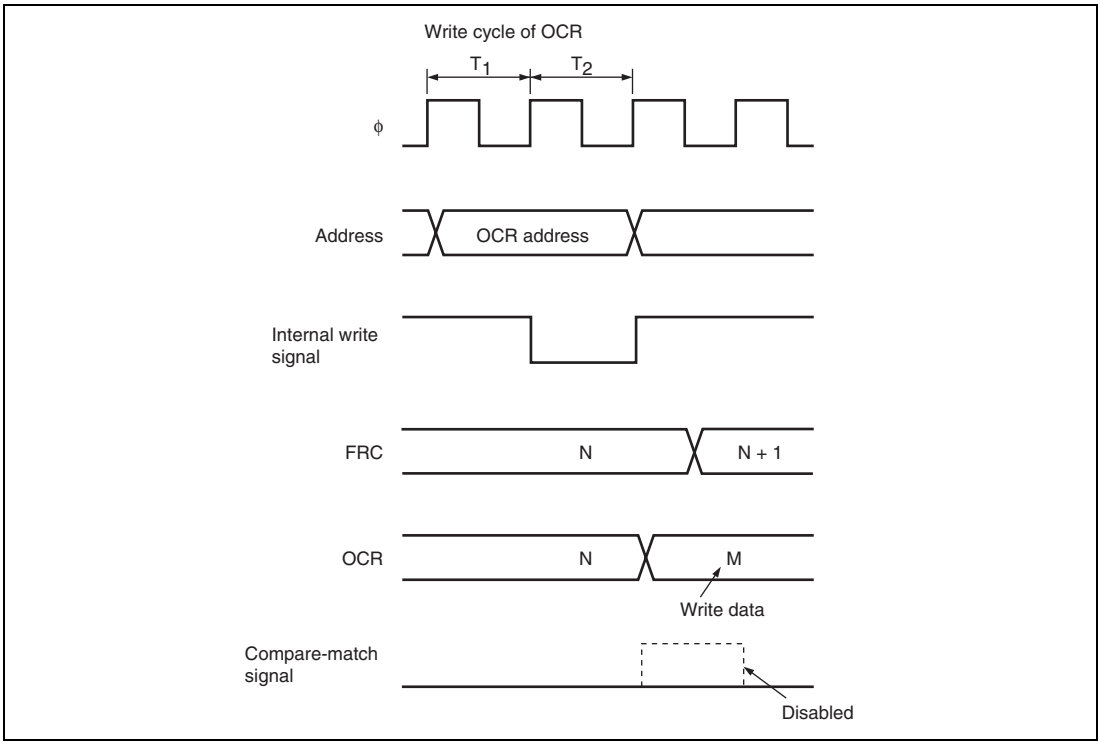


Figure 9.19 Conflict between OCR Write and Compare-Match (When Automatic Addition Function is Not Used)

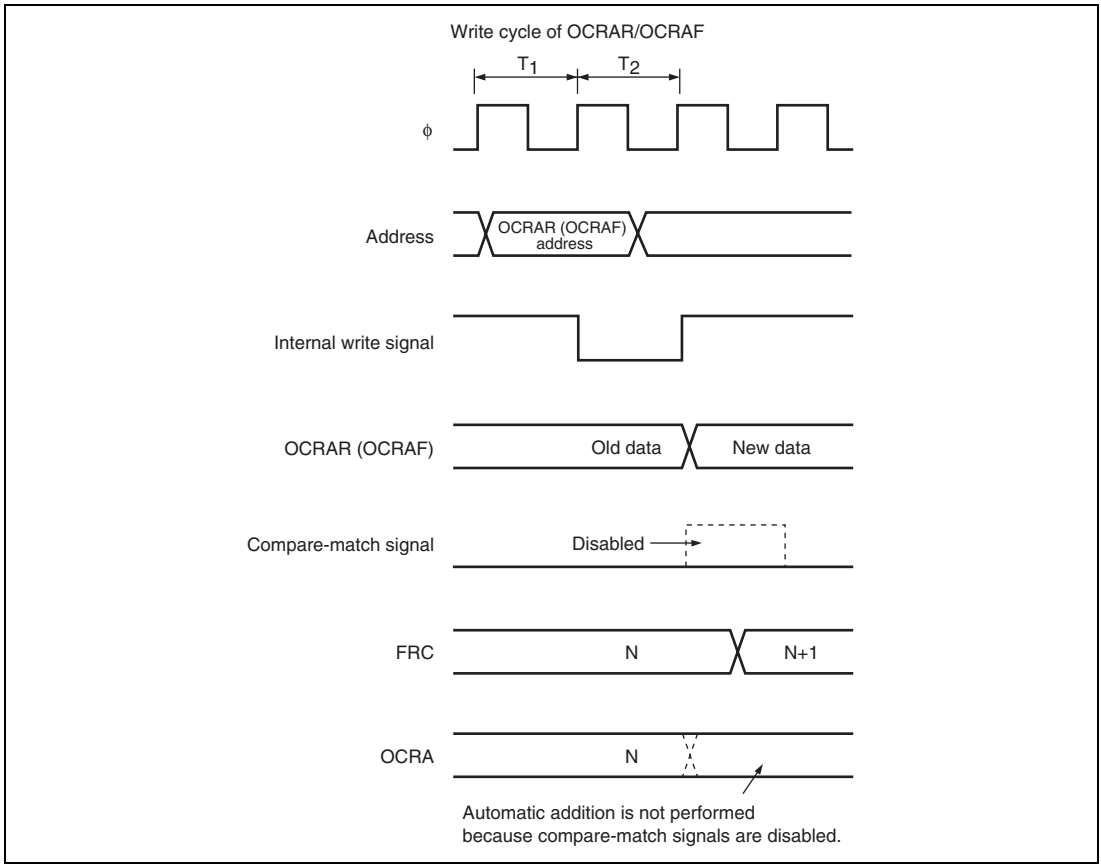


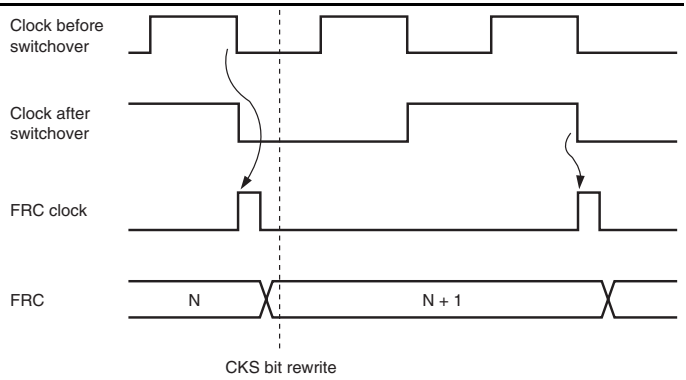
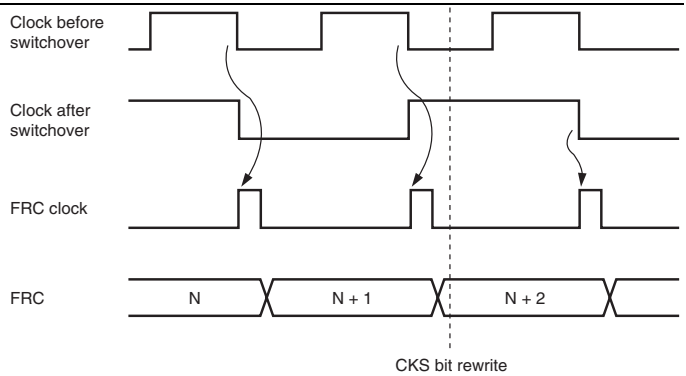
Figure 9.20 Conflict between OCRAR/OCRAF Write and Compare-Match (When Automatic Addition Function is Used)

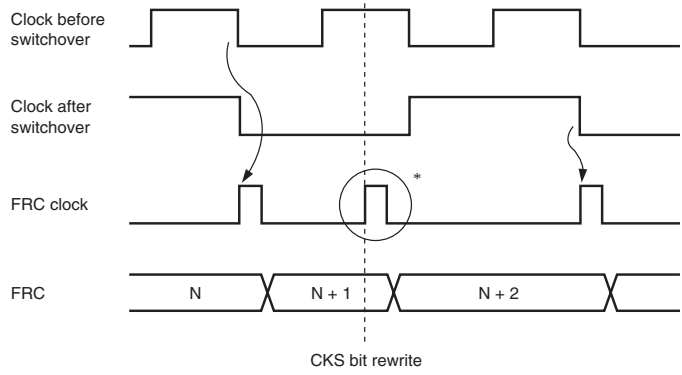
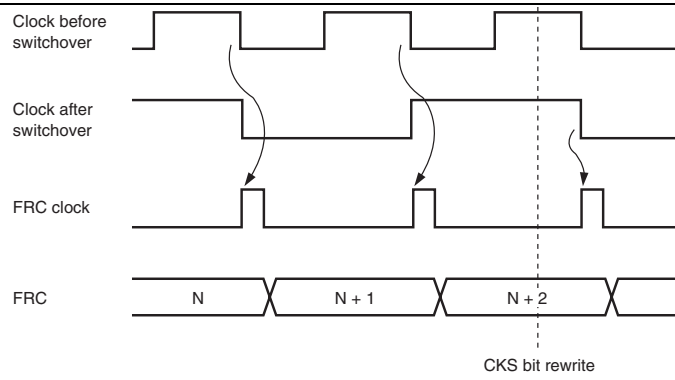
9.7.4 Switching of Internal Clock and FRC Operation

When the internal clock is changed, the changeover may cause FRC to increment. This depends on the time at which the clock is switched (bits CKS1 and CKS0 are rewritten), as shown in table 9.3.

When an internal clock is used, the FRC clock is generated on detection of the falling edge of the internal clock scaled from the system clock (ϕ). If the clock is changed when the old source is high and the new source is low, as in case no. 3 in table 9.3, the changeover is regarded as a falling edge that triggers the FRC clock, and FRC is incremented. Switching between an internal clock and external clock can also cause FRC to increment.

Table 9.3 Switching of Internal Clock and FRC Operation

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	FRC Operation
1	Switching from low to low	
2	Switching from low to high	

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	FRC Operation
3	Switching from high to low	
4	Switching from high to high	

Note: * Generated on the assumption that the switchover is a falling edge; FRC is incremented.

9.7.5 Module Stop Mode Setting

FRT operation can be enabled or disabled using the module stop control register. The initial setting is for FRT operation to be halted. Register access is enabled by canceling the module stop mode. For details, refer to section 18, Power-Down Modes.

Section 10 8-Bit Timer (TMR)

This LSI has three channels of on-chip 8-bit timer modules (TMR_0, TMR_1, and TMR_Y) made up of 8-bit counters. The 8-bit timer module can count external events, and can also be used as a multifunction timer in a variety of applications, such as generation of counter reset, interrupt requests, and pulse output with an arbitrary duty cycle using a compare-match signal with two registers.

10.1 Features

- Selection of clock sources
  - TMR_0, TMR_1: The counter input clock can be selected from six internal clocks and an external clock
  - TMR_Y: The counter input clock can be selected from three internal clocks and an external clock
- Selection of three ways to clear the counters
  - The counters can be cleared on compare-match A or compare-match B, or by an external reset signal.
- Timer output controlled by two compare-match signals
  - The timer output signal in each channel is controlled by two independent compare-match signals, enabling the timer to be used for various applications, such as the generation of pulse output or PWM output with an arbitrary duty cycle. (The TMR_Y does not have a timer output pin.)
- Cascading of TMR_0 and TMR_1
  - Operation as a 16-bit timer can be performed using TMR_0 as the upper half and TMR_1 as the lower half (16-bit count mode).
  - TMR_1 can be used to count TMR_0 compare-match occurrences (compare-match count mode).
- Multiple interrupt sources for each channel

  TMR_0, TMR_1, and TMR_Y: Three types of interrupts: Compare-match A, compare-match B, and overflow

Figures 10.1 and 10.2 show block diagrams of the 8-bit timer module.

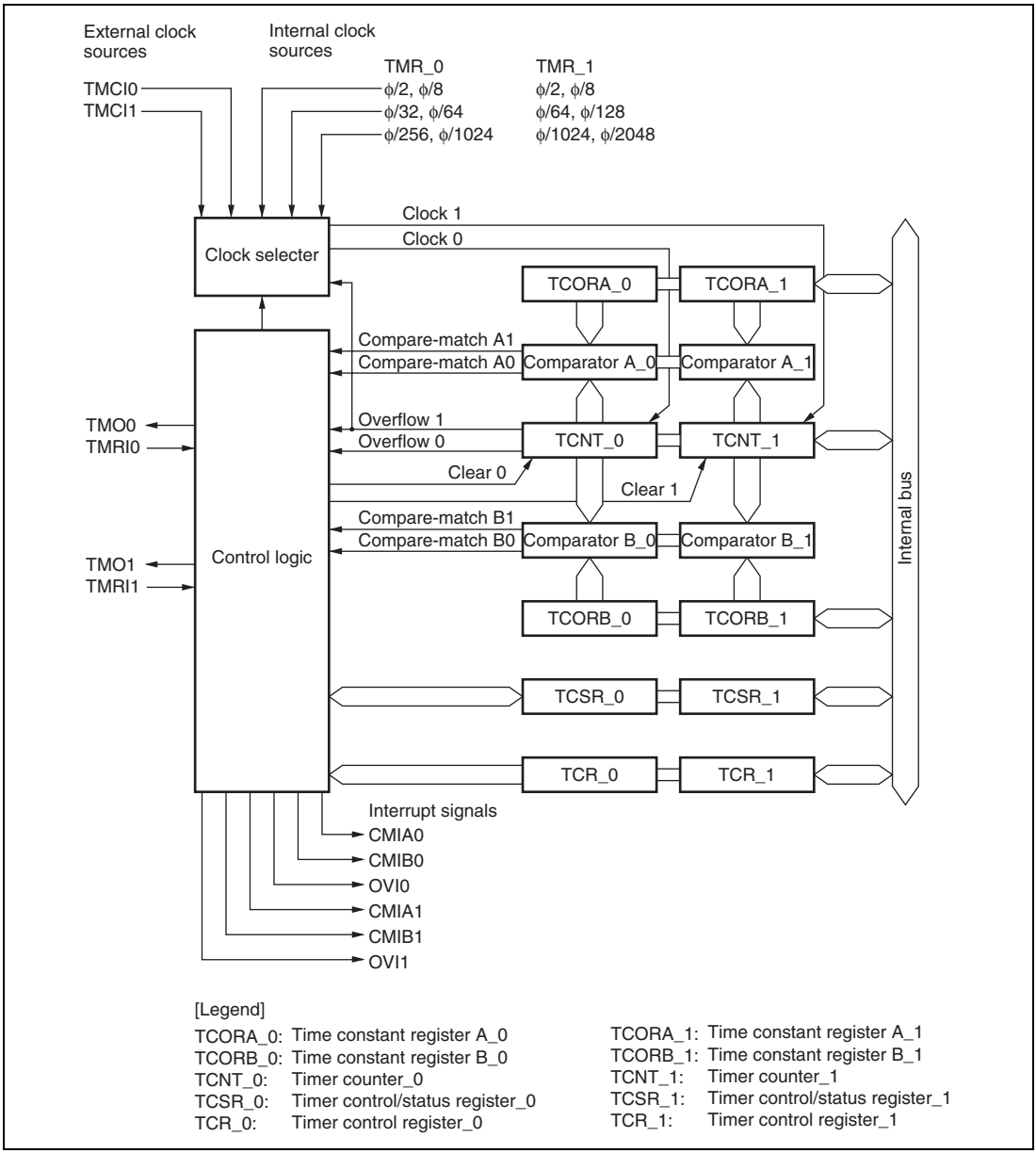
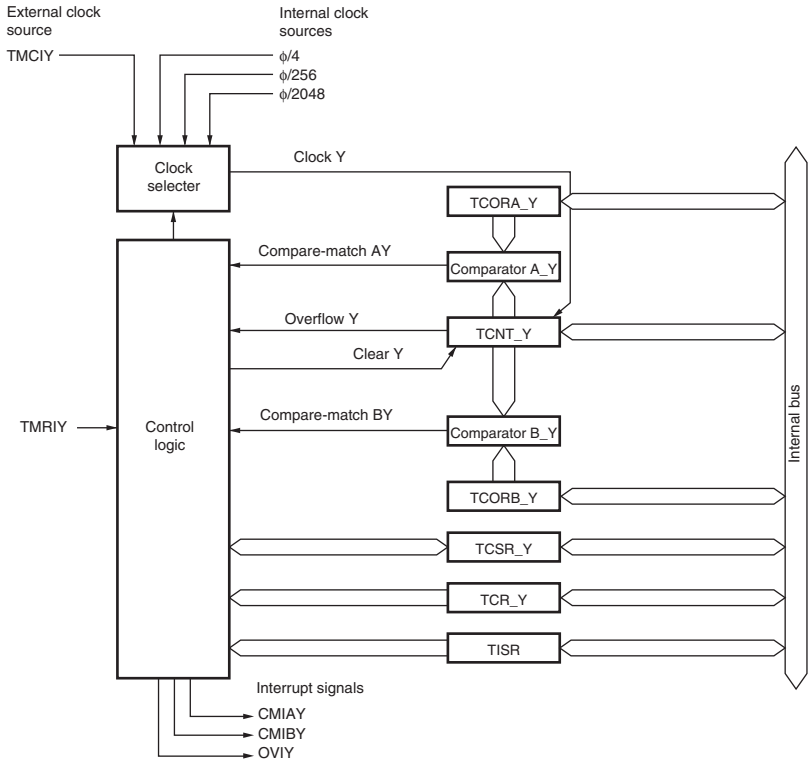


Figure 10.1 Block Diagram of 8-Bit Timers (TMR_0 and TMR_1)



[Legend]
TCORA_Y: Time constant register A_Y
TCORB_Y: Time constant register B_Y
TCNT_Y: Timer counter_Y
TCSR_Y: Timer control/status register_Y
TCR_Y: Timer control register_Y
TISR: Timer input select register

Figure 10.2 Block Diagram of 8-Bit Timers (TMR_Y)

10.2 Input/Output Pins

Table 10.1 summarizes the input and output pins of the TMR.

Table 10.1 Pin Configuration

Channel	Name	Symbol	I/O	Function
TMR_0	Timer output	TMO0	Output	Output controlled by compare-match
	Timer clock input	TMCI0	Input	External clock input for the counter
	Timer reset input	TMRI0	Input	External reset input for the counter
TMR_1	Timer output	TMO1	Output	Output controlled by compare-match
	Timer clock input	TMCI1	Input	External clock input for the counter
	Timer reset input	TMRI1	Input	External reset input for the counter
TMR_Y	Timer clock/reset input	TMIY (TMCIY/TMRIY)	Input	External clock input for the counter/ external reset input for the counter

10.3 Register Descriptions

The TMR has the following registers. For details on the serial timer control register, refer to section 3.2.3, Serial Timer Control Register (STCR).

- Timer counter (TCNT)
- Time constant register A (TCORA)
- Time constant register B (TCORB)
- Timer control register (TCR)
- Timer control/status register (TCSR)
- Timer input select register (TISR)*

Note: * TISR is only for the TMR_Y.

10.3.1 Timer Counter (TCNT)

Each TCNT is an 8-bit readable/writable up-counter. TCNT_0 and TCNT_1 comprise a single 16-bit register, so they can be accessed together by word access. The clock source is selected by the CKS2 to CKS0 bits in TCR. TCNT can be cleared by an external reset input signal, compare-match A signal or compare-match B signal. The method of clearing can be selected by the CCLR1 and CCLR0 bits in TCR. When TCNT overflows (changes from H'FF to H'00), the OVF bit in TCSR is set to 1. TCNT is initialized to H'00.

10.3.2 Time Constant Register A (TCORA)

TCORA is an 8-bit readable/writable register. TCORA_0 and TCORA_1 comprise a single 16-bit register, so they can be accessed together by word access. TCORA is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag A (CMFA) in TCSR is set to 1. Note however that comparison is disabled during the T2 state of a TCORA write cycle. The timer output from the TMO pin can be freely controlled by these compare-match A signals and the settings of output select bits OS1 and OS0 in TCSR. TCORA is initialized to H'FF.

10.3.3 Time Constant Register B (TCORB)

TCORB is an 8-bit readable/writable register. TCORB_0 and TCORB_1 comprise a single 16-bit register, so they can be accessed together by word access. TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag B (CMFB) in TCSR is set to 1. Note however that comparison is disabled during the T2 state of a TCORB write cycle. The timer output from the TMO pin can be freely controlled by these compare-match B signals and the settings of output select bits OS3 and OS2 in TCSR. TCORB is initialized to H'FF.

10.3.4 Timer Control Register (TCR)

TCR selects the TCNT clock source and the condition by which TCNT is cleared, and enables/disables interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare-Match Interrupt Enable B Selects whether the CMFB interrupt request (CMIB) is enabled or disabled when the CMFB flag in TCSR is set to 1. 0: CMFB interrupt request (CMIB) is disabled 1: CMFB interrupt request (CMIB) is enabled
6	CMIEA	0	R/W	Compare-Match Interrupt Enable A Selects whether the CMFA interrupt request (CMIA) is enabled or disabled when the CMFA flag in TCSR is set to 1. 0: CMFA interrupt request (CMIA) is disabled 1: CMFA interrupt request (CMIA) is enabled
5	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether the OVF interrupt request (OVI) is enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt request (OVI) is disabled 1: OVF interrupt request (OVI) is enabled
4	CCLR1	0	R/W	Counter Clear 1, 0
3	CCLR0	0	R/W	These bits select the method by which the timer counter is cleared. 00: Clearing is disabled 01: Cleared on compare-match A 10: Cleared on compare-match B 11: Cleared on rising edge of external reset input
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	These bits select the clock input to TCNT and count condition, together with the ICKS1 and ICKS0 bits in STCR. For details, see table 10.2.
0	CKS0	0	R/W	

Table 10.2 Clock Input to TCNT and Count Condition

	TCR			STCR		
Channel	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR_0	0	0	0	—	—	Disables clock input
	0	0	1	—	0	Increments at falling edge of internal clock φ/8
	0	0	1	—	1	Increments at falling edge of internal clock φ/2
	0	1	0	—	0	Increments at falling edge of internal clock φ/64
	0	1	0	—	1	Increments at falling edge of internal clock φ/32
	0	1	1	—	0	Increments at falling edge of internal clock φ/1024
	0	1	1	—	1	Increments at falling edge of internal clock φ/256
	1	0	0	—	—	Increments at overflow signal from TCNT_1*
TMR_1	0	0	0	—	—	Disables clock input
	0	0	1	0	—	Increments at falling edge of internal clock φ/8
	0	0	1	1	—	Increments at falling edge of internal clock φ/2
	0	1	0	0	—	Increments at falling edge of internal clock φ/64
	0	1	0	1	—	Increments at falling edge of internal clock φ/128
	0	1	1	0	—	Increments at falling edge of internal clock φ/1024
	0	1	1	1	—	Increments at falling edge of internal clock φ/2048
	1	0	0	—	—	Increments at compare-match A from TCNT_0*

	TCR			STCR		
Channel	**CKS2**	**CKS1**	**CKS0**	**ICKS1**	**ICKS0**	**Description**
TMR_Y	0	0	0	—	—	Disables clock input
	0	0	1	—	—	Increments at falling edge of internal clock $\phi/4$
	0	1	0	—	—	Increments at falling edge of internal clock $\phi/256$
	0	1	1	—	—	Increments at falling edge of internal clock $\phi/2048$
	1	0	0	—	—	Disables clock input
Common	1	0	1	—	—	Increments at rising edge of external clock
	1	1	0	—	—	Increments at falling edge of external clock
	1	1	1	—	—	Increments at both rising and falling edges of external clock.

Note: * If the TMR_0 clock input is set as the TCNT_1 overflow signal and the TMR_1 clock input is set as the TCNT_0 compare-match signal simultaneously, a count-up clock cannot be generated.

10.3.5 Timer Control/Status Register (TCSR)

TCSR indicates the status flags and controls compare-match output.

- TCSR_0

Bit	Bit Name	Initial Value	R/W	Description
7	CMFB	0	R/(W)*	Compare-Match Flag B [Setting condition] When the values of TCNT_0 and TCORB_0 match [Clearing conditions] • Read CMFB when CMFB = 1, then write 0 in CMFB
6	CMFA	0	R/(W)*	Compare-Match Flag A [Setting condition] When the values of TCNT_0 and TCORA_0 match [Clearing conditions] • Read CMFA when CMFA = 1, then write 0 in CMFA
5	OVF	0	R/(W)*	Timer Overflow Flag [Setting condition] When TCNT_0 overflows from H'FF to H'00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4	ADTE	0	R/W	A/D Trigger Enable Enables or disables A/D converter start requests by compare-match A. 0: A/D converter start requests by compare-match A are disabled 1: A/D converter start requests by compare-match A are enabled

Bit	Bit Name	Initial Value	R/W	Description
3	OS3	0	R/W	Output Select 3, 2
2	OS2	0	R/W	These bits specify how the TMO0 pin output level is to be changed by compare-match B of TCORB_0 and TCNT_0. 00: No change 01: 0 is output 10: 1 is output 11: Output is inverted (toggle output)
1	OS1	0	R/W	Output Select 1, 0
0	OS0	0	R/W	These bits specify how the TMO0 pin output level is to be changed by compare-match A of TCORA_0 and TCNT_0. 00: No change 01: 0 is output 10: 1 is output 11: Output is inverted (toggle output)

Note: * Only 0 can be written for clearing the flag.

- TCSR_1

Bit	Bit Name	Initial Value	R/W	Description
7	CMFB	0	R/(W)*	Compare-Match Flag B [Setting condition] When the values of TCNT_1 and TCORB_1 match [Clearing conditions] • Read CMFB when CMFB = 1, then write 0 in CMFB
6	CMFA	0	R/(W)*	Compare-Match Flag A [Setting condition] When the values of TCNT_1 and TCORA_1 match [Clearing conditions • Read CMFA when CMFA = 1, then write 0 in CMFA
5	OVF	0	R/(W)*	Timer Overflow Flag [Setting condition] When TCNT_1 overflows from H'FF to H'00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4	—	1	R	Reserved This bit is always read as 1 and cannot be modified.
3	OS3	0	R/W	Output Select 3, 2
2	OS2	0	R/W	These bits specify how the TMO1 pin output level is to be changed by compare-match B of TCORB_1 and TCNT_1. 00: No change 01: 0 is output 10: 1 is output 11: Output is inverted (toggle output)

Bit	Bit Name	Initial Value	R/W	Description
1	OS1	0	R/W	Output Select 1, 0
0	OS0	0	R/W	These bits specify how the TMO1 pin output level is to be changed by compare-match A of TCORA_1 and TCNT_1. 00: No change 01: 0 is output 10: 1 is output 11: Output is inverted (toggle output)

Note: * Only 0 can be written for clearing the flag.

- TCSR_Y

Bit	Bit Name	Initial Value	R/W	Description
7	CMFB	0	R/(W)*[1]	Compare-Match Flag B [Setting condition] When the values of TCNT_Y and TCORB_Y match [Clearing conditions] • Read CMFB when CMFB = 1, then write 0 in CMFB
6	CMFA	0	R/(W)*[1]	Compare-Match Flag A [Setting condition] When the values of TCNT_Y and TCORA_Y match [Clearing conditions] • Read CMFA when CMFA = 1, then write 0 in CMFA
5	OVF	0	R/(W)*[1]	Timer Overflow Flag [Setting condition] When TCNT_Y overflows from H'FF to H'00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4		0	R	Reserved This bit is always read as 0 and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
3	OS3	0	R/W	Output Select 3, 2
2	OS2	0	R/W	These bits specify how the TMOY pin*[2] output level is to be changed by compare-match B of TCORB_Y and TCNT_Y. 00: No change 01: 0 is output 10: 1 is output 11: Output is inverted (toggle output)
1	OS1	0	R/W	Output Select 1, 0
0	OS0	0	R/W	These bits specify how the TMOY pin*[2] output level is to be changed by compare-match A of TCORA_Y and TCNT_Y. 00: No change 01: 0 is output 10: 1 is output 11: Output is inverted (toggle output)

Notes: 1. Only 0 can be written for clearing the flag.
2. This product does not have a TMOY external output pin.

10.3.6 Timer Input Select Register (TISR)

TISR enables or disables to input a signal on the external counter clock/external counter reset input pin.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 1	R/(W)	Reserved The initial value should not be modified.
0	IS	0	R/W	Input Select Enables or disables to input a signal to be used as an external clock or an external reset for the TMR_Y counter on the TMIY (TMCIY/TMRIY) pin. 0: Disables a signal input on the TMIY (TMCIY/TMRIY) pin 1: Enables a signal input on the TMIY (TMCIY/TMRIY) pin

10.4 Operation

10.4.1 Pulse Output

Figure 10.3 shows an example for outputting an arbitrary duty pulse.

1. Clear the CCLR1 bit in TCR to 0 so that TCNT is cleared according to the compare match of TCORA, and then set the CCLR0 bit to 1.
2. Set the OS3 to OS0 bits in TCSR to B'0110 so that 1 is output according to the compare match of TCORA and 0 is output according to the compare match of TCORB.

According to the above settings, the waveforms with the TCORA cycle and TCORB pulse width can be output without the intervention of software.

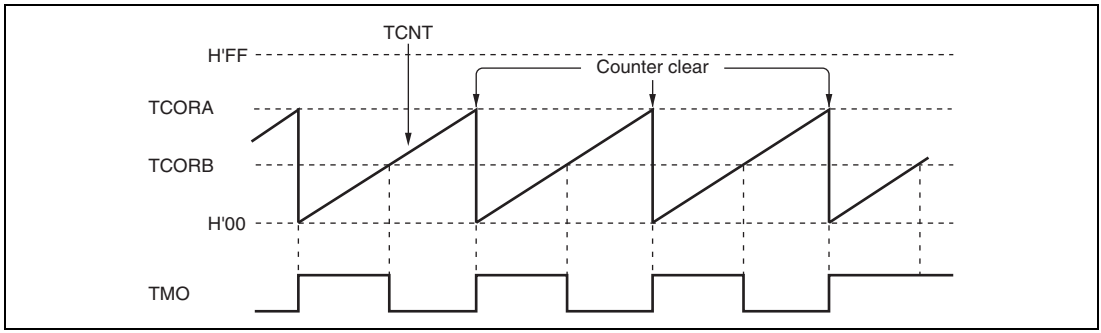


Figure 10.3 Pulse Output Example

10.5 Operation Timing

10.5.1 TCNT Count Timing

Figure 10.4 shows the TCNT count timing with an internal clock source. Figure 10.5 shows the TCNT count timing with an external clock source. The pulse width of the external clock signal must be at least 1.5 system clocks (ϕ) for a single edge and at least 2.5 system clocks (ϕ) for both edges. The counter will not increment correctly if the pulse width is less than these values.

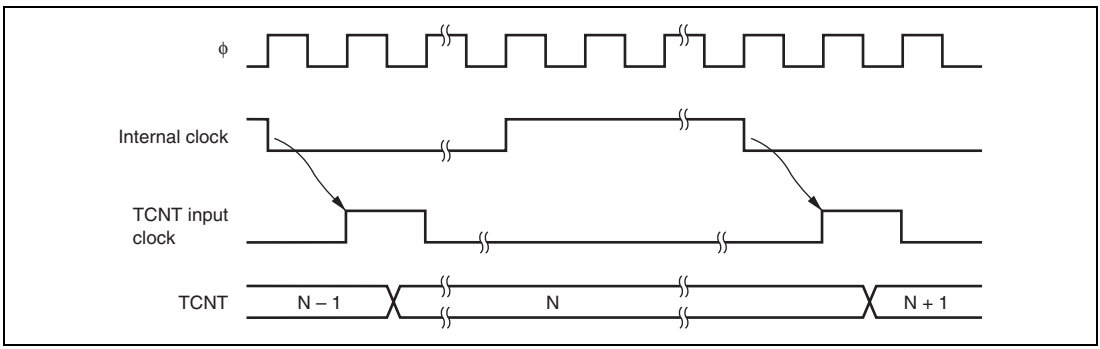


Figure 10.4 Count Timing for Internal Clock Input

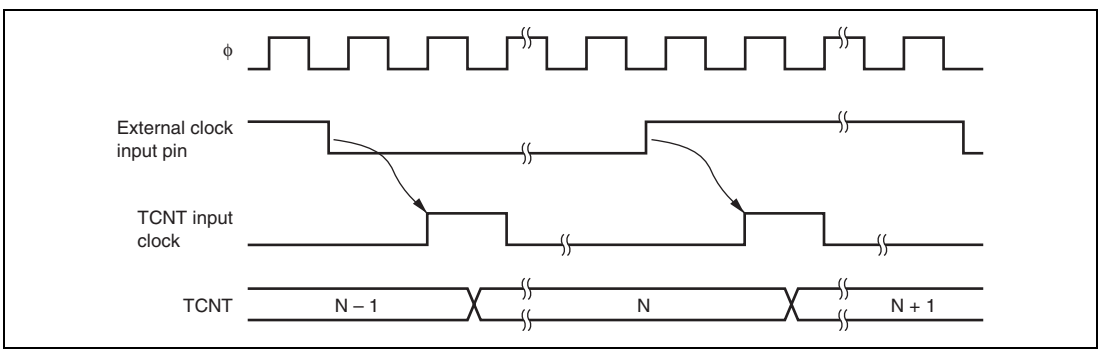


Figure 10.5 Count Timing for External Clock Input (Both Edges)

10.5.2 Timing of CMFA and CMFB Setting at Compare-Match

The CMFA and CMFB flags in TCSR are set to 1 by a compare-match signal generated when the TCNT and TCOR values match. The compare-match signal is generated at the last state in which the match is true, just when the timer counter is updated. Therefore, when TCNT and TCOR match, the compare-match signal is not generated until the next TCNT input clock. Figure 10.6 shows the timing of CMF flag setting.

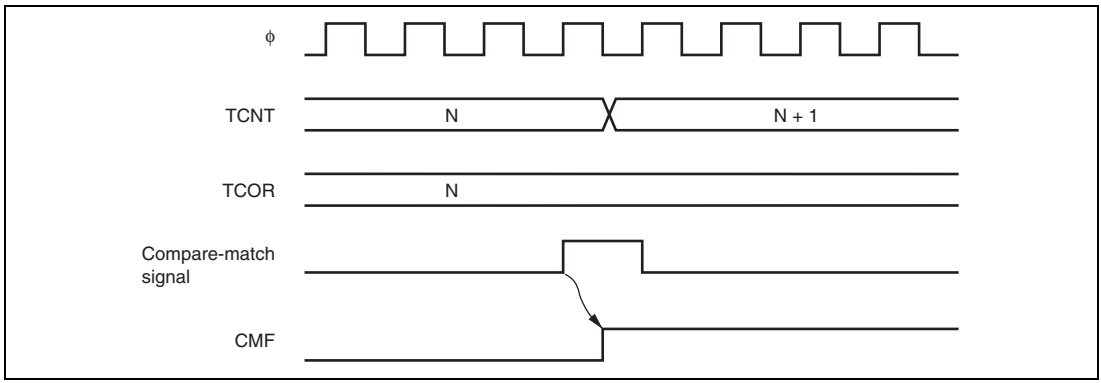


Figure 10.6 Timing of CMF Setting at Compare-Match

10.5.3 Timing of Timer Output at Compare-Match

When a compare-match signal occurs, the timer output changes as specified by the OS3 to OS0 bits in TCSR. Figure 10.7 shows the timing of timer output when the output is set to toggle by a compare-match A signal.

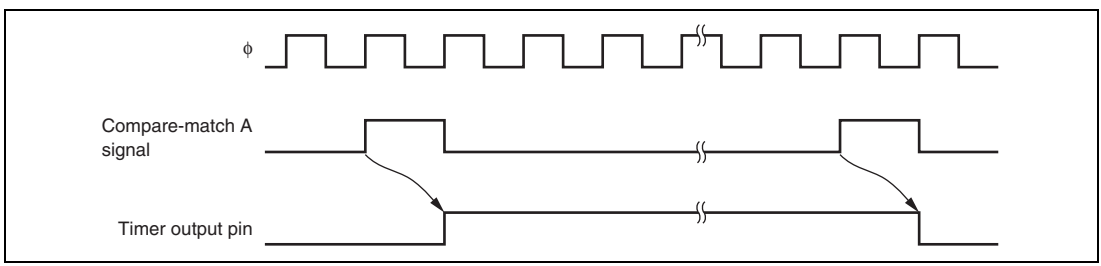


Figure 10.7 Timing of Toggled Timer Output by Compare-Match A Signal

10.5.4 Timing of Counter Clear at Compare-Match

TCNT is cleared when compare-match A or compare-match B occurs, depending on the setting of the CCLR1 and CCLR0 bits in TCR. Figure 10.8 shows the timing of clearing the counter by a compare-match.

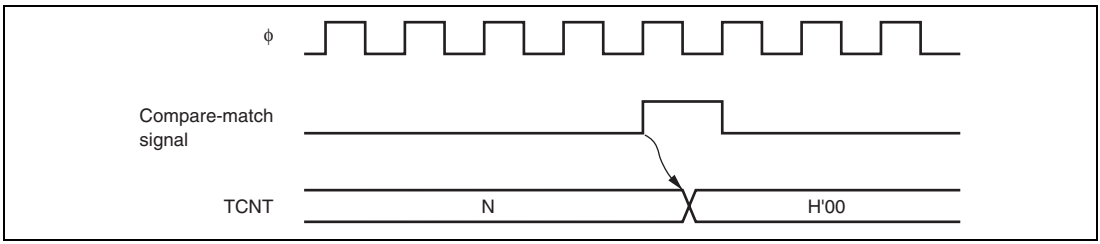


Figure 10.8 Timing of Counter Clear by Compare-Match

10.5.5 TCNT External Reset Timing

TCNT is cleared at the rising edge of an external reset input, depending on the settings of the CCLR1 and CCLR0 bits in TCR. The width of the clearing pulse must be at least 1.5 states. Figure 10.9 shows the timing of clearing the counter by an external reset input.

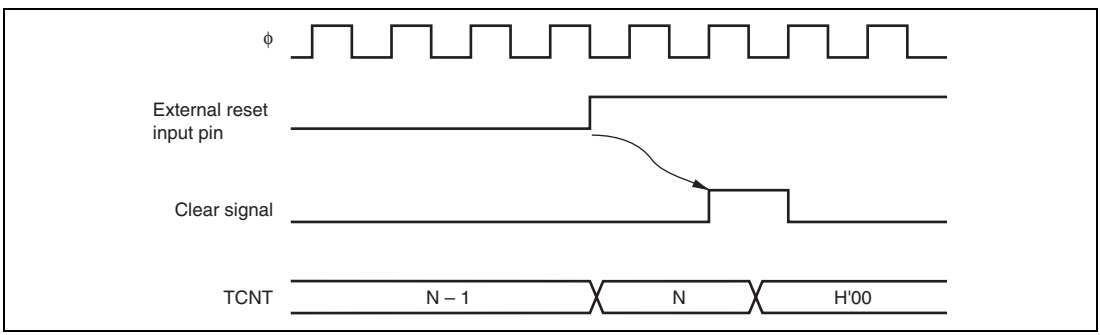


Figure 10.9 Timing of Counter Clear by External Reset Input

10.5.6 Timing of Overflow Flag (OVF) Setting

The OVF bit in TCSR is set to 1 when the TCNT overflows (changes from H'FF to H'00). Figure 10.10 shows the timing of OVF flag setting.

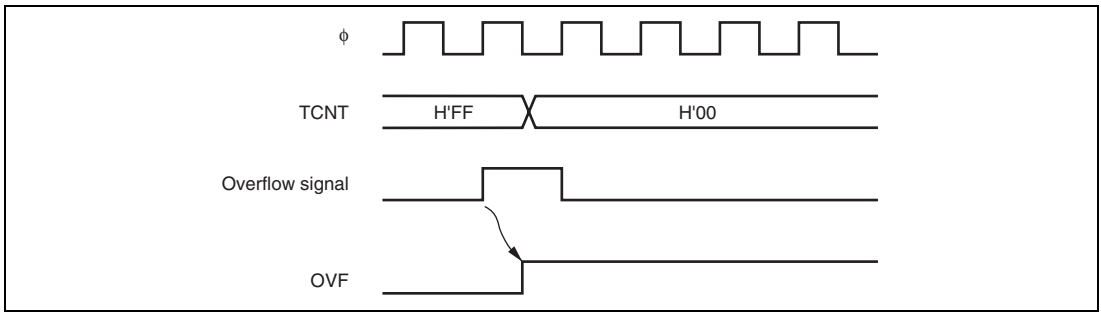


Figure 10.10 Timing of OVF Flag Setting

10.6 Operation with Cascaded Connection

If bits CKS2 to CKS0 in either TCR_0 or TCR_1 are set to B'100, the 8-bit timers of the two channels are cascaded. With this configuration, a single 16-bit timer can be used (16-bit count mode) or the compare-matches of the 8-bit timer of channel 0 can be counted by the 8-bit timer of channel 1 (compare-match count mode).

10.6.1 16-Bit Count Mode

When bits CKS2 to CKS0 in TCR_0 are set to B'100, the timer functions as a single 16-bit timer with channel 0 occupying the upper 8 bits and channel 1 occupying the lower 8 bits.

Setting of Compare-Match Flags:

- The CMF flag in TCSR_0 is set to 1 when a 16-bit compare-match occurs.
- The CMF flag in TCSR_1 is set to 1 when a lower 8-bit compare-match occurs.

Counter Clear Specification:

- If the CCLR1 and CCLR0 bits in TCR_0 have been set for counter clear at compare-match, the 16-bit counter (TCNT_0 and TCNT_1 together) is cleared when a 16-bit compare-match occurs. The 16-bit counter (TCNT_0 and TCNT_1 together) is also cleared when counter clear by the TMI0 pin has been set.
- The settings of the CCLR1 and CCLR0 bits in TCR_1 are ignored. The lower 8 bits cannot be cleared independently.

Pin Output:

- Control of output from the TMO0 pin by bits OS3 to OS0 in TCSR_0 is in accordance with the 16-bit compare-match conditions.
- Control of output from the TMO1 pin by bits OS3 to OS0 in TCSR_1 is in accordance with the lower 8-bit compare-match conditions.

10.6.2 Compare-Match Count Mode

When bits CKS2 to CKS0 in TCR_1 are B'100, TCNT_1 counts the occurrence of compare-match A for channel 0. Channels 0 and 1 are controlled independently. Conditions such as setting of the CMF flag, generation of interrupts, output from the TMO pin, and counter clearing are in accordance with the settings for each channel.

10.7 Interrupt Sources

TMR_0, TMR_1, and TMR_Y can generate three types of interrupts: CMIA, CMIB, and OVI. Table 10.3 shows the interrupt sources and priorities. Each interrupt source can be enabled or disabled independently by interrupt enable bits in TCR or TCSR. Independent signals are sent to the interrupt controller for each interrupt.

Table 10.3 Interrupt Sources of 8-Bit Timers TMR_0, TMR_1, TMR_Y, and TMR_X

Channel	Name	Interrupt Source	Interrupt Flag	Interrupt Priority
TMR_0	CMIA0	TCORA_0 compare-match	CMFA	High
	CMIB0	TCORB_0 compare-match	CMFB	
	OVI0	TCNT_0 overflow	OVF	
TMR_1	CMIA1	TCORA_1 compare-match	CMFA	
	CMIB1	TCORB_1 compare-match	CMFB	
	OVI1	TCNT_1 overflow	OVF	
TMR_Y	CMIAY	TCORA_Y compare-match	CMFA	
	CMIBY	TCORB_Y compare-match	CMFB	
	OVIY	TCNT_Y overflow	OVF	Low

10.8 Usage Notes

10.8.1 Conflict between TCNT Write and Clear

If a counter clear signal is generated during the T2 state of a TCNT write cycle as shown in figure 10.11, clearing takes priority, so that the counter is cleared and the write is not performed.

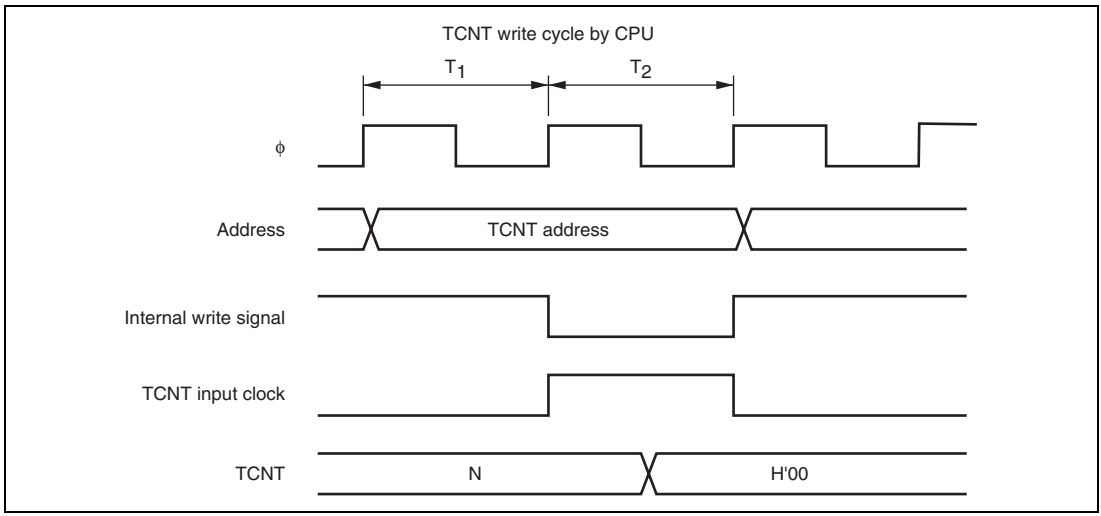


Figure 10.11 Conflict between TCNT Write and Clear

10.8.2 Conflict between TCNT Write and Increment

If a TCNT input clock is generated during the T2 state of a TCNT write cycle as shown in figure 10.12, the write takes priority and the counter is not incremented.

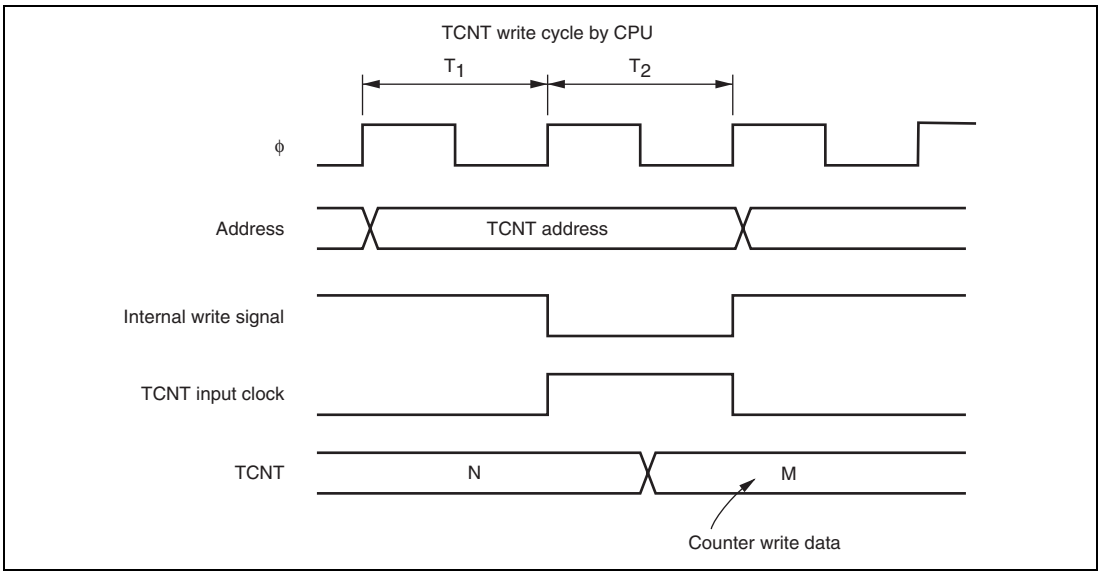


Figure 10.12 Conflict between TCNT Write and Increment

10.8.3 Conflict between TCOR Write and Compare-Match

If a compare-match occurs during the T2 state of a TCOR write cycle as shown in figure 10.13, the TCOR write takes priority and the compare-match signal is disabled.

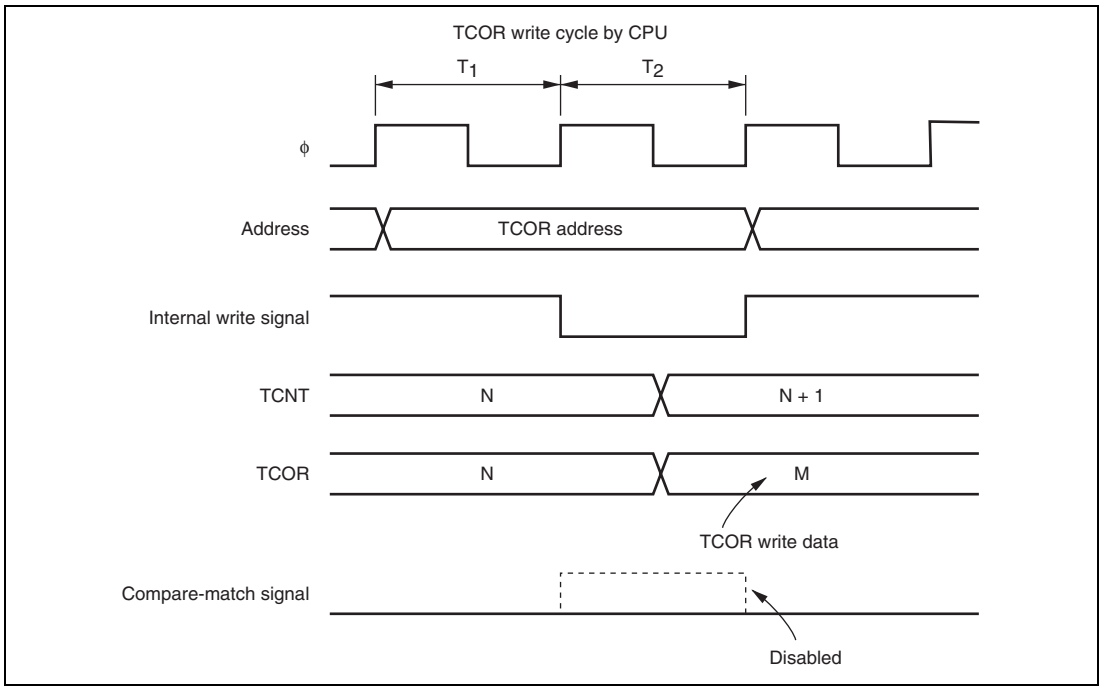


Figure 10.13 Conflict between TCOR Write and Compare-Match

10.8.4 Conflict between Compare-Matches A and B

If compare-matches A and B occur at the same time, the 8-bit timer operates in accordance with the priorities for the output states set for compare-match A and compare-match B, as shown in table 10.4.

Table 10.4 Timer Output Priorities

Output Setting	Priority
Toggle output	High
1 output	
0 output	
No change	Low

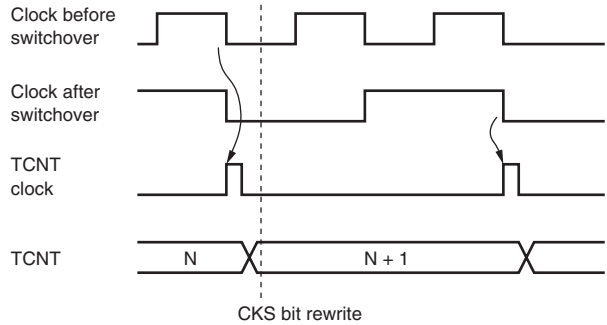
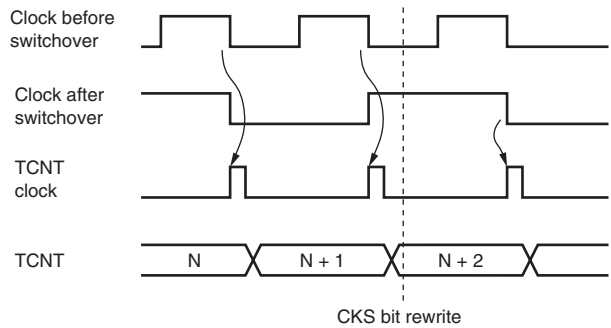
10.8.5 Switching of Internal Clocks and TCNT Operation

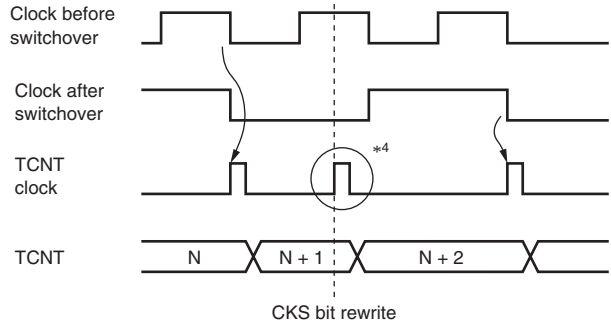
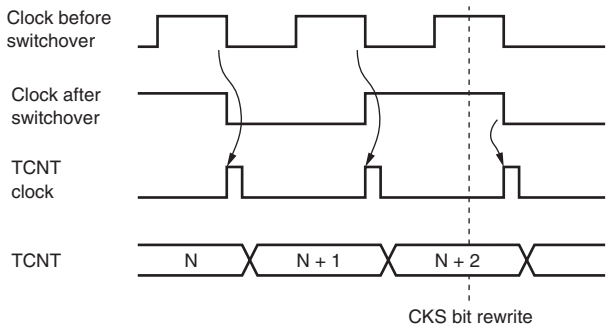
TCNT may increment erroneously when internal clocks are switched. Table 10.5 shows the relationship between the timing at which internal clocks are switched (by writing to the CKS1 and CKS0 bits) and the TCNT operation.

When the TCNT clock is generated from an internal clock, the falling edge of the internal clock pulse is always monitored. If the signal levels of the clocks before and after switching change from high to low as shown in item 3, the change is considered as the falling edge. Therefore, a TCNT clock pulse is generated and TCNT is incremented.

The erroneous incrementation of TCNT can also happen when switching between internal and external clocks.

Table 10.5 Switching of Internal Clocks and TCNT Operation

No.	Timing of Changing Signal Levels by CKS1 and CKS0	TCNT Clock Operation
1	Signal level switching from low to low level*[1]	
2	Signal level switching from low to high level*[2]	

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
3	Signal level switching from high to low level*3	
4	Signal level switching from high to high level	

Notes: 1. Includes switching from low to stop, and from stop to low.
2. Includes switching from stop to high.
3. Includes switching from high to stop.
4. Generated on the assumption that the switchover is a falling edge; TCNT is incremented.

10.8.6 Mode Setting with Cascaded Connection

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1 are not generated, and thus the counters will stop operating. Simultaneous setting of these two modes should therefore be avoided.

10.8.7 Module Stop Mode Setting

TMR operation can be enabled or disabled using the module stop control register. The initial setting is for TMR operation to be halted. Register access is enabled by canceling the module stop mode. For details, refer to section 18, Power-Down Modes.

Section 11 Watchdog Timer (WDT)

This LSI incorporates two watchdog timer channels (WDT_0 and WDT_1). The watchdog timer can generate an internal reset signal or an internal NMI interrupt signal if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow. Simultaneously, it can output an overflow signal ($\overline{\text{RESO}}$) externally.

When this watchdog function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows. A block diagram of the WDT_0 and WDT_1 is shown in figure 11.1.

11.1 Features

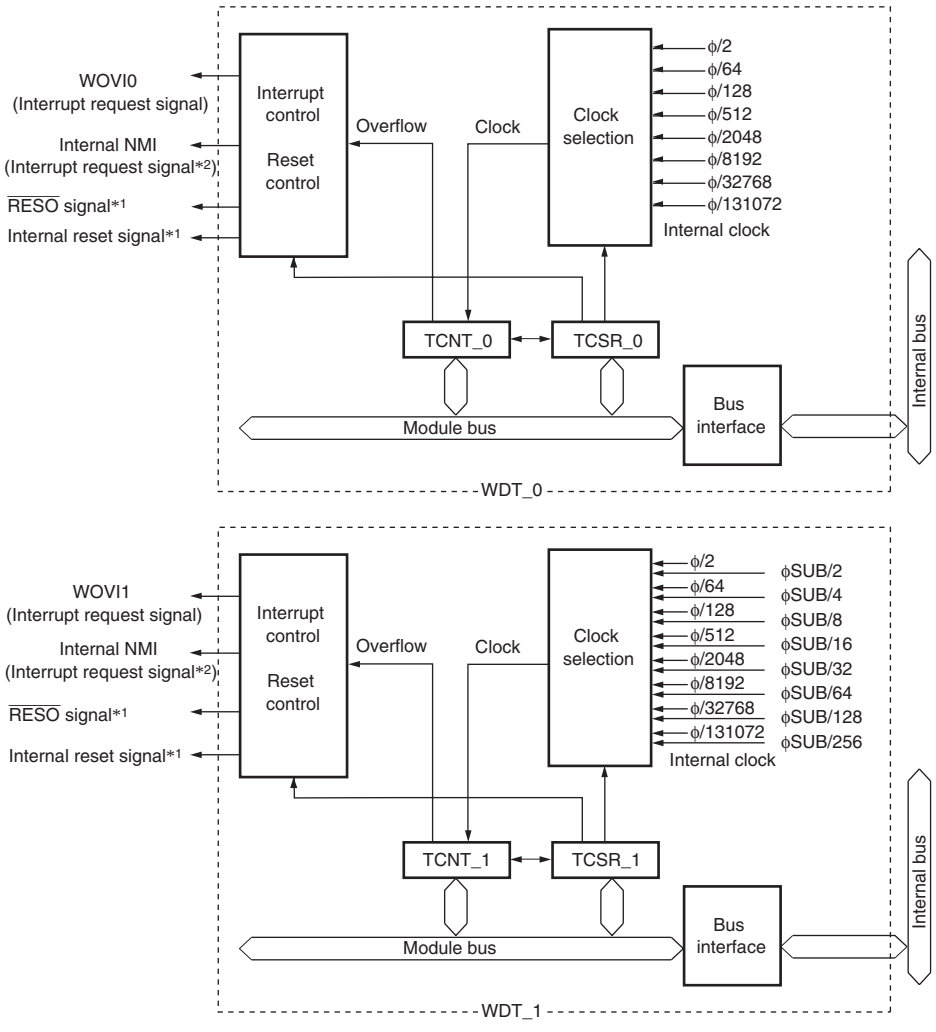
- Selectable from eight (WDT_0) or 16 (WDT_1) counter input clocks.
- Switchable between watchdog timer mode and interval timer mode

Watchdog Timer Mode:

- If the counter overflows, an internal reset or an internal NMI interrupt is generated.
- When the LSI is selected to be internally reset at counter overflow, a low level signal is output from the $\overline{\text{RESO}}$ pin if the counter overflows. (Available only for the H8S/2144B.)

Internal Timer Mode:

- If the counter overflows, an internal timer interrupt (WOVI) is generated.



[Legend]

TCSR_0: Timer control/status register_0
TCNT_0: Timer counter_0
TCSR_1: Timer control/status register_1
TCNT_1: Timer counter_1

Notes: 1. The RESO signal outputs the low level signal when the internal reset signal is generated due to a TCNT overflow of either WDT_0 or WDT_1. The internal reset signal first resets the WDT in which the overflow has occurred first. [H8S/2144B]

2. The internal NMI interrupt signal can be independently output from either WDT_0 or WDT_1. The interrupt controller does not distinguish the NMI interrupt request from WDT_0 from that from WDT_1.

Figure 11.1 Block Diagram of WDT

11.2 Input/Output Pins

The WDT has the pins listed in table 11.1.

Table 11.1 Pin Configuration

Name	Symbol	I/O	Function
Reset output pin	$\overline{\text{RESO}}$	Output	Outputs the counter overflow signal in watchdog timer mode (Available only for the H8S/2144B)
External sub-clock input pin	EXCL	Input	Inputs the clock pulses to the WDT_1 prescaler counter

11.3 Register Descriptions

The WDT has the following registers. To prevent accidental overwriting, TCSR and TCNT have to be written to in a method different from normal registers. For details, refer to section 11.6.1, Notes on Register Access. For details on the system control register, refer to section 3.2.2, System Control Register (SYSCR).

- Timer counter (TCNT)
- Timer control/status register (TCSR)

11.3.1 Timer Counter (TCNT)

TCNT is an 8-bit readable/writable up-counter.

TCNT is initialized to H'00 when the TME bit in the timer control/status register (TCSR) is cleared to 0.

11.3.2 Timer Control/Status Register (TCSR)

TCSR selects the clock source to be input to TCNT, and the timer mode.

- TCSR_0

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting condition] When TCNT overflows (changes from H'FF to H'00) However, when internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] • When TCSR is read when OVF = 1*[2], then 0 is written to OVF • When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
4	—	0	R/(W)	Reserved The initial value should not be modified.
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested

Bit	Bit Name	Initial Value	R/W	Description
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	Selects the clock source to be input to. The overflow frequency for ϕ = 10 MHz is enclosed in parentheses.
0	CKS0	0	R/W	000: ϕ/2 (frequency: 51.2 μs)
				001: ϕ/64 (frequency: 1.64 ms)
				010: ϕ/128 (frequency: 3.28 ms)
				011: ϕ/512 (frequency: 13.1 ms)
				100: ϕ/2048 (frequency: 52.4 ms)
				101: ϕ/8192 (frequency: 209.7 ms)
				110: ϕ/32768 (frequency: 0.84 s)
				111: ϕ/131072 (frequency: 3.36 s)

Notes: 1. Only 0 can be written, to clear the flag.
2. When OVF is polled with the interval timer interrupt disabled, OVF = 1 must be read at least twice.

- TCSR_1

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*[1]	Overflow Flag Indicates that TCNT has overflowed (changes from H'FF to H'00). [Setting condition] When TCNT overflows (changes from H'FF to H'00) However, when internal reset request generation is selected in watchdog timer mode, OVF is cleared automatically by the internal reset. [Clearing conditions] When TCSR is read when OVF = 1*[2], then 0 is written to OVF When 0 is written to TME
6	WT/$\overline{IT}$	0	R/W	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Interval timer mode 1: Watchdog timer mode
5	TME	0	R/W	Timer Enable When this bit is set to 1, TCNT starts counting. When this bit is cleared, TCNT stops counting and is initialized to H'00.
4	PSS	0	R/W	Prescaler Select Selects the clock source to be input to TCNT. 0: Counts the divided cycle of ϕ–based prescaler (PSM) 1: Counts the divided cycle of ϕSUB–based prescaler (PSS)
3	RST/$\overline{NMI}$	0	R/W	Reset or NMI Selects to request an internal reset or an NMI interrupt when TCNT has overflowed. 0: An NMI interrupt is requested 1: An internal reset is requested

Bit	Bit Name	Initial Value	R/W	Description
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	Selects the clock source to be input to TCNT. The overflow cycle for ϕ = 10 MHz and ϕSUB = 32.768 kHz is enclosed in parentheses.
0	CKS0	0	R/W	
				When PSS = 0:
				000: ϕ/2 (frequency: 51.2 μs)
				001: ϕ/64 (frequency: 1.64 ms)
				010: ϕ/128 (frequency: 3.28 ms)
				011: ϕ/512 (frequency: 13.1 ms)
				100: ϕ/2048 (frequency: 52.4 ms)
				101: ϕ/8192 (frequency: 209.7 ms)
				110: ϕ/32768 (frequency: 0.84 s)
				111: ϕ/131072 (frequency: 3.36 s)
				When PSS = 1:
				000: ϕSUB/2 (cycle: 15.6 ms)
				001: ϕSUB/4 (cycle: 31.3 ms)
				010: ϕSUB/8 (cycle: 62.5 ms)
				011: ϕSUB/16 (cycle: 125 ms)
				100: ϕSUB/32 (cycle: 250 ms)
				101: ϕSUB/64 (cycle: 500 ms)
				110: ϕSUB/128 (cycle: 1 s)
				111: ϕ/256 (cycle: 2 s)

Notes: 1. Only 0 can be written, to clear the flag.
2. When OVF is polled with the interval timer interrupt disabled, OVF = 1 must be read at least twice.

11.4 Operation

11.4.1 Watchdog Timer Mode

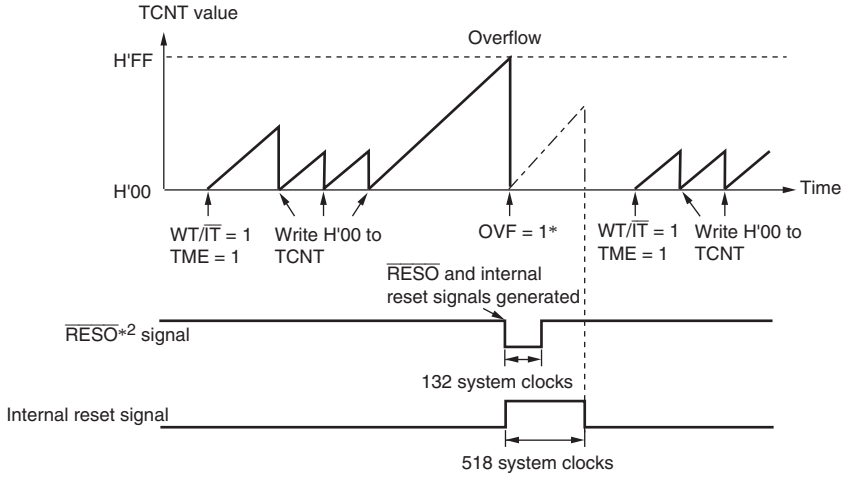
To use the WDT as a watchdog timer, set the WT/$\overline{\text{IT}}$ bit and the TME bit in TCSR to 1. While the WDT is used as a watchdog timer, if TCNT overflows without being rewritten because of a system malfunction or another error, an internal reset or NMI interrupt request is generated. TCNT does not overflow while the system is operating normally. Software must prevent TCNT overflows by rewriting the TCNT value (normally be writing H'00) before overflows occurs.

If the RST/$\overline{\text{NMI}}$ bit of TCSR is set to 1, when the TCNT overflows, an internal reset signal for this LSI is issued for 518 system clocks, and the low level signal is simultaneously output from the $\overline{\text{RESO}}$ pin for 132 states, as shown in figure 11.2. If the RST/$\overline{\text{NMI}}$ bit is cleared to 0, when the TCNT overflows, an NMI interrupt request is generated. Here, the output from the $\overline{\text{RESO}}$ pin remains high.

An internal reset request from the watchdog timer and a reset input from the $\overline{\text{RES}}$ pin are processed in the same vector. Reset source can be identified by the XRST bit status in SYSCR. If a reset caused by a signal input to the $\overline{\text{RES}}$ pin occurs at the same time as a reset caused by a WDT overflow, the $\overline{\text{RES}}$ pin reset has priority and the XRST bit in SYSCR is set to 1.

An NMI interrupt request from the watchdog timer and an interrupt request from the NMI pin are processed in the same vector. Do not handle an NMI interrupt request from the watchdog timer and an interrupt request from the NMI pin at the same time.

Note: * The $\overline{\text{RESO}}$ pin is available only for the H8S/2144B.



[Legend]

WT/$\overline{IT}$: Timer mode select bit
TME: Timer enable bit
OVF: Overflow flag

Notes: 1. After the OVF bit becomes 1, it is cleared to 0 by an internal reset. The XRST bit is also cleared to 0.
2. Available only for the H8S/2144B.

Figure 11.2 Watchdog Timer Mode (RST/$\overline{NMI}$ = 1) Operation

11.4.2 Interval Timer Mode

When the WDT is used as an interval timer, an interval timer interrupt (WOVI) is generated each time the TCNT overflows, as shown in figure 11.3. Therefore, an interrupt can be generated at intervals.

When the TCNT overflows in interval timer mode, an interval timer interrupt (WOVI) is requested at the same time the OVF bit of TCSR is set to 1. The timing is shown figure 11.4.

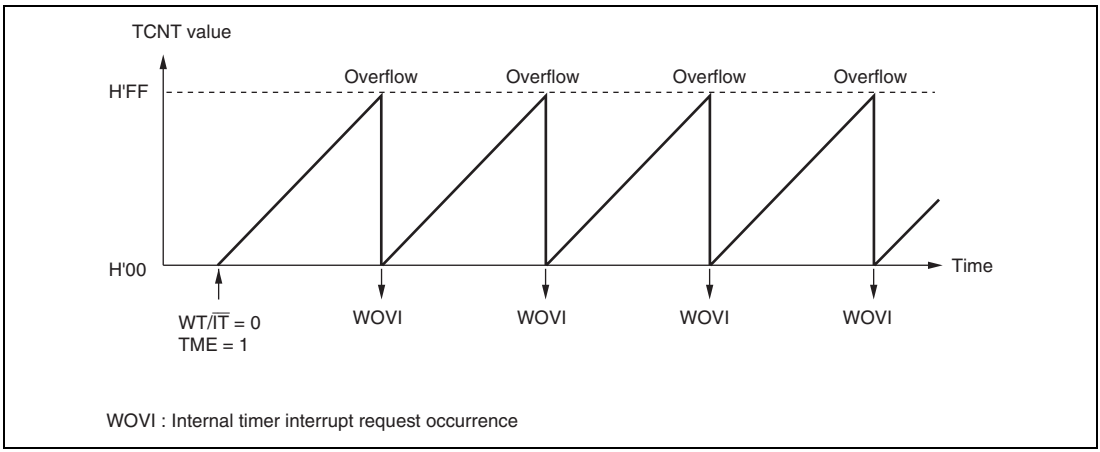


Figure 11.3 Interval Timer Mode Operation

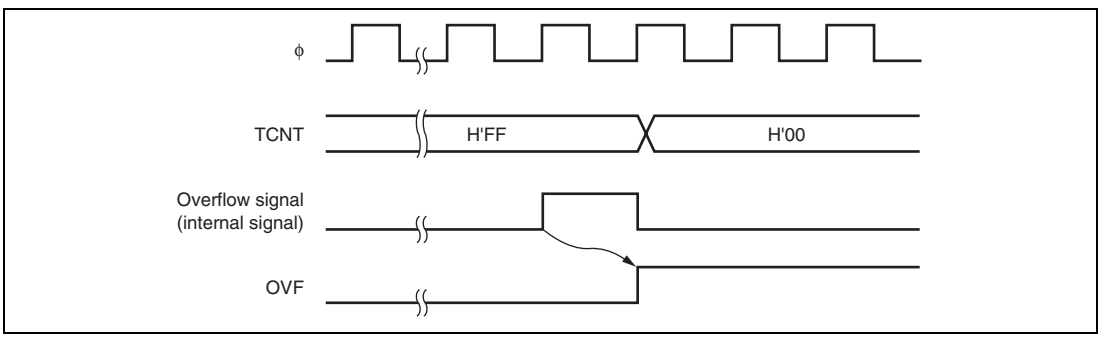


Figure 11.4 OVF Flag Set Timing

11.4.3 $\overline{\text{RESO}}$ Signal Output Timing (Available for H8S/2144B)

When TCNT overflows in watchdog timer mode, the OVF bit in TCSR is set to 1. When the RST/$\overline{\text{NMI}}$ bit is 1 here, the internal reset signal is generated for the entire LSI. At the same time, the low level signal is output from the $\overline{\text{RESO}}$ pin. The timing is shown in figure 11.5.

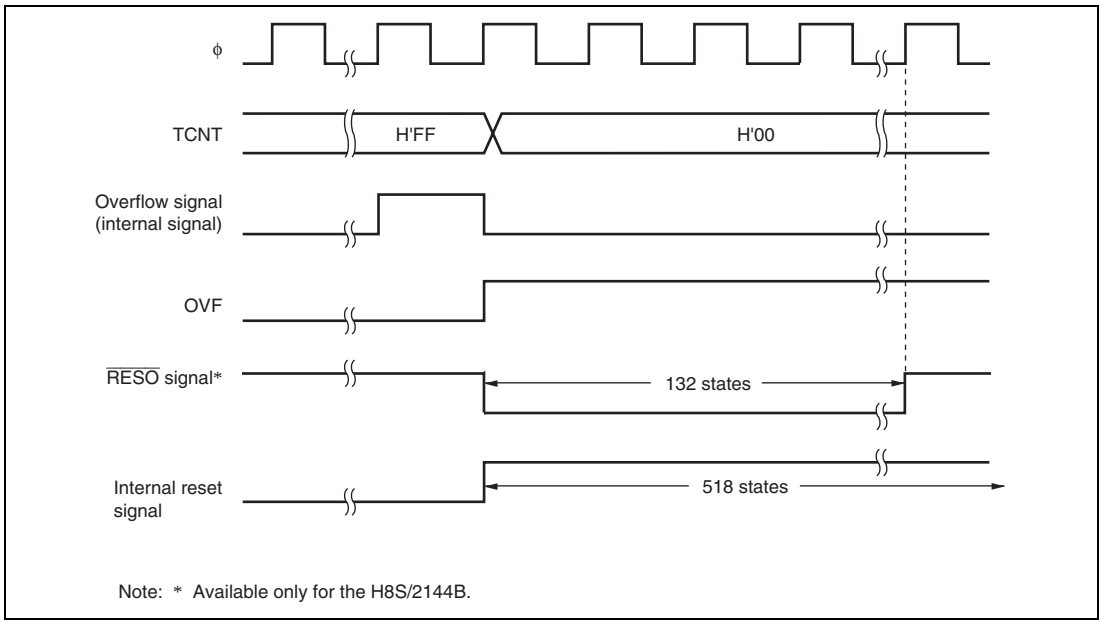


Figure 11.5 Output Timing of $\overline{\text{RESO}}$ signal

11.5 Interrupt Sources

During interval timer mode operation, an overflow generates an interval timer interrupt (WOVI). The interval timer interrupt is requested whenever the OVF flag is set to 1 in TCSR. OVF must be cleared to 0 in the interrupt handling routine.

When the NMI interrupt request is selected in watchdog timer mode, an NMI interrupt request is generated by an overflow.

Table 11.2 WDT Interrupt Source

Name	Interrupt Source	Interrupt Flag
WOVI	TCNT overflow	OVF

11.6 Usage Notes

11.6.1 Notes on Register Access

The watchdog timer's registers, TCNT and TCSR differ from other registers in being more difficult to write to. The procedures for writing to and reading from these registers are given below.

Writing to TCNT and TCSR (Example of WDT_0): These registers must be written to by a word transfer instruction. They cannot be written to by a byte transfer instruction.

TCNT and TCSR both have the same write address. Therefore, satisfy the relative condition shown in figure 11.6 to write to TCNT or TCSR. To write to TCNT, the upper bytes must contain the value H'5A and the lower bytes must contain the write data before the transfer instruction execution. To write to TCSR, the upper bytes must contain the value H'A5 and the lower bytes must contain the write data.

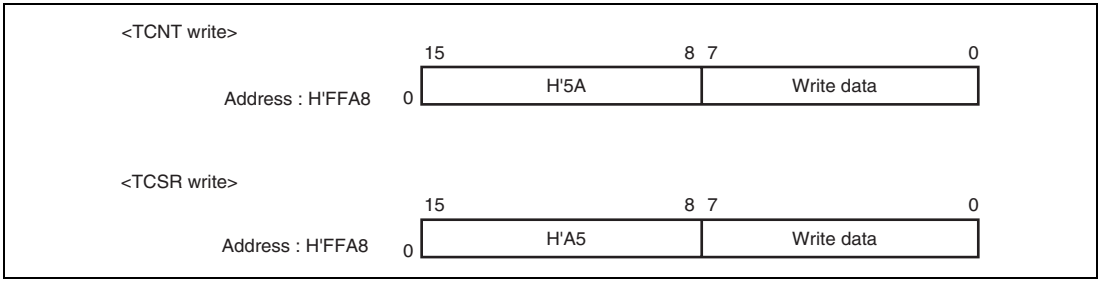


Figure 11.6 Writing to TCNT and TCSR (WDT_0)

Reading from TCNT and TCSR (Example of WDT_0): These registers are read in the same way as other registers. The read address is H'FFA8 for TCSR and H'FFA9 for TCNT.

11.6.2 Conflict between Timer Counter (TCNT) Write and Increment

If a timer counter clock pulse is generated during the T2 state of a TCNT write cycle, the write takes priority and the timer counter is not incremented. Figure 11.7 shows this operation.

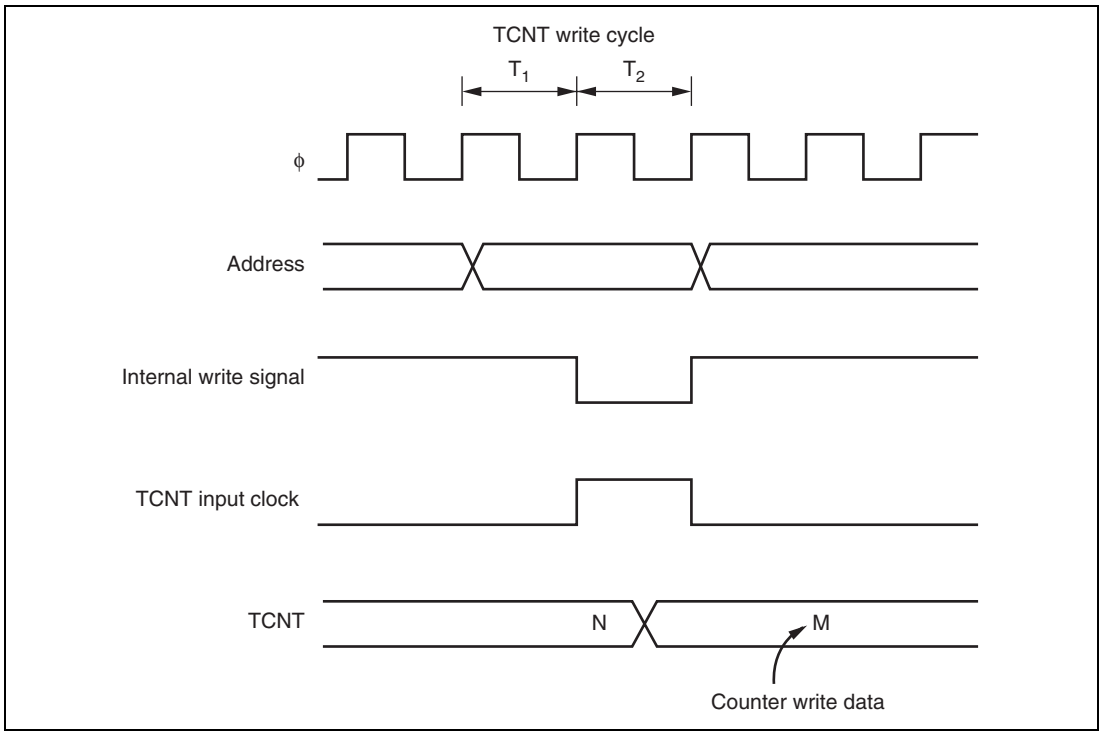


Figure 11.7 Conflict between TCNT Write and Increment

11.6.3 Changing Values of CKS2 to CKS0 Bits

If bits CKS2 to CKS0 in TCSR are written to while the WDT is operating, errors could occur in the incrementation. Software must stop the watchdog timer (by clearing the TME bit to 0) before changing the values of bits CKS2 to CKS0.

11.6.4 Switching between Watchdog Timer Mode and Interval Timer Mode

If the mode is switched from watchdog timer to interval timer, while the WDT is operating, errors could occur in the incrementation. Software must stop the watchdog timer (by clearing the TME bit to 0) before switching the mode.

11.6.5 System Reset by $\overline{\text{RESO}}$ Signal (Available for H8S/2144B)

Inputting the $\overline{\text{RESO}}$ output signal to the $\overline{\text{RESO}}$ pin of this LSI prevents the LSI from being initialized correctly; the $\overline{\text{RESO}}$ signal must not be logically connected to the $\overline{\text{RES}}$ pin of the LSI. To reset the entire system by the $\overline{\text{RESO}}$ signal, use the circuit as shown in figure 11.8.

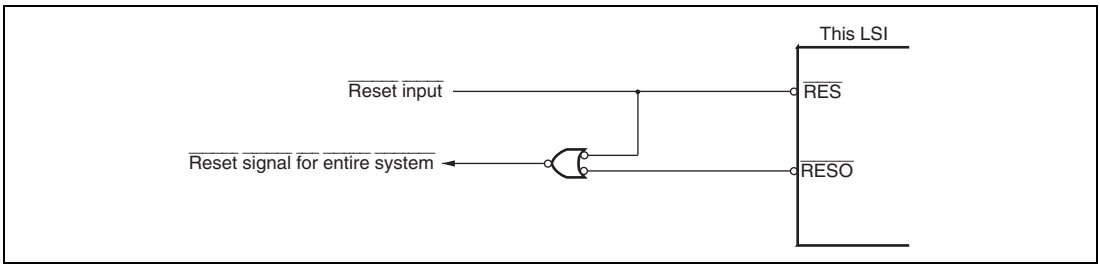


Figure 11.8 Sample Circuit for Resetting System by $\overline{\text{RESO}}$ Signal

11.6.6 Counter Values during Transitions between High-Speed, Sub-Active, and Watch Modes

When WDT_1 is used as a clock counter and is allowed to transit between high-speed mode and sub-active or watch mode, the counter does not display the correct value due to internal clock switching.

Specifically, when transiting from high-speed mode to sub-active or watch mode, that is, when the control clock for WDT_1 switches from the main clock to the sub-clock, the counter incrementing timing is delayed for approximately two to three clock cycles.

Similarly, when transiting from sub-active or watch mode to high-speed mode, the clock is not supplied until stabilized internal oscillation is available because the main clock oscillator is halted in sub-clock mode. The counter is therefore prevented from incrementing for the time specified by the STS2 to STS0 bits in SBYCR after internal oscillation starts, thus producing counter value differences for this time.

Special care must be taken when using WDT_1 as a clock counter. Note that no counter value difference is produced while operated in the same mode.

Section 12 Serial Communication Interface (SCI and IrDA)

This LSI has three independent serial communication interface (SCI) channels. The SCI can handle both asynchronous and clock synchronous serial communication. Asynchronous serial data communication can be carried out with standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). A function is also provided for serial communication between processors (multiprocessor communication function) in asynchronous mode.

SCI_2 can handle communication using the waveform based on the Infrared Data Association (IrDA) standard version 1.0.

12.1 Features

- Choice of asynchronous or clock synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously. Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception of serial data.
- The on-chip baud rate generator allows any bit rate to be selected

  An external clock can be selected as a transfer clock source.
- Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

  Four interrupt sources — transmit-end, transmit-data-empty, receive-data-full, and receive error

Asynchronous Mode:

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RxD pin level directly in case of a framing error

Clock Synchronous Mode:

- Data length: 8 bits
- Receive error detection: Overrun errors
- Serial data communication with other LSIs that have the clock synchronized communication function

A block diagram of the SCI is shown in figure 12.1.

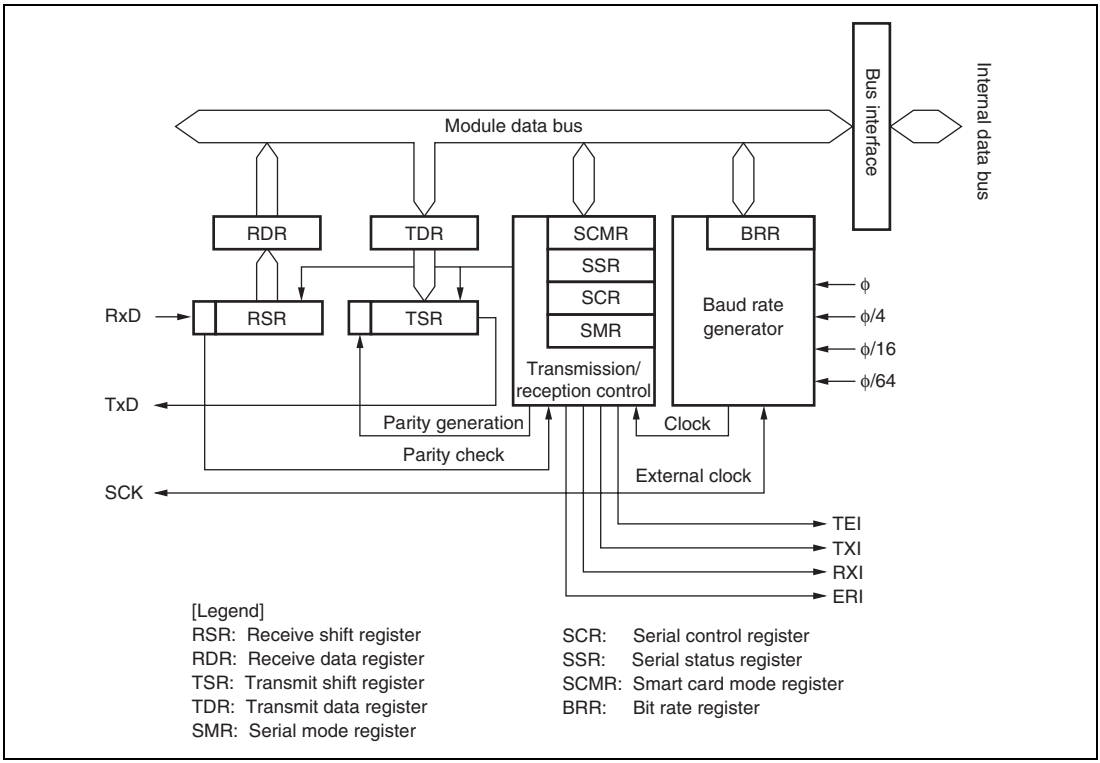


Figure 12.1 Block Diagram of SCI

12.2 Input/Output Pins

Table 12.1 shows the input/output pins for each SCI channel.

Table 12.1 Pin Configuration

Channel	Symbol*	Input/Output	Function
0	SCK0	Input/Output	Channel 0 clock input/output
	RxD0	Input	Channel 0 receive data input
	TxD0	Output	Channel 0 transmit data output
1	SCK1	Input/Output	Channel 1 clock input/output
	RxD1	Input	Channel 1 receive data input
	TxD1	Output	Channel 1 transmit data output
2	SCK2	Input/Output	Channel 2 clock input/output
	RxD2/IrRxD	Input	Channel 2 receive data input (normal/IrDA)
	TxD2/IrTxD	Output	Channel 2 transmit data output (normal/IrDA)

Note * Pin names SCK, RxD, and TxD are used in the text for all channels, omitting the channel designation.

12.3 Register Descriptions

The SCI has the following registers for each channel.

- Receive shift register (RSR)
- Receive data register (RDR)
- Transmit data register (TDR)
- Transmit shift register (TSR)
- Serial mode register (SMR)
- Serial control register (SCR)
- Serial status register (SSR)
- Serial interface mode register (SCMR)
- Bit rate register (BRR)
- Keyboard comparator control register (KBCOMP)

12.3.1 Receive Shift Register (RSR)

RSR is a shift register used to receive serial data that converts it into parallel data. When one frame of data has been received, it is transferred to RDR automatically. RSR cannot be directly accessed by the CPU.

12.3.2 Receive Data Register (RDR)

RDR is an 8-bit register that stores receive data. When the SCI has received one frame of serial data, it transfers the received serial data from RSR to RDR where it is stored. After this, RSR can receive the next data. Since RSR and RDR function as a double buffer in this way, continuous receive operations can be performed. After confirming that the RDRF bit in SSR is set to 1, read RDR for only once. RDR cannot be written to by the CPU. RDR is initialized to H'00.

12.3.3 Transmit Data Register (TDR)

TDR is an 8-bit register that stores transmit data. When the SCI detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission. The double-buffered structures of TDR and TSR enables continuous serial transmission. If the next transmit data has already been written to TDR when one frame of data is transmitted, the SCI transfers the written data to TSR to continue transmission. Although TDR can be read from or written to by the CPU at all times, to achieve reliable serial transmission, write transmit data to TDR for only once after confirming that the TDRE bit in SSR is set to 1. TDR is initialized to H'FF.

12.3.4 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first transfers transmit data from TDR to TSR, then sends the data to the TxD pin. TSR cannot be directly accessed by the CPU.

12.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI's serial transfer format and select the on-chip baud rate generator clock source.

Bit	Bit Name	Initial Value	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length. LSB-first is fixed and the MSB of TDR is not transmitted in transmission. In clock synchronous mode, a fixed data length of 8 bits is used.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. For a multiprocessor format, parity bit addition and checking are not performed regardless of the PE bit setting.
4	O/$\overline{E}$	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first stop bit is checked. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

Bit	Bit Name	Initial Value	R/W	Description
2	MP	0	R/W	Multiprocessor Mode (enabled only in asynchronous mode) When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and O/$\overline{E}$ bit settings are invalid in multiprocessor mode.
1	CKS1	0	R/W	Clock Select 1,0
0	CKS0	0	R/W	These bits select the clock source for the on-chip baud rate generator. 00: ϕ clock (n = 0) 01: ϕ/4 clock (n = 1) 10: ϕ/16 clock (n = 2) 11: ϕ/64 clock (n = 3) For the relation between the bit rate register setting and the baud rate, see section 12.3.9, Bit Rate Register (BRR). n is the decimal display of the value of n in BRR.

12.3.6 Serial Control Register (SCR)

SCR is a register that performs enabling or disabling of SCI transfer operations and interrupt requests, and selection of the transfer clock source. For details on interrupt requests, refer to section 12.8, Interrupt Sources.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt requests are enabled.
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and ORER status flags in SSR is disabled. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. For details, refer to section 12.5, Multiprocessor Communication Function.
2	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, a TEI interrupt request is enabled.

Bit	Bit Name	Initial Value	R/W	Description
1	CKE1	0	R/W	Clock Enable 1, 0
0	CKE0	0	R/W	These bits select the clock source and SCK pin function. Asynchronous mode 00: Internal clock (SCK pin functions as I/O port.) 01: Internal clock (Outputs a clock of the same frequency as the bit rate from the SCK pin.) 1X: External clock (Inputs a clock with a frequency 16 times the bit rate from the SCK pin.) Clock synchronous mode 0X: Internal clock (SCK pin functions as clock output.) 1X: External clock (SCK pin functions as clock input.)

[Legend]

X: Don't care

12.3.7 Serial Status Register (SSR)

SSR is a register containing status flags of the SCI and multiprocessor bits for transfer. TDRE, RDRF, ORER, PER, and FER can only be cleared.

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	1	R/(W)*	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and TDR is ready for data write [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates that receive data is stored in RDR. [Setting condition] • When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 The RDRF flag is not affected and retains its previous value when the RE bit in SCR is cleared to 0.
5	ORER	0	R/(W)*	Overrun Error [Setting condition] • When the next data is received while RDRF = 1 [Clearing condition] • When 0 is written to ORER after reading ORER = 1

Bit	Bit Name	Initial Value	R/W	Description
4	FER	0	R/(W)*	Framing Error [Setting condition] • When the stop bit is 0 [Clearing condition] • When 0 is written to FER after reading FER = 1 In 2-stop-bit mode, only the first stop bit is checked.
3	PER	0	R/(W)*	Parity Error [Setting condition] • When a parity error is detected during reception [Clearing condition] • When 0 is written to PER after reading PER = 1
2	TEND	1	R	Transmit End [Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1
1	MPB	0	R	Multiprocessor Bit MPB stores the multiprocessor bit in the receive frame. When the RE bit in SCR is cleared to 0 its previous state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT stores the multiprocessor bit to be added to the transmit frame.

Note: * Only 0 can be written, to clear the flag.

12.3.8 Serial Interface Mode Register (SCMR)

SCMR selects SCI functions and its format.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	R	Reserved These bits are always read as 1 and cannot be modified.
3	SDIR	0	R/W	Data Transfer Direction Selects the serial/parallel conversion format. 0: TDR contents are transmitted with LSB-first. Receive data is stored as LSB first in RDR. 1: TDR contents are transmitted with MSB-first. Receive data is stored as MSB first in RDR. The SDIR bit is valid only when the 8-bit data format is used for transmission/reception; when the 7-bit data format is used, data is always transmitted/received with LSB-first.
2	SINV	0	R/W	Data Invert Specifies inversion of the data logic level. The SINV bit does not affect the logic level of the parity bit. When the parity bit is inverted, invert the O/$\overline{E}$ bit in SMR. 0: TDR contents are transmitted as they are. Receive data is stored as it is in RDR. 1: TDR contents are inverted before being transmitted. Receive data is stored in inverted form in RDR.
1	—	1	R	Reserved This bit is always read as 1 and cannot be modified.
0	SMIF	0	R/W	Serial Communication Interface Mode Select: 0: Normal asynchronous or clock synchronous mode 1: Reserved mode

12.3.9 Bit Rate Register (BRR)

BRR is an 8-bit register that adjusts the bit rate. As the SCI performs baud rate generator control independently for each channel, different bit rates can be set for each channel. Table 12.2 shows the relationships between the N setting in BRR and bit rate B for normal asynchronous mode and clock synchronous mode. The initial value of BRR is H'FF, and it can be read from or written to by the CPU at all times.

Table 12.2 Relationships between N Setting in BRR and Bit Rate B

Mode	Bit Rate	Error
Asynchronous mode	$B = \frac{\phi \times 10^6}{64 \times 2^{2n-1} \times (N+1)}$	$\text{Error (\%)} = \{ \frac{\phi \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1 \} \times 100$
Clock synchronous mode	$B = \frac{\phi \times 10^6}{64 \times 2^{2n-1} \times (N+1)}$	—

[Legend]

B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

ϕ: Operating frequency (MHz)

n: Determined by the SMR settings shown in the following table.

SMR Setting

CKS1	CKS0	n
0	0	0
0	1	1
1	0	2
1	1	3

Table 12.3 shows sample N settings in BRR in normal asynchronous mode. Table 12.4 shows the maximum bit rate settable for each frequency. Table 12.6 shows sample N settings in BRR in clock synchronous mode. Tables 12.5 and 12.7 show the maximum bit rates with external clock input.

Table 12.3 BRR Settings for Various Bit Rates (Asynchronous Mode)

	Operating Frequency ϕ (MHz)											
	2			2.097152			2.4576			3		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	–0.04	1	174	–0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	–0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	–2.48	0	15	0.00	0	19	–2.34
9600	—	—	—	0	6	–2.48	0	7	0.00	0	9	–2.34
19200	—	—	—	—	—	—	0	3	0.00	0	4	–2.34
31250	0	1	0.00	—	—	—	—	—	—	0	2	0.00
38400	—	—	—	—	—	—	0	1	0.00	—	—	—

	Operating Frequency ϕ (MHz)											
	3.6864			4			4.9152			5		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	64	0.70	2	70	0.03	2	86	0.31	2	88	–0.25
150	1	191	0.00	1	207	0.16	1	255	0.00	2	64	0.16
300	1	95	0.00	1	103	0.16	1	127	0.00	1	129	0.16
600	0	191	0.00	0	207	0.16	0	255	0.00	1	64	0.16
1200	0	95	0.00	0	103	0.16	0	127	0.00	0	129	0.16
2400	0	47	0.00	0	51	0.16	0	63	0.00	0	64	0.16
4800	0	23	0.00	0	25	0.16	0	31	0.00	0	32	–1.36
9600	0	11	0.00	0	12	0.16	0	15	0.00	0	15	1.73
19200	0	5	0.00	—	—	—	0	7	0.00	0	7	1.73
31250	—	—	—	0	3	0.00	0	4	–1.70	0	4	0.00
38400	0	2	0.00	—	—	—	0	3	0.00	0	3	1.73

[Legend]

—: Can be set, but there will be a degree of error.

Note: * Make the settings so that the error does not exceed 1%.

	Operating Frequency ϕ (MHz)											
	6			6.144			7.3728			8		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	106	–0.44	2	108	0.08	2	130	–0.07	2	141	0.03
150	2	77	0.16	2	79	0.00	2	95	0.00	2	103	0.16
300	1	155	0.16	1	159	0.00	1	191	0.00	1	207	0.16
600	1	77	0.16	1	79	0.00	1	95	0.00	1	103	0.16
1200	0	155	0.16	0	159	0.00	0	191	0.00	0	207	0.16
2400	0	77	0.16	0	79	0.00	0	95	0.00	0	103	0.16
4800	0	38	0.16	0	39	0.00	0	47	0.00	0	51	0.16
9600	0	19	–2.34	0	19	0.00	0	23	0.00	0	25	0.16
19200	0	9	–2.34	0	9	0.00	0	11	0.00	0	12	0.16
31250	0	5	0.00	0	5	2.40	—	—	—	0	7	0.00
38400	0	4	–2.34	0	4	0.00	0	5	0.00	—	—	—

	Operating Frequency ϕ (MHz)											
	9.8304			10			12			12.288		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

[Legend]

—: Can be set, but there will be a degree of error.

Note: * Make the settings so that the error does not exceed 1%.

	Operating Frequency ϕ (MHz)											
	14			14.7456			16			17.2032		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	64	0.70	3	70	0.03	3	75	0.48
150	2	181	0.16	2	191	0.00	2	207	0.16	2	223	0.00
300	2	90	0.16	2	95	0.00	2	103	0.16	2	111	0.00
600	1	181	0.16	1	191	0.00	1	207	0.16	1	223	0.00
1200	1	90	0.16	1	95	0.00	1	103	0.16	1	111	0.00
2400	0	181	0.16	0	191	0.00	0	207	0.16	0	223	0.00
4800	0	90	0.16	0	95	0.00	0	103	0.16	0	111	0.00
9600	0	45	–0.93	0	47	0.00	0	51	0.16	0	55	0.00
19200	0	22	–0.93	0	23	0.00	0	25	0.16	0	27	0.00
31250	0	13	0.00	0	14	–1.70	0	15	0.00	0	16	1.20
38400	—	—	—	0	11	0.00	0	12	0.16	0	16	0.00

	Operating Frequency ϕ (MHz)								
	18			19.6608			20		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	79	–0.12	3	86	0.31	3	88	–0.25
150	2	233	0.16	2	255	0.00	3	64	0.16
300	2	116	0.16	2	127	0.00	2	129	0.16
600	1	233	0.16	1	255	0.00	2	64	0.16
1200	1	166	0.16	1	127	0.00	1	129	0.16
2400	0	233	0.16	0	255	0.00	1	64	0.16
4800	0	166	0.16	0	127	0.00	0	129	0.16
9600	0	58	–0.69	0	63	0.00	0	64	0.16
19200	0	28	1.02	0	31	0.00	0	32	–1.36
31250	0	17	0.00	0	19	–1.70	0	19	0.00
38400	0	14	–2.34	0	15	0.00	0	15	1.73

[Legend]

—: Can be set, but there will be a degree of error.

Note: * Make the settings so that the error does not exceed 1%.

Table 12.4 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N	ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
2	62500	0	0	9.8304	307200	0	0
2.097152	65536	0	0	10	312500	0	0
2.4576	76800	0	0	12	375000	0	0
3	93750	0	0	12.288	384000	0	0
3.6864	115200	0	0	14	437500	0	0
4	125000	0	0	14.7456	460800	0	0
4.9152	153600	0	0	16	500000	0	0
5	156250	0	0	17.2032	537600	0	0
6	187500	0	0	18	562500	0	0
6.144	192000	0	0	19.6608	614400	0	0
7.3728	230400	0	0	20	625000	0	0
8	250000	0	0				

Table 12.5 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)	ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
2	0.5000	31250	9.8304	2.4576	153600
2.097152	0.5243	32768	10	2.5000	156250
2.4576	0.6144	38400	12	3.0000	187500
3	0.7500	46875	12.288	3.0720	192000
3.6864	0.9216	57600	14	3.5000	218750
4	1.0000	62500	14.7456	3.6864	230400
4.9152	1.2288	76800	16	4.0000	250000
5	1.2500	78125	17.2032	4.3008	268800
6	15.000	93750	18	4.5000	281250
6.144	1.5360	96000	19.6608	4.9152	307200
7.3728	1.8432	115200	20	5.0000	312500
8	2.0000	125000			

Table 12.6 BRR Settings for Various Bit Rates (Clock Synchronous Mode)

Bit Rate (bit/s)	Operating Frequency ϕ (MHz)											
	2		4		8		10		16		20	
	n	N	n	N	n	N	n	N	n	N	n	N
110	3	70	—	—								
250	2	124	2	249	3	124	—	—	3	249		
500	1	249	2	124	2	249	—	—	3	124	—	—
1k	1	124	1	249	2	124	—	—	2	249	—	—
2.5k	0	199	1	99	1	199	1	249	2	99	2	124
5k	0	99	0	199	1	99	1	124	1	199	1	249
10k	0	49	0	99	0	199	0	249	1	99	1	124
25k	0	19	0	39	0	79	0	99	0	159	0	199
50k	0	9	0	19	0	39	0	49	0	79	0	99
100k	0	4	0	9	0	19	0	24	0	39	0	49
250k	0	1	0	3	0	7	0	9	0	15	0	19
500k	0	0*	0	1*	0	3	0	4	0	7	0	9
1M			0	0	0	1			0	3	0	4
2.5M							0	0*			0	1
5M											0	0*

[Legend]

Blank: Cannot be set.

—: Can be set, but there will be a degree of error.

*: Continuous transfer or reception is not possible.

Table 12.7 Maximum Bit Rate with External Clock Input (Clock Synchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)	ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
2	0.3333	333333.3	12	2.0000	2000000.0
4	0.6667	666666.7	14	2.3333	2333333.3
6	1.0000	1000000.0	16	2.6667	2666666.7
8	1.3333	1333333.3	18	3.0000	3000000.0
10	1.6667	1666666.7	20	3.3333	3333333.3

12.3.10 Keyboard Comparator Control Register (KBCOMP)

KBCOMP selects the functions of the SCI and A/D converter.

Bit	Bit Name	Initial Value	R/W	Description
7	IrE	0	R/W	IrDA Enable Specifies SCI_2 I/O pins for either normal SCI or IrDA. 0: TxD2/IrTxD and RxD2/IrRxD pins function as TxD2 and RxD2 pins, respectively 1: TxD2/IrTxD and RxD2/IrRxD pins function as IrTxD and IrRxD pins, respectively
6 5 4	IrCKS2 IrCKS1 IrCKS0	0 0 0	R/W R/W R/W	IrDA Clock Select 2 to 0 These bits specify the high-level width of the clock pulse during IrTxD output pulse encoding when the IrDA function is enabled. 000: B × 3/16 (B: Bit rate) 001: φ /2 010: φ /4 011: φ /8 100: φ /16 101: φ /32 110: φ /64 111: φ /128
3 2 1 0	KBADE KBCH2 KBCH1 KBCH0	0 0 0 0	R/W R/W R/W R/W	Bits related to the A/D converter For details, refer to section 14.3.4, Keyboard Comparator Control Register (KBCOMP).

12.4 Operation in Asynchronous Mode

Figure 12.2 shows the general format for asynchronous serial communication. One frame consists of a start bit (low level), followed by transmit/receive data, a parity bit, and finally stop bits (high level). In asynchronous serial communication, the transmission line is usually held in the mark state (high level). The SCI monitors the transmission line, and when it goes to the space state (low level), recognizes a start bit and starts serial communication. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer and reception.

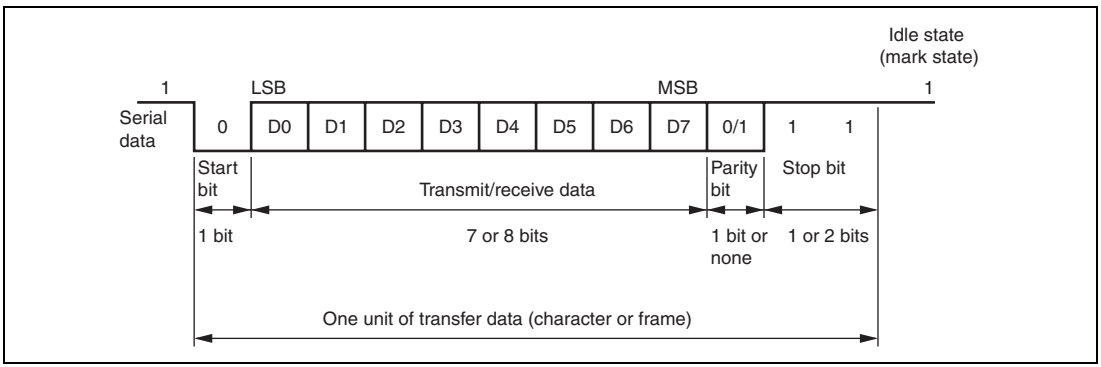


Figure 12.2 Data Format in Asynchronous Communication (Example with 8-Bit Data, Parity, Two Stop Bits)

12.4.1 Data Transfer Format

Table 12.8 shows the data transfer formats that can be used in asynchronous mode. Any of 12 transfer formats can be selected according to the SMR setting. For details on the multiprocessor bit, refer to section 12.5, Multiprocessor Communication Function.

Table 12.8 Serial Transfer Formats (Asynchronous Mode)

SMR Settings				Serial Transmit/Receive Format and Frame Length
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	0	0	S 8-bit data STOP
0	0	0	1	S 8-bit data STOP STOP
0	1	0	0	S 8-bit data P STOP
0	1	0	1	S 8-bit data P STOP STOP
1	0	0	0	S 7-bit data STOP
1	0	0	1	S 7-bit data STOP STOP
1	1	0	0	S 7-bit data P STOP
1	1	0	1	S 7-bit data P STOP STOP
0	—	1	0	S 8-bit data MPB STOP
0	—	1	1	S 8-bit data MPB STOP STOP
1	—	1	0	S 7-bit data MPB STOP
1	—	1	1	S 7-bit data MPB STOP STOP

12.4.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a basic clock with a frequency of 16 times the bit rate. In reception, the SCI samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Since receive data is latched internally at the rising edge of the 8th pulse of the basic clock, data is latched at the middle of each bit, as shown in figure 12.3. Thus the reception margin in asynchronous mode is determined by formula (1) below.

$$M = \{ (0.5 - \frac{1}{2N}) - \frac{D - 0.5}{N} (1 + F) - (L - 0.5) F \} \times 100 \quad [\%] \quad \cdots \quad \text{Formula (1)}$$

M: Reception margin (%)
N : Ratio of bit rate to clock (N = 16)
D : Clock duty (D = 0.5 to 1.0)
L : Frame length (L = 9 to 12)
F : Absolute value of clock rate deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined by the formula below.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100 \quad [\%] = 46.875\ \%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed in system design.

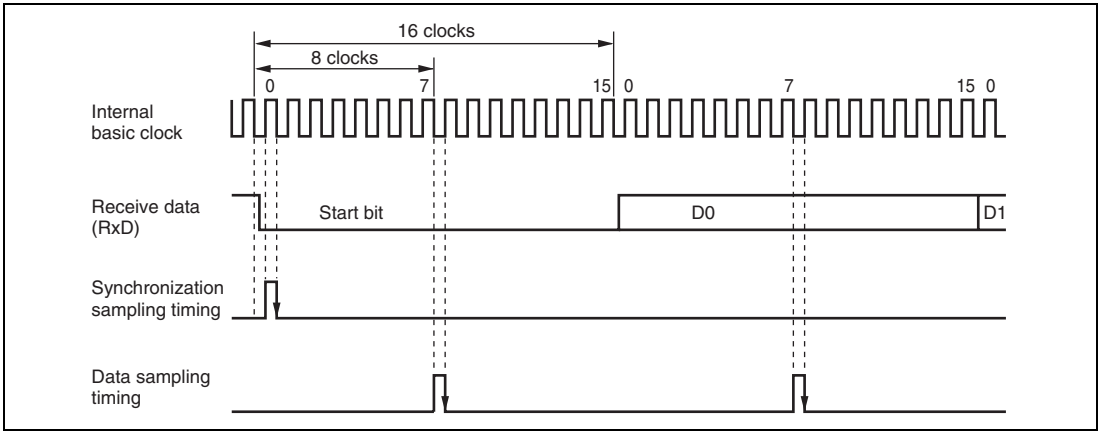


Figure 12.3 Receive Data Sampling Timing in Asynchronous Mode

12.4.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK pin can be selected as the SCI's transfer clock, according to the setting of the C/$\overline{A}$ bit in SMR and the CKE1 and CKE0 bits in SCR. When an external clock is input at the SCK pin, the clock frequency should be 16 times the bit rate used.

When the SCI is operated on an internal clock, the clock can be output from the SCK pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 12.4.

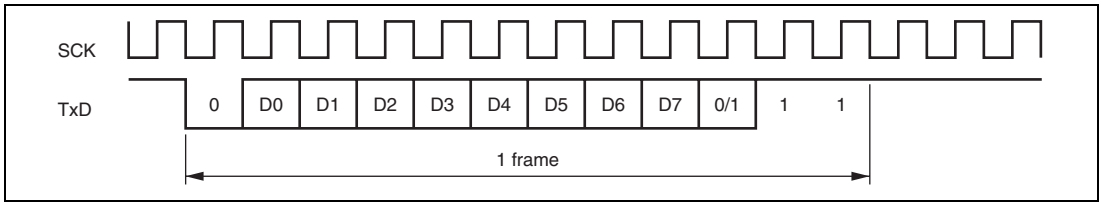
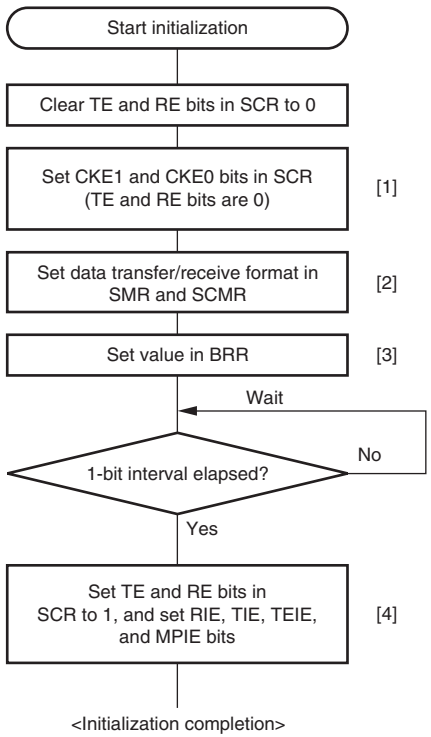


Figure 12.4 Relation between Output Clock and Transmit Data Phase (Asynchronous Mode)

12.4.4 SCI Initialization (Asynchronous Mode)

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as shown in figure 12.5. When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag in SSR is set to 1. Note that clearing the RE bit to 0 does not initialize the contents of the RDRF, PER, FER, and ORER flags in SSR, or the contents of RDR. When an external clock is used in asynchronous mode, the clock must be supplied even during initialization.



[1] Set the clock selection in SCR. Be sure to clear bits RIE, TIE, TEIE, and MPIE, and bits TE and RE, to 0.

When the clock is selected in asynchronous mode, it is output immediately after SCR settings are made.

[2] Set the data transfer/receive format in SMR and SCMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Also set the RIE, TIE, TEIE, and MPIE bits.

Setting the TE and RE bits enables the TxD and RxD pins to be used.

Figure 12.5 Sample SCI Initialization Flowchart

12.4.5 Data Transmission (Asynchronous Mode)

Figure 12.6 shows an example of the operation for transmission in asynchronous mode. In transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in SSR, and if it is cleared to 0, recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit in SCR is set to 1 at this time, a transmit data empty interrupt request (TXI) is generated. Because the TXI interrupt routine writes the next transmit data to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.
3. Data is sent from the TxD pin in the following order: start bit, transmit data, parity bit or multiprocessor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks the TDRE flag at the timing for sending the stop bit.
5. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
6. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the “mark state” is entered in which 1 is output. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated.

Figure 12.7 shows a sample flowchart for transmission in asynchronous mode.

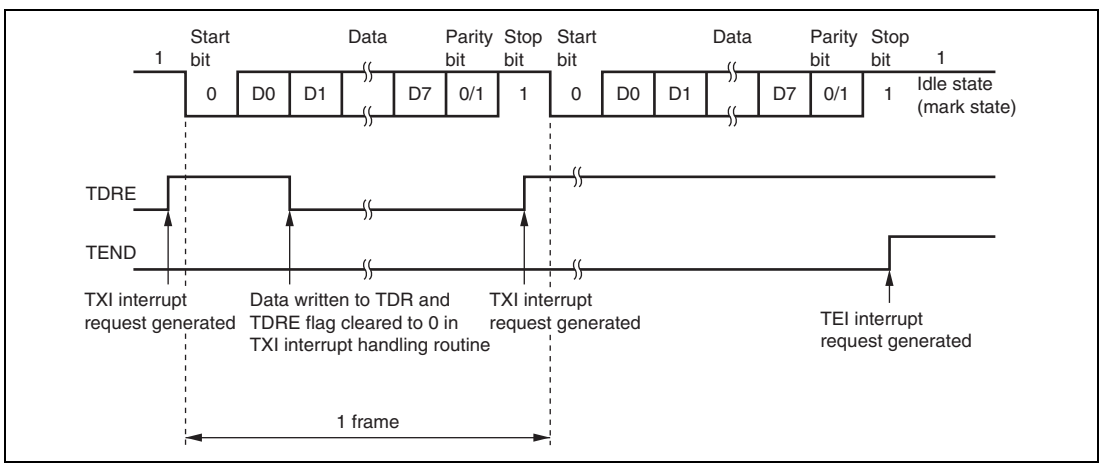
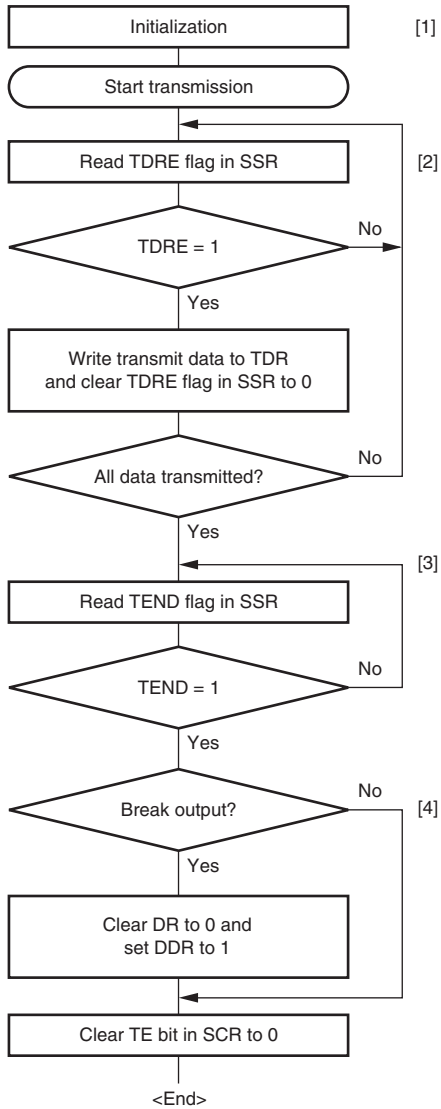


Figure 12.6 Example of SCI Transmit Operation in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, a frame of 1s is output, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:

To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and clear the TDRE flag to 0.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set DDR for the port corresponding to the TxD pin to 1, clear DR to 0, then clear the TE bit in SCR to 0.

Figure 12.7 Sample Serial Transmission Flowchart

12.4.6 Serial Data Reception (Asynchronous Mode)

Figure 12.8 shows an example of the operation for reception in asynchronous mode. In serial reception, the SCI operates as described below.

1. The SCI monitors the communication line, and if a start bit is detected, performs internal synchronization, receives receive data in RSR, and checks the parity bit and stop bit.
2. If an overrun error (when reception of the next data is completed while the RDRF flag in SSR is still set to 1) occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error (when the stop bit is 0) is detected, the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated.
5. If reception finishes successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has finished, continuous reception can be enabled.

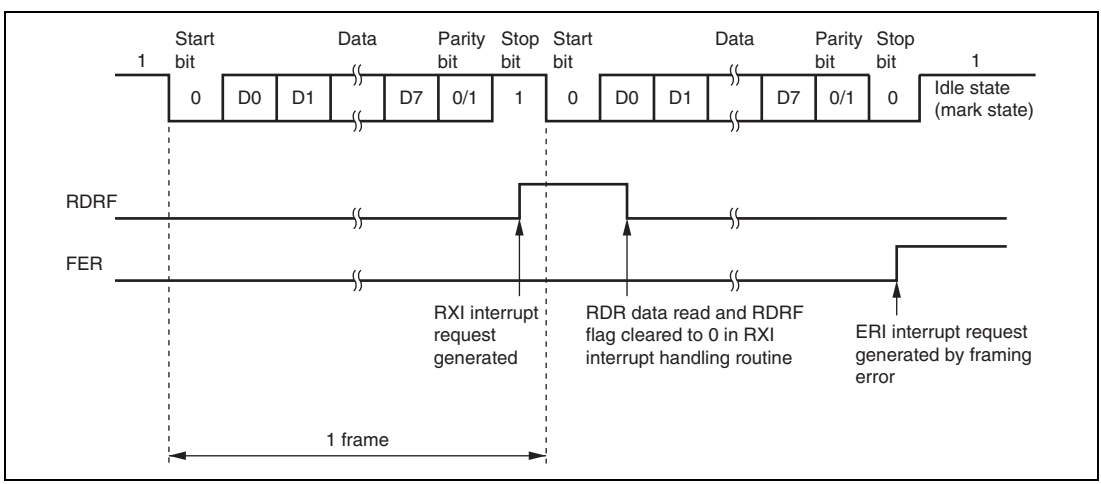


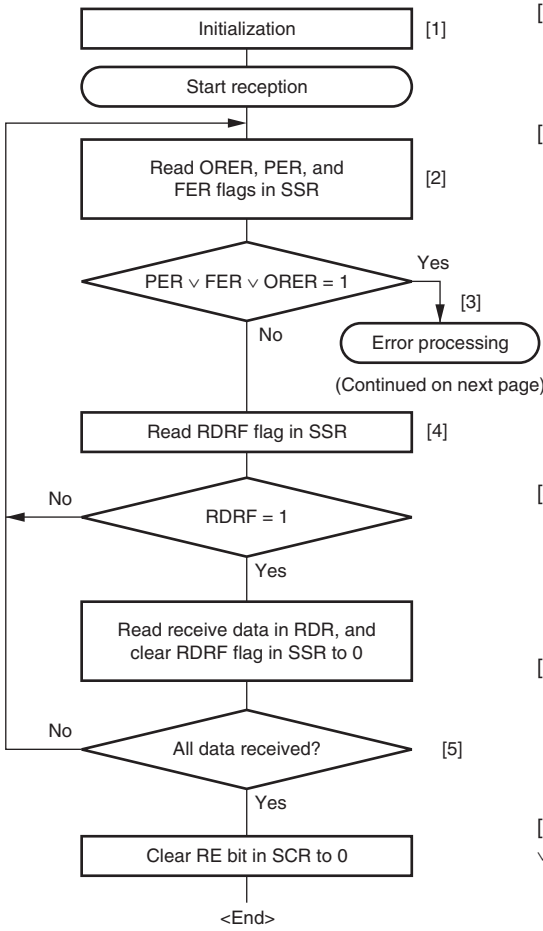
Figure 12.8 Example of SCI Receive Operation in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)

Table 12.9 shows the states of the SSR status flags and receive data handling when a receive error is detected. If a receive error is detected, the RDRF flag retains its state before receiving data. Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 12.9 shows a sample flow chart for serial data reception.

Table 12.9 SSR Status Flags and Receive Data Handling

SSR Status Flag					
RDRF*	**ORER**	**FER**	**PER**	**Receive Data**	**Receive Error Type**
1	1	0	0	Lost	Overrun error
0	0	1	0	Transferred to RDR	Framing error
0	0	0	1	Transferred to RDR	Parity error
1	1	1	0	Lost	Overrun error + framing error
1	1	0	1	Lost	Overrun error + parity error
0	0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	1	Lost	Overrun error + framing error + parity error

Note: * The RDRF flag retains the state it had before data reception.



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error processing and break detection:
If a receive error occurs, read the ORER, PER, and FER flags in SSR to identify the error. After performing the appropriate error processing, ensure that the ORER, PER, and FER flags are all cleared to 0. Reception cannot be resumed if any of these flags are set to 1. In the case of a framing error, a break can be detected by reading the value of the input port corresponding to the RxD pin.

[4] SCI status check and receive data read:
Read SSR and check that RDRF = 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit for the current frame is received, read the RDRF flag, read RDR, and clear the RDRF flag to 0.

[Legend]
∨ : Logical OR

Figure 12.9 Sample Serial Reception Flowchart (1)

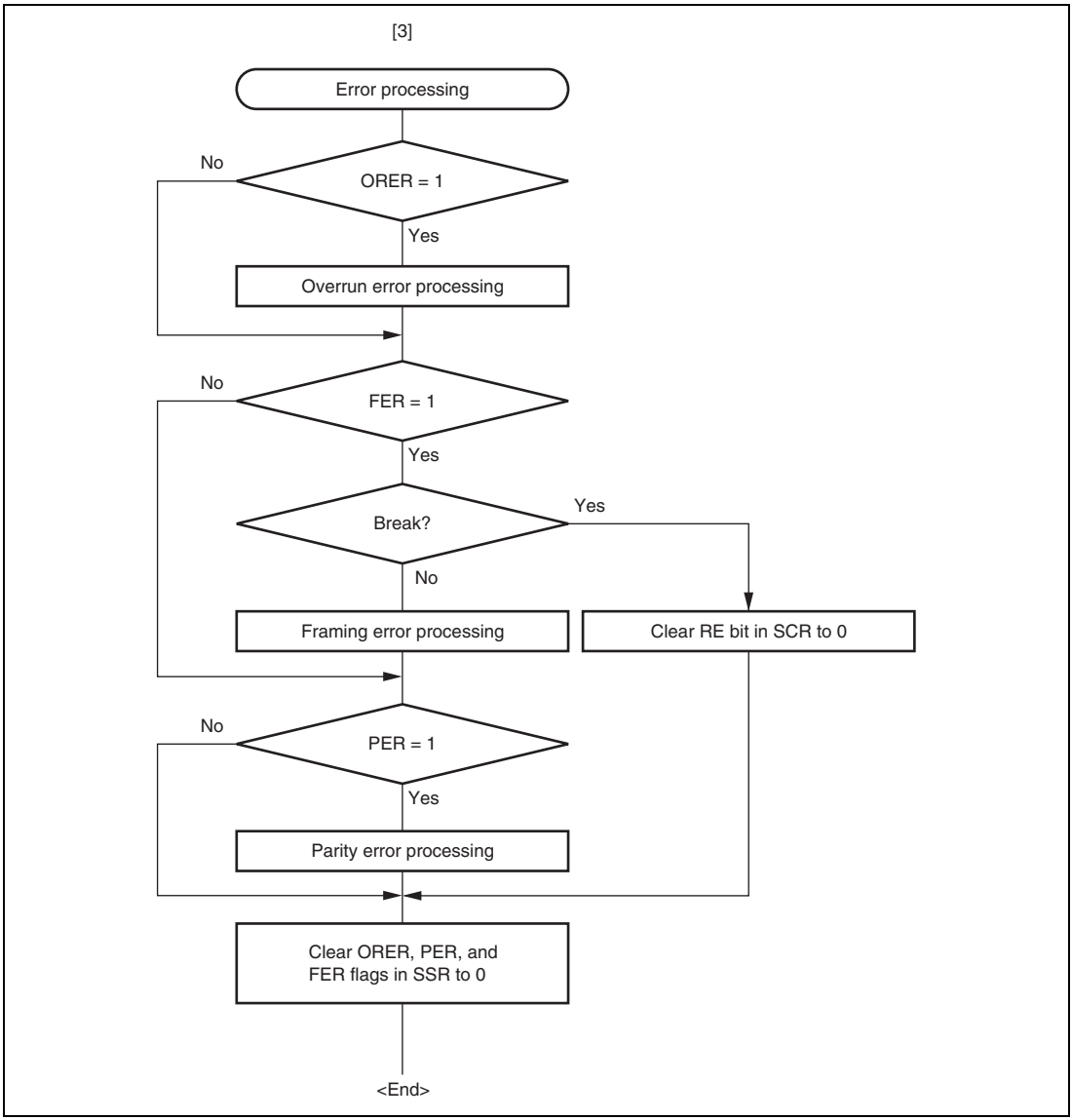


Figure 12.9 Sample Serial Reception Flowchart (2)

12.5 Multiprocessor Communication Function

Use of the multiprocessor communication function enables data transfer to be performed among a number of processors sharing communication lines by means of asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data. When multiprocessor communication is carried out, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles: an ID transmission cycle which specifies the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle, and if the multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 12.10 shows an example of inter-processor communication using the multiprocessor format. The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added. The receiving station skips data until data with a 1 multiprocessor bit is sent. When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose ID does not match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI uses the MPIE bit in SCR to implement this function. When the MPIE bit is set to 1, transfer of receive data from RSR to RDR, error flag detection, and setting the SSR status flags, RDRF, FER, and ORER in SSR to 1 are prohibited until data with a 1 multiprocessor bit is received. On reception of a receive character with a 1 multiprocessor bit, the MPB bit in SSR is set to 1 and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is invalid. All other bit settings are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

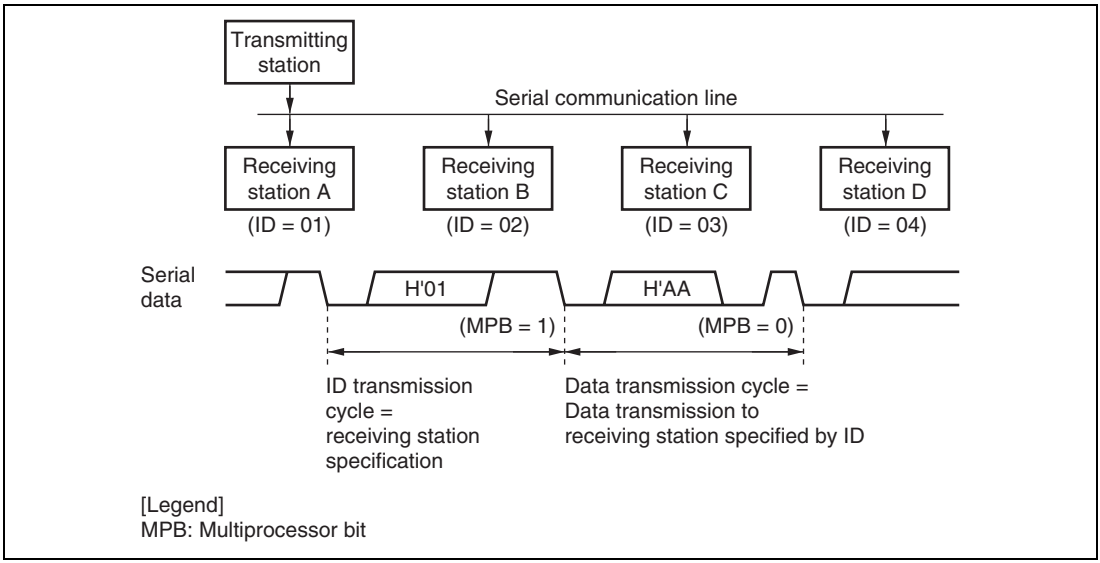
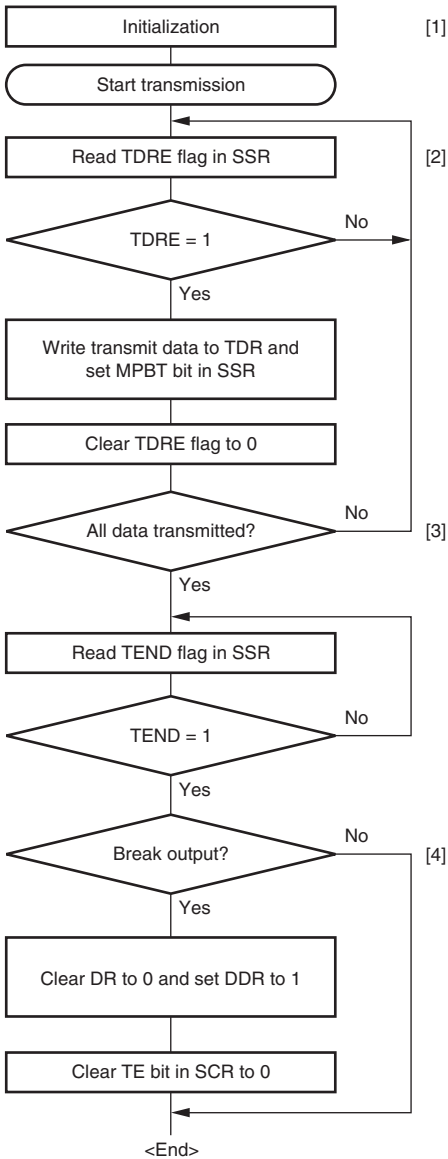


Figure 12.10 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

12.5.1 Multiprocessor Serial Data Transmission

Figure 12.11 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SSR to 1 before transmission. For a data transmission cycle, clear the MPBT bit in SSR to 0 before transmission. All other SCI operations are the same as those in asynchronous mode.



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, a frame of 1s is output, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. Set the MPBT bit in SSR to 0 or 1.
Finally, clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set port DDR to 1, clear DR to 0, and then clear the TE bit in SCR to 0.

Figure 12.11 Sample Multiprocessor Serial Transmission Flowchart

12.5.2 Multiprocessor Serial Data Reception

Figure 12.13 shows a sample flowchart for multiprocessor serial data reception. If the MPIE bit in SCR is set to 1, data is skipped until data with a 1 multiprocessor bit is sent. On receiving data with a 1 multiprocessor bit, the receive data is transferred to RDR. An RXI interrupt request is generated at this time. All other SCI operations are the same as in asynchronous mode. Figure 12.12 shows an example of SCI operation for multiprocessor format reception.

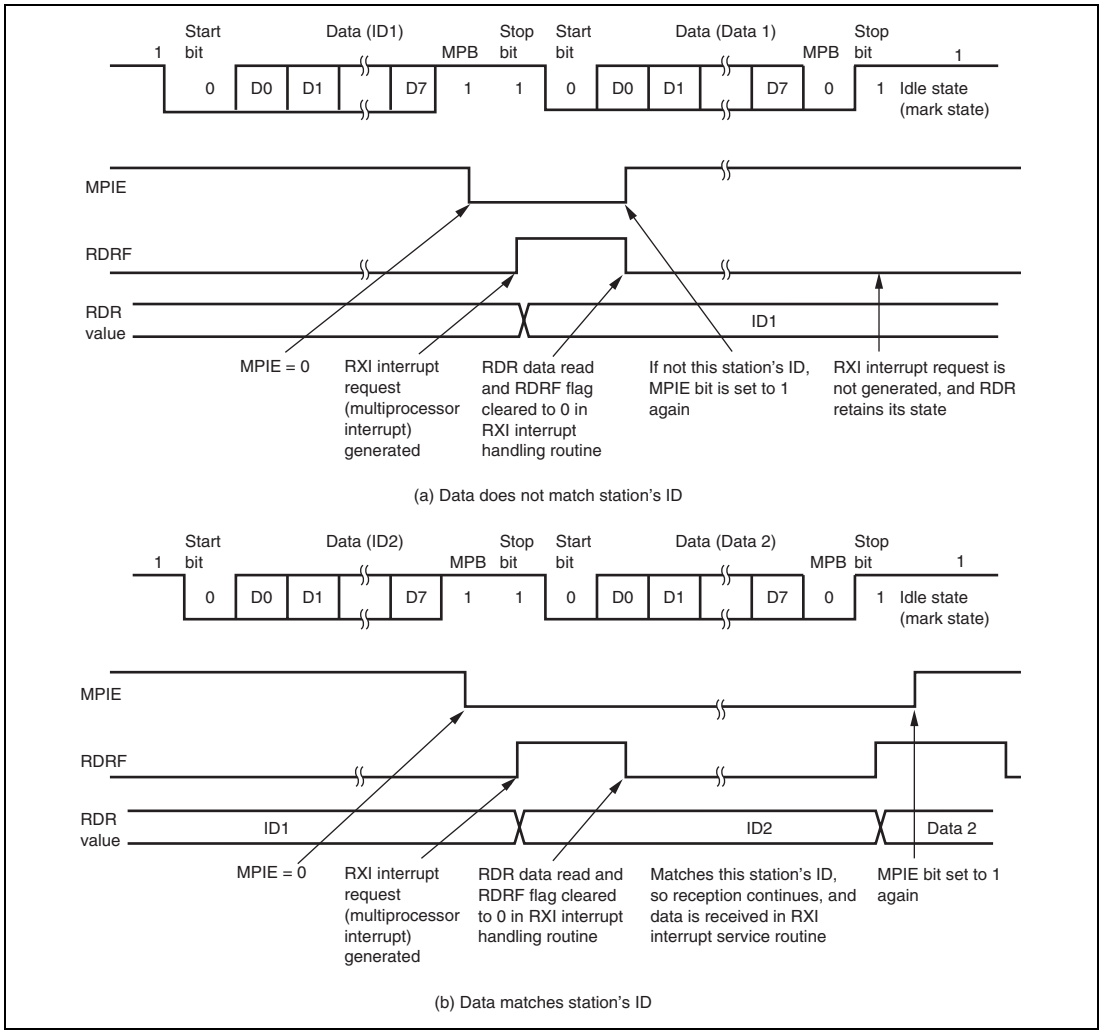


Figure 12.12 Example of SCI Receive Operation (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

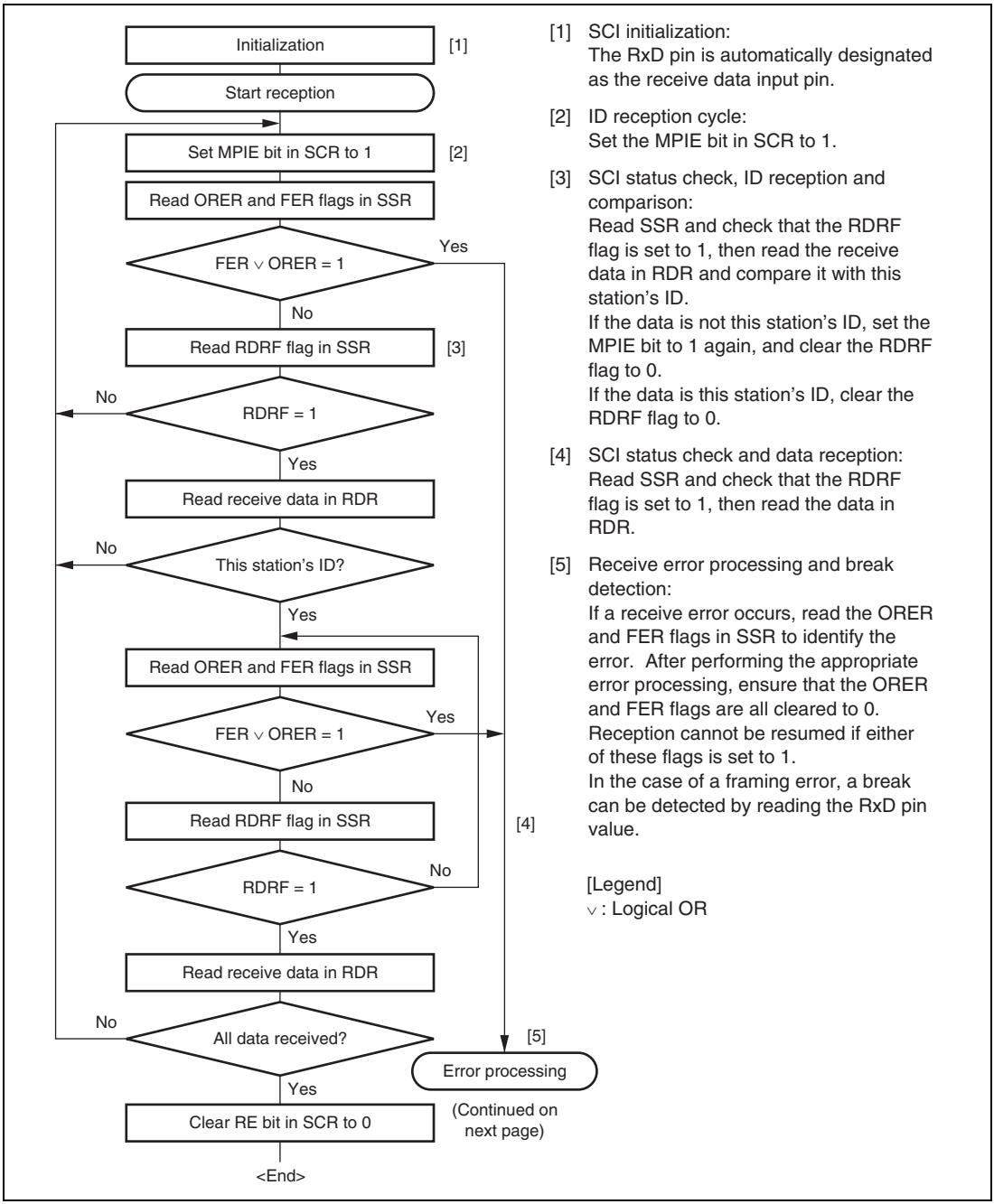


Figure 12.13 Sample Multiprocessor Serial Reception Flowchart (1)

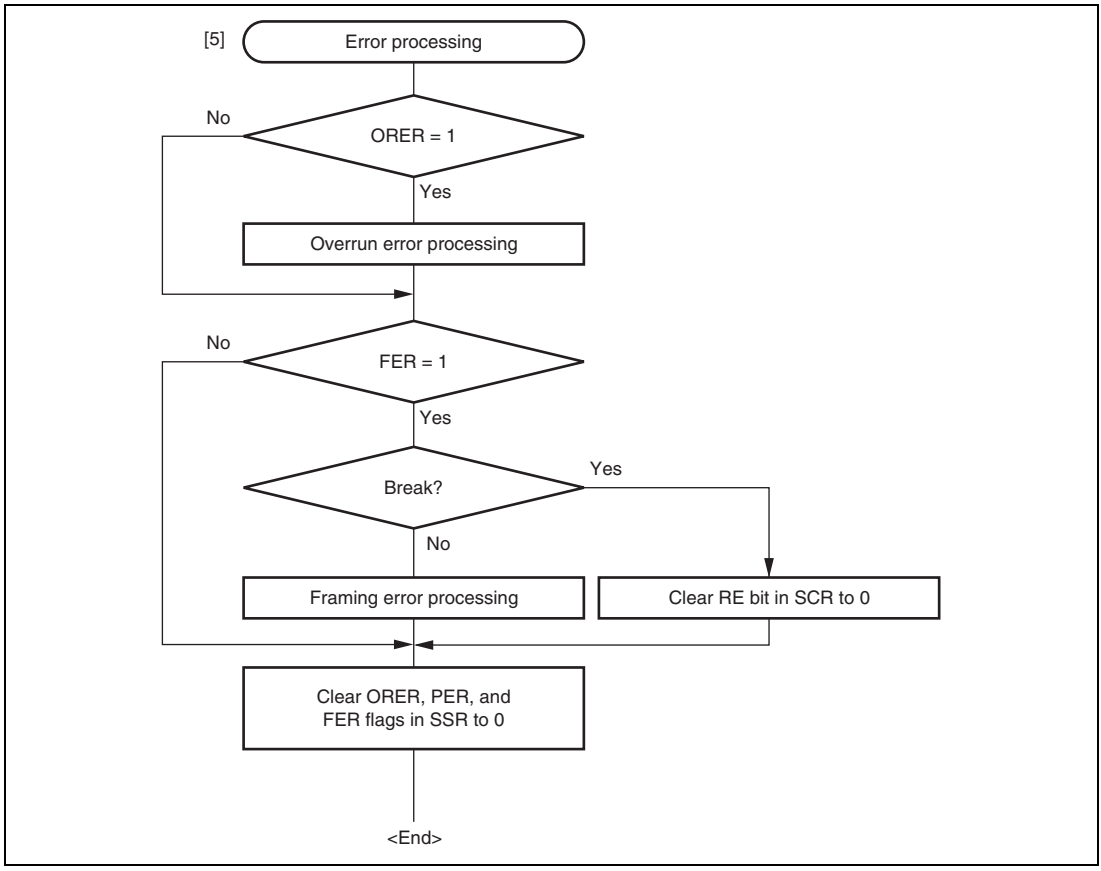


Figure 12.13 Sample Multiprocessor Serial Reception Flowchart (2)

12.6 Operation in Clock Synchronous Mode

Figure 12.14 shows the general format for clock synchronous communication. In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the MSB state. In clock synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

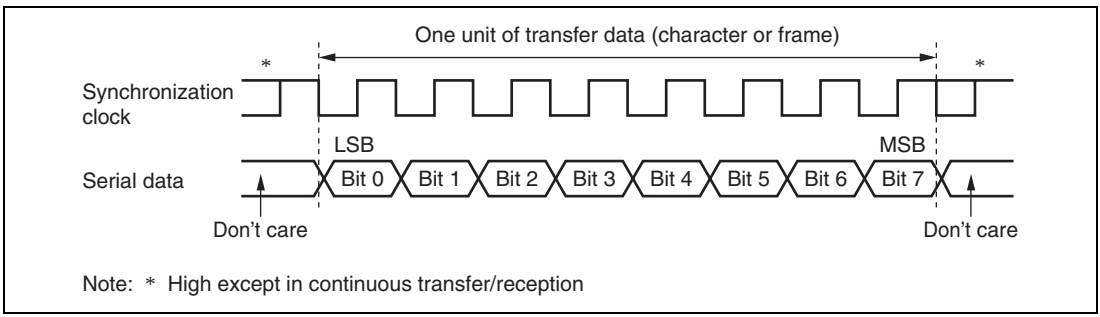


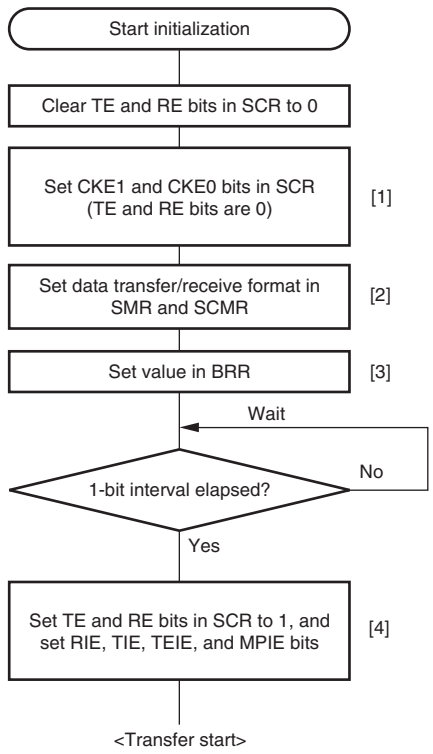
Figure 12.14 Data Format in Clock Synchronous Communication (LSB-First)

12.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of the CKE1 and CKE0 bits in SCR. When the SCI is operated on an internal clock, the synchronization clock is output from the SCK pin. Eight synchronization clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

12.6.2 SCI Initialization (Clock Synchronous Mode)

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as described in a sample flowchart in figure 12.15. When the operating mode, transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag in SSR is set to 1. However, clearing the RE bit to 0 does not initialize the RDRF, PER, FER, and ORER flags in SSR, or RDR.



[1] Set the clock selection in SCR. Be sure to clear bits RIE, TIE, TEIE, and MPIE, TE and RE to 0.

[2] Set the data transfer/receive format in SMR and SCMR.

[3] Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Also set the RIE, TIE TEIE, and MPIE bits.
Setting the TE and RE bits enables the TxD and RxD pins to be used.

Note: * In simultaneous transmit and receive operations, the TE and RE bits should both be cleared to 0 or set to 1 simultaneously.

Figure 12.15 Sample SCI Initialization Flowchart

12.6.3 Serial Data Transmission (Clock Synchronous Mode)

Figure 12.16 shows an example of SCI operation for transmission in clock synchronous mode. In serial transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in SSR, and if it is 0, recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit in SCR is set to 1 at this time, a TXI interrupt request is generated. Because the TXI interrupt routine writes the next transmit data to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.
3. 8-bit data is sent from the TxD pin synchronized with the output clock when output clock mode has been specified and synchronized with the input clock when use of an external clock has been specified.
4. The SCI checks the TDRE flag at the timing for sending the last bit.
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TxD pin maintains the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated. The SCK pin is fixed high.

Figure 12.17 shows a sample flow chart for serial data transmission. Even if the TDRE flag is cleared to 0, transmission will not start while a receive error flag (ORER, FER, or PER) is set to 1. Make sure to clear the receive error flags to 0 before starting transmission. Note that clearing the RE bit to 0 does not clear the receive error flags.

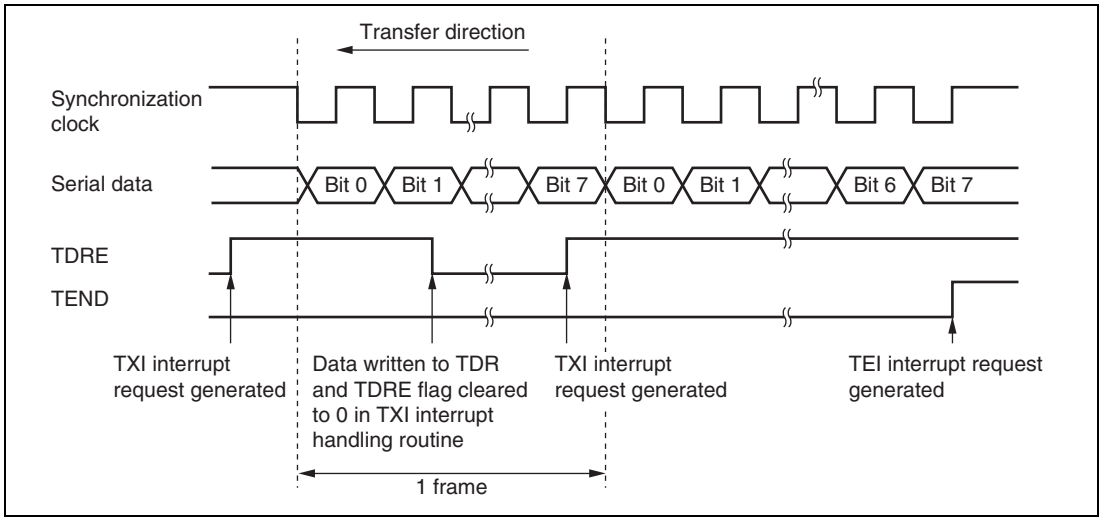
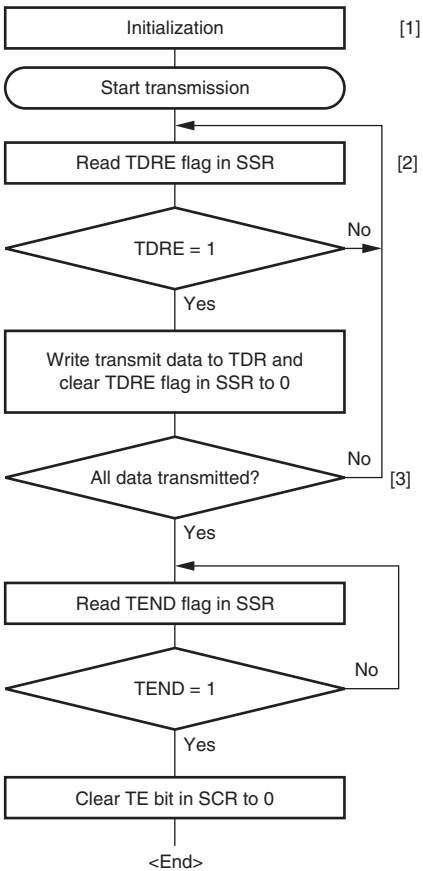


Figure 12.16 Example of SCI Transmit Operation in Clock Synchronous Mode



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0.

Figure 12.17 Sample Serial Transmission Flowchart

12.6.4 Serial Data Reception (Clock Synchronous Mode)

Figure 12.18 shows an example of SCI operation for reception in clock synchronous mode. In serial reception, the SCI operates as described below.

1. The SCI performs internal initialization in synchronization with a synchronization clock input or output, starts receiving data, and stores the receive data in RSR.
2. If an overrun error (when reception of the next data is completed while the RDRF flag is still set to 1) occurs, the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR. The RDRF flag remains to be set to 1.
3. If reception finishes successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has finished, continuous reception can be enabled.

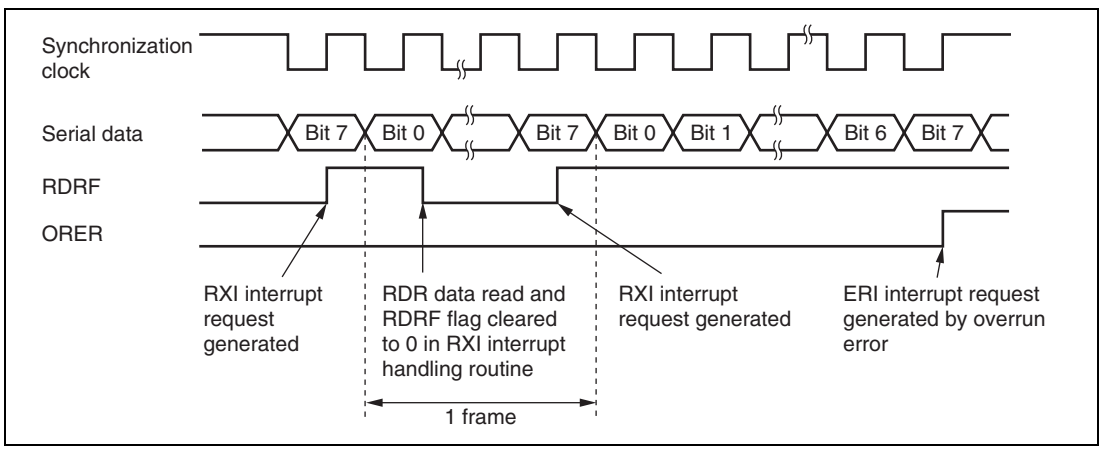
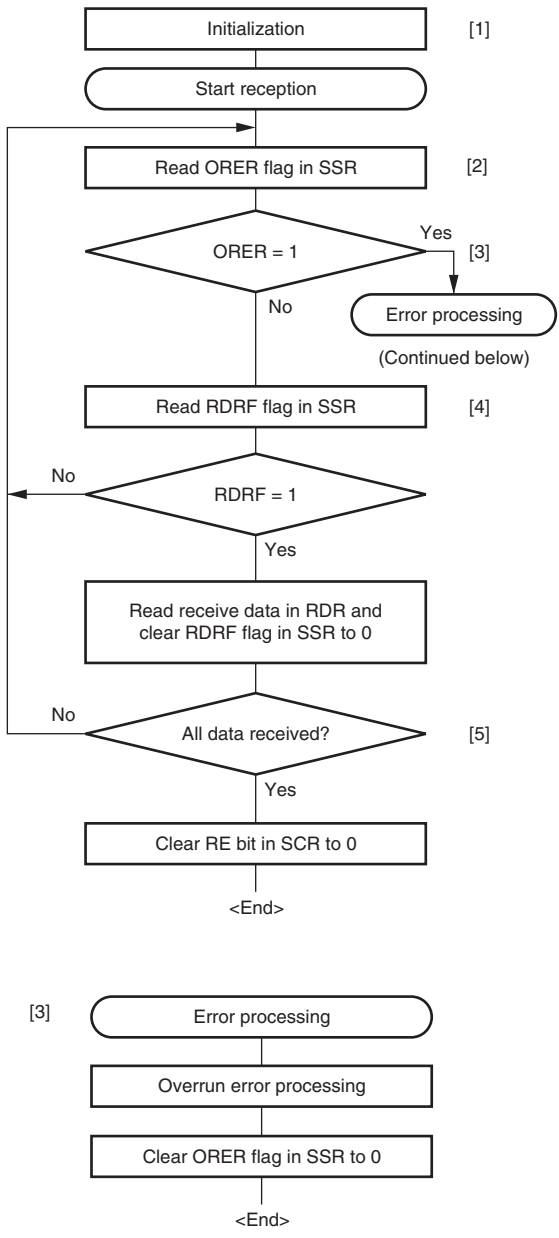


Figure 12.18 Example of SCI Receive Operation in Clock Synchronous Mode

Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 12.19 shows a sample flowchart for serial data reception.



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, and after performing the appropriate error processing, clear the ORER flag to 0. Transfer cannot be resumed if the ORER flag is set to 1.

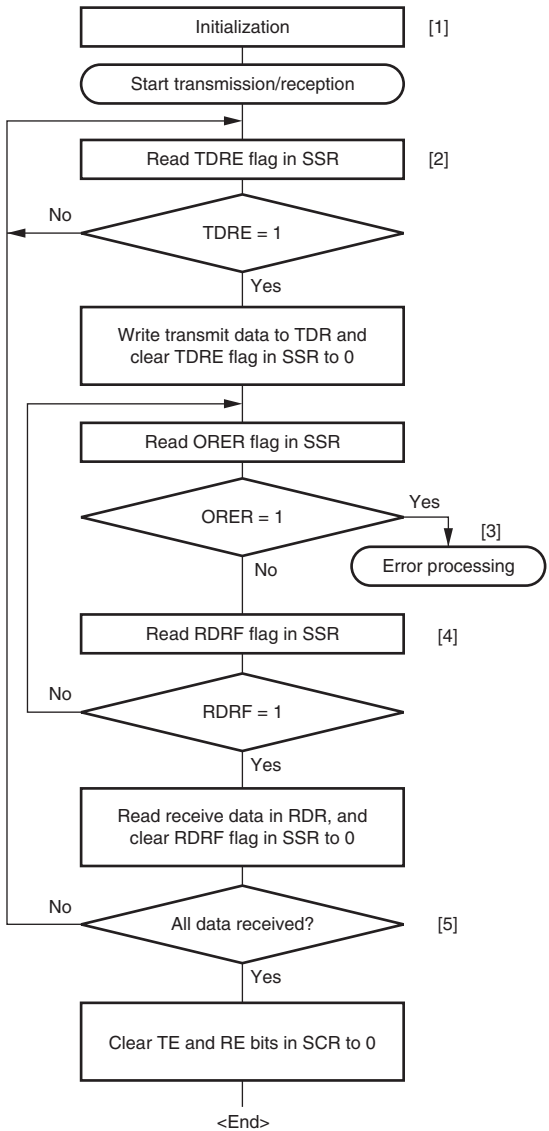
[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0.
Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0 should be finished.

Figure 12.19 Sample Serial Reception Flowchart

12.6.5 Simultaneous Serial Data Transmission and Reception (Clock Synchronous Mode)

Figure 12.20 shows a sample flowchart for simultaneous serial transmit and receive operations. After initializing the SCI, the following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, check that the SCI has finished transmission and the TDRE and TEND flags in SSR are set to 1, clear the TE bit in SCR to 0, and then set the TE and RE bits to 1 simultaneously with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, check that the SCI has finished reception, and clear the RE bit to 0. Then after checking that the RDRF bit in SSR and receive error flags (ORER, FER, and PER) are cleared to 0, set the TE and RE bits to 1 simultaneously with a single instruction.



[1] SCI initialization:
The TxD pin is designated as the transmit data output pin, and the RxD pin is designated as the receive data input pin, enabling simultaneous transmit and receive operations.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.
Transition of the TDRE flag from 0 to 1 can also be identified by a TXI interrupt.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, and after performing the appropriate error processing, clear the ORER flag to 0. Transmission/reception cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission/reception, before the MSB (bit 7) of the current frame is received, reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0 should be finished. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to TDR and clear the TDRE flag to 0.

Note: * When switching from transmit or receive operation to simultaneous transmit and receive operations, first clear the TE bit and RE bit to 0, then set both these bits to 1 simultaneously.

Figure 12.20 Sample Flowchart of Simultaneous Serial Transmission and Reception

12.7 IrDA Operation

IrDA operation can be used with SCI_2. Figure 12.21 shows an IrDA block diagram.

If the IrDA function is enabled using the IrE bit in KBCOMP, the TxD2 and RxD2 pins in SCI_2 are allowed to encode and decode the waveform based on the IrDA standard version 1.0 (function as the IrTxD and IrRxD pins). Connecting these pins to the infrared data transceiver achieves infrared data communication based on the system defined by the IrDA standard version 1.0.

In the system defined by the IrDA standard version 1.0, communication is started at a transfer rate of 9600 bps, which can be modified as required. The IrDA interface provided by this LSI does not incorporate the capability of automatic modification of the transfer rate; the transfer rate must be modified through programming.

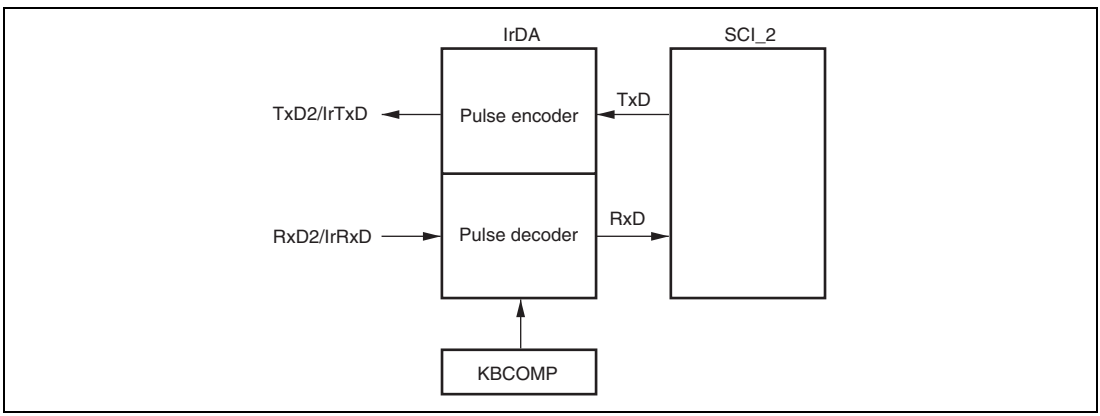


Figure 12.21 IrDA Block Diagram

Transmission: During transmission, the output signals from the SCI (UART frames) are converted to IR frames using the IrDA interface (see figure 12.22).

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit interval) is output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0 bits in KBCOMP.

The high-level pulse width is defined to be 1.41 µs at minimum and (3/16 + 2.5%) × bit rate or (3/16 × bit rate) + 1.08 µs at maximum. For example, when the frequency of system clock ϕ is 20 MHz, a high-level pulse width of at least 1.4 µs to 1.6 µs can be specified.

For serial data of level 1, no pulses are output.

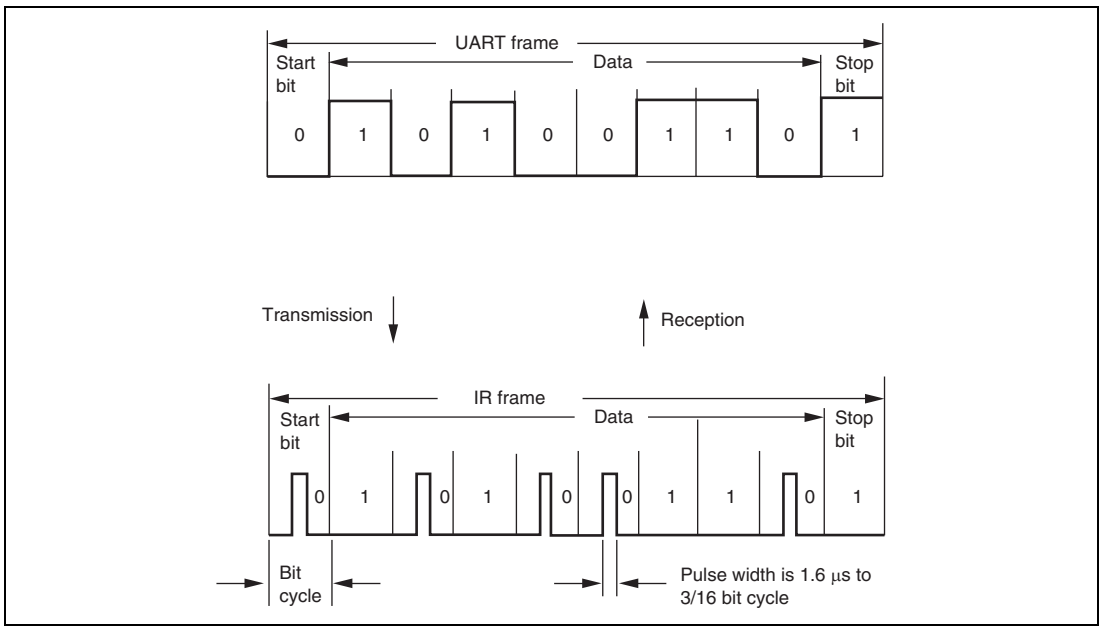


Figure 12.22 IrDA Transmission and Reception

Reception: During reception, IR frames are converted to UART frames using the IrDA interface before inputting to SCI_2.

Data of level 0 is output each time a high-level pulse is detected and data of level 1 is output when no pulse is detected in a bit cycle. If a pulse has a high-level width of less than 1.41 µs, the minimum width allowed, the pulse is recognized as level 0.

High-Level Pulse Width Selection: Table 12.10 shows possible settings for bits IrCKS2 to IrCKS0 (minimum pulse width), and this LSI's operating frequencies and bit rates, for making the pulse width shorter than 3/16 times the bit rate in transmission.

Table 12.10 IrCKS2 to IrCKS0 Bit Settings

Operating Frequency	Bit Rate (bps) (Upper Row) / Bit Interval × 3/16 (µs) (Lower Row)					
	2400	9600	19200	38400	57600	115200
ϕ (MHz)	78.13	19.53	9.77	4.88	3.26	1.63
2	010	010	010	010	010	—
2.097152	010	010	010	010	010	—
2.4576	010	010	010	010	010	—
3	011	011	011	011	011	—
3.6864	011	011	011	011	011	011
4.9152	011	011	011	011	011	011
5	011	011	011	011	011	011
6	100	100	100	100	100	100
6.144	100	100	100	100	100	100
7.3728	100	100	100	100	100	100
8	100	100	100	100	100	100
9.8304	100	100	100	100	100	100
10	100	100	100	100	100	100
12	101	101	101	101	101	101
12.288	101	101	101	101	101	101
14	101	101	101	101	101	101
14.7456	101	101	101	101	101	101
16	101	101	101	101	101	101
16.9344	101	101	101	101	101	101
17.2032	101	101	101	101	101	101
18	101	101	101	101	101	101
19.6608	101	101	101	101	101	101
20	101	101	101	101	101	101

[Legend]

—: An SCI bit rate setting cannot be made.

12.8 Interrupt Sources

Table 12.11 shows the interrupt sources in serial communication interface. A different interrupt vector is assigned to each interrupt source, and individual interrupt sources can be enabled or disabled using the enable bits in SCR.

When the TDRE flag in SSR is set to 1, a TXI interrupt request is generated. When the TEND flag in SSR is set to 1, a TEI interrupt request is generated.

When the RDRF flag in SSR is set to 1, an RXI interrupt request is generated. When the ORER, PER, or FER flag in SSR is set to 1, an ERI interrupt request is generated.

A TEI interrupt is requested when the TEND flag is set to 1 while the TEIE bit is set to 1. If a TEI interrupt and a TXI interrupt are requested simultaneously, the TXI interrupt has priority for acceptance. However, note that if the TDRE and TEND flags are cleared simultaneously by the TXI interrupt routine, the SCI cannot branch to the TEI interrupt routine later.

Table 12.11 SCI Interrupt Sources

Channel	Name	Interrupt Source	Interrupt Flag	Priority
0	ERI0	Receive error	ORER, FER, PER	High
	RXI0	Receive data full	RDRF	
	TXI0	Transmit data empty	TDRE	
	TEI0	Transmit end	TEND	
1	ERI1	Receive error	ORER, FER, PER	
	RXI1	Receive data full	RDRF	
	TXI1	Transmit data empty	TDRE	
	TEI1	Transmit end	TEND	
2	ERI2	Receive error	ORER, FER, PER	
	RXI2	Receive data full	RDRF	
	TXI2	Transmit data empty	TDRE	
	TEI2	Transmit end	TEND	Low

12.9 Usage Notes

12.9.1 Module Stop Mode Setting

SCI operation can be disabled or enabled using the module stop control register. The initial setting is for SCI operation to be halted. Register access is enabled by clearing module stop mode. For details, refer to section 18, Power-Down Modes.

12.9.2 Break Detection and Processing

When framing error detection is performed, a break can be detected by reading the RxD pin value directly. In a break, the input from the RxD pin becomes all 0s, and so the FER flag in SSR is set, and the PER flag may also be set. Note that, since the SCI continues the receive operation even after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

12.9.3 Mark State and Break Detection

When the TE bit in SCR is 0, the TxD pin is used as an I/O port whose direction (input or output) and level are determined by DR and DDR of the port. This can be used to set the TxD pin to the mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both DDR and DR to 1. Since the TE bit is cleared to 0 at this point, the TxD pin becomes an I/O port, and 1 is output from the TxD pin. To send a break during serial transmission, first set DDR to 1 and DR to 0, and then clear the TE bit to 0. When the TE bit is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TxD pin becomes an I/O port, and 0 is output from the TxD pin.

12.9.4 Receive Error Flags and Transmit Operations (Clock Synchronous Mode Only)

Transmission cannot be started when a receive error flag (ORER, FER, or RER) is SSR is set to 1, even if the TDRE flag in SSR is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that the receive error flags cannot be cleared to 0 even if the RE bit in SCR is cleared to 0.

12.9.5 Relation between Writing to TDR and TDRE Flag

Data can be written to TDR irrespective of the TDRE flag status in SSR. However, if the new data is written to TDR when the TDRE flag is 0, that is, when the previous data has not been transferred to TSR yet, the previous data in TDR is lost. Be sure to write transmit data to TDR after verifying that the TDRE flag is set to 1.

12.9.6 SCI Operations during Mode Transitions

Transmission: Before making a transition to module stop, software standby, or sub-sleep mode, stop all transmit operations (TE = TIE = TEIE = 0). TSR, TDR, and SSR are reset. The states of the output pins during each mode depend on the port settings, and the pins output a high-level signal after mode cancellation. If a transition is made during data transmission, the data being transmitted will be undefined.

To transmit data in the same transmission mode after mode cancellation, set TE to 1, read SSR, write to TDR, clear TDRE in this order, and then start transmission. To transmit data in a different transmission mode, initialize the SCI first.

Figure 12.23 shows a sample flowchart for mode transition during transmission. Figures 12.24 and 12.25 show the pin states during transmission.

Reception: Before making a transition to module stop, software standby, watch, sub-active, or sub-sleep mode, stop reception (RE = 0). RSR, RDR, and SSR are reset. If a transition is made during data reception, the data being received will be invalid.

To receive data in the same reception mode after mode cancellation, set RE to 1, and then start reception. To receive data in a different reception mode, initialize the SCI first.

Figure 12.27 shows a sample flowchart for mode transition during reception.

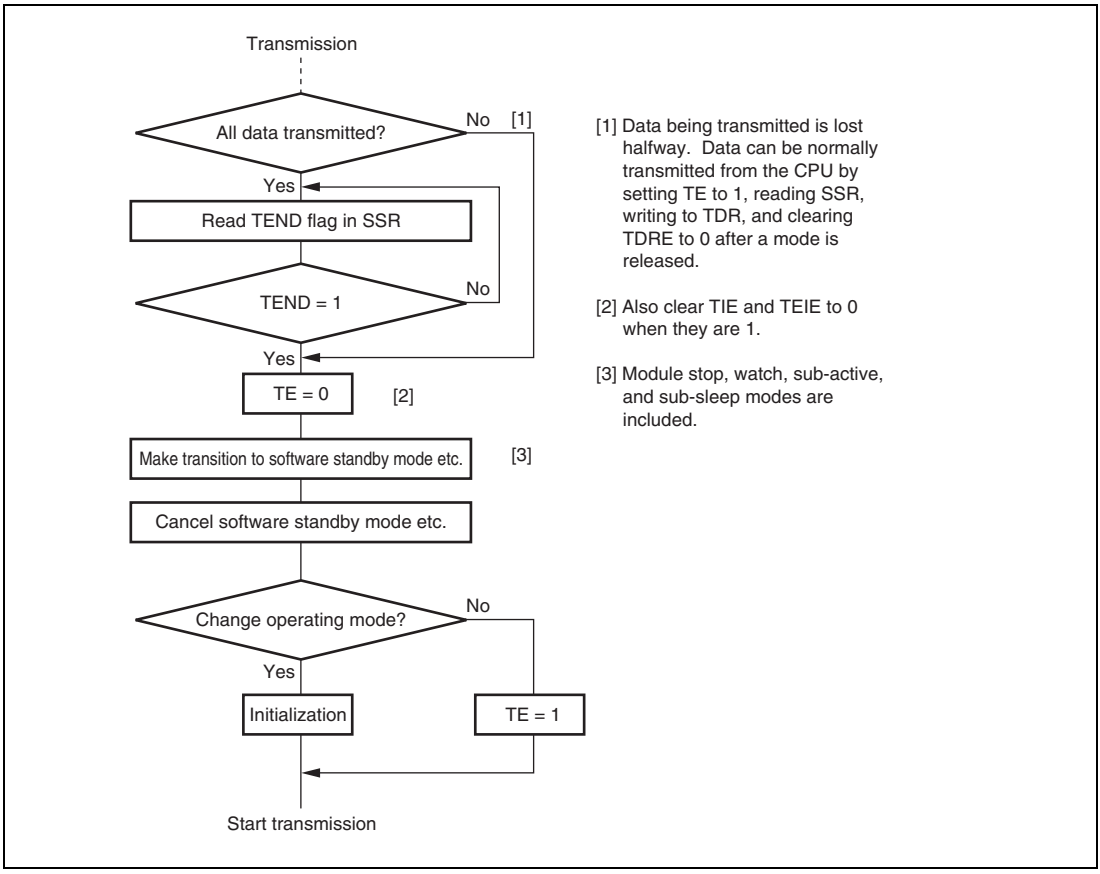


Figure 12.23 Sample Flowchart for Mode Transition during Transmission

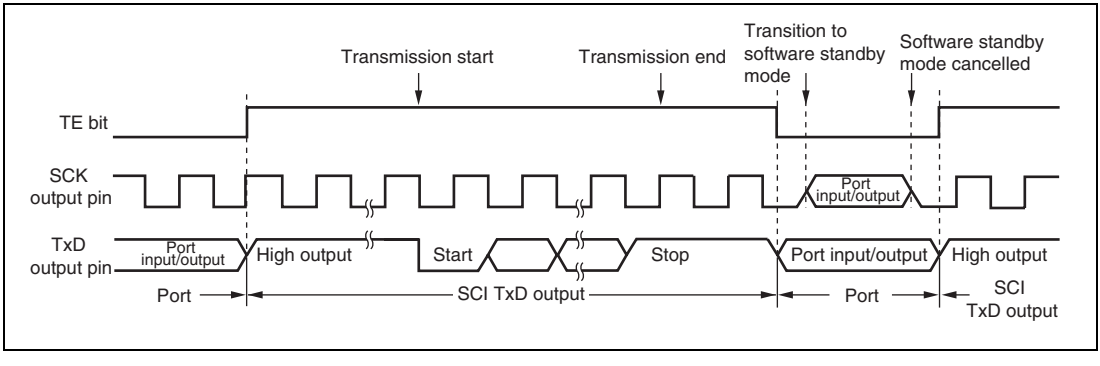


Figure 12.24 Pin States during Transmission in Asynchronous Mode (Internal Clock)

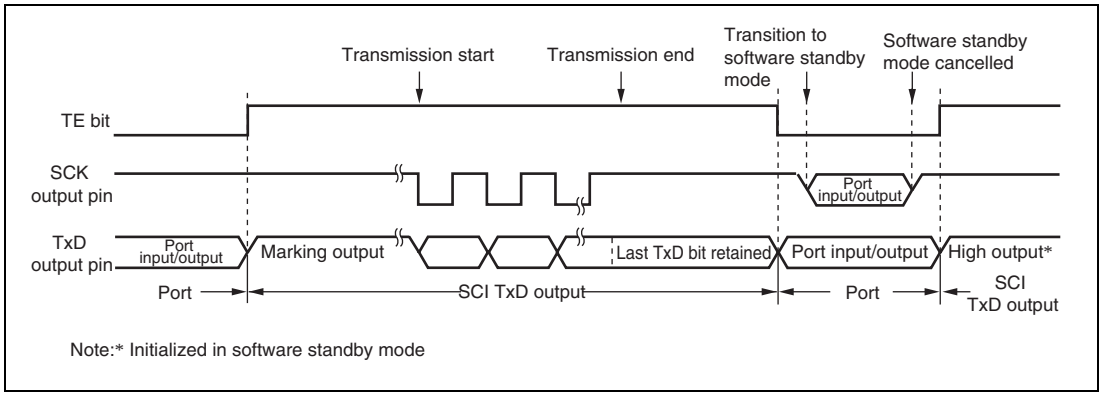


Figure 12.25 Pin States during Transmission in Clock Synchronous Mode (Internal Clock)

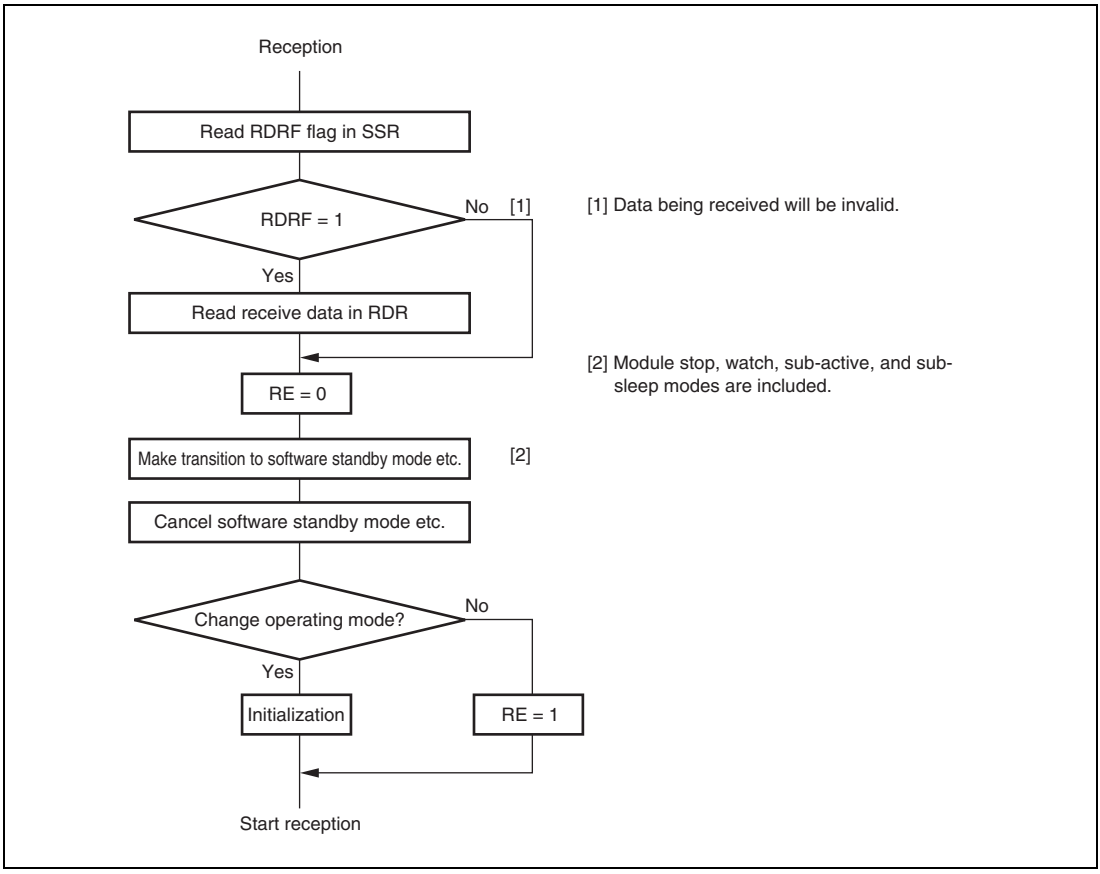


Figure 12.26 Sample Flowchart for Mode Transition during Reception

12.9.7 Notes on Switching from SCK Pins to Port Pins

When SCK pins are switched to port pins after transmission has completed, pins are enabled for port output after outputting a low pulse of half a cycle as shown in figure 12.28.

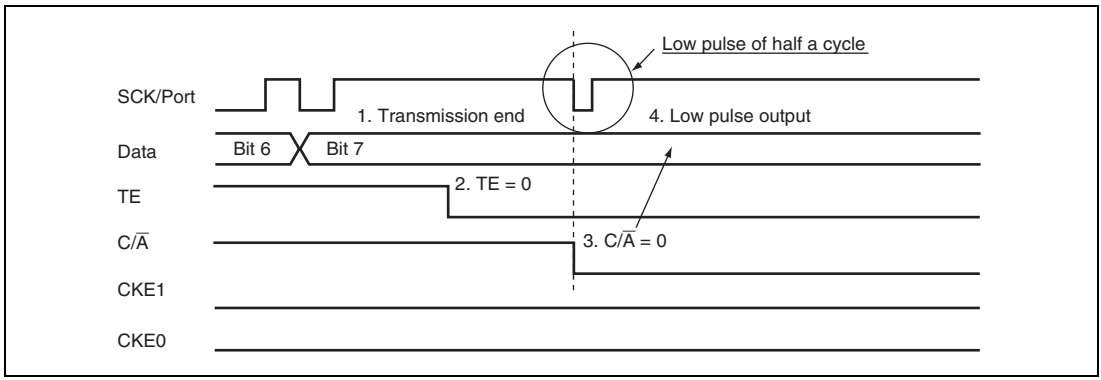


Figure 12.27 Switching from SCK Pins to Port Pins

To prevent the low pulse output that is generated when switching the SCK pins to the port pins, specify the SCK pins for input (pull up the SCK/port pins externally), and follow the procedure below with DDR = 1, DR = 1, C/$\overline{A}$ = 1, CKE1 = 0, CKE1 = 0, and TE = 1.

1. End serial data transmission
2. TE bit = 0
3. CKE1 bit = 1
4. C/$\overline{A}$ bit = 0 (switch to port output)
5. CKE1 bit = 0

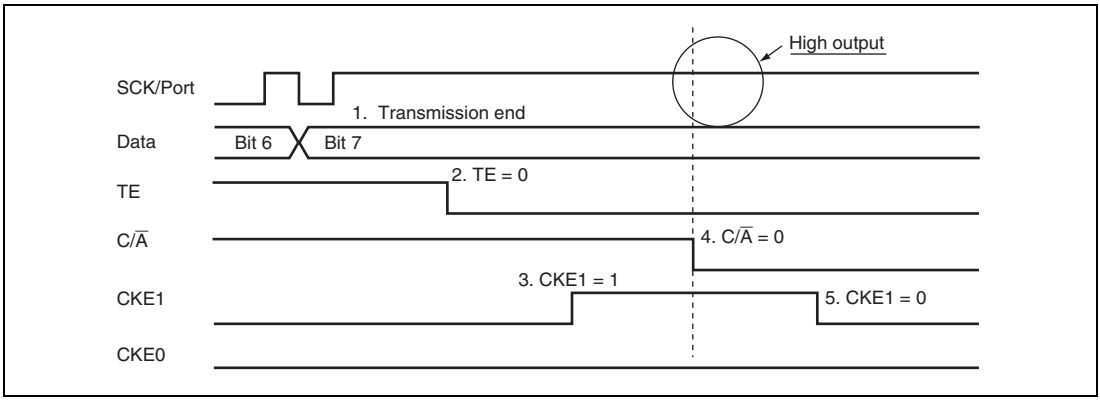


Figure 12.28 Prevention of Low Pulse Output at Switching from SCK Pins to Port Pins

Section 13 D/A Converter

13.1 Features

- 8-bit resolution
- Two output channels
- Conversion time: Max. 10 µs (when load capacitance is 20 pF)
- Output voltage: 0 V to AVref for the H8S/2144B and 0 V to AVcc for the H8S/2134B
- D/A output retaining function in software standby mode

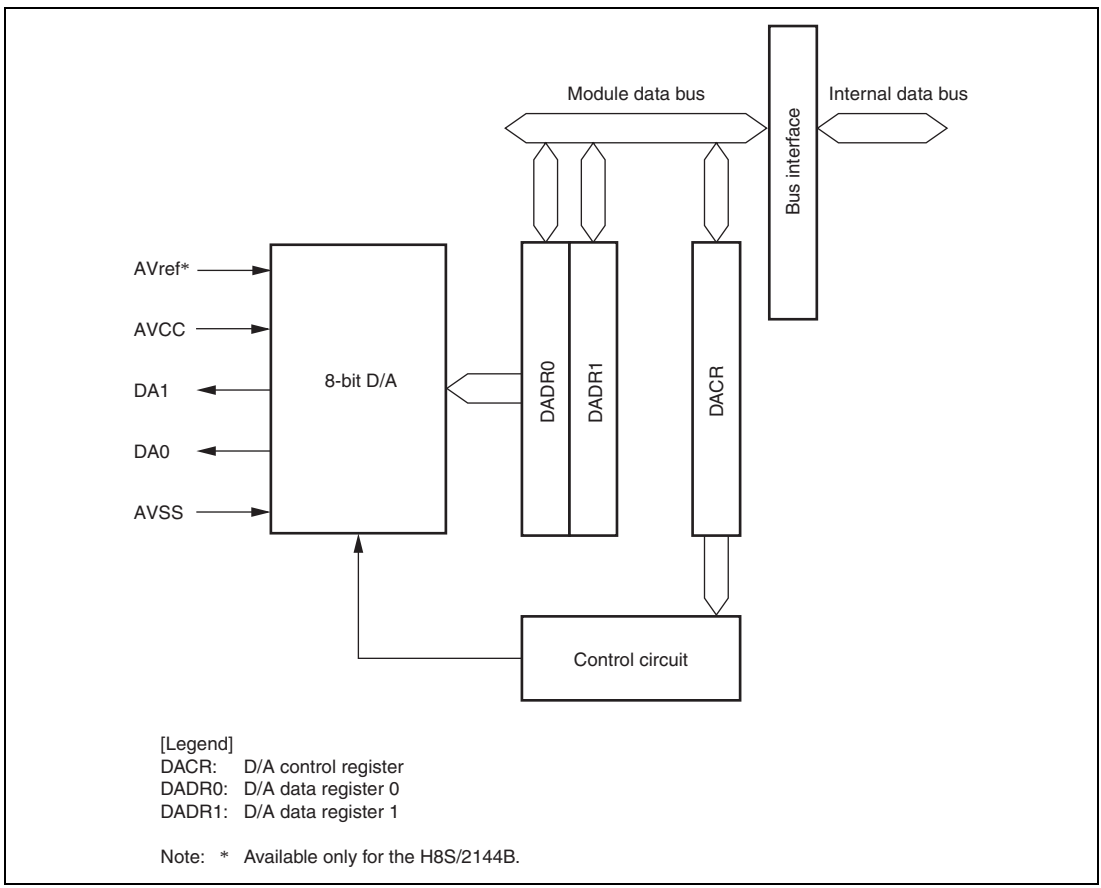


Figure 13.1 Block Diagram of D/A Converter

13.2 Input/Output Pins

Table 13.1 summarizes the input/output pins used by the D/A converter.

Table 13.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power supply pin	AVCC	Input	Analog block power supply
Analog ground pin	AVSS	Input	Analog block ground and reference voltage
Analog output pin 0	DA0	Output	Channel 0 analog output
Analog output pin 1	DA1	Output	Channel 1 analog output
Reference power supply pin	AVref*	Input	Analog block reference voltage

Note: * Available only for the H8S/2144B.

13.3 Register Descriptions

The D/A converter has the following registers.

- D/A data register 0 (DADR0)
- D/A data register 1 (DADR1)
- D/A control register (DACR)

13.3.1 D/A Data Registers 0 and 1 (DADR0, DADR1)

DADR0 and DADR1 are 8-bit readable/writable registers that store data for D/A conversion. When analog output is permitted, D/A data register contents are converted and output to analog output pins. DADR0 and DADR1 are initialized to H′00.

13.3.2 D/A Control Register (DACR)

DACR controls D/A converter operation.

Bit	Bit Name	Initial Value	R/W	Description
7	DAOE1	0	R/W	D/A Output Enable 1 Controls D/A conversion and analog output. 0: Analog output DA1 is disabled 1: D/A conversion for channel 1 and analog output DA1 are enabled
6	DAOE0	0	R/W	D/A Output Enable 0 Controls D/A conversion and analog output. 0: Analog output DA0 is disabled 1: D/A conversion for channel 0 and analog output DA0 are enabled
5	DAE	0	R/W	D/A Enable Controls D/A conversion in conjunction with the DAOE0 and DAOE1 bits. When the DAE bit is cleared to 0, D/A conversion for channels 0 and 1 is controlled individually. When the DAE bit is set to 1, D/A conversion for channels 0 and 1 are controlled as one. Conversion result output is controlled by the DAOE0 and DAOE1 bits. For details, see table 13.2 below.
4 to 0	—	All 1	R	Reserved These bits are always read as 1 and cannot be modified.

Table 13.2 D/A Channel Enable

Bit 7	Bit 6	Bit 5	
DAOE1	**DAOE0**	**DAE**	**Description**
0	0	—	Disables D/A conversion
	1	0	Enables D/A conversion for channel 0
			Disables D/A conversion for channel 1
		1	Enables D/A conversion for channels 0 and 1
1	0	0	Disables D/A conversion for channel 0
			Enables D/A conversion for channel 1
		1	Enables D/A conversion for channels 0 and 1
	1	—	Enables D/A conversion for channels 0 and 1

13.4 Operation

The D/A converter incorporates two channels of the D/A circuits and can be converted individually.

When the DAOE bit in DACR is set to 1, D/A conversion is enabled and conversion results are output.

An example of D/A conversion of channel 0 is shown below. The operation timing is shown in figure 13.2.

1. Write conversion data to DADR0.
2. When the DAOE0 bit in DACR is set to 1, D/A conversion starts. After the interval of t_{DCONV}, conversion results are output from the analog output pin DA0. The conversion results are output continuously until DADR0 is modified or the DAOE0 bit is cleared to 0. The output value is calculated by the following formula:

   DADR contents/256 × AVref

3. Conversion starts immediately after DADR0 is modified. After the interval of t_{DCONV}, conversion results are output.
4. When the DAOE0 bit is cleared to 0, analog output is disabled.

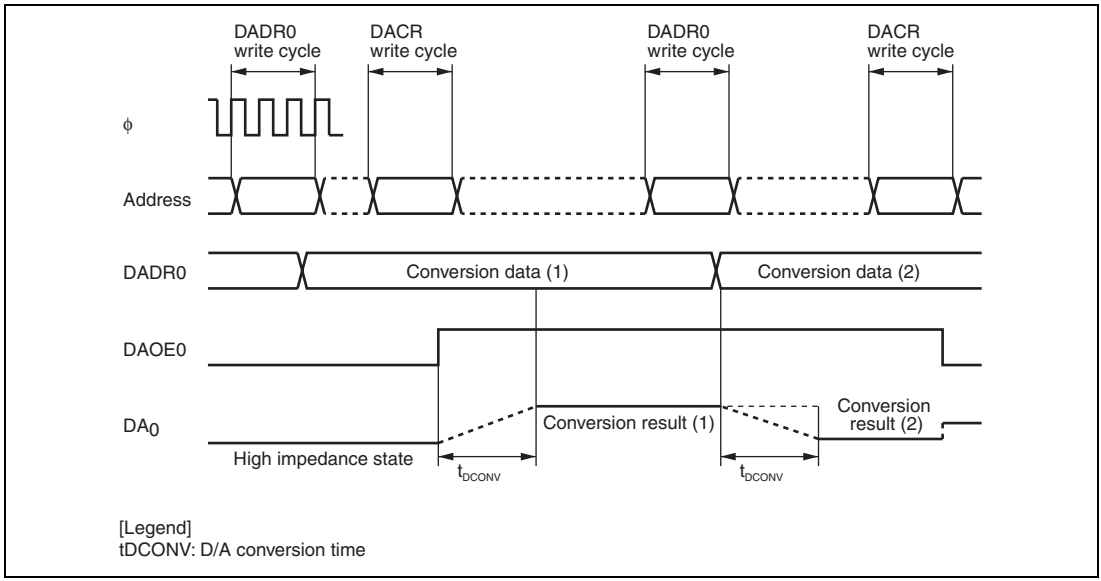


Figure 13.2 D/A Converter Operation Example

13.5 Usage Note

When this LSI enters software standby mode with D/A conversion enabled, the D/A output is retained, and the analog power supply current is equal to as during D/A conversion. If the analog power supply current needs to be reduced in software standby mode, clear the DAOE1, DAOE0, and DAE bits all to 0 to disable D/A output.

13.5.1 Module Stop Mode Setting

D/A converter operation can be enabled or disabled using the module stop control register. The initial setting is for D/A converter operation to be halted. Register access is enabled by canceling module stop mode. For details, refer to section 18, Power-Down Modes.

Section 14 A/D Converter

This LSI includes a 10-bit successive-approximation-type A/D converter that allows up to eight analog input channels and up to 16 digital input channels* to be selected. A/D conversion for digital input is effective as a comparator in multiple input testing.

Note: * Up to eight channels in the H8S/2134B

14.1 Features

- 10-bit resolution
- Input channels: eight analog input channels and 16 digital input channels*[1]
- Analog conversion voltage range can be specified using the reference power supply voltage pin (AVref*[2]) as an analog reference voltage.
- Conversion time: 13.4 µs per channel (at 10-MHz operation)
- Two kinds of operating modes
  - Single mode: Single-channel A/D conversion
  - Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  - Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Three kinds of conversion start
  - Software, 8-bit timer (TMR) conversion start trigger, or external trigger signal.
- Interrupt request
  - A/D conversion end interrupt (ADI) request can be generated

Notes: 1. Up to eight channels in the H8S/2134B
2. Available only for the H8S/2144B.

A block diagram of the A/D converter is shown in figure 14.1.

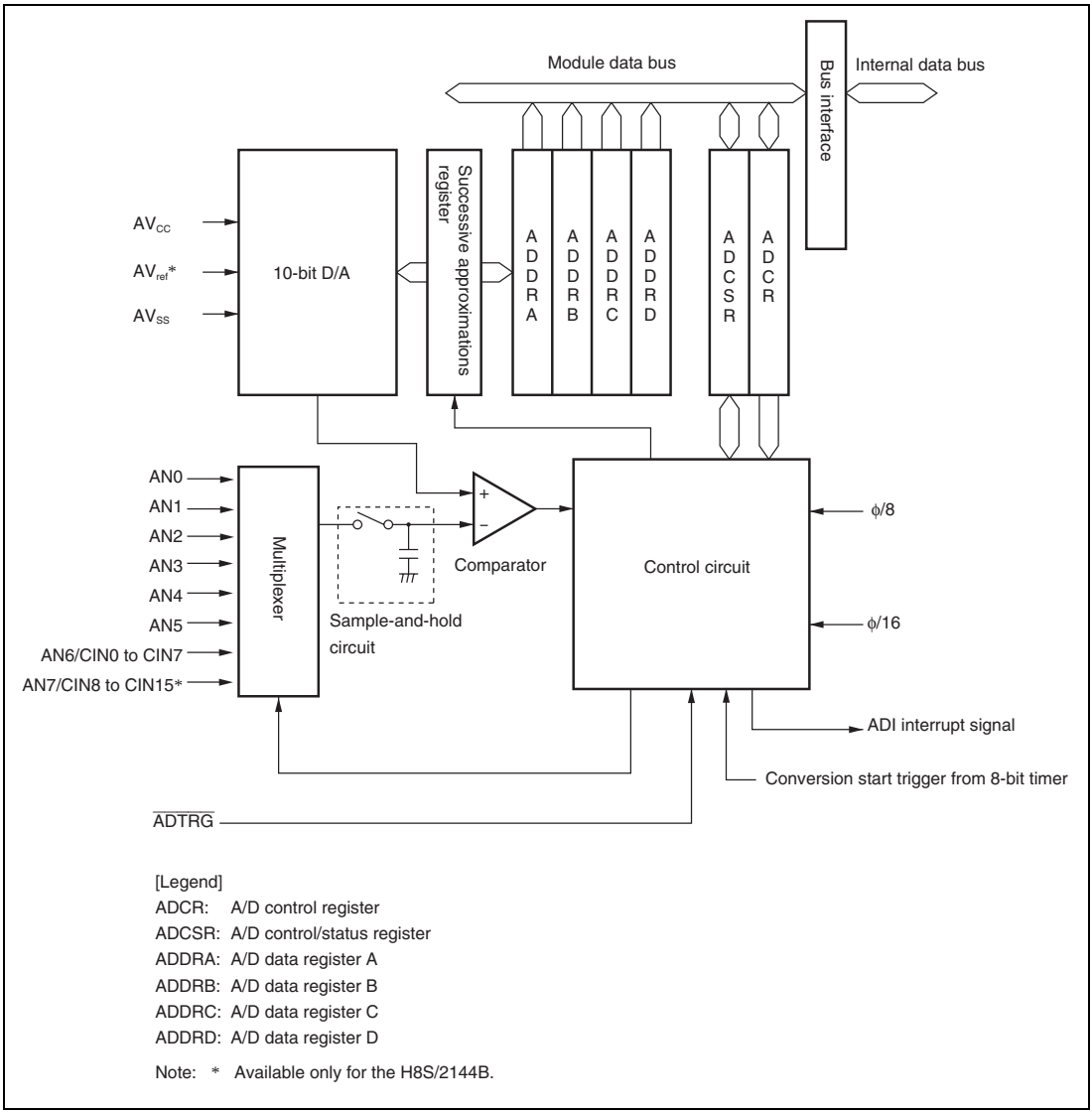


Figure 14.1 Block Diagram of A/D Converter

14.2 Input/Output Pins

Table 14.1 summarizes the pins used by the A/D converter. The 8 analog input pins are divided into two groups consisting of four channels. Analog input pins 0 to 3 (AN0 to AN3) comprising group 0 and analog input pins 4 to 7 (AN4 to AN7) comprising group 1. Expanded A/D conversion input pins (CIN0 to CIN15) can be selected with the AN6 and AN7 pins. The AVcc and AVss pins are the power supply pins for the analog block in the A/D converter.

Table 14.1 Pin Configuration

Pin Name	Symbol	I/O	Function
Analog power supply pin	AV_{CC}	Input	Analog block power supply and reference voltage
Analog ground pin	AV_{SS}	Input	Analog block ground and reference voltage
Reference power supply pin	AVref	Input	Reference voltage for A/D conversion (Available only for the H8S/2144B.)
Analog input pin 0	AN0	Input	Group 0 analog input pins
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	Group 1 analog input pins
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
A/D external trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input pin for starting A/D conversion
Expanded A/D conversion input pins 0 to 15	CIN0 to CIN15	Input	Expanded A/D conversion input (digital input) channels 0 to 15. Can be used as digital input pins. Channels 0 to 7 are available for the H8S/2134B.

14.3 Register Descriptions

The A/D converter has the following registers.

- A/D data register A (ADDRA)
- A/D data register B (ADDRB)
- A/D data register C (ADDRC)
- A/D data register D (ADDRD)
- A/D control/status register (ADCSR)
- A/D control register (ADCR)
- Keyboard comparator control register (KBCOMP)

14.3.1 A/D Data Registers A to D (ADDRA to ADDRD)

There are four 16-bit read-only ADDR registers, ADDRA to ADDRD, used to store the results of A/D conversion. The ADDR registers, which store a conversion result for each channel, are shown in table 14.2.

The converted 10-bit data is stored to bits 15 to 6. The lower 6-bit data is always read as 0.

The data bus between the CPU and the A/D converter is 8-bit width. The upper byte can be read directly from the CPU, but the lower byte should be read via a temporary register. The temporary register contents are transferred from the ADDR when the upper byte data is read. When reading the ADDR, read the upper byte before lower byte or in word units.

Table 14.2 Analog Input Channels and Corresponding ADDR Registers

Analog Input Channel		A/D Data Register to Store A/D Conversion Results
Group 0	**Group 1**	
AN0	AN4	ADDRA
An1	AN5	ADDRB
AN2	AN6, or CIN0 to CIN7	ADDRC
AN3	AN7, or CIN8 to CIN15*	ADDRD

Note: * Available only for the H8S/2144B.

14.3.2 A/D Control/Status Register (ADCSR)

ADCSR controls A/D conversion operations.

Bit	Bit Name	Initial Value	R/W	Description
7	ADF	0	R/(W)*[1]	A/D End Flag A status flag that indicates the end of A/D conversion. [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends on all channels specified in scan mode [Clearing conditions] • When 0 is written after reading ADF = 1
6	ADIE	0	R/W	A/D Interrupt Enable Enables ADI interrupt by ADF when this bit is set to 1
5	ADST	0	R/W	A/D Start Setting this bit to 1 starts A/D conversion. Clearing this bit to 0 stops A/D conversion. In single mode, this bit is cleared to 0 automatically when conversion on the specified channel ends. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, or a transition to standby mode or module stop mode.
4	SCAN	0	R/W	Scan Mode Selects the A/D conversion operating mode. The setting of this bit must be made when conversion is halted (ADST = 0). 0: Single mode 1: Scan mode
3	CKS	0	R/W	Clock Select Sets A/D conversion time. The input channel setting must be made when conversion is halted (ADST = 0). 0: Conversion time is 266 states (max) 1: Conversion time is 134 states (max) Switch conversion time while ADST is 0.

Bit	Bit Name	Initial Value	R/W	Description	
2	CH2	0	R/W	Channel Select 2 to 0	
1	CH1	0	R/W	Select analog input channels. The input channel setting must be made when conversion is halted (ADST = 0).	
0	CH0	0	R/W	When SCAN = 0:	When SCAN = 1:
				000: AN0	000: AN0
				001: AN1	001: AN0 and AN1
				010: AN2	010: AN0 to AN2
				011: AN3	011: AN0 to AN3
				100: AN4	100: AN4
				101: AN5	101: AN4 and AN5
				110: AN6, or CIN0 to CIN7	110: AN4 to AN6 or CIN0 to CIN7
				111: AN7, or CIN8 to CIN15*[2]	111: AN4 to AN6 or CIN0 to CIN7, or AN7 or CIN8 to CIN15*[2]

Notes: 1. Only 0 can be written for clearing the flag.
2. CIN8 to CIN15 are available only for the H8S/2144B.

14.3.3 A/D Control Register (ADCR)

ADCR enables A/D conversion started by an external trigger signal.

Bit	Bit Name	Initial Value	R/W	Description
7	TRGS1	0	R/W	Timer Trigger Select 1 and 0
6	TRGS0	0	R/W	Enable the start of A/D conversion by a trigger signal. Only set bits TRGS1 and TRGS0 when conversion is halted (ADST = 0). 00: A/D conversion start by external trigger is disabled 01: A/D conversion start by external trigger is disabled 10: A/D conversion start by conversion trigger from TMR is enabled 11: A/D conversion start by $\overline{\text{ADTRG}}$ pin is enabled
5 to 0	—	All 1	R	Reserved These bits are always read as 1 and cannot be modified.

14.3.4 Keyboard Comparator Control Register (KBCOMP)

KBCOMP selects the CIN input channel for which A/D conversion is performed and enables or disables the comparator scan function of CIN15 to CIN0.

Bit	Bit Name	Initial Value	R/W	Description
7	IrE	0	R/W	These bits are related to the SCI. For details, refer to section 12.3.10, Keyboard Comparator Control Register (KBCOMP).
6	IrCKS2	0	R/W	
5	IrCKS1	0	R/W	
4	IrCKS0	0	R/W	
3	KBADE	0	R/W	Keyboard A/D Enable (AN6, AN7) Selects whether channels 6 and 7 of the A/D converter are used as analog pins or digital pins, in combination with the KBCH2 to KBCH0 bits. For details, refer to description for bits 2 to 0. Analog pins of the A/D converter are set to digital pins (CIN0 to CIN7 and CIN8 to CIN15*).
2	KBCH2	0	R/W	Keyboard A/D Channel Select 2 to 0
1	KBCH1	0	R/W	These bits select a channel of digital input pins for A/D conversion, in combination with the KBADE bit. The input channel setting must be made while conversion is halted.
0	KBCH0	0	R/W	

Channel 6	Channel 7
0xxx: Selects AN6	AN7
1000: Selects CIN0	CIN8*
1001: Selects CIN1	CIN9*
1010: Selects CIN2	CIN10*
1011: Selects CIN3	CIN11*
1100: Selects CIN4	CIN12*
1101: Selects CIN5	CIN13*
1110: Selects CIN6	CIN14*
1111: Selects CIN7	CIN15*

[Legend]

x: Don't care

Note: * CIN8 to CIN15 are available only for the H8S/2144B.

14.4 Operation

The A/D converter operates by successive approximation with 10-bit resolution. It has two operating modes: single mode and scan mode. When changing the operating mode or analog input channel, to prevent incorrect operation, first clear the ADST bit to 0 in ADCSR to halt A/D conversion. The ADST bit can be set at the same time as the operating mode or analog input channel is changed.

14.4.1 Single Mode

In single mode, A/D conversion is to be performed only once on the specified single channel. Operations are as follows.

1. A/D conversion on the specified channel is started when the ADST bit in ADCSR is set to 1, by software or an external trigger input.
2. When A/D conversion is completed, the result is transferred to the A/D data register corresponding to the channel.
3. On completion of A/D conversion, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When conversion ends, the ADST bit is automatically cleared to 0, and the A/D converter enters wait state.

14.4.2 Scan Mode

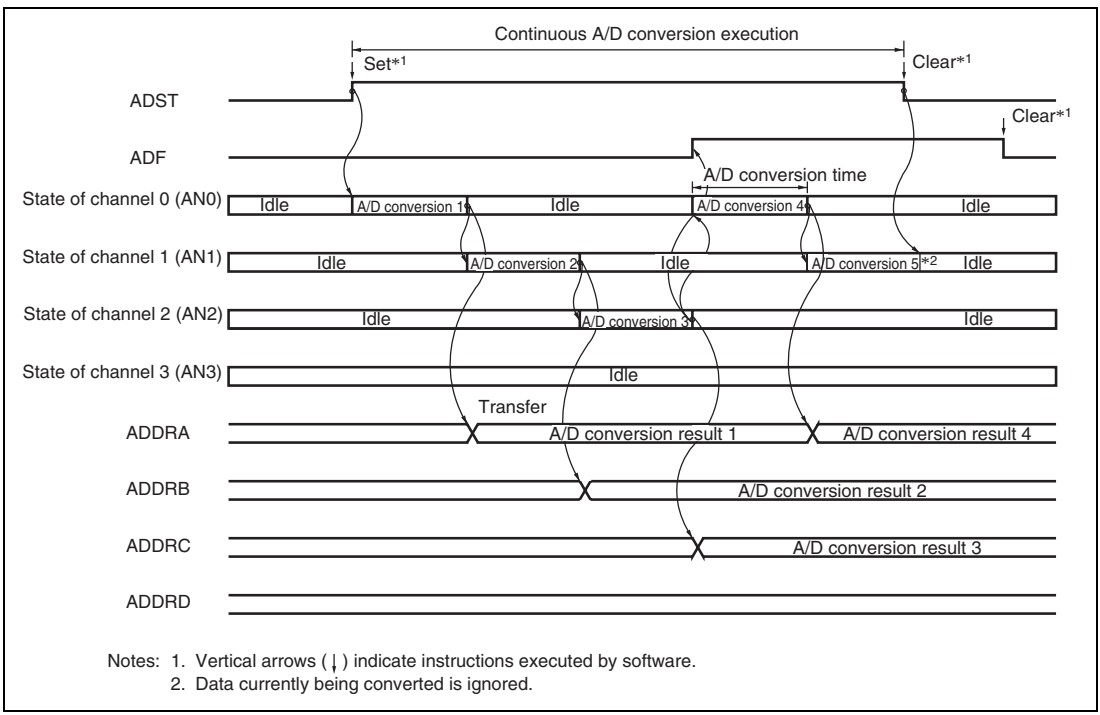
Scan mode is useful for monitoring analog inputs in a group of one or more channels. When the ADST bit is set to 1 by software, or by timer or external trigger input, A/D conversion starts on the first channel in the group (AN0 when CH2 = 0; AN4 when CH2 = 1).

When two or more channels are selected, after conversion of the first channel ends, conversion of the second channel (AN1 or AN5) starts immediately. A/D conversion continues cyclically on the selected channels until the ADST bit is cleared to 0. The conversion results are transferred for storage into the ADDR registers corresponding to the channels.

Typical operations when three channels (AN0 to AN2) are selected in scan mode are described below.

Figure 14.2 shows the operation timing.

1. Scan mode is selected (SCAN = 1), scan group 0 is selected (CH2 = 0), analog input channels AN0 to AN2 are selected (CH1 = 1, CH0 = 0), and A/D conversion is started (ADST = 1).
2. When A/D conversion of the first channel (AN0) is completed, the result is transferred to ADDRA. Next, conversion of the second channel (AN1) starts automatically.
3. Conversion proceeds in the same way through the third channel (AN2).
4. When conversion of all the selected channels (AN0 to AN2) is completed, the ADF flag is set to 1 and conversion of the first channel (AN0) starts again. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends.
5. Steps 2 to 4 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops. After that, if the ADST bit is set to 1, A/D conversion starts again from the first channel (AN0).



Notes: 1. Vertical arrows (↓) indicate instructions executed by software.
2. Data currently being converted is ignored.

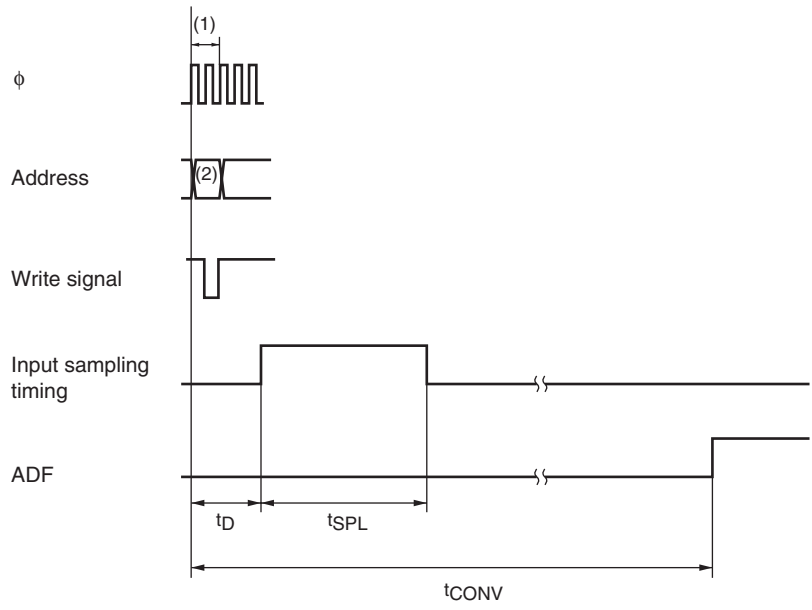
Figure 14.2 Example of A/D Converter Operation (Scan Mode, Channels AN0 to AN2 Selected)

14.4.3 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit. The A/D converter samples the analog input when the A/D conversion start delay time (t_D) passes after the ADST bit in ADCSR is set to 1, then starts A/D conversion. Figure 14.3 shows the A/D conversion timing. Table 14.3 indicates the A/D conversion time.

As indicated in figure 14.3, the A/D conversion time (t_{CONV}) includes t_D and the input sampling time (t_{SPL}). The length of t_D varies depending on the timing of the write access to ADCSR. The total conversion time therefore varies within the ranges indicated in table 14.3.

In scan mode, the values given in table 14.3 apply to the first conversion time. In the second and subsequent conversions, the conversion time is 256 state (fixed) when CKS = 0 and 128 states (fixed) when CKS = 1.



[Legend]
(1) : ADCSR write cycle
(2) : ADCSR address
t_D : A/D conversion start delay
t_{SPL} : Input sampling time
t_{CONV} : A/D conversion time

Figure 14.3 A/D Conversion Timing

Table 14.3 A/D Conversion Time (Single Mode)

		CKS = 0			CKS = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay time	t_D	10	—	17	6	—	9
Input sampling time	t_{SPL}	—	63	—	—	31	—
A/D conversion time	t_{CONV}	259	—	266	131	—	134

Note: * Values in the table indicate the number of states.

14.4.4 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGS1 and TRGS0 bits are set to B'11 in ADCR, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge at the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCSR, starting A/D conversion. Other operations, in both single and scan modes, are the same as when the ADST bit has been set to 1 by software. Figure 14.4 shows the timing.

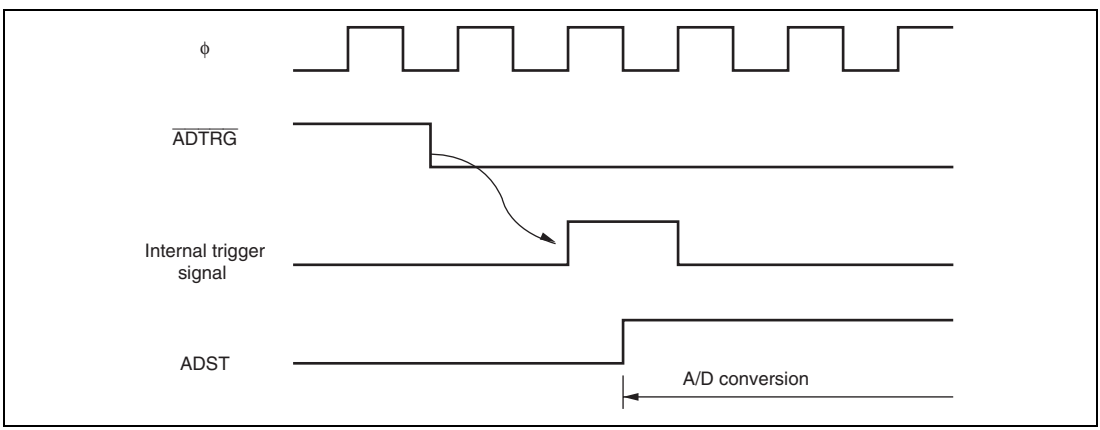


Figure 14.4 External Trigger Input Timing

14.5 Interrupt Sources

The A/D converter generates an A/D conversion end interrupt (ADI) at the end of A/D conversion. Setting the ADIE bit to 1 enables ADI interrupt requests while the ADF bit in ADCSR is set to 1 after A/D conversion is completed.

14.6 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 14.5).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value B'0000000000 (H'000) to B'0000000001 (H'001) (see figure 14.6).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from B'1111111110 (H'3FE) to B'1111111111 (H'3FF) (see figure 14.6).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristics between the zero voltage and the full-scale voltage. Does not include the offset error, full-scale error, or quantization error (see figure 14.6).
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes the offset error, full-scale error, quantization error, and nonlinearity error.

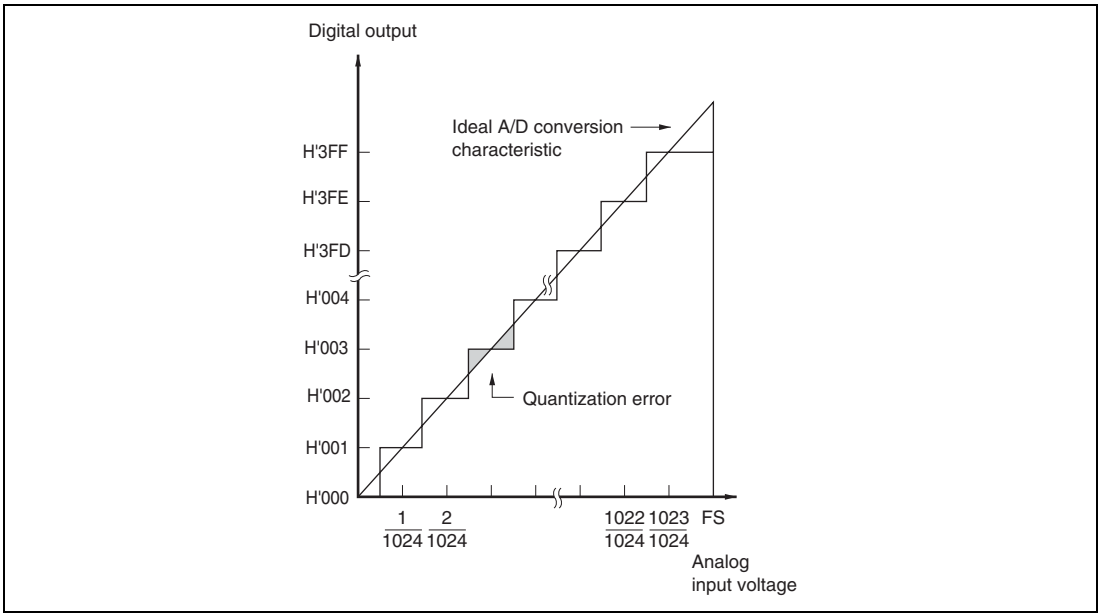


Figure 14.5 A/D Conversion Accuracy Definitions

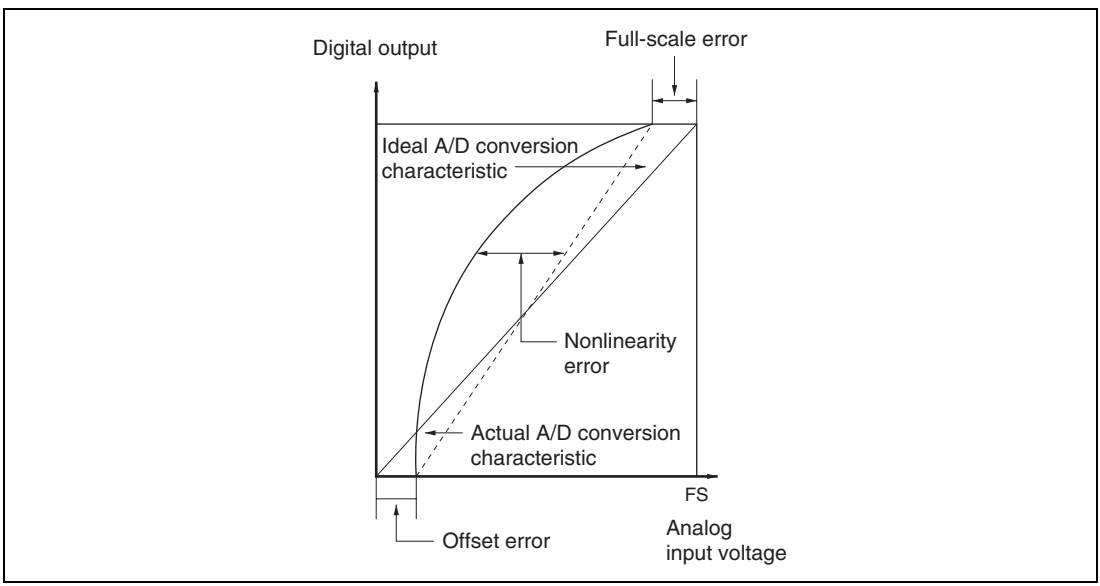


Figure 14.6 A/D Conversion Accuracy Definitions

14.7 Usage Notes

14.7.1 Permissible Signal Source Impedance

Analog inputs of this LSI are designed so that the conversion accuracy is guaranteed for an input signal for which the signal source impedance is 5 kΩ or less. This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance exceeds 5 kΩ, charging may be insufficient and it may not be possible to guarantee the A/D conversion accuracy. However, if a large capacitance is provided externally in single mode, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, since a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., voltage fluctuation ratio of 5 mV/µs or greater) (see figure 14.7). When converting a high-speed analog signal or converting in scan mode, a low-impedance buffer should be inserted. For details on the 5-V version, refer to section 20, Electrical Characteristics.

14.7.2 Influences on Absolute Accuracy

Adding capacitance results in coupling with ground, and therefore noise in ground may adversely affect the absolute accuracy. Be sure to make the connection to an electrically stable ground such as AVss.

Care is also required to insure that filter circuits do not communicate with digital signals on the mounting board, so acting as antennas.

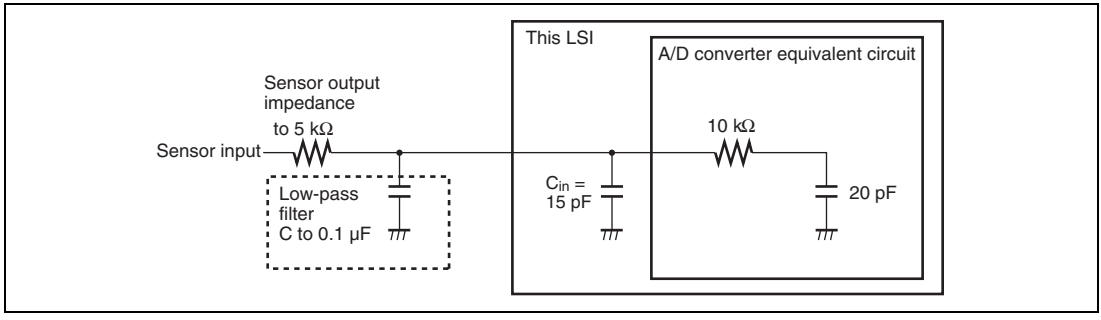


Figure 14.7 Example of Analog Input Circuit

14.7.3 Setting Range of Analog Power Supply and Other Pins

If conditions shown below are not met, the reliability of this LSI may be adversely affected.

- Analog input voltage range
  The voltage applied to analog input pin ANn during A/D conversion should be in the following range.
  — AVss ≤ ANn ≤ AVref* for the H8S/2144B (n = 0 to 7)
  Note: * AVref is available only for the H8S/2144B.
  — AVss ≤ ANn ≤ AVcc for the H8S/2134B (n = 0 to 7).
- Digital input voltage range
  The voltage applied to digital input pin CINn should be in the following range.
  — AVss ≤ CINn ≤ AVref* and Vss ≤ CINn ≤ Vcc for the H8S/2144B (n = 0 to 15)
  Note: * AVref is available only for the H8S/2144B.
  — AVss ≤ CINn ≤ AVcc and Vss ≤ CINn ≤ Vcc for the H8S/2134B (n = 0 to 7)
- Relation between AVcc, AVss and Vcc, Vss
  For the relationship between AVcc, AVss and Vcc, Vss, set AVss = Vss. If the A/D converter is not used, the AVcc and AVss pins must on no account be left open.
- AVref* pin reference voltage specification range
  The reference voltage of the AVref* pin should be in the range AVref* ≤ AVcc.
  Note: * AVref is available only for the H8S/2144B.

14.7.4 Notes on Board Design

In board design, digital circuitry and analog circuitry should be as mutually isolated as possible, and layout in which digital circuit signal lines and analog circuit signal lines cross or are in close proximity should be avoided as far as possible. Failure to do so may result in incorrect operation of the analog circuitry due to inductance, adversely affecting A/D conversion values. Also, digital circuitry must be isolated from the analog input signals (AN0 to AN7), analog reference voltage (AVref*), and analog power supply (AVcc) by the analog ground (AVss). Also, the analog ground (AVss) should be connected at one point to a stable digital ground (Vss) on the board.

Note: * AVref is available only for the H8S/2144B.

14.7.5 Notes on Noise Countermeasures

A protection circuit connected to prevent damage due to an abnormal voltage such as an excessive surge at the analog input pins (AN0 to AN7) and analog reference voltage (AVref*) should be connected between AVcc and AVss as shown in figure 14.8. Also, the bypass capacitors connected to AVcc and AVref*, and the filter capacitor connected to AN2 to AN7, must be connected to AVSS.

If a filter capacitor is connected, the input currents at the analog input pins (AN0 to AN7) are averaged, and so an error may arise. Also, when A/D conversion is performed frequently, as in scan mode, if the current charged and discharged by the capacitance of the sample-and-hold circuit in the A/D converter exceeds the current input via the input impedance (Rin), an error will arise in the analog input pin voltage. Careful consideration is therefore required when deciding the circuit constants.

Note: * AVref is available only for the H8S/2144B.

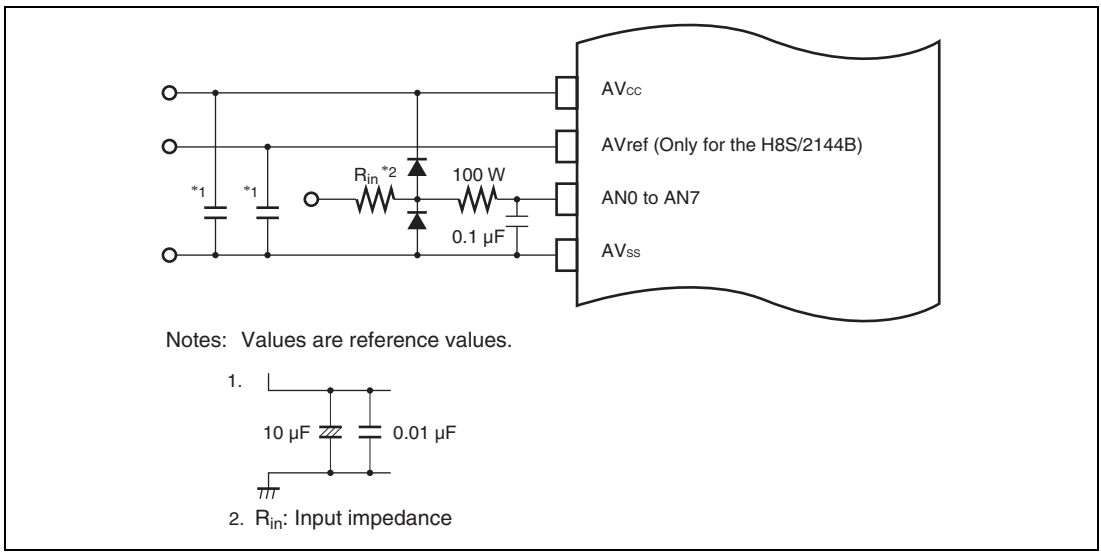
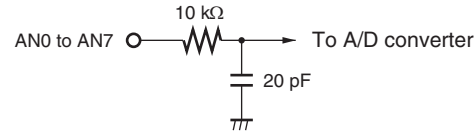


Figure 14.8 Example of Analog Input Protection Circuit



Note:* Values are reference values.

Figure 14.9 Equivalent Circuit of Analog Input Pin

14.7.6 Module Stop Mode Setting

A/D converter operation can be enabled or disabled using the module stop control register. The initial setting is for A/D converter operation to be halted. Register access is enabled by canceling module stop mode. For details, refer to section 18, Power-Down Modes.

Section 15 RAM

This LSI has an on-chip high-speed static RAM. The RAM is connected to the CPU by a 16-bit data bus, enabling one-state access by the CPU to both byte data and word data.

The on-chip RAM can be enabled or disabled by means of the RAME bit in the system control register (SYSCR). For details on SYSCR, refer to section 3.2.2, System Control Register (SYSCR).

Product Classification		RAM Capacitance	RAM Address
Flash memory version	H8S/2144B	4 kbytes	H'E080 to H'EFFF, H'FF00 to H'FF7F
	H8S/2134B	4 kbytes	H'E080 to H'EFFF, H'FF00 to H'FF7F

Section 16 ROM

This LSI has an on-chip ROM (flash memory or masked ROM). The features of the flash memory are summarized below.

A block diagram of the flash memory is shown in figure 16.1.

16.1 Features

- Size

Product Classification	RAM Capacitance	ROM Address
H8S/2144B	128 kbytes	H'000000 to H'01FFFF (mode 2) H'0000 to H'DFFF (mode 3)
H8S/2134B	128 kbytes	H'000000 to H'01FFFF (mode 2) H'0000 to H'DFFF (mode 3)

- Programming/erasing methods

  The flash memory is programmed 128 bytes at a time. Erasure is performed in single-block units. The flash memory is configured as follows: 32 kbytes × 2 blocks, 8 kbytes × 2 blocks, 16 kbytes × 1 block, 28 kbytes × 1 block, and 1 kbyte × 4 blocks

  To erase the entire flash memory, each block must be erased in turn.
- Programming/erasing time

  It takes 10 ms (typ.) to program the flash memory 128 bytes at a time; 80 µs (typ.) per 1 byte. Erasing one block takes 100 ms (typ.).
- Reprogramming capability

  The flash memory can be reprogrammed up to 100 times.
- Two flash memory on-board programming modes
  - Boot mode
  - User program mode

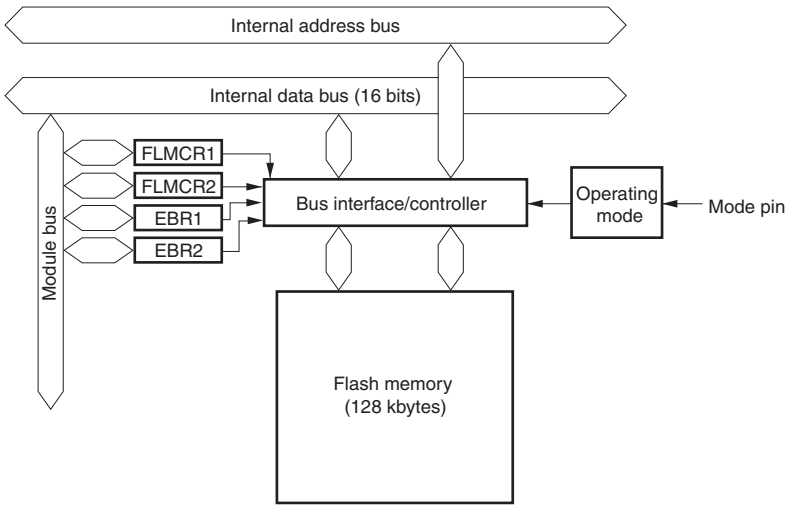
  On-board programming/erasing can be done in boot mode in which the boot program built into the chip is started for erasure or programming of the entire flash memory. In user program mode, individual blocks can be erased or programmed.
- Automatic bit rate adjustment

  With data transfer in boot mode, this LSI's bit rate can be automatically adjusted to match the transfer bit rate of the host.

- Programming/erasing protection

  Sets protection against flash memory programming/erasing via hardware, software, or error protection.
- Programmer mode

  In addition to on-board programming mode, programmer mode is supported to program or erase the flash memory using a PROM programmer.



[Legend]
FLMCR1: Flash memory control register 1
FLMCR2: Flash memory control register 2
EBR1: Erase block register 1
EBR2: Erase block register 2

Figure 16.1 Block Diagram of Flash Memory

16.2 Mode Transitions

When the mode pins are set in the reset state and a reset-start is executed, this LSI enters an operating mode as shown in figure 16.2. In user mode, flash memory can be read but not programmed or erased. The boot, user program, and programmer modes are provided as modes to write and erase the flash memory.

The differences between boot mode and user program mode are shown in table 16.1. Figure 16.3 shows the boot mode and figure 16.4 shows the user program mode.

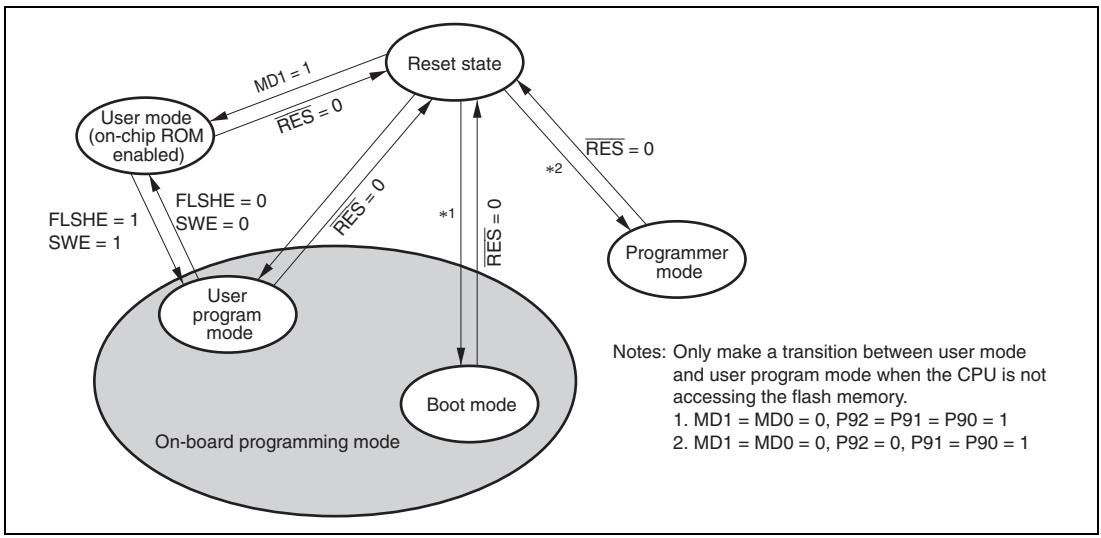


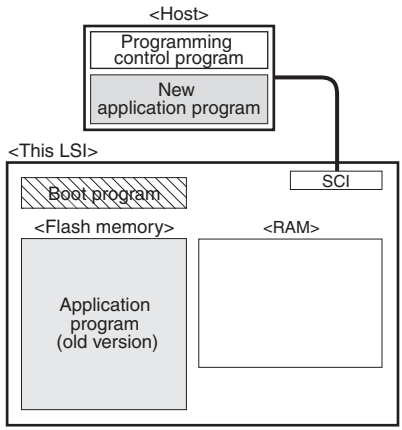
Figure 16.2 Flash Memory State Transitions

Table 16.1 Differences between Boot Mode and User Program Mode

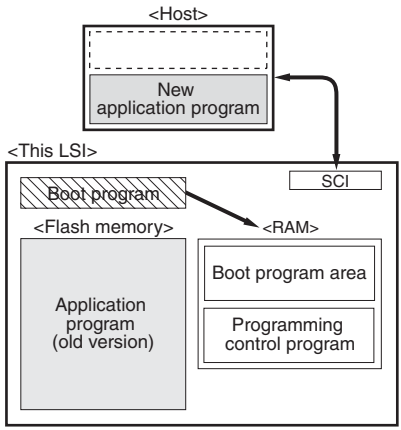
	Boot Mode	User Program Mode
Total erasure	Yes	Yes
Block erasure	No	Yes
Programming control program*	Programming/programming-verifying	Programming/programming-verifying
		Erasing/erasing-verifying

Note: * Should be provided by the user, in accordance with the recommended algorithm.

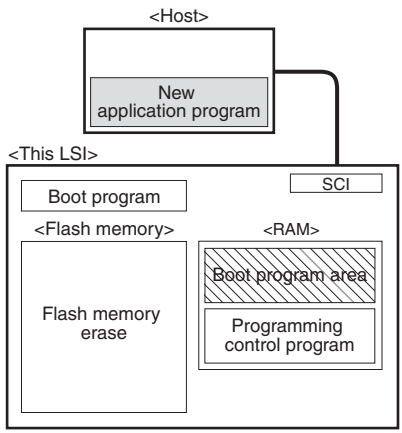
1. Initial state
   The flash memory is erased at shipment. The following describes how to write over an old-version application program or data in the flash memory. The user should prepare the programming control program and new application program beforehand in the host.



2. SCI communication check
   When boot mode is entered, the boot program in this LSI (originally incorporated in the chip) is started and SCI communication is checked. Then the boot program required for flash memory erasing is automatically transferred to the RAM boot program area.



3. Flash memory initialization
   The erase program in the boot program area (in RAM) is executed, and the flash memory is initialized (to H'FF). In boot mode, total flash memory erasure is performed, without regard to blocks.



4. Programming new application program
   The programming control program transferred from the host to RAM via SCI communication is executed, and the new application program in the host is written into the flash memory.

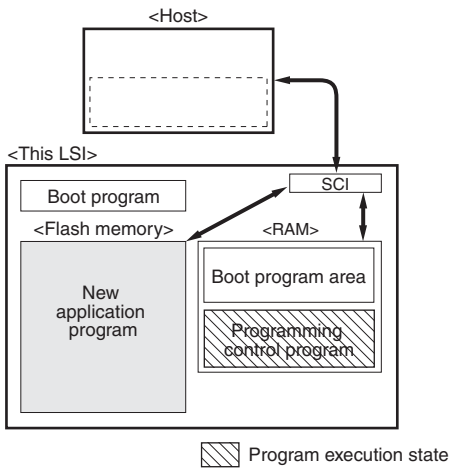
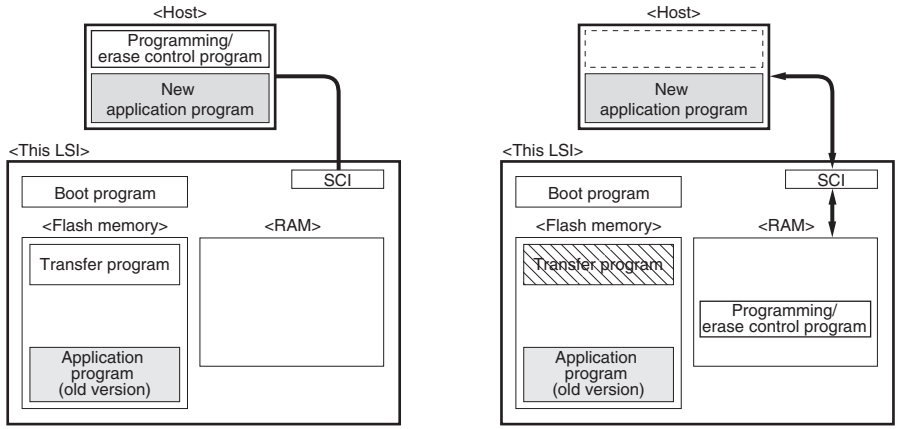


Figure 16.3 Boot Mode

1. Initial state
   (1) The program that will transfer the programming/erase control program from flash memory to on-chip RAM should be written into the flash memory by the user beforehand.
   (2) The programming/erase control program should be prepared in the host or in the flash memory.

2. Programming/erase control program transfer
   The transfer program in the flash memory is executed and the programming/erase control program is transferred to RAM.



3. Flash memory initialization
   The programming/erase program in RAM is executed, and the flash memory is initialized (to H'FF). Erasing can be performed in block units, but not in byte units.

4. Writing new application program
   Next, the new application program in the host is written into the erased flash memory blocks. Do not write to unerased blocks.

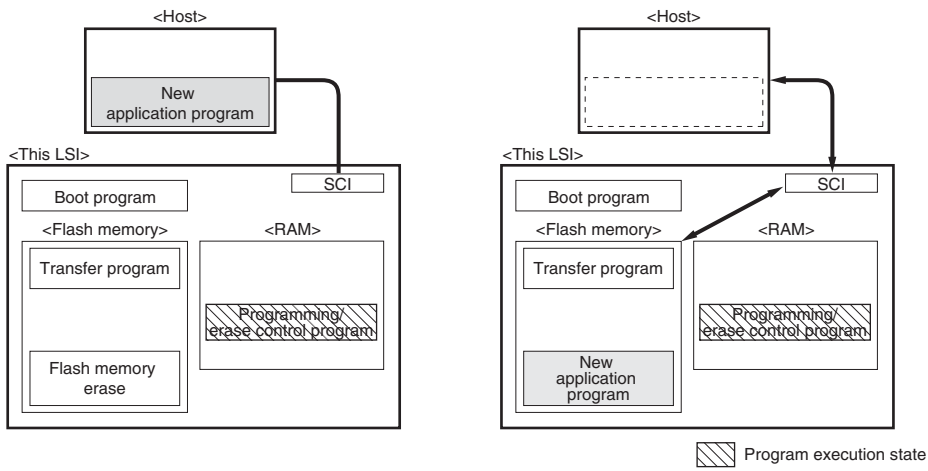


Figure 16.4 User Program Mode (Example)

16.3 Block Configuration

16.3.1 Block Configuration

Figure 16.5 shows the block configuration of 128-kbyte flash memory. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. The flash memory is divided into 8 kbytes (2 blocks), 16 kbytes (1 block), 28 kbytes (1 block), and 1 kbyte (4 blocks). Erasing is performed in these divided units. Programming is performed in 128-byte units starting from an address whose lower bits are H'00 or H'80.

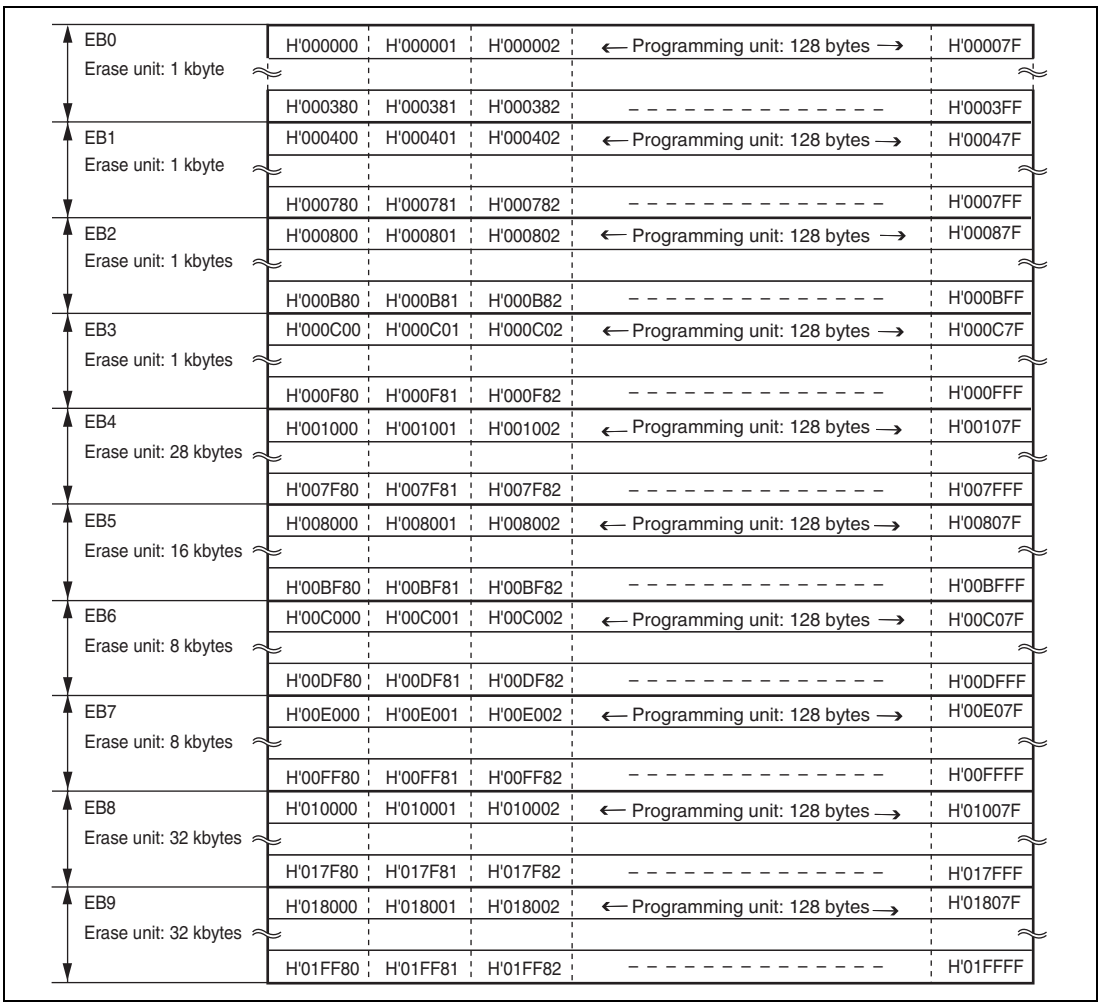


Figure 16.5 Flash Memory Block Configuration

16.4 Input/Output Pins

The flash memory is controlled by means of the pins shown in table 16.2.

Table 16.2 Pin Configuration

Pin Name	I/O	Function
$\overline{\text{RES}}$	Input	Reset
MD1	Input	Sets this LSI's operating mode
MD0	Input	Sets this LSI's operating mode
P92	Input	Sets this LSI's operating mode
P91	Input	Sets this LSI's operating mode
P90	Input	Sets this LSI's operating mode
TxD1	Output	Serial transmit data output
RxD1	Input	Serial receive data input

16.5 Register Descriptions

The flash memory has the following registers. To access FLMCR1, FLMCR2, EBR1, or EBR2, the FLSHE bit in the serial/timer control register (STCR) should be set to 1. For details on the serial/timer control register, refer to section 3.2.3, Serial/Timer Control Register (STCR).

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Erase block register 2 (EBR2)

16.5.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1, used together with FLMCR2, makes the flash memory enter the programming mode, programming-verifying mode, erasure mode, or erasure-verifying mode. For details on register setting, refer to section 16.8, Flash Memory Programming/Erasing.

FLMCR1 is initialized to H'80 by a reset, or in hardware standby mode, software standby mode, sub-active mode, sub-sleep mode, or watch mode.

Bit	Bit Name	Initial Value	R/W	Description
7	FWE	1	R	Flash Write Enable Controls programming/erasing of on-chip flash memory. This bit is always read as 0, and cannot be modified.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, the EV, PV, E, and P bits in this register, the ESU and PSU bits in FLMCR2, and all EBR1 and EBR2 bits cannot be set to 1. Do not clear these bits and SWE to 0 simultaneously.
5	—	0	R	Reserved
4	—	0	R	These bits are always read as 0 and cannot be modified.
3	EV	0	R/W	Erasing-Verifying When this bit is set to 1 while SWE = 1, the flash memory transits to erasure-verifying mode. When it is cleared to 0, erasure-verifying mode is cancelled.
2	PV	0	R/W	Programming-Verifying When this bit is set to 1 while SWE = 1, the flash memory transits to programming-verifying mode. When it is cleared to 0, programming-verifying mode is cancelled.
1	E	0	R/W	Erasure When this bit is set to 1 while SWE = 1 and ESU = 1, the flash memory enters the erasing mode. When it is cleared to 0, erasing mode is cancelled.

Bit	Bit Name	Initial Value	R/W	Description
0	P	0	R/W	Program When this bit is set to 1 while SWE = 1 and PSU = 1, the flash memory enters the programming mode. When it is cleared to 0, programming mode is cancelled.

16.5.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 monitors the state of flash memory programming/erasing protection (error protection) and sets up the flash memory to transit to programming/erasing mode. FLMCR2 is initialized to H'00 by a reset or in hardware standby mode. The ESU and PSU bits are cleared to 0 in software standby mode, sub-active mode, sub-sleep mode, or watch mode, or when the SWE bit in FLMCR1 is cleared to 0.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Flash memory error Indicates that an error has occurred during flash memory programming/erasing. When this bit is set to 1, flash memory goes to the error-protection state. For details, see section 16.9.3, Error Protection.
6 to 2	—	All 0	R/(W)	Reserved The initial values should not be modified.
1	ESU	0	R/W	Erase Setup When this bit is set to 1 while SWE = 1, the flash memory transits to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E bit in FLMCR1 to 1.
0	PSU	0	R/W	Program Setup When this bit is set to 1 while SWE = 1, the flash memory enters the programming setup state. When it is cleared to 0, the programming setup state is cancelled. Set this bit to 1 before setting the P bit in FLMCR1 to 1.

16.5.3 Erase Block Registers 1 and 2 (EBR1, EBR2)

EBR1 and EBR2 are used to specify the flash memory erase block. EBR1 and EBR2 are initialized to H’00 by a reset, or in hardware standby mode, software standby mode, sub-active mode, sub-sleep mode, or watch mode, or when the SWE bit in FLMCR1 is cleared to 0. Set only one bit to 1 at a time, otherwise all bits in EBR1 and EBR2 are automatically cleared to 0.

- EBR1

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	—	All 0	R/(W)	Reserved The initial values should not be modified.

- EBR2

Bit	Bit Name	Initial Value	R/W	Description
7	EB7	0	R/W*	When this bit is set to 1, 8 kbytes of EB7 (H'00E000 to H’00FFFF) are to be erased.
6	EB6	0	R/W	When this bit is set to 1, 8 kbytes of EB6 (H'00C000 to H’00DFFF) are to be erased.
5	EB5	0	R/W	When this bit is set to 1, 16 kbytes of EB5 (H'008000 to H'00BFFF) are to be erased.
4	EB4	0	R/W	When this bit is set to 1, 28 kbytes of EB4 (H'001000 to H'007FFF) are to be erased.
3	EB3	0	R/W	When this bit is set to 1, 1 kbyte of EB3 (H'000C00 to H'000FFF) is to be erased.
2	EB2	0	R/W	When this bit is set to 1, 1 kbyte of EB2 (H'000800 to H'000BFF) is to be erased.
1	EB1	0	R/W	When this bit is set to 1, 1 kbyte of EB1 (H'000400 to H'0007FF) is to be erased.
0	EB0	0	R/W	When this bit is set to 1, 1 kbyte of EB0 (H'000000 to H'0003FF) is to be erased.

Note: * In normal mode, this bit is always read as 0 and cannot be modified.

16.6 Operating Modes

The flash memory is connected to the CPU via a 16-bit data bus, enabling byte data and word data to be accessed in a single state. Even addresses are connected to the upper 8 bits and odd addresses are connected to the lower 8 bits. Note that word data must start from an even address.

On-chip ROM is enabled or disabled by the mode select pins (MD1 and MD0) and the EXPE bit in MDCR, as summarized in table 16.3.

In normal mode (mode 3), up to 56 kbytes of ROM can be used.

Table 16.3 Operating Modes and ROM

Operating Modes			Mode Pins		MDCR	
MCU Operating Mode	**CPU Operating Mode**	**Mode**	**MD1**	**MD0**	**EXPE**	**On-Chip ROM**
Mode 1	Normal	Expanded mode with on-chip ROM disabled	0	1	1	Disabled
Mode 2	Advanced	Single-chip mode	1	0	0	Enabled (128 kbytes)
	Advanced	Expanded mode with on-chip ROM enabled	1	0	1	
Mode 3	Normal	Single-chip mode	1	1	0	Enabled (56 kbytes)
	Normal	Expanded mode with on-chip ROM enabled	1	1	1	

16.7 On-Board Programming Modes

An on-board programming mode is used to perform on-chip flash memory programming, erasing, and verification. This LSI has two on-board programming modes: boot mode and user program mode. Table 16.4 shows pin settings for boot mode. In user program mode, operation by software is enabled by setting control bits. For details on flash memory mode transitions, see figure 16.2.

Table 16.4 On-Board Programming Mode Settings

Mode Setting		MD1	MD0	P92	P91	P90
Boot mode		0	0	1*	1*	1*
User program mode	Mode 2 (advanced mode)	1	0	—	—	—
	Mode 3 (normal mode)	1	1	—	—	—

Note: * Can be used as an I/O port after the boot mode activation.

16.7.1 Boot Mode

Table 16.5 shows the boot mode operations between reset end and branching to the programming control program.

1. When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. Prepare a programming control program in accordance with the description in section 16.8, Flash Memory Programming/Erasing. In boot mode, if any data exists in the flash memory (except in the case that all data are 1), all blocks in the flash memory are erased. Use boot mode at initial writing in the on-board state, or forced recovery when user program mode cannot be executed because the program to be initiated in user program mode was mistakenly erased.
2. The SCI_1 should be set to asynchronous mode, and the transfer format as follows: 8-bit data, 1 stop bit, and no parity.
3. When the boot program is initiated, this LSI measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. This LSI then calculates the bit rate of transmission from the host, and adjusts the SCI_1 bit rate to match that of the host. The reset should end with the RxD1 pin high. The RxD1 and TxD1 pins should be pulled up on the board if necessary. After the reset ends, it takes approximately 100 states before this LSI is ready to measure the low-level period.

4. After matching the bit rates, this LSI transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to this LSI. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and this LSI. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 16.6.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. Addresses H'FFE080 to H'FFE87F is the area to which the programming control program is transferred from the host. Note, however, that ID codes are assigned to addresses H'FFE080 to H'FFE087. The boot program area cannot be used until the execution state in boot mode switches to the programming control program. Figure 16.8 shows the on-chip RAM area in boot mode.
6. Before branching to the programming control program (H'FFE088 in the RAM area), this LSI terminates transfer operations by the SCI_1 (by clearing the RE and TE bits in SCR to 0), but the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of write data or verifying data with the host. The TxD1 pin is in high-level output state. The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, since the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by a reset. Cancel the reset*[1] after driving the reset pin low, waiting at least 20 states, and then setting the mode pins. Boot mode is also cleared when a WDT overflow occurs.
8. Do not change the mode pin input levels in boot mode. If mode pin input levels are changed from low to high during reset, operating modes are switched and the state of ports that are also used for address output and bus control output signals ($\overline{AS}$, $\overline{RD}$, and $\overline{HWR}$) are changed*[5]. Therefore, set these pins carefully not to be output signals during reset or not to conflict with LSI external signals.
9. All interrupts are disabled during programming or erasing of the flash memory.

Notes: 1. After a reset is released, the timing for setting the signal levels on mode pins must satisfy the mode programming setup time (t_{MDS} = 4 cycles).

2. The ports that also have address output functions output low as address output when the mode pins are set to mode 1 during a reset. In modes other than mode 1, it enters the high impedance state. Bus control output signals output high when the mode pins are set to mode 1 during a reset. In modes other than mode 1, it enters the high impedance state.

Table 16.5 Boot Mode Operation

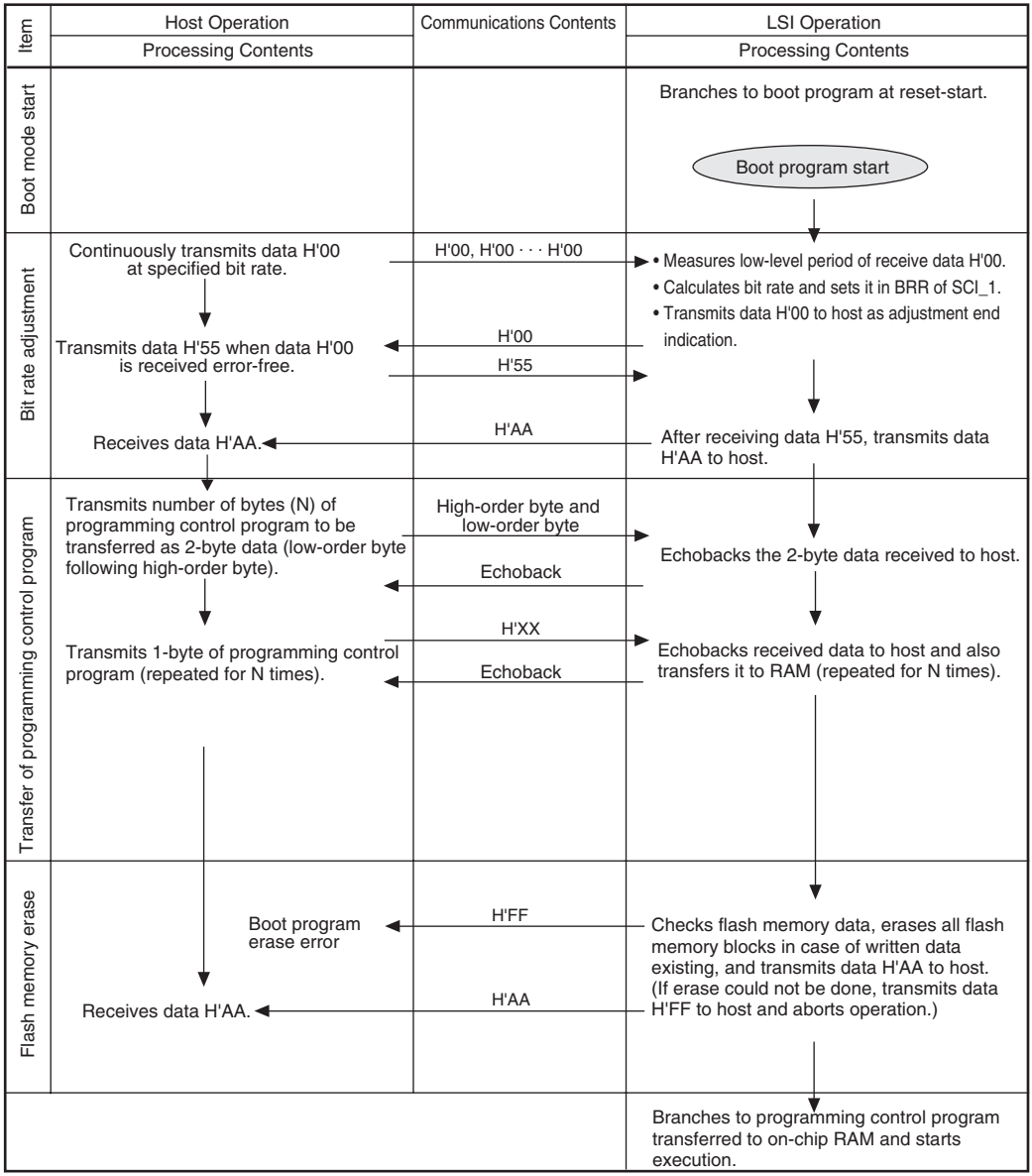
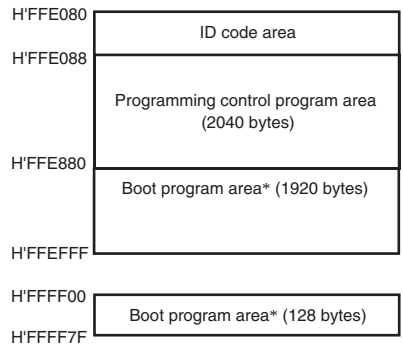


Table 16.6 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate is Possible

Host Bit Rate	System Clock Frequency Range of This LSI
19200 bps	8 to 20 MHz
9600 bps	4 to 20 MHz
4800 bps	2 to 18 MHz



Note: The boot program area and area which is not used cannot be used until a transition is made to the execution state for the programming control program transferred to RAM. Note that the contents of the boot program area in RAM are remained after a branch is made to the programming control program.

Figure 16.6 On-Chip RAM Area in Boot Mode

In boot mode, this LSI checks the contents of the 8-byte ID code area as shown below to confirm that the programming control program corresponds with this LSI. To originally write a programming control program to be used in boot mode, the above 8-byte ID code must be added at the beginning of the program.

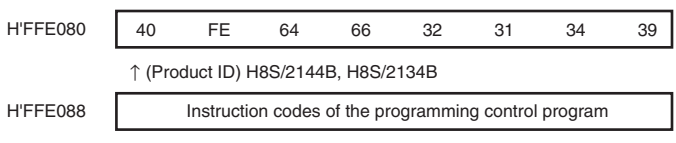


Figure 16.7 ID Code Area

16.7.2 User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user programming/erasing control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user programming/erasing control program or a program which provides the user programming/erasing control program from external memory. Because the flash memory itself cannot be read during programming/erasing, transfer the user programming/erasing control program to on-chip RAM, as like in boot mode. Figure 16.10 shows a sample procedure for programming/erasing in user program mode. Prepare a user programming/erasing control program in accordance with the description in section 16.8, Flash Memory Programming/Erasing.

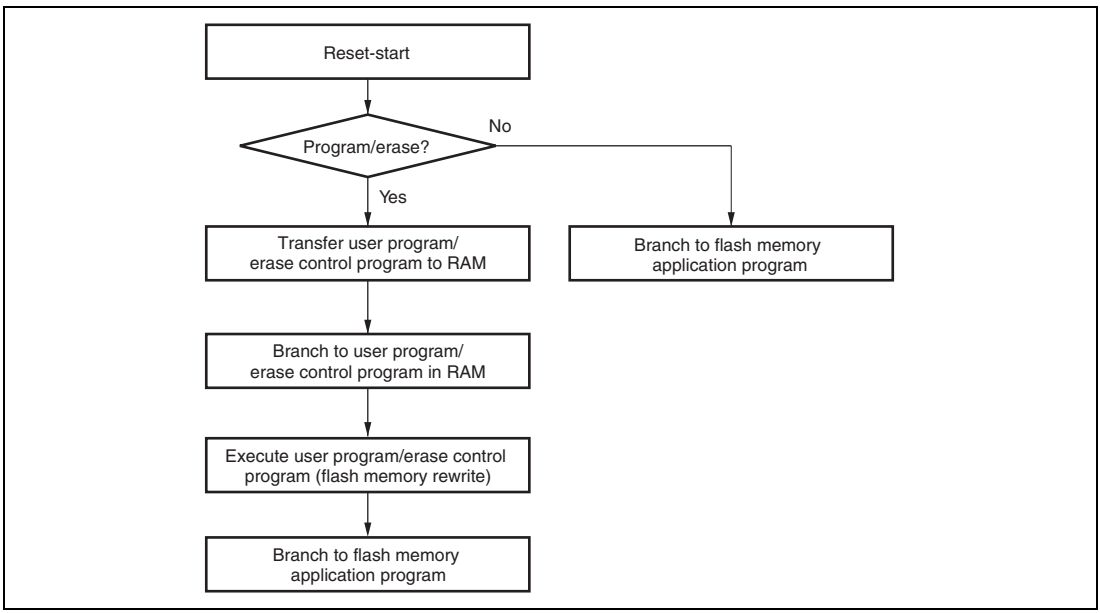


Figure 16.8 Programming/Erasing Flowchart Example in User Program Mode

16.8 Flash Memory Programming/Erasing

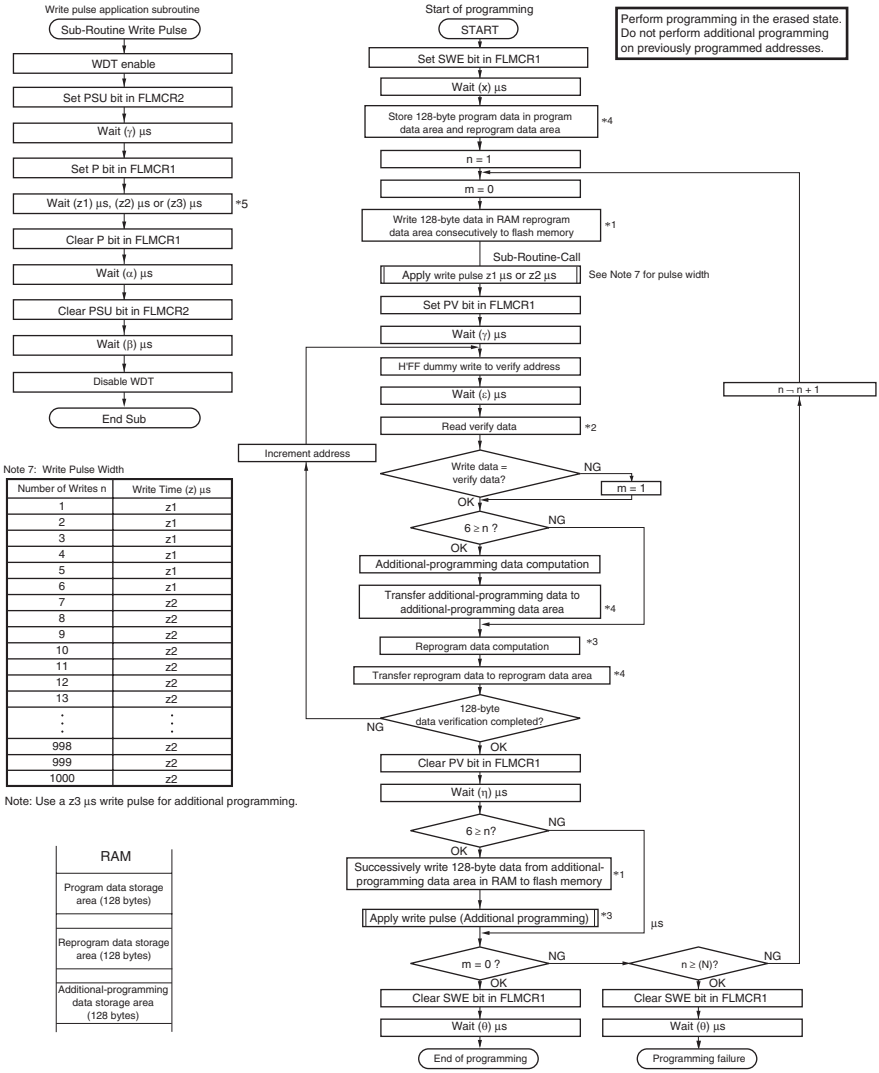
A software method, using the CPU, is employed to program and erase flash memory in the on-board programming modes. Depending on the FLMCR1 and FLMCR2 settings, the flash memory operates in one of the following four modes: programming mode, programming-verifying mode, erasing mode, and erasing-verifying mode. The programming control program in boot mode and the user programming/erasing control program in user program mode use these operating modes in combination to perform programming/erasing. Flash memory programming and erasing should be performed in accordance with the descriptions in section 16.8.1, Programming/Programming-Verifying and section 16.8.2, Erasing/Erasing-Verifying, respectively.

16.8.1 Programming/Programming-Verifying

When writing data or programs to the flash memory, the programming/programming-verifying flowchart shown in figure 16.11 should be followed. Performing programming operations according to this flowchart will enable data or programs to be written to the flash memory without subjecting this LSI to voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to which programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer must be performed even if writing fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. Prepare the following data storage areas in RAM: a 128-byte programming data area, a 128-byte reprogramming data area, and a 128-byte additional-programming data area. Perform reprogramming data computation and additional programming data computation according to figure 16.9.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data area or additional-programming data area to the flash memory. The programming address and 128-byte data are latched in the flash memory. The lower 8 bits of the start address in the flash memory destination area must be H'00 or H'80.
5. The time during which the P bit is set to 1 is the programming time. Figure 16.9 shows the allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. The overflow cycle should be longer than $(y + z2 + \alpha + \beta)$ µs.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 2 bits are B'00. Verify data can be read in words from the address to which a dummy write was performed.

8. The maximum number of repetitions of the programming/programming-verifying sequence to the same bit is (N).



Note 7: Write Pulse Width

Number of Writes n	Write Time (z) µs
1	z1
2	z1
3	z1
4	z1
5	z1
6	z1
7	z2
8	z2
9	z2
10	z2
11	z2
12	z2
13	z2
⋮	⋮
998	z2
999	z2
1000	z2

Note: Use a z3 µs write pulse for additional programming.

Notes: 1. Data transfer is performed by byte transfer. The lower 8 bits of the first address written to must be H'00 or H'80. A 128-byte data transfer must be performed even if writing fewer than 128 bytes; in this case, H'FF data must be written to the extra addresses.
2. Verify data is read in 16-bit (word) units.
3. Even bits for which programming has been completed will be subjected to programming once again if the result of the subsequent verify operation is NG.
4. A 128-byte area for storing program data, a 128-byte area for storing reprogram data, and a 128-byte area for storing additional data must be provided in RAM. The contents of the reprogram data area and additional data area are modified as programming proceeds.
5. A write pulse of z1 µs or z2 µs is applied according to the progress of the programming operation. See Note7 for details of the pulse widths. When writing of additional-programming data is executed, a z3 µs write pulse should be applied. Reprogram data X' means reprogram data when the write pulse is applied.
6. The values of x, y, z1, z2, z3, α, β, γ, ε, η, θ, and N are shown in section 20.1.6, Flash Memory Characteristics, and section 20.2.6, Flash Memory Characteristics.

Reprogram Data Computation Table

Original Data (D)	Verify Data (V)	Reprogram Data (X)	Comments
0	0	1	Programming completed
0	1	0	Programming incomplete; reprogram
1	0	1	
1	1	1	Still in erased state; no action

Additional-Programming Data Computation Table

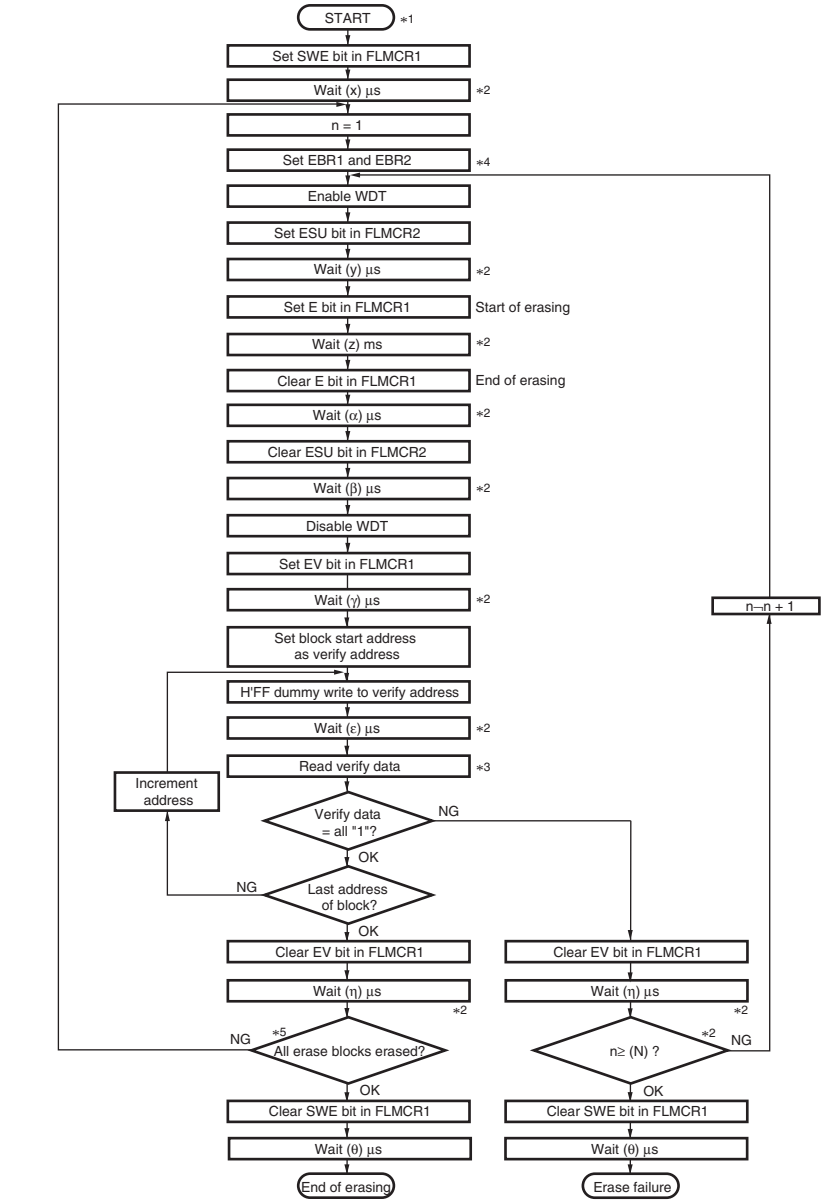
Reprogram Data (X')	Verify Data (V)	Additional-Programming Data (Y)	Comments
0	0	0	Additional programming to be executed
0	1	1	Additional programming not to be executed
1	0	1	
1	1	1	Additional programming not to be executed

Figure 16.9 Programming/Programming-Verifying Flowchart

16.8.2 Erasing/Erasing-Verifying

When erasing flash memory, the erasing/erasing-verifying flowchart shown in figure 16.10 should be followed.

1. Prewriting (setting erase block data to all 0) is not necessary.
2. Erasing is performed in block units. Make only a single-block specification in erase block registers 1 and 2 (EBR1 and EBR2). To erase multiple blocks, each block must be erased in turn.
3. The time during which the E bit is set to 1 is the flash memory erase time.
4. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. An overflow cycle of approximately ($y + z + \alpha + \beta$) ms is allowed.
5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower two bits are B'00. Verify data can be read in longwords from the address to which a dummy write was performed.
6. If the read data is unerased, set erase mode again, and repeat the erasing/erasure-verifying sequence as before. The maximum number of repetitions of the erasing/erasure-verifying sequence is N.



Notes: 1. Prewriting (writing 0 to all data in erased block) is not necessary.
2. The values of x, y, z, α, β, γ, ε, η, θ, and N are shown in section 20.1.6, Flash Memory Characteristics, and section 20.2.6, Flash Memory Characteristics.
3. Verify data is read in 16-bit (word) units.
4. Set only a single bit in EBR1 and EBR2. Do not set more than one bit.
5. Erasing is performed in block units. To erase multiple blocks, each block must be erased in turn.

Figure 16.10 Erasing/Erasing-Verifying Flowchart

16.9 Programming/Eraseing Protection

There are three kinds of flash memory programming/erasing protection: hardware protection, software protection, and error protection.

16.9.1 Hardware Protection

Hardware protection is a state in which programming/erasing of flash memory is forcibly disabled or aborted by a reset (including WDT overflow reset), or a transition to hardware standby mode, software standby mode, sub-active mode, sub-sleep mode or watch mode. Flash memory control registers 1 and 2 (FLMCR1 and FLMCR2) and erase block registers 1 and 2 (EBR1 and EBR2) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

16.9.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE bit in FLMCR1 to 0. When software protection is in effect, setting the P or E bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block registers 1 and 2 (EBR1 and EBR2), erase protection can be set for individual blocks. When EBR1 and EBR2 are set to H'00, erase protection is set for all blocks.

16.9.3 Error Protection

In error protection, an error is detected when the CPU’s runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the programming/erasing algorithm, and the programming/erasing operation is aborted. Aborting the programming/erasing operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling (excluding a reset) during programming/erasing
- When a SLEEP instruction is executed (transits to software standby mode, sleep mode, sub-active mode, sub-sleep mode, or watch mode) during programming/erasing
- When the bus ownership is released during programming/erasing

The FLMCR1, FLMCR2, EBR1, and EBR2 settings are retained, but programming mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be entered by setting the P or E bit to 1. However, because the PV and EV bit settings are retained, a transition to the verifying mode can be made. The error protection state can be cancelled by a reset or in hardware standby mode.

16.10 Interrupts during Flash Memory Programming/Erasing

In order to give the highest priority to programming/erasing operations, disable all interrupts including NMI input during flash memory programming/erasing (the P or E bit in FlMCR1 is set to 1) or boot program execution*[1].

1. If an interrupt is generated during programming/erasing, operation in accordance with the programming/erasing algorithm is not guaranteed.
2. CPU runaway may occur because normal vector reading cannot be performed in interrupt exception handling during programming/erasing*[2].
3. If an interrupt occurs during boot program execution, the normal boot mode sequence cannot be executed.

Notes: 1. Interrupt requests must be disabled inside and outside the CPU until the programming control program has completed programming.

2. The vector may not be read correctly for the following two reasons:

   If flash memory is read while being programmed or erased (while the P or E bit in FLMCR1 is set to 1), correct read data will not be obtained (undefined values will be returned).

   If the interrupt entry in the vector table has not been programmed yet, interrupt exception handling will not be executed correctly.

16.11 Programmer Mode

In programmer mode, the on-chip flash memory can be programmed/erased by a PROM programmer via a socket adapter, just like for a discrete flash memory. Use a PROM programmer that supports Renesas Technology 128-kbyte flash memory for microcomputer built-in type*. Figure 16.11 shows a memory map in programmer mode.

Note: Set the programming voltage of the PROM programmer to 3.3V.

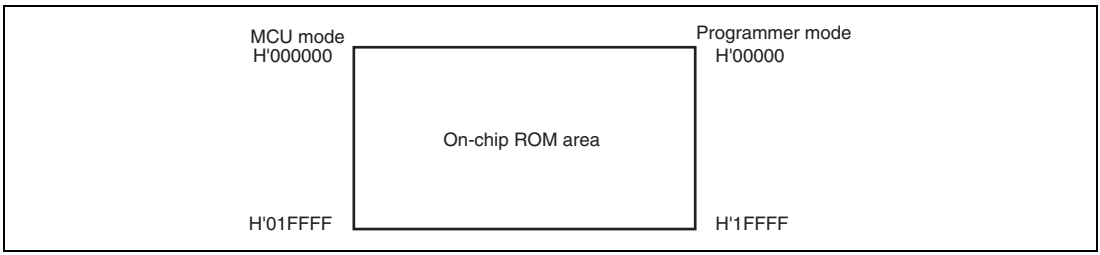


Figure 16.11 Memory Map in Programmer Mode

16.12 Usage Notes

The following lists notes on the use of on-board programming modes and programmer mode.

1. Perform programming/erasing with the specified voltage and timing.
   If a voltage higher than the rated voltage is applied, the product may be fatally damaged. Use a PROM programmer that supports Renesas Technology 128-kbyte flash memory for microcomputer built-in type. Do not set the programmer to HN28F101 or the programming voltage to 5.0 V.
2. Notes on power on/off
   At powering on or off the Vcc power supply, fix the $\overline{\text{RES}}$ pin to low and set the flash memory to hardware protection state. This power on/off timing must also be satisfied at a power-off and power-on caused by a power failure and other factors.
3. Perform flash memory programming/erasing in accordance with the recommended algorithm
   In the recommended algorithm, flash memory programming/erasing can be performed without subjecting this LSI to voltage stress or sacrificing program data reliability. When setting the P or E bit in FLMCR1 to 1, set the watchdog timer against program runaway.

4. Do not set/clear the SWE bit during program execution in the flash memory.

   Do not set/clear the SWE bit during program execution in the flash memory. An interval of at least 100 µs is necessary between program execution or data reading in flash memory and SWE bit clearing. When the SWE bit is set to 1, flash memory data can be modified, however, flash memory data can be read only in programming-verifying or erasing-verifying mode. Do not access the flash memory for a purpose other than verification during programming/erasing. Do not clear the SWE bit during programming, erasing, or verifying.

5. Do not use interrupts during flash memory programming/erasing

   In order to give the highest priority to programming/erasing operation, disable all interrupts including NMI input when the flash memory is programmed or erased.

6. Do not perform additional programming. Programming must be performed in the erased state.

   Program the area with 128-byte programming-unit blocks in on-board programming or programmer mode only once. Perform programming in the state where the programming-unit block is fully erased.

7. Ensure that the PROM programmer is correctly attached before programming.

   If the socket, socket adapter, or product index does not match the specifications, too much current flows and the product may be damaged.

8. Do not touch the socket adapter or LSI while programming.

   Touching either of these can cause contact faults and write errors.

Section 17 Clock Pulse Generator

This LSI incorporates a clock pulse generator, which generates the system clock (φ), bus master clock, and internal clock.

The clock pulse generator consists of an oscillator, duty correction circuit, clock select circuit, medium-speed clock divider, bus master clock select circuit, subclock input circuit, and waveform forming circuit. Figure 17.1 shows a block diagram of the clock pulse generator.

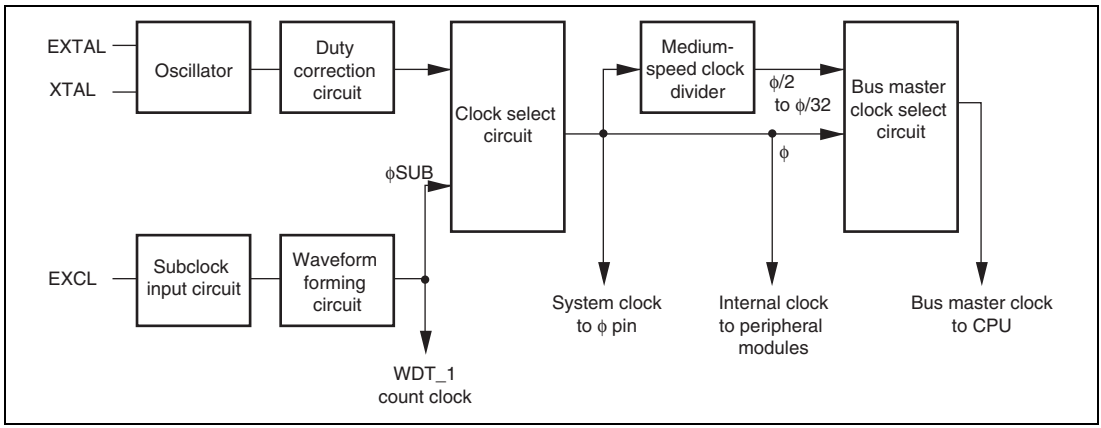


Figure 17.1 Block Diagram of Clock Pulse Generator

The bus master clock is selected as either high-speed mode or medium-speed mode by software according to the settings of the SCK2 to SCK0 bits in the standby control register. For details on the standby control register, refer to section 18.1.1, Standby Control Register (SBYCR).

The subclock input is controlled by software according to the EXCLE bit setting in the low power control register. For details on the low power control register, refer to section 18.1.2, Low Power Control Register (LPWRCR).

17.1 Oscillator

Clock pulses can be supplied either by connecting a crystal resonator, or by providing external clock input.

17.1.1 Connecting Crystal Resonator

Figure 17.2 shows a typical method of connecting a crystal resonator. An appropriate damping resistance R_d, given in table 17.1, should be used. An AT-cut parallel-resonance crystal resonator should be used.

Figure 17.3 shows the equivalent circuit of a crystal resonator. A resonator having the characteristics given in table 17.2 should be used.

A crystal resonator with frequency identical to that of the system clock (ϕ) should be used.

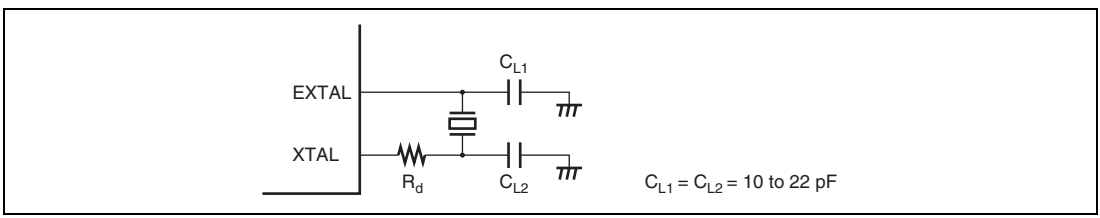


Figure 17.2 Typical Connection to Crystal Resonator

Table 17.1 Damping Resistance Values

Frequency (MHz)	2	4	8	10	12	16	20
R_d (Ω)	1 k	500	200	0	0	0	0

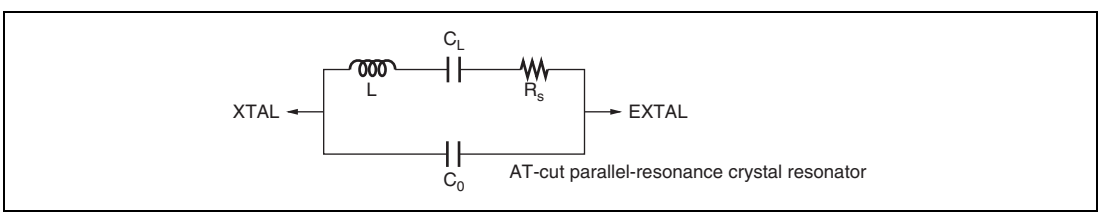


Figure 17.3 Equivalent Circuit of Crystal Resonator

Table 17.2 Crystal Resonator Parameters

Frequency (MHz)	2	4	8	10	12	16	20
R_S (max) (Ω)	500	120	80	70	60	50	40
C_0 (max) (pF)				7			

17.1.2 External Clock Input Method

Figure 17.4 shows a typical method of connecting an external clock signal. To leave the XTAL pin open, incidental capacitance should be 10 pF or less.

To input an inverted clock to the XTAL pin, the external clock should be set to high in standby mode, subactive mode, subsleep mode, and watch mode. External clock input conditions are shown in table 17.3. The frequency of the external clock should be the same as that of the system clock (ϕ).

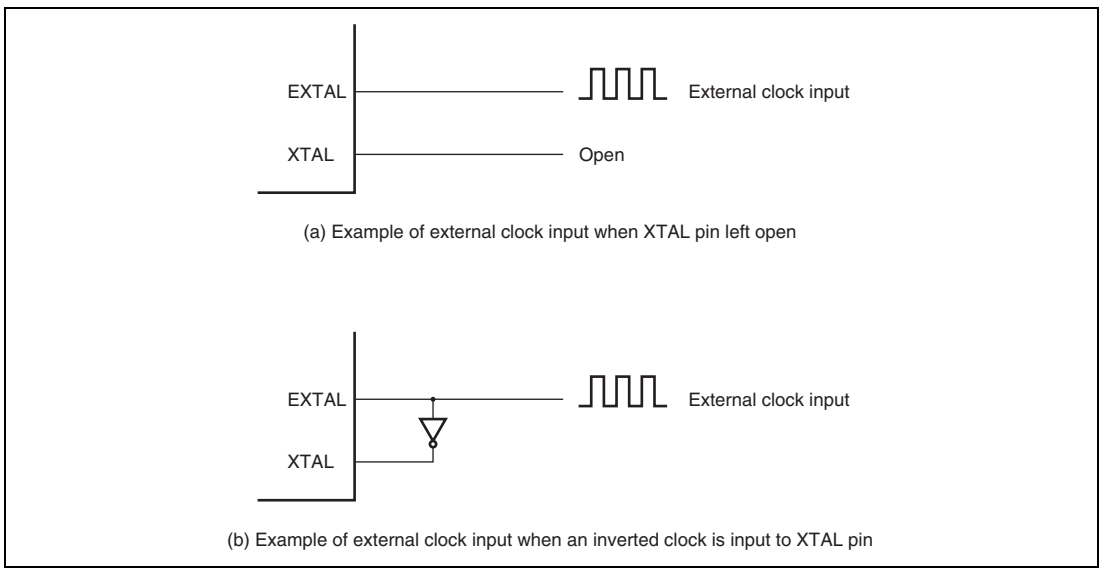


Figure 17.4 Example of External Clock Input

Table 17.3 External Clock Input Conditions

		V_{cc} = 4.0 to 5.5 V		V_{cc} = 5.0 V ± 10 %				
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Test Conditions**	
External clock input pulse width low level	t_{EXL}	25	—	20	—	ns	Figure 17.5	
External clock input pulse width high level	t_{EXH}	25	—	20	—	ns		
External clock rising time	t_{EXr}	—	5	—	5	ns		
External clock falling time	t_{EXf}	—	5	—	5	ns		
Clock pulse width low level	t_{CL}	0.4	0.6	0.4	0.6	t_{cyc}	$\phi \geq 5$ MHz	Figure 20.4
		80	—	80	—	ns	$\phi < 5$ MHz	
Clock pulse width high level	t_{CH}	0.4	0.6	0.4	0.6	t_{cyc}	$\phi \geq 5$ MHz	
		80	—	80	—	ns	$\phi < 5$ MHz	

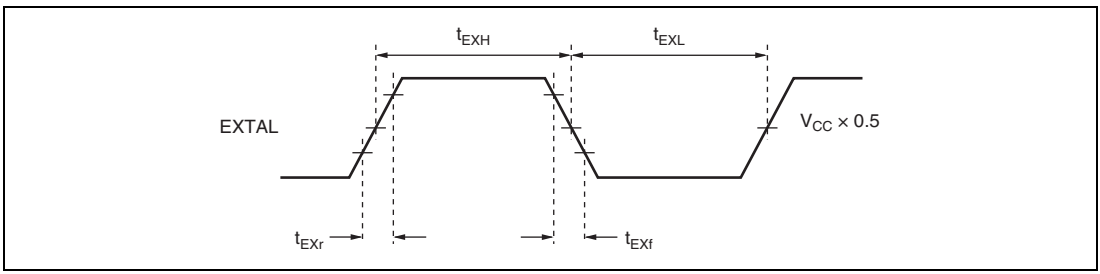


Figure 17.5 External Clock Input Timing

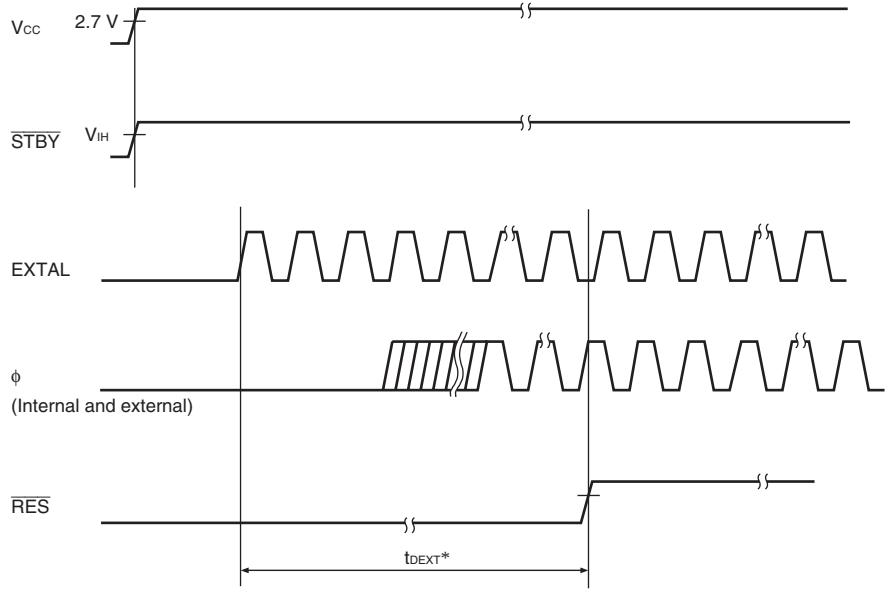
The oscillator and duty correction circuit have a function to adjust the waveform of the external clock input that is input to the EXTAL pin. When a specified clock signal is input to the EXTAL pin, internal clock signal output is determined after the external clock output stabilization delay time (t_{DEXT}) has passed. As the clock signal output is not determined during the t_{DEXT} cycle, a reset signal should be set to low to hold it in reset state. Table 17.4 shows the external clock output stabilization delay time. Figure 17.6 shows the timing of the external clock output stabilization delay time.

Table 17.4 External Clock Output Stabilization Delay Time

Condition: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V

Item	Symbol	Min.	Max.	Unit	Remarks
External clock output stabilization delay time	t_{DEXT}*	500	—	µs	Figure 17.6

Note: * t_{DEXT} includes a $\overline{RES}$ pulse width (t_{RESW}).



Note: * The external clock output stabilization delay time (t_{DEXT}) includes a $\overline{RES}$ pulse width (t_{RESW}).

Figure 17.6 Timing of External Clock Output Stabilization Delay Time

17.2 Duty Correction Circuit

The duty correction circuit is valid when the oscillating frequency is 5 MHz or more. It corrects the duty of a clock that is output from the oscillator, and generates the system clock (ϕ).

17.3 Medium-Speed Clock Divider

The medium-speed clock divider divides the system clock (ϕ), and generates ϕ/2, ϕ/4, ϕ/8, ϕ/16, and ϕ/32 clocks.

17.4 Bus Master Clock Select Circuit

The bus master clock select circuit selects a clock to supply the bus master with either the system clock (ϕ) or medium-speed clock (ϕ/2, ϕ/4, ϕ/8, ϕ/16, or ϕ/32) by the SCK2 to SCK0 bits in SBYCR.

17.5 Subclock Input Circuit

The subclock input circuit controls subclock input from the EXCL pin. To use the subclock, a 32.768-kHz external clock should be input from the EXCL pin. At this time, the P96DDR bit in P9DDR should be cleared to 0, and the EXCLE bit in LPWRCR should be set to 1.

Subclock input conditions are shown in table 17.5. When the subclock is not used, subclock input should not be enabled.

Table 17.5 Subclock Input Conditions

		Vcc = 4.0 to 5.5 V				
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Measurement Condition**
Subclock input pulse width low level	t_{EXCLL}	—	15.26	—	µs	Figure 17.7
Subclock input pulse width high level	t_{EXCLH}	—	15.26	—	µs	
Subclock input rising time	t_{EXCLr}	—	—	10	ns	
Subclock input falling time	t_{EXCLf}	—	—	10	ns	

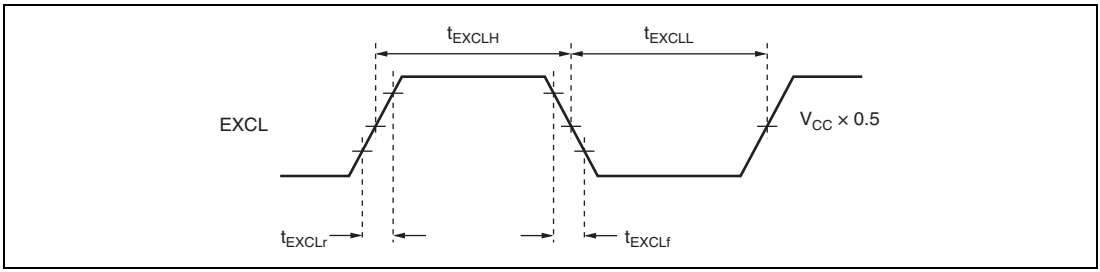


Figure 17.7 Subclock Input Timing

17.6 Subclock Waveform Forming Circuit

To remove noise from the subclock input at the EXCL pin, the subclock is sampled by a divided ϕ clock. The sampling frequency is set by the NESEL bit in LPWRCR.

The subclock is not sampled in subactive mode, subsleep mode, or watch mode.

17.7 Clock Select Circuit

The clock select circuit selects the system clock that is used in this LSI.

A clock generated by an oscillator to which the EXTAL and XTAL pins are input is selected as a system clock when returning from high-speed mode, medium-speed mode, sleep mode, reset state, or standby mode.

A subclock input from the EXCL pin is selected as a system clock in subactive mode, subsleep mode, or watch mode. At this time, modules such as the CPU, TMR_0, TMR_1, WDT_0, WDT_1, ports, and interrupt controller and their functions operate depending on the ϕSUB. The count clock and sampling clock for each timer are divided ϕSUB clocks.

17.8 Usage Notes

17.8.1 Note on Resonator

Since all kinds of characteristics of the resonator are closely related to the board design by the user, use the example of resonator connection in this document for only reference; be sure to use an resonator that has been sufficiently evaluated by the user. Consult with the resonator manufacturer about the resonator circuit ratings which vary depending on the stray capacitances of the resonator and installation circuit. Make sure the voltage applied to the oscillator pins does not exceed the maximum rating.

17.8.2 Notes on Board Design

When using a crystal resonator, the crystal resonator and its load capacitors should be placed as close as possible to the XTAL and EXTAL pins.

Other signal lines should be routed away from the oscillator circuit to prevent inductive interference with the correct oscillation as shown in figure 17.8.

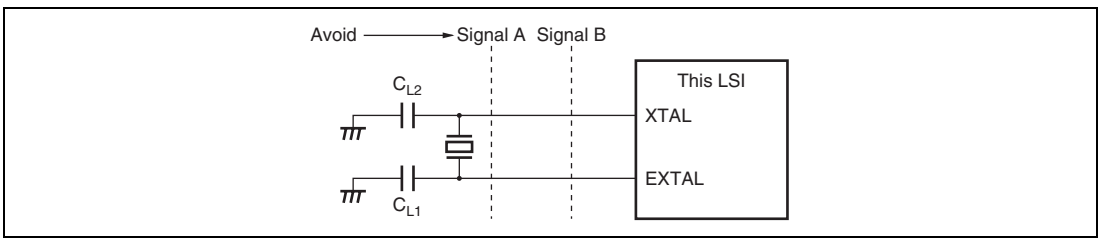


Figure 17.8 Note on Board Design of Oscillator Circuit Section

Section 18 Power-Down Modes

For operating modes after the reset state is released, this LSI has not only the normal program execution state but also seven power-down modes in which power dissipation is significantly reduced. In addition, there is also module stop mode in which reduced power dissipation can be achieved by individually stopping on-chip peripheral modules.

- Medium-speed mode
  System clock frequency for the CPU operation can be selected as $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$,or $\phi/32$.
- Subactive mode
  The CPU operates based on the subclock and on-chip peripheral modules other than TMR_0, TMR_1, WDT_0, and WDT_1 stop operating.
- Sleep mode
  The CPU stops but on-chip peripheral modules continue operating.
- Subsleep mode
  The CPU and on-chip peripheral modules other than TMR_0, TMR_1, WDT_0, and WDT_1 stop operating.
- Watch mode
  The CPU and on-chip peripheral modules other than WDT_1 stop operating.
- Software standby mode
  Clock oscillation stops, and the CPU and on-chip peripheral modules stop operating.
- Hardware standby mode
  Clock oscillation stops, and the CPU and on-chip peripheral modules enter reset state.
- Module stop mode
  Independently of above operating modes, on-chip peripheral modules that are not used can be stopped individually.

18.1 Register Descriptions

Power-down modes are controlled by the following registers. To access SBYCR, LPWRCR, MSTPCRH, and MSTPCRL, the FLSHE bit in the serial timer control register (STCR) must be cleared to 0. For details on STCR, see section 3.2.3, Serial Timer Control Register (STCR).

- Standby control register (SBYCR)
- Low power control register (LPWRCR)
- Module stop control register H (MSTPCRH)
- Module stop control register L (MSTPCRL)

18.1.1 Standby Control Register (SBYCR)

SBYCR controls power-down modes.

Bit	Bit Name	Initial Value	R/W	Description
7	SSBY	0	R/W	Software Standby Specifies the operating mode to be entered after executing the SLEEP instruction. When the SLEEP instruction is executed in high-speed mode or medium-speed mode: 0: Shifts to sleep mode 1: Shifts to software standby mode, subactive mode, or watch mode When the SLEEP instruction is executed in subactive mode: 0: Shifts to subsleep mode 1: Shifts to watch mode or high-speed mode Note that the SSBY bit is not changed even if a mode transition occurs by an interrupt.
6	STS2	0	R/W	Standby Timer Select 2 to 0 Selects the wait time for clock stabilization from clock oscillation start when canceling software standby mode, watch mode, or subactive mode. Select a wait time of 8 ms (oscillation stabilization time) or more, depending on the operating frequency. Table 18.1 shows the relationship between the STS2 to STS0 values and wait time. With an external clock, there are no specific wait requirements. Normally the minimum value is recommended.
5	STS1	0	R/W	
4	STS0	0	R/W	
3	—	0	R	Reserved This bit is always read as 0, and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Selects a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	When making a transition to subactive mode or watch mode, SCK2 to SCK0 must be cleared to 0.
				000: High-speed mode
				001: Medium-speed clock: ϕ/2
				010: Medium-speed clock: ϕ/4
				011: Medium-speed clock: ϕ/8
				100: Medium-speed clock: ϕ/16
				101: Medium-speed clock: ϕ/32
				11X: —

Legend
X: Don't care

Table 18.1 Operating Frequency and Wait Time

STS2	STS1	STS0	Wait Time	20 MHz	10 MHz	8 MHz	6 MHz	4 MHz	2 MHz	Unit
0	0	0	8192 states	0.4	0.8	1.0	1.3	20.	4.1	ms
0	0	1	16384 states	0.8	1.6	2.0	2.7	4.1	8.2	
0	1	0	32768 states	2.0	3.3	4.1	5.5	8.2	16.4	
0	1	1	65536 states	4.1	6.6	8.2	10.9	16.4	32.8	
1	0	0	131072 states	8.2	13.1	16.4	21.8	32.8	65.5	
1	0	1	262144 states	16.4	26.2	32.8	43.6	65.6	131.2	
1	1	0	Reserved	—	—	—	—	—	—	—
1	1	1	16 states*	0.8	1.6	2.0	2.7	4.0	8.0	µs

Shaded cells indicate the recommended specification.

Note: * This setting cannot be made in the flash-memory version of this LSI.

18.1.2 Low-Power Control Register (LPWRCR)

LPWRCR controls power-down modes.

Bit	Bit Name	Initial Value	R/W	Description
7	DTON	0	R/W	Direct Transfer On Flag Specifies the operating mode to be entered after executing the SLEEP instruction. When the SLEEP instruction is executed in high-speed mode or medium-speed mode: 0: Shifts to sleep mode, software standby mode, or watch mode 1: Shifts directly to subactive mode, or shifts to sleep mode or software standby mode When the SLEEP instruction is executed in subactive mode: 0: Shifts to subsleep mode or watch mode 1: Shifts directly to high-speed mode, or shifts to subsleep mode
6	LSON	0	R/W	Low-Speed On Flag Specifies the operating mode to be entered after executing the SLEEP instruction. This bit also controls whether to shift to high-speed mode or subactive mode when watch mode is released. When the SLEEP instruction is executed in high-speed mode or medium-speed mode: 0: Shifts to sleep mode, software standby mode, or watch mode 1: Shifts to watch mode or subactive mode When the SLEEP instruction is executed in subactive mode: 0: Shifts directly to watch mode or high-speed mode 1: Shifts to subsleep mode or watch mode When watch mode is released: 0: Shifts to high-speed mode 1: Shifts to subactive mode

Bit	Bit Name	Initial Value	R/W	Description
5	NESEL	0	R/W	Noise Elimination Sampling Frequency Select Selects the frequency by which the subclock (φSUB) input from the EXCL pin is sampled using the clock (φ) generated by the system clock pulse generator. Clear this bit to 0 when φ is 5 MHz or more. 0: Sampling using φ/32 clock 1: Sampling using φ/4 clock
4	EXCLE	0	R/W	Subclock Input Enable Enables/disables subclock input from the EXCL pin. 0: Disables subclock input from the EXCL pin 1: Enables subclock input from the EXCL pin
3	—	0	R/W	Reserved An undefined value is read from this bit. This bit should not be set to 1.
2 to 0	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

18.1.3 Module Stop Control Registers H and L (MSTPCRH, MSTPCRL)

MSTPCRH and MSTPCRL specify on-chip peripheral modules to shift to module stop mode in module units. Each module can enter module stop mode by setting the corresponding bit to 1.

- MSTPCRH

Bit	Bit Name	Initial Value	R/W	Corresponding Module
7	MSTP15	0*	R/W	—
6	MSTP14	0	R/W	—
5	MSTP13	1	R/W	16-bit free-running timer (FRT)
4	MSTP12	1	R/W	8-bit timers (TMR_0, TMR_1)
3	MSTP11	1	R/W	14-bit PWM timer (PWMX)
2	MSTP10	1	R/W	D/A converter
1	MSTP9	1	R/W	A/D converter
0	MSTP8	1	R/W	8-bit timer (TMR_Y)

Note: * Do not set this bit to 1.

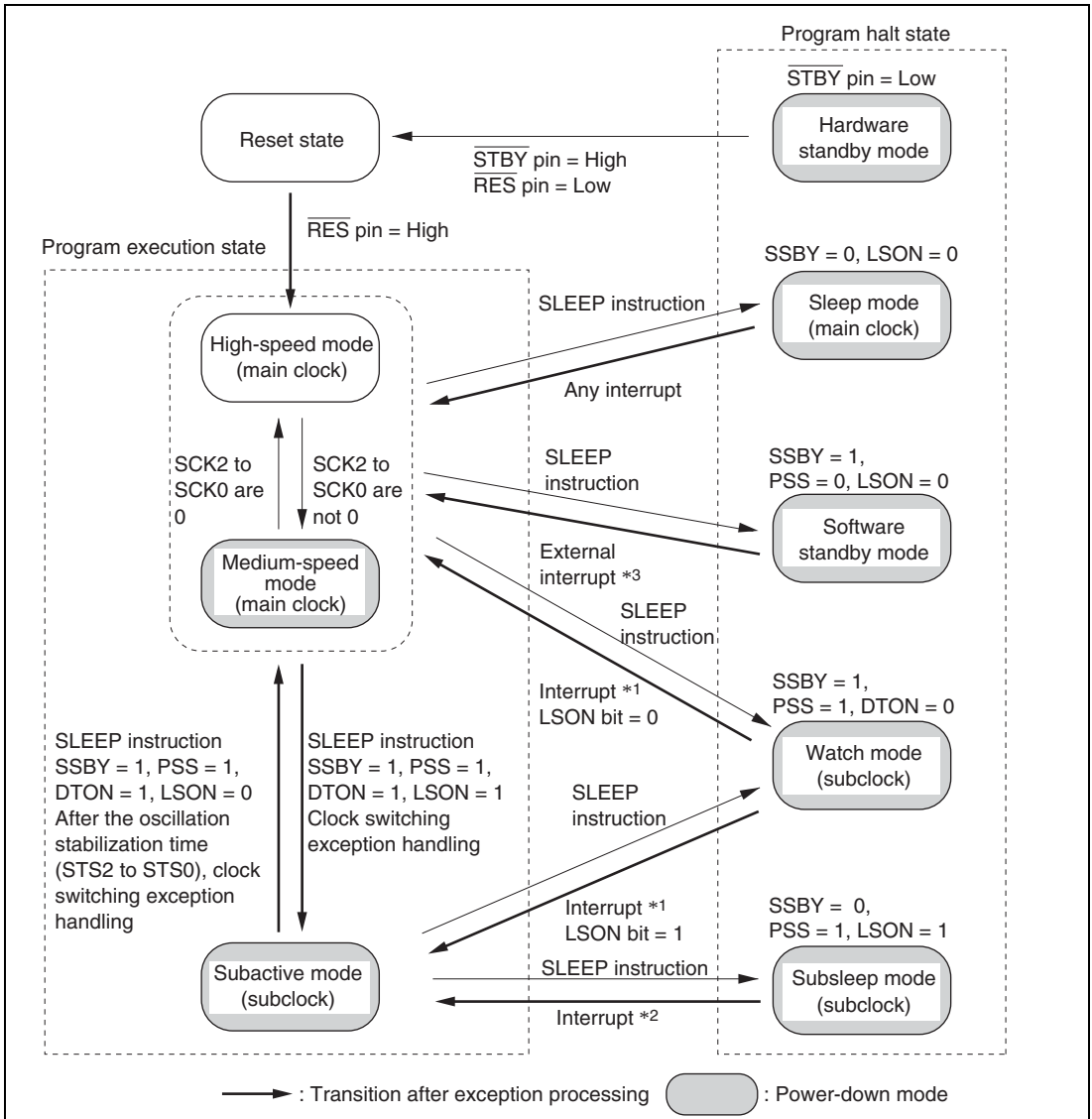
- MSTPCRL

Bit	Bit Name	Initial Value	R/W	Corresponding Module
7	MSTP7	1	R/W	Serial communication interface_0 (SCI_0)
6	MSTP6	1	R/W	Serial communication interface_1 (SCI_1)
5	MSTP5	1	R/W	Serial communication interface_2 (SCI_2)
4	MSTP4	1	R/W	—
3	MSTP3	1	R/W	—
2	MSTP2	1	R/W	Keyboard matrix interrupt mask register (KMIMR), keyboard matrix interrupt mask register A (KMIMRA), port 6 pull-up MOS control register (KMPCR)
1	MSTP1	1*	R/W	—
0	MSTP0	1	R/W	—

Note: * This bit can be read from or written to, however, operation is not affected.

18.2 Mode Transitions and LSI States

Figure 18.1 shows the enabled mode transition diagram. The mode transition from program execution state to program halt state is performed by the SLEEP instruction. The mode transition from program halt state to program execution state is performed by an interrupt. The $\overline{\text{STBY}}$ input causes a mode transition from any state to hardware standby mode. The $\overline{\text{RES}}$ input causes a mode transition from a state other than hardware standby mode to the reset state. Table 18.2 shows the LSI internal states in each operating mode.



Notes: 1. NMI, IRQ0 to IRQ2, IRQ6, IRQ7, and WDT1 interrupts
2. NMI, IRQ0 to IRQ7, WDT0, WDT1, TMR0, and TMR1 interrupts
3. NMI, IRQ0 to IRQ2, IRQ6, and IRQ7 interrupts

- When a transition is made between modes by means of an interrupt, the transition cannot be made on interrupt source generation alone. Ensure that interrupt handling is performed after accepting the interrupt request.
- Always select high-speed mode before making a transition to watch mode or sub-active mode.

Figure 18.1 Mode Transition Diagram

Table 18.2 LSI Internal States in Each Mode

Function		High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Sub-Active	Sub-Sleep	Software Standby	Hardware Standby
System clock pulse generator		Functioning	Functioning	Functioning	Functioning	Halted	Halted	Halted	Halted	Halted
Subclock pulse generator		Functioning	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning	Halted	Halted
CPU	Instruction execution	Functioning	Medium-speed operation	Halted	Functioning	Halted	Subclock operation	Halted	Halted	Halted
	Registers			Retained		Retained		Retained	Retained	Undefined
External interrupts	NMI	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning	Halted
	IRQ0 to IRQ7									
	KIN0 to KIN15									
Peripheral modules	WDT_1	Functioning	Functioning	Functioning	Functioning	Subclock operation	Subclock operation	Subclock operation	Halted (retained)	Halted (reset)
	WDT_0					Halted (retained)				
	TMR_0, TMR_1				Functioning/Halted (retained)					
	FRT						Halted (retained)	Halted (retained)		
	TMR_Y									
	SCI_0				Functioning/Halted (reset)	Halted (reset)	Halted (reset)	Halted (reset)	Halted (reset)	
	SCI_1									
	SCI_2									
	PWMX									
	D/A converter									
	A/D converter									
	RAM				Functioning	Retained	Functioning	Retained	Retained	Retained
	I/O							Functioning		High impedance

Note: * "Halted (retained)" means that internal register values are retained. The internal state is "operation suspended."

"Halted (reset)" means that internal register values and internal states are initialized.

In module stop mode, only modules for which a stop setting has been made are halted (reset or retained).

18.3 Medium-Speed Mode

The CPU makes a transition to medium-speed mode as soon as the current bus cycle ends according to the setting of the SCK2 to SCK0 bits in SBYCR. In medium-speed mode, the CPU operates on the operating clock ($\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, or $\phi/32$). On-chip peripheral modules other than the bus masters always operate on the system clock (ϕ).

In medium-speed mode, a bus access is executed in the specified number of states with respect to the bus master operating clock. For example, if $\phi/4$ is selected as the operating clock, on-chip memory is accessed in 4 states, and internal I/O registers in 8 states.

By clearing all of bits SCK2 to SCK0 to 0, a transition is made to high-speed mode at the end of the current bus cycle.

If a SLEEP instruction is executed when the SSBY bit in SBYCR is cleared to 0, and the LSON bit in LPWRCR is cleared to 0, a transition is made to sleep mode. When sleep mode is cleared by an interrupt, medium-speed mode is restored. When the SLEEP instruction is executed with the SSBY bit set to 1, the LSON bit cleared to 0, and the PSS bit in TCSR (WDT_1) cleared to 0, operation shifts to software standby mode. When software standby mode is cleared by an external interrupt, medium-speed mode is restored.

When the $\overline{\text{RES}}$ pin is set low and medium-speed mode is released, operation shifts to the reset state. The same applies in the case of a reset caused by overflow of the watchdog timer.

When the $\overline{\text{STBY}}$ pin is driven low, medium-speed mode is released and a transition is made to hardware standby mode.

Figure 18.2 shows an example of medium-speed mode timing.

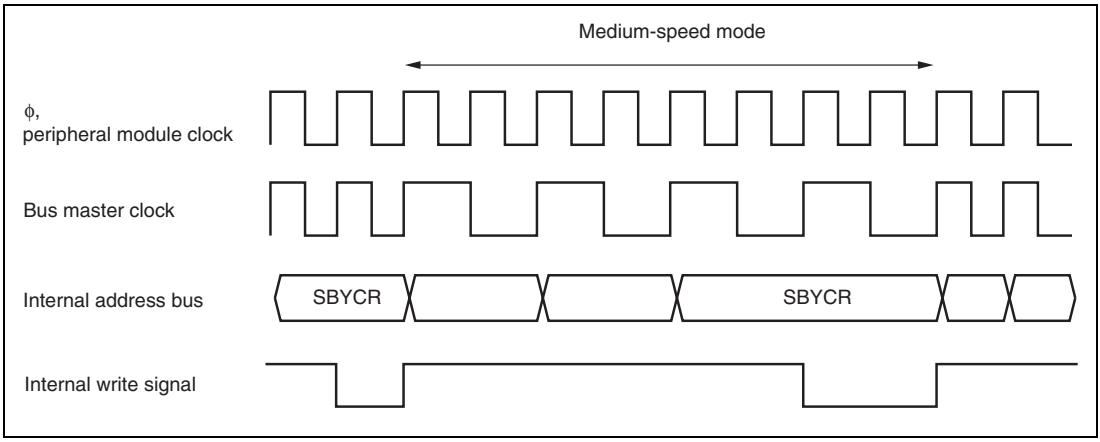


Figure 18.2 Medium-Speed Mode Timing

18.4 Sleep Mode

The CPU makes a transition to sleep mode if the SLEEP instruction is executed when the SSBY bit in SBYCR is cleared to 0 and the LSON bit in LPWRCR is cleared to 0. In sleep mode, CPU operation stops but the peripheral modules do not stop. The contents of the CPU's internal registers are retained.

Sleep mode is exited by any interrupt, the $\overline{\text{RES}}$ pin, or the $\overline{\text{STBY}}$ pin.

When an interrupt occurs, sleep mode is exited and interrupt exception handling starts. Sleep mode is not exited if the interrupt is disabled, or interrupts other than NMI are masked by the CPU.

Setting the $\overline{\text{RES}}$ pin level low cancels sleep mode and selects the reset state. After the oscillation stabilization time has passed, driving the $\overline{\text{RES}}$ pin high causes the CPU to start reset exception handling.

When the $\overline{\text{STBY}}$ pin level is driven low, sleep mode is released and a transition is made to hardware standby mode.

18.5 Software Standby Mode

The CPU makes a transition to software standby mode when the SLEEP instruction is executed while the SSBY bit in SBYCR is set to 1, the LSON bit in LPWRCR is cleared to 0, and the PSS bit in TCSR (WDT_1) is cleared to 0.

In software standby mode, the CPU, on-chip peripheral modules, and clock pulse generator all stop. However, the contents of the CPU's internal registers, on-chip RAM data, and the states of I/O ports and on-chip peripheral modules other than the SCI and PWMX are retained as long as the prescribed voltage is supplied.

Software standby mode is cleared by an external interrupt (NMI, IRQ0 to IRQ2, IRQ6, or IRQ7), the $\overline{\text{RES}}$ pin input, or $\overline{\text{STBY}}$ pin input.

When an external interrupt request signal is input, system clock oscillation starts, and after the elapse of the time set in bits STS2 to STS0 in SBYCR, software standby mode is cleared, and interrupt exception handling is started. When clearing software standby mode with an IRQ0 to IRQ2, IRQ6, or IRQ7 interrupt, set the corresponding enable bit to 1 and ensure that no interrupt with a higher priority than interrupts IRQ0 to IRQ2, IRQ6, and IRQ7 is generated. Software standby mode cannot be cleared if an interrupt enable bit corresponding to an IRQ0 to IRQ2, IRQ6, or IRQ7 interrupt is cleared to 0 or if the interrupt has been masked on the CPU side.

When the $\overline{\text{RES}}$ pin is driven low, system clock oscillation is started. At the same time as system clock oscillation starts, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until clock oscillation stabilizes. When the $\overline{\text{RES}}$ pin goes high after clock oscillation stabilizes, the CPU begins reset exception handling.

When the $\overline{\text{STBY}}$ pin is driven low, software standby mode is released and a transition is made to hardware standby mode.

Figure 18.3 shows an example in which a transition is made to software standby mode at the falling edge of the NMI pin, and software standby mode is cleared at the rising edge of the NMI pin.

In this example, an NMI interrupt is accepted with the NMIEG bit in SYSCR cleared to 0 (falling edge specification), then the NMIEG bit is set to 1 (rising edge specification), the SSBY bit is set to 1, and a SLEEP instruction is executed, causing a transition to software standby mode.

Software standby mode is then cleared at the rising edge of the NMI pin.

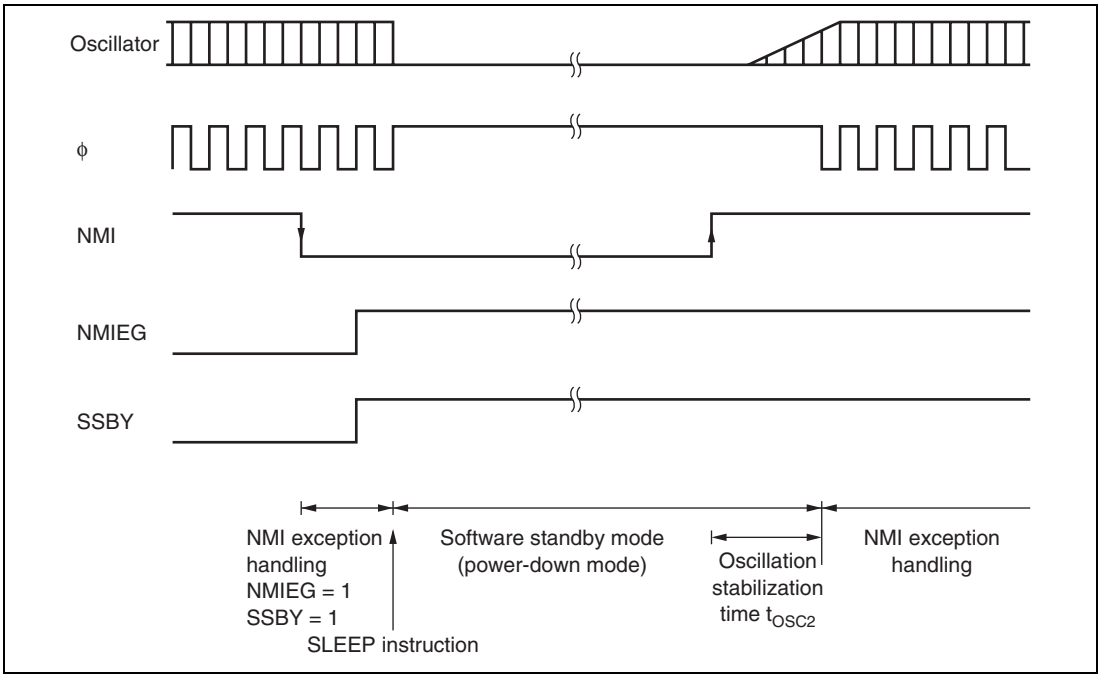


Figure 18.3 Application Example in Software Standby Mode

18.6 Hardware Standby Mode

The CPU makes a transition to hardware standby mode from any mode when the $\overline{\text{STBY}}$ pin is driven low.

In hardware standby mode, all functions enter the reset state. As long as the prescribed voltage is supplied, on-chip RAM data is retained. The I/O ports are set to the high-impedance state.

In order to retain on-chip RAM data, the RAME bit in SYSCR should be cleared to 0 before driving the $\overline{\text{STBY}}$ pin low. Do not change the state of the mode pins (MD1 and MD0) while this LSI is in hardware standby mode.

Hardware standby mode is cleared by the $\overline{\text{STBY}}$ pin input or the $\overline{\text{RES}}$ pin input.

When the $\overline{\text{STBY}}$ pin is driven high while the $\overline{\text{RES}}$ pin is low, clock oscillation is started. Ensure that the $\overline{\text{RES}}$ pin is held low until system clock oscillation stabilizes. When the $\overline{\text{RES}}$ pin is subsequently driven high after the clock oscillation stabilization time has passed, reset exception handling starts.

Figure 18.4 shows an example of hardware standby mode timing.

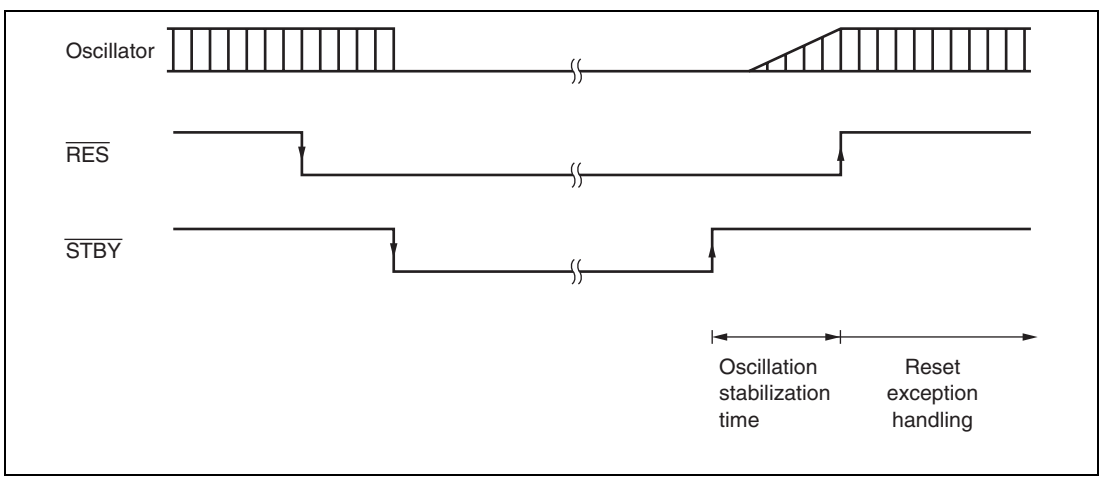


Figure 18.4 Hardware Standby Mode Timing

18.7 Watch Mode

The CPU makes a transition to watch mode when the SLEEP instruction is executed in high-speed mode or subactive mode with the SSBY bit in SBYCR set to 1, the DTON bit in LPWRCR cleared to 0, and the PSS bit in TCSR (WDT_1) set to 1.

In watch mode, the CPU is stopped and peripheral modules other than WDT_1 are also stopped. The contents of the CPU's internal registers, several on-chip peripheral module registers, and on-chip RAM data are retained and the I/O ports retain their values before transition as long as the prescribed voltage is supplied.

Watch mode is exited by an interrupt (WOVI1, NMI, IRQ0 to IRQ2, IRQ6, or IRQ7), $\overline{\text{RES}}$ pin input, or $\overline{\text{STBY}}$ pin input.

When an interrupt occurs, watch mode is exited and a transition is made to high-speed mode or medium-speed mode when the LSON bit in LPWRCR cleared to 0 or to subactive mode when the LSON bit is set to 1. When a transition is made to high-speed mode, a stable clock is supplied to the entire LSI and interrupt exception handling starts after the time set in the STS2 to STS0 bits in SBYCR has elapsed. In the case of an IRQ0 to IRQ2, IRQ6, or IRQ7 interrupt, watch mode is not exited if the corresponding enable bit has been cleared to 0. In the case of interrupts from the on-chip peripheral modules, watch mode is not exited if the interrupt enable register has been set to disable the reception of that interrupt, or the interrupt is masked by the CPU.

When the $\overline{\text{RES}}$ pin is driven low, system clock oscillation starts. Simultaneously with the start of system clock oscillation, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until clock oscillation is stabilized. If the $\overline{\text{RES}}$ pin is driven high after the clock oscillation stabilization time has passed, the CPU begins reset exception handling.

If the $\overline{\text{STBY}}$ pin is driven low, the LSI enters hardware standby mode.

18.8 Subsleep Mode

The CPU makes a transition to subsleep mode when the SLEEP instruction is executed in subactive mode with the SSBY bit in SBYCR cleared to 0, the LSON bit in LPWRCR set to 1, and the PSS bit in TCSR (WDT_1) set to 1.

In subsleep mode, the CPU is stopped. Peripheral modules other than TMR_0, TMR_1, WDT_0, and WDT_1 are also stopped. The contents of the CPU's internal registers, several on-chip peripheral module registers, and on-chip RAM data are retained and the I/O ports retain their values before transition as long as the prescribed voltage is supplied.

Subsleep mode is exited by an interrupt (interrupts by on-chip peripheral modules, NMI, IRQ0 to IRQ7), the $\overline{\text{RES}}$ pin input, or the $\overline{\text{STBY}}$ pin input.

When an interrupt occurs, subsleep mode is exited and interrupt exception handling starts.

In the case of an IRQ0 to IRQ7 interrupt, subsleep mode is not exited if the corresponding enable bit has been cleared to 0. In the case of interrupts from the on-chip peripheral modules, subsleep mode is not exited if the interrupt enable register has been set to disable the reception of that interrupt, or the interrupt is masked by the CPU.

When the $\overline{\text{RES}}$ pin is driven low, system clock oscillation starts. Simultaneously with the start of system clock oscillation, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until clock oscillation is stabilized. If the $\overline{\text{RES}}$ pin is driven high after the clock oscillation stabilization time has passed, the CPU begins reset exception handling.

If the $\overline{\text{STBY}}$ pin is driven low, the LSI enters hardware standby mode.

18.9 Subactive Mode

The CPU makes a transition to subactive mode when the SLEEP instruction is executed in high-speed mode with the SSBY bit in SBYCR set to 1, the DTON bit and LSON bit in LPWRCR set to 1, and the PSS bit in TCSR (WDT_1) set to 1. When an interrupt occurs in watch mode, and if the LSON bit in LPWRCR is 1, a direct transition is made to subactive mode. Similarly, if an interrupt occurs in subsleep mode, a transition is made to subactive mode.

In subactive mode, the CPU operates at a low speed based on the subclock and sequentially executes programs. Peripheral modules other than TMR_0, TMR_1, WDT_0, and WDT_1 are also stopped.

When operating the CPU in subactive mode, the SCK2 to SCK0 bits in SBYCR must be cleared to 0.

Subactive mode is exited by the SLEEP instruction, $\overline{\text{RES}}$ pin input, or $\overline{\text{STBY}}$ pin input.

When the SLEEP instruction is executed with the SSBY bit in SBYCR set to 1, the DTON bit in LPWRCR cleared to 0, and the PSS bit in TCSR (WDT_1) set to 1, the CPU exits subactive mode and a transition is made to watch mode. When the SLEEP instruction is executed with the SSBY bit in SBYCR cleared to 0, the LSON bit in LPWRCR set to 1, and the PSS bit in TCSR (WDT_1) set to 1, a transition is made to subsleep mode. When the SLEEP instruction is executed with the SSBY bit in SBYCR set to 1, the DTON bit and LSON bit in LPWRCR set to 10, and the PSS bit in TCSR (WDT_1) set to 1, a direct transition is made to high-speed mode.

For details of direct transitions, see section 18.11, Direct Transitions.

When the $\overline{\text{RES}}$ pin is driven low, system clock oscillation starts. Simultaneously with the start of system clock oscillation, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until the clock oscillation is stabilized. If the $\overline{\text{RES}}$ pin is driven high after the clock oscillation stabilization time has passed, the CPU begins reset exception handling.

If the $\overline{\text{STBY}}$ pin is driven low, the LSI enters hardware standby mode.

18.10 Module Stop Mode

Module stop mode can be individually set for each on-chip peripheral module.

When the corresponding MSTP bit in MSTPCR is set to 1, module operation stops at the end of the bus cycle and a transition is made to module stop mode. In turn, when the corresponding MSTP bit is cleared to 0, module stop mode is released and the module operation resumes at the end of the bus cycle. In module stop mode, the internal states of modules other than the SCI, D/A converter, A/D converter, and PWMX are retained.

After the reset state is released, all modules are in module stop mode.

While an on-chip peripheral module is in module stop mode, read/write access to its registers is disabled.

18.11 Direct Transitions

The CPU executes programs in three modes: high-speed, medium-speed, and subactive. When a direct transition is made from high-speed mode to subactive mode, there is no interruption of program execution. A direct transition is enabled by setting the DTON bit in LPWRCR to 1 and then executing the SLEEP instruction. After a transition, direct transition exception handling starts.

The CPU makes a transition to subactive mode when the SLEEP instruction is executed in high-speed mode with the SSBY bit in SBYCR set to 1, the LSON bit and DTON bit in LPWRCR set to 11, and the PSS bit in TSCR (WDT_1) set to 1.

To make a direct transition to high-speed mode after the time set in the STS2 to STS0 bits in SBYCR has elapsed, execute the SLEEP instruction in subactive mode with the SSBY bit in SBYCR set to 1, the LSON bit and DTON bit in LPWRCR set to 01, and the PSS bit in TSCR (WDT_1) set to 1.

18.12 Usage Notes

18.12.1 I/O Port Status

The status of the I/O ports is retained in software standby mode. Therefore, when a high level is output, the current consumption is not reduced by the amount of current to support the high level output.

18.12.2 Current Consumption while Waiting for Oscillation to be Stabilized

The current consumption while waiting for oscillation to be stabilized is higher than that while oscillation is stabilized.

Section 19 List of Registers

The register list gives information on the on-chip I/O register addresses, how the register bits are configured, and the register states in each operating mode. The information is given as shown below.

1. Register Addresses (address order)
- Registers are listed from the lower allocation addresses.
- The MSB-side address is indicated for 16-bit addresses.
- Registers are classified by functional modules.
- The access size is indicated.

2. Register Bits
- Bit configurations of the registers are described in the same order as the Register Addresses (address order) above.
- Reserved bits are indicated by — in the bit name column.
- The bit number in the bit-name column indicates that the whole register is allocated as a counter or for holding data.
- 16-bit registers are indicated from the bit on the MSB side.

3. Register States in Each Operating Mode
- Register states are described in the same order as the Register Addresses (address order) above.
- The register states described here are for the basic operating modes. If there is a specific reset for an on-chip peripheral module, refer to the section on that on-chip peripheral module.

4. Register Select Conditions
- Register states are described in the same order as the Register Addresses (address order) above.
- For details on the register select conditions, refer to section 3.2.2, System Control Register (SYSCR), 3.2.3, Serial Timer Control Register (STCR), 18.1.3, Module Stop Control Registers H, L (MSTPCRH, MSTPCRL), and the register descriptions for each module.

19.1 Register Addresses (Address Order)

The data bus width indicates the numbers of bits by which the register is accessed.

The number of access states indicates the number of states based on the specified reference clock.

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Keyboard comparator control register	KBCOMP	8	H'FEE4	IrDA/ Extended A/D	8	2
Interrupt control register A	ICRA	8	H'FEE8	INT	8	2
Interrupt control register B	ICRB	8	H'FEE9	INT	8	2
Interrupt control register C	ICRC	8	H'FEEA	INT	8	2
IRQ status register	ISR	8	H'FEEB	INT	8	2
IRQ sense control register H	ISCRH	8	H'FEEC	INT	8	2
IRQ sense control register L	ISCRL	8	H'FEED	INT	8	2
Address break control register	ABRKCR	8	H'FEF4	INT	8	2
Break address register A	BARA	8	H'FEF5	INT	8	2
Break address register B	BARB	8	H'FEF6	INT	8	2
Break address register C	BARC	8	H'FEF7	INT	8	2
Flash memory control register 1	FLMCR1	8	H'FF80	FLASH	8	2
Flash memory control register 2	FLMCR2	8	H'FF81	FLASH	8	2
Erase block register 1	EBR1	8	H'FF82	FLASH	8	2
System control register 2	SYSCR2	8	H'FF83	SYSTEM	8	2
Erase block register 2	EBR2	8	H'FF83	FLASH	8	2
Standby control register	SBYCR	8	H'FF84	SYSTEM	8	2
Low power control register	LPWRCR	8	H'FF85	SYSTEM	8	2
Module stop control register H	MSTPCRH	8	H'FF86	SYSTEM	8	2
Module stop control register L	MSTPCRL	8	H'FF87	SYSTEM	8	2
Serial mode register_1	SMR_1	8	H'FF88	SCI_1	8	2
Bit rate register_1	BRR_1	8	H'FF89	SCI_1	8	2
Serial control register_1	SCR_1	8	H'FF8A	SCI_1	8	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Transmit data register_1	TDR_1	8	H'FF8B	SCI_1	8	2
Serial status register_1	SSR_1	8	H'FF8C	SCI_1	8	2
Receive data register_1	RDR_1	8	H'FF8D	SCI_1	8	2
Smart card mode register_1	SCMR_1	8	H'FF8E	SCI_1	8	2
Timer interrupt enable register	TIER	8	H'FF90	FRT	8	2
Timer control/status register	TCSR	8	H'FF91	FRT	8	2
Free running counter H	FRCH	8	H'FF92	FRT	8	2
Free running counter L	FRCL	8	H'FF93	FRT	8	2
Output control register AH	OCRAH	8	H'FF94	FRT	8	2
Output control register BH	OCRBH	8	H'FF94	FRT	8	2
Output control register AL	OCRAL	8	H'FF95	FRT	8	2
Output control register BL	OCRBL	8	H'FF95	FRT	8	2
Timer control register	TCR	8	H'FF96	FRT	8	2
Timer output compare control register	TOCR	8	H'FF97	FRT	8	2
Input capture register AH	ICRAH	8	H'FF98	FRT	8	2
Output control register ARH	OCRARH	8	H'FF98	FRT	8	2
Input capture register AL	ICRAL	8	H'FF99	FRT	8	2
Output control register ARL	OCRARL	8	H'FF99	FRT	8	2
Input capture register BH	ICRBH	8	H'FF9A	FRT	8	2
Output control register AFH	OCRAFH	8	H'FF9A	FRT	8	2
Input capture register BL	ICRBL	8	H'FF9B	FRT	8	2
Output control register AFL	OCRAFL	8	H'FF9B	FRT	8	2
Input capture register CH	ICRCH	8	H'FF9C	FRT	8	2
Output compare register DMH	OCRDMH	8	H'FF9C	FRT	8	2
Input capture register CL	ICRCL	8	H'FF9D	FRT	8	2
Output compare register DML	OCRDML	8	H'FF9D	FRT	8	2
Input capture register DH	ICRDH	8	H'FF9E	FRT	8	2
Input capture register DL	ICRDL	8	H'FF9F	FRT	8	2
Serial mode register_2	SMR_2	8	H'FFA0	SCI_2	8	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
PWM (D/A) control register	DACR	8	H'FFA0	PWMX	8	2
PWM (D/A) data register AH	DADRAH	8	H'FFA0	PWMX	8	2
PWM (D/A) data register AL	DADRAL	8	H'FFA1	PWMX	8	2
Bit rate register_2	BRR_2	8	H'FFA1	SCI_2	8	2
Serial control register_2	SCR_2	8	H'FFA2	SCI_2	8	2
Transmit data register_2	TDR_2	8	H'FFA3	SCI_2	8	2
Serial status register_2	SSR_2	8	H'FFA4	SCI_2	8	2
Receive data register_2	RDR_2	8	H'FFA5	SCI_2	8	2
Smart card mode register_2	SCMR_2	8	H'FFA6	SCI_2	8	2
PWM (D/A) counter H	DACNTH	8	H'FFA6	PWMX	8	2
PWM (D/A) data register BH	DADRBH	8	H'FFA6	PWMX	8	2
PWM (D/A) counter L	DACNTL	8	H'FFA7	PWMX	8	2
PWM (D/A) data register BL	DADRBL	8	H'FFA7	PWMX	8	2
Timer control/status register_0	TCSR_0	8	H'FFA8	WDT	8	2
Timer counter_0	TCNT_0	8	H'FFA8 (write)	WDT_0	8	2
Timer counter_0	TCNT_0	8	H'FFA9 (read)	WDT_0	8	2
Port A output data register	PAODR	8	H'FFAA	PORT	8	2
Port A input data register	PAPIN	8	H'FFAB	PORT	8	2
Port A data direction register	PADDR	8	H'FFAB	PORT	8	2
Port 1 pull-up MOS control register	P1PCR	8	H'FFAC	PORT	8	2
Port 2 pull-up MOS control register	P2PCR	8	H'FFAD	PORT	8	2
Port 3 pull-up MOS control register	P3PCR	8	H'FFAE	PORT	8	2
Port 1 data direction register	P1DDR	8	H'FFB0	PORT	8	2
Port 2 data direction register	P2DDR	8	H'FFB1	PORT	8	2
Port 1 data register	P1DR	8	H'FFB2	PORT	8	2
Port 2 data register	P2DR	8	H'FFB3	PORT	8	2
Port 3 data direction register	P3DDR	8	H'FFB4	PORT	8	2
Port 4 data direction register	P4DDR	8	H'FFB5	PORT	8	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Port 3 data register	P3DR	8	H'FFB6	PORT	8	2
Port 4 data register	P4DR	8	H'FFB7	PORT	8	2
Port 5 data direction register	P5DDR	8	H'FFB8	PORT	8	2
Port 6 data direction register	P6DDR	8	H'FFB9	PORT	8	2
Port 5 data register	P5DR	8	H'FFBA	PORT	8	2
Port 6 data register	P6DR	8	H'FFBB	PORT	8	2
Port B output data register	PBODR	8	H'FFBC	PORT	8	2
Port B input data register	PBPIN	8	H'FFBD (read)	PORT	8	2
Port 8 data direction register	P8DDR	8	H'FFBD (write)	PORT	8	2
Port 7 input data register	P7PIN	8	H'FFBE (read)	PORT	8	2
Port B data direction register	PBDDR	8	H'FFBE (write)	PORT	8	2
Port 8 data register	P8DR	8	H'FFBF	PORT	8	2
Port 9 data direction register	P9DDR	8	H'FFC0	PORT	8	2
Port 9 data register	P9DR	8	H'FFC1	PORT	8	2
Interrupt enable register	IER	8	H'FFC2	INT	8	2
Serial timer control register	STCR	8	H'FFC3	SYSTEM	8	2
System control register	SYSCR	8	H'FFC4	SYSTEM	8	2
Mode control register	MDCR	8	H'FFC5	SYSTEM	8	2
Bus control register	BCR	8	H'FFC6	BSC	8	2
Wait state control register	WSCR	8	H'FFC7	BSC	8	2
Timer control register_0	TCR_0	8	H'FFC8	TMR_0	8	2
Timer control register_1	TCR_1	8	H'FFC9	TMR_1	8	2
Timer control/status register_0	TCSR_0	8	H'FFCA	TMR_0	8	2
Timer control/status register_1	TCSR_1	8	H'FFCB	TMR_1	16	2
Time constant register A_0	TCORA_0	8	H'FFCC	TMR_0	16	2
Time constant register A_1	TCORA_1	8	H'FFCD	TMR_1	16	2
Time constant register B_0	TCORB_0	8	H'FFCE	TMR_0	16	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Time constant register B_1	TCORB_1	8	H'FFCF	TMR_1	16	2
Timer counter_0	TCNT_0	8	H'FFD0	TMR_0	16	2
Timer counter_1	TCNT_1	8	H'FFD1	TMR_1	16	2
Serial mode register_0	SMR_0	8	H'FFD8	SCI_0	8	2
Bit rate register_0	BRR_0	8	H'FFD9	SCI_0	8	2
Serial control register_0	SCR_0	8	H'FFDA	SCI_0	8	2
Transmit data register_0	TDR_0	8	H'FFDB	SCI_0	8	2
Serial status register_0	SSR_0	8	H'FFDC	SCI_0	8	2
Receive data register_0	RDR_0	8	H'FFDD	SCI_0	8	2
Smart card mode register_0	SCMR_0	8	H'FFDE	SCI_0	8	2
A/D data register AH	ADDRAH	8	H'FFE0	A/D converter	8	2
A/D data register AL	ADDRAL	8	H'FFE1	A/D converter	8	2
A/D data register BH	ADDRBH	8	H'FFE2	A/D converter	8	2
A/D data register BL	ADDRBL	8	H'FFE3	A/D converter	8	2
A/D data register CH	ADDRCH	8	H'FFE4	A/D converter	8	2
A/D data register CL	ADDRCL	8	H'FFE5	A/D converter	8	2
A/D data register DH	ADDRDH	8	H'FFE6	A/D converter	8	2
A/D data register DL	ADDRDL	8	H'FFE7	A/D converter	8	2
A/D control/status register	ADCSR	8	H'FFE8	A/D converter	8	2
A/D control register	ADCR	8	H'FFE9	A/D converter	8	2
Timer control/status register_1	TCSR_1	8	H'FFEA	WDT_1	8	2
Timer counter_1	TCNT_1	8	H'FFEA (write)	WDT_1	8	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Timer counter_1	TCNT_1	8	H'FFEB (read)	WDT_1	8	2
Timer control register_Y	TCR_Y	8	H'FFF0	TMR_Y	16	2
Keyboard matrix interrupt register 6	KMIMR	8	H'FFF1	INT	8	2
Timer control/status register_Y	TCSR_Y	8	H'FFF1	TMR_Y	16	2
Pull-up MOS control register	KMPCR	8	H'FFF2	PORT	8	2
Time constant register A_Y	TCORA_Y	8	H'FFF2	TMR_Y	16	2
Keyboard matrix interrupt register A	KMIMRA	8	H'FFF3	INT	8	2
Time constant register B_Y	TCORB_Y	8	H'FFF3	TMR_Y	16	2
Timer counter_Y	TCNT_Y	8	H'FFF4	TMR_Y	16	2
Timer input select register	TISR	8	H'FFF5	TMR_Y	16	2
D/A data register 0	DADR0	8	H'FFF8	D/A converter	8	2
D/A data register 1	DADR1	8	H'FFF9	D/A converter	8	2
D/A control register	DACR	8	H'FFFA	D/A converter	8	2

19.2 Register Bits

Register addresses and bit names of the on-chip peripheral modules are described below.

16-bit registers are shown as 2 lines.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
KBCOMP	IrE	IrCKS2	IrCKS1	IrCKS0	KBADE	KBCH2	KBCH1	KBCH0	IrDA/ expanded A/D
ICRA	ICRA7	ICRA6	ICRA5	ICRA4	ICRA3	ICRA2	ICRA1	ICRA0	INT
ICRB	ICRB7	ICRB6	ICRB5	ICRB4	ICRB3	ICRB2	ICRB1	ICRB0	
ICRC	ICRC7	ICRC6	ICRC5	ICRC4	ICRC3	ICRC2	ICRC1	ICRC0	
ISR	IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F	
ISCRH	IRQ7SCB	IRQ7SCA	IRQ6SCB	IRQ6SCA	IRQ5SCB	IRQ5SCA	IRQ4SCB	IRQ4SCA	
ISCRL	IRQ3SCB	IRQ3SCA	IRQ2SCB	IRQ2SCA	IRQ1SCB	IRQ1SCA	IRQ0SCB	IRQ0SCA	
ABRKCR	CMF	—	—	—	—	—	—	BIE	
BARA	A23	A22	A21	A20	A19	A18	A17	A16	
BARB	A15	A14	A13	A12	A11	A10	A9	A8	
BARC	A7	A6	A5	A4	A3	A2	A1	—	
FLMCR1	FWE	SWE	—	—	EV	PV	E	P	FLASH
FLMCR2	FLER	—	—	—	—	—	ESU	PSU	
EBR1	—	—	—	—	—	—	EB9	EB8	
SYSCR2	KWUL1	KWUL0	P6PUE	—	—	—	—	—	SYSTEM
EBR2	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	FLASH
SBYCR	SSBY	STS2	STS1	STS0	—	SCK2	SCK1	SCK0	SYSTEM
LPWRCR	DTON	LSON	NESEL	EXCLE	—	—	—	—	
MSTPCRH	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	
MSTPCRL	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0	
SMR_1	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI_1
BRR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
SCR_1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	SCI_1
TDR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SSR_1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
RDR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SCMR_1	—	—	—	—	SDIR	SINV	—	SMIF	
TIER	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—	FRT
TCSR	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	CCLRA	
FRCH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
FRCL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRAH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
OCRBH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
OCRAL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRBL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0	
TOCR	ICRDMS	OCRAMS	ICRS	OCRS	OEA	OEB	OLVLA	OLVLB	
ICRAH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
OCRARH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
ICRAL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRARL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ICRBH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
OCRAFH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
ICRBL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRAFL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ICRCH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
OCRDMH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
ICRCL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRDML	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ICRDH	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
ICRDL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
SMR_2	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI_2
DACR	TEST	PWME	—	—	OEB	OEA	OS	CKS	PWMX
DADRAH	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	
DADRAL	DA5	DA4	DA3	DA2	DA1	DA0	CFS	—	
BRR_2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	SCI_2
SCR_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SSR_2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
RDR_2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SCMR_2	—	—	—	—	SDIR	SINV	—	SMIF	
DACNTH	UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0	PWMX
DADRBH	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	
DACNTL	UC8	UC9	UC10	UC11	UC12	UC13	—	REGS	
DADRBL	DA5	DA4	DA3	DA2	DA1	DA0	CFS	REGS	
TCSR_0	OVF	WT/$\overline{IT}$	TME	—	RST/$\overline{NMI}$	CKS2	CKS1	CKS0	WDT_0
TCNT_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
PAODR	PA7ODR	PA6ODR	PA5ODR	PA4ODR	PA3ODR	PA2ODR	PA1ODR	PA0ODR	PORT
PAPIN	PA7PIN	PA6PIN	PA5PIN	PA4PIN	PA3PIN	PA2PIN	PA1PIN	PA0PIN	
PADDR	PA7DDR	PA6DDR	PA5DDR	PA4DDR	PA3DDR	PA2DDR	PA1DDR	PA0DDR	
P1PCR	P17PCR	P16PCR	P15PCR	P14PCR	P13PCR	P12PCR	P11PCR	P10PCR	
P2PCR	P27PCR	P26PCR	P25PCR	P24PCR	P23PCR	P22PCR	P21PCR	P20PCR	
P3PCR	P37PCR	P36PCR	P35PCR	P34PCR	P33PCR	P32PCR	P31PCR	P30PCR	
P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR	
P2DDR	P27DDR	P26DDR	P25DDR	P24DDR	P23DDR	P22DDR	P21DDR	P20DDR	
P1DR	P17DR	P16DR	P15DR	P14DR	P13DR	P12DR	P11DR	P10DR	
P2DR	P27DR	P26DR	P25DR	P24DR	P23DR	P22DR	P21DR	P20DR	
P3DDR	P37DDR	P36DDR	P35DDR	P34DDR	P33DDR	P32DDR	P31DDR	P30DDR	
P4DDR	P47DDR	P46DDR	P45DDR	P44DDR	P43DDR	P42DDR	P41DDR	P40DDR	
P3DR	P37DR	P36DR	P35DR	P34DR	P33DR	P32DR	P31DR	P30DR	
P4DR	P47DR	P46DR	P45DR	P44DR	P43DR	P42DR	P41DR	P40DR	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
P5DDR	—	—	—	—	—	P52DDR	P51DDR	P50DDR	PORT
P6DDR	P67DDR	P66DDR	P65DDR	P64DDR	P63DDR	P62DDR	P61DDR	P60DDR	
P5DR	—	—	—	—	—	P52DR	P51DR	P50DR	
P6DR	P67DR	P66DR	P65DR	P64DR	P63DR	P62DR	P61DR	P60DR	
PBODR	PB7ODR	PB6ODR	PB5ODR	PB4ODR	PB3ODR	PB2ODR	PB1ODR	PB0ODR	
PBPIN	PB7PIN	PB6PIN	PB5PIN	PB4PIN	PB3PIN	PB2PIN	PB1PIN	PB0PIN	
P8DDR	—	P86DDR	P85DDR	P84DDR	P83DDR	P82DDR	P81DDR	P80DDR	
P7PIN	P77PIN	P76PIN	P75PIN	P74PIN	P73PIN	P72PIN	P71PIN	P70PIN	
PBDDR	PB7DDR	PB6DDR	PB5DDR	PB4DDR	PB3DDR	PB2DDR	PB1DDR	PB0DDR	
P8DR	—	P86DR	P85DR	P84DR	P83DR	P82DR	P81DR	P80DR	
P9DDR	P97DDR	P96DDR	P95DDR	P94DDR	P93DDR	P92DDR	P91DDR	P90DDR	
P9DR	P97DR	P96DR	P95DR	P94DR	P93DR	P92DR	P91DR	P90DR	
IER	IRQ7E	IRQ6E	IRQ5E	IRQ4E	IRQ3E	IRQ2E	IRQ1E	IRQ0E	INT
STCR	IICS	—	—	IICE	FLSHE	—	ICKS1	ICKS0	SYSTEM
SYSCR	—	IOSE	INTM1	INTM0	XRST	NMIEG	HIE	RAME	
MDCR	EXPE	—	—	—	—	—	MDS1	MDS0	
BCR	—	ICIS0	BRSTRM	BRSTS1	BRSTS0	—	IOS1	IOS0	BSC
WSCR	—	—	ABW	AST	WMS1	WMS0	WC1	WC0	
TCR_0	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_0, TMR_1
TCR_1	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	
TCSR_0	CMFB	CMFA	OVF	ADTE	OS3	OS2	OS1	OS0	
TCSR_1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	
TCORA_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCORA_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCORB_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCORB_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCNT_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCNT_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SMR_0	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI_0
BRR_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
SCR_0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	SCI_0
TDR_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SSR_0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
RDR_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SCMR_0	—	—	—	—	SDIR	SINV	—	SMIF	
ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter
ADDRAL	AD1	AD0	—	—	—	—	—	—	
ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
ADDRBL	AD1	AD0	—	—	—	—	—	—	
ADDRCH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
ADDRCL	AD1	AD0	—	—	—	—	—	—	
ADDRDH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
ADDRDL	AD1	AD0	—	—	—	—	—	—	
ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
ADCR	TRGS1	TRGS0	—	—	—	—	—	—	
TCSR_1	OVF	WT/$\overline{IT}$	TME	PSS	RST/$\overline{NMI}$	CKS2	CKS1	CKS0	WDT_1
TCNT_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR_Y	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_Y
KMIMR	KMIMR7	KMIMR6	KMIMR5	KMIMR4	KMIMR3	KMIMR2	KMIMR1	KMIMR0	INT
TCSR_Y	CMFB	CMFA	OVF	ICIE	OS3	OS2	OS1	OS0	TMR_Y
KMPCR	KMIMR7	KMIMR6	KMIMR5	KMIMR4	KMIMR3	KMIMR2	KMIMR1	KMIMR0	PORT
TCORA_Y	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_Y
KMIMRA	KMIMR15	KMIMR14	KMIMR13	KMIMR12	KMIMR11	KMIMR10	KMIMR9	KMIMR8	INT
TCORB_Y	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	TMR_Y
TCNT_Y	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TISR	—	—	—	—	—	—	—	IS	
DADR_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	D/A converter
DADR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
DACR	DAOE1	DAOE0	DAE	—	—	—	—	—	

19.3 Register States in Each Operating Mode

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
KBCOMP	Initialized	—	—	—	—	—	—	—	Initialized	IrDA/ A/D converter
ICRA	Initialized	—	—	—	—	—	—	—	Initialized	INT
ICRB	Initialized	—	—	—	—	—	—	—	Initialized	
ICRC	Initialized	—	—	—	—	—	—	—	Initialized	
ISR	Initialized	—	—	—	—	—	—	—	Initialized	
ISCRH	Initialized	—	—	—	—	—	—	—	Initialized	
ISCRL	Initialized	—	—	—	—	—	—	—	Initialized	
ABRKCR	Initialized	—	—	—	—	—	—	—	Initialized	INT
BARA	Initialized	—	—	—	—	—	—	—	Initialized	
BARB	Initialized	—	—	—	—	—	—	—	Initialized	
BARC	Initialized	—	—	—	—	—	—	—	Initialized	
FLMCR1	Initialized	—	Initialized	—	Initialized	Initialized	—	Initialized	Initialized	FLASH
FLMCR2	Initialized	—	Initialized	—	Initialized	Initialized	—	Initialized	Initialized	
EBR1	Initialized	—	Initialized	—	Initialized	Initialized	—	Initialized	Initialized	
SYSCR2	Initialized	—	—	—	—	—	—	—	Initialized	SYSTEM
EBR2	Initialized	—	Initialized	—	Initialized	Initialized	—	Initialized	Initialized	FLASH
SBYCR	Initialized	—	—	—	—	—	—	—	Initialized	SYSTEM
LPWRCR	Initialized	—	—	—	—	—	—	—	Initialized	
MSTPCRH	Initialized	—	—	—	—	—	—	—	Initialized	
MSTPCRL	Initialized	—	—	—	—	—	—	—	Initialized	
SMR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	SCI_1
BRR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SCR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
TDR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SSR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
RDR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SCMR_1	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
TIER	Initialized	—	—	—	—	—	—	—	Initialized	FRT
TCSR	Initialized	—	—	—	—	—	—	—	Initialized	
FRCH	Initialized	—	—	—	—	—	—	—	Initialized	
FRCL	Initialized	—	—	—	—	—	—	—	Initialized	
OCRAH	Initialized	—	—	—	—	—	—	—	Initialized	
OCRBH	Initialized	—	—	—	—	—	—	—	Initialized	
OCRAL	Initialized	—	—	—	—	—	—	—	Initialized	
OCRBL	Initialized	—	—	—	—	—	—	—	Initialized	
TCR	Initialized	—	—	—	—	—	—	—	Initialized	
TOCR	Initialized	—	—	—	—	—	—	—	Initialized	
ICRAH	Initialized	—	—	—	—	—	—	—	Initialized	
OCRARH	Initialized	—	—	—	—	—	—	—	Initialized	
ICRAL	Initialized	—	—	—	—	—	—	—	Initialized	
OCRARL	Initialized	—	—	—	—	—	—	—	Initialized	
ICRBH	Initialized	—	—	—	—	—	—	—	Initialized	
OCRAFH	Initialized	—	—	—	—	—	—	—	Initialized	
ICRBL	Initialized	—	—	—	—	—	—	—	Initialized	
OCRAFL	Initialized	—	—	—	—	—	—	—	Initialized	
ICRCH	Initialized	—	—	—	—	—	—	—	Initialized	
OCRDMH	Initialized	—	—	—	—	—	—	—	Initialized	
ICRCL	Initialized	—	—	—	—	—	—	—	Initialized	
OCRDML	Initialized	—	—	—	—	—	—	—	Initialized	
ICRDH	Initialized	—	—	—	—	—	—	—	Initialized	
ICRDL	Initialized	—	—	—	—	—	—	—	Initialized	
SMR_2	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	SCI_2
DACR	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	PWMX
DADRAH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
DADRAL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
BRR_2	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	SCI_2
SCR_2	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
TDR_2	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SSR_2	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
RDR_2	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SCMR_2	Initialized	—	—	—	—	—	—	—	Initialized	
DACNTH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	PWMX
DADRBH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
DACNTL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
DADRBL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
TCSR_0	Initialized	—	—	—	—	—	—	—	Initialized	WDT_0
TCNT_0	Initialized	—	—	—	—	—	—	—	Initialized	
PAODR	Initialized	—	—	—	—	—	—	—	Initialized	PORT
PAPIN	—	—	—	—	—	—	—	—	—	
PADDR	Initialized	—	—	—	—	—	—	—	Initialized	
P1PCR	Initialized	—	—	—	—	—	—	—	Initialized	
P2PCR	Initialized	—	—	—	—	—	—	—	Initialized	
P3PCR	Initialized	—	—	—	—	—	—	—	Initialized	
P1DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P2DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P1DR	Initialized	—	—	—	—	—	—	—	Initialized	
P2DR	Initialized	—	—	—	—	—	—	—	Initialized	
P3DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P4DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P3DR	Initialized	—	—	—	—	—	—	—	Initialized	
P4DR	Initialized	—	—	—	—	—	—	—	Initialized	
P5DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P6DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P5DR	Initialized	—	—	—	—	—	—	—	Initialized	

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
P6DR	Initialized	—	—	—	—	—	—	—	Initialized	PORT
PBODR	Initialized	—	—	—	—	—	—	—	Initialized	
PBPIN	—	—	—	—	—	—	—	—	—	
P8DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P7PIN	—	—	—	—	—	—	—	—	—	
PBDDR	Initialized	—	—	—	—	—	—	—	Initialized	
P8DR	Initialized	—	—	—	—	—	—	—	Initialized	
P9DDR	Initialized	—	—	—	—	—	—	—	Initialized	
P9DR	Initialized	—	—	—	—	—	—	—	Initialized	
IER	Initialized	—	—	—	—	—	—	—	Initialized	INT
STCR	Initialized	—	—	—	—	—	—	—	Initialized	SYSTEM
SYSCR	Initialized	—	—	—	—	—	—	—	Initialized	
MDCR	Initialized	—	—	—	—	—	—	—	Initialized	
BCR	Initialized	—	—	—	—	—	—	—	Initialized	BSC
WSCR	Initialized	—	—	—	—	—	—	—	Initialized	
TCR_0	Initialized	—	—	—	—	—	—	—	Initialized	TMR_0, TMR_1
TCR_1	Initialized	—	—	—	—	—	—	—	Initialized	
TCSR_0	Initialized	—	—	—	—	—	—	—	Initialized	
TCSR_1	Initialized	—	—	—	—	—	—	—	Initialized	
TCORA_0	Initialized	—	—	—	—	—	—	—	Initialized	
TCORA_1	Initialized	—	—	—	—	—	—	—	Initialized	
TCORB_0	Initialized	—	—	—	—	—	—	—	Initialized	
TCORB_1	Initialized	—	—	—	—	—	—	—	Initialized	
TCNT_0	Initialized	—	—	—	—	—	—	—	Initialized	
TCNT_1	Initialized	—	—	—	—	—	—	—	Initialized	
SMR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	SCI_0
BRR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
SCR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	SCI_0
TDR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SSR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
RDR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
SCMR_0	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRAH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	A/D converter
ADDRAL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRBH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRBL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRCH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRCL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRDH	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADDRDL	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADCSR	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
ADCR	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	
TCSR_1	Initialized	—	—	—	—	—	—	—	Initialized	WDT_1
TCNT_1	Initialized	—	—	—	—	—	—	—	Initialized	
TCR_Y	Initialized	—	—	—	—	—	—	—	Initialized	TMR_Y
KMIMR	Initialized	—	—	—	—	—	—	—	Initialized	INT
TCSR_Y	Initialized	—	—	—	—	—	—	—	Initialized	TMR_Y
KMPCR	Initialized	—	—	—	—	—	—	—	Initialized	PORT
TCORA_Y	Initialized	—	—	—	—	—	—	—	Initialized	TMR_Y
KMIMRA	Initialized	—	—	—	—	—	—	—	Initialized	INT
TCORB_Y	Initialized	—	—	—	—	—	—	—	Initialized	TMR_Y
TCNT_Y	Initialized	—	—	—	—	—	—	—	Initialized	TMR_Y
TISR	Initialized	—	—	—	—	—	—	—	Initialized	TMR_Y
DADR0	Initialized	—	—	—	—	—	—	—	Initialized	D/A converter
DADR1	Initialized	—	—	—	—	—	—	—	Initialized	
DACR	Initialized	—	—	—	—	—	—	—	Initialized	

19.4 Register Select Conditions

Lower Address	Register Name	Register Selected Conditions: H8S/2144B	Register Selected Conditions: H8S/2134B	Module Name
H'FEE4	KBCOMP	Always selected	Always selected	IrDA/ extended A/D
H'FEE8	ICRA	Always selected	Always selected	INT
H'FEE9	ICRB			
H'FEEA	ICRC			
H'FEEB	ISR			
H'FEEC	ISCRH			
H'FEED	ISCRL			
H'FEF4	ABRKCR			
H'FEF5	BARA			
H'FEF6	BARB			
H'FEF7	BARC			
H'FF80	FLMCR1	FLSHE = 1 in STCR	FLSHE = 1 in STCR	FLASH
H'FF81	FLMCR2			
H'FF82	EBR1	FLSHE = 1 in STCR	FLSHE = 1 in STCR	FLASH
H'FF83	SYSCR2	FLSHE = 0 in STCR	FLSHE = 0 in STCR	SYSTEM
	EBR2	FLSHE = 1 in STCR	FLSHE = 1 in STCR	FLASH
H'FF84	SBYCR	FLSHE = 0 in STCR	FLSHE = 0 in STCR	SYSTEM
H'FF85	LPWRCR			
H'FF86	MSTPCRH			
H'FF87	MSTPCRL			
H'FF88	SMR_1	MSTP6 = 0, IICE = 0 in STCR	MSTP6 = 0,IICE = 0 in STCR	SCI_1
H'FF89	BRR_1	MSTP6 = 0, IICE = 0 in STCR	MSTP6 = 0, IICE = 0 in STCR	

Lower Address	Register Name	Register Selected Conditions				Module Name
		H8S/2144B		H8S/2134B		
H'FF8A	SCR_1	MSTP6 = 0		MSTP6 = 0		SCI_1
H'FF8B	TDR_1					
H'FF8C	SSR_1					
H'FF8D	RDR_1					
H'FF8E	SCMR_1	MSTP6 = 0, IICE = 0 in STCR		MSTP6 = 0, IICE = 0 in STCR		
H'FF90	TIER	MSTP13 = 0		MSTP13 = 0		FRT
H'FF91	TCSR					
H'FF92	FRCH					
H'FF93	FRCL					
H'FF94	OCRAH	MSTP13 = 0	OCRS = 0 in TOCR	MSTP13 = 0	OCRS = 0 in TOCR	
	OCRBH		OCRS = 1 in TOCR		OCRS = 1 in TOCR	
H'FF95	OCRAL		OCRS = 0 in TOCR		OCRS = 0 in TOCR	
	OCRBL		OCRS = 1 in TOCR		OCRS = 1 in TOCR	
H'FF96	TCR					
H'FF97	TOCR					
H'FF98	ICRAH		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRARH		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF99	ICRAL		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRARL		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9A	ICRBH		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRAFH		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9B	ICRBL		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRAFL		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9C	ICRCH		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRDMH		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9D	ICRCL		ICRS = 0 in TOCR		ICRS = 0 in TOCR	
	OCRDML		ICRS = 1 in TOCR		ICRS = 1 in TOCR	
H'FF9E	ICRDH					
H'FF9F	ICRDL					

Lower Address	Register Name	Register Selected Conditions: H8S/2144B		Register Selected Conditions: H8S/2134B		Module Name
H'FFA0	SMR_2	MSTP5 = 0, IICE = 0 in STCR		MSTP5 = 0, IICE = 0 in STCR		SCI_2
	DADRAH	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/DADRB	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/DADRB	PWMX
	DACR		REGS = 1 in DACNT/DADRB		REGS = 1 in DACNT/DADRB	
H'FFA1	BRR_2	MSTP5 = 0, IICE = 0 in STCR		MSTP5 = 0, IICE = 0 in STCR		SCI_2
	DADRAL	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/DADRB	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/DADRB	PWMX
H'FFA2	SCR_2	MSTP5 = 0		MSTP5 = 0		SCI_2
H'FFA3	TDR_2					
H'FFA4	SSR_2					
H'FFA5	RDR_2					
H'FFA6	SCMR_2	MSTP5 = 0, IICE = 0 in STCR		MSTP5 = 0, IICE = 0 in STCR		SCI_2
	DADRBH	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/DADRB	MSTP11 = 0, IICE = 1 in STCR	REGS = 0 in DACNT/DADRB	PWMX
	DACNTH		REGS = 1 in DACNT/DADRB		REGS = 1 in DACNT/DADRB	
H'FFA7	DADRBL		REGS = 0 in DACNT/DADRB		REGS = 0 in DACNT/DADRB	
	DACNTL		REGS = 1 in DACNT/DADRB		REGS = 1 in DACNT/DADRB	
H'FFA8	TCSR_0	Always selected		Always selected		WDT_0
	TCNT_0 (write)					
H'FFA9	TCNT_0 (read)					
H'FFAA	PAODR	Always selected		Always selected		PORT
H'FFAB	PAPIN (read)					
	PADDR (write)					
H'FFAC	P1PCR					
H'FFAD	P2PCR					
H'FFAE	P3PCR					

Lower Address	Register Name	Register Selected Conditions: H8S/2144B	Register Selected Conditions: H8S/2134B	Module Name
H'FFB0	P1DDR	Always selected	Always selected	PORT
H'FFB1	P2DDR			
H'FFB2	P1DR			
H'FFB3	P2DR			
H'FFB4	P3DDR			
H'FFB5	P4DDR			
H'FFB6	P3DR			
H'FFB7	P4DR			
H'FFB8	P5DDR			
H'FFB9	P6DDR			
H'FFBA	P5DR			
H'FFBB	P6DR			
H'FFBC	PBODR			
H'FFBD	P8DDR (write)			
	PBPIN (read)			
H'FFBE	P7PIN (read)			
	PBDDR (write)			
H'FFBF	P8DR			
H'FFC0	P9DDR			
H'FFC1	P9DR			
H'FFC2	IER	Always selected	Always selected	INT
H'FFC3	STCR	Always selected	Always selected	SYSTEM
H'FFC4	SYSCR			
H'FFC5	MDCR			
H'FFC6	BCR	Always selected	Always selected	BSC
H'FFC7	WSCR			
H'FFC8	TCR_0	MSTP12 = 0	MSTP12 = 0	TMR_0, TMR_1
H'FFC9	TCR_1			
H'FFCA	TCSR_0			
H'FFCB	TCSR_1			

Lower Address	Register Name	Register Selected Conditions: H8S/2144B	Register Selected Conditions: H8S/2134B	Module Name
H'FFCC	TCORA_0	MSTP12 = 0	MSTP12 = 0	TMR_0, TMR_1
H'FFCD	TCORA_1			
H'FFCE	TCORB_0			
H'FFCF	TCORB_1			
H'FFD0	TCNT_0			
H'FFD1	TCNT_1			
H'FFD8	SMR_0	MSTP7 = 0, IICE = 0 in STCR	MSTP7 = 0, IICE = 0 in STCR	SCI_0
H'FFD9	BRR_0	MSTP7 = 0, IICE = 0 in STCR	MSTP7 = 0, IICE = 0 in STCR	SCI_0
H'FFDA	SCR_0	MSTP7 = 0	MSTP7 = 0	SCI_0
H'FFDB	TDR_0			
H'FFDC	SSR_0			
H'FFDD	RDR_0			
H'FFDE	SCMR_0	MSTP7 = 0, IICE = 0 in STCR	MSTP7 = 0, IICE = 0 in STCR	
H'FFE0	ADDRAH	MSTP9 = 0	MSTP9 = 0	A/D
H'FFE1	ADDRAL			
H'FFE2	ADDRBH			
H'FFE3	ADDRBL			
H'FFE4	ADDRCH			
H'FFE5	ADDRCL			
H'FFE6	ADDRDH			
H'FFE7	ADDRDL			
H'FFE8	ADCSR			
H'FFE9	ADCR			
H'FFEA	TCSR_1	Always selected	Always selected	WDT_1
	TCNT_1 (write)			
H'FFEB	TCNT_1 (read)			
H'FFF0	TCR_Y	MSPT8 = 0, HIE = 0 in SYSCR	MSPT8 = 0, HIE = 0 in SYSCR	TMR_Y

Lower Address	Register Name	Register Selected Conditions		Module Name
		H8S/2144B	H8S/2134B	
H'FFF1	KMIMR	MSPT2 = 0, HIE = 0 in SYSCR	MSPT2 = 0, HIE = 0 in SYSCR	INT
	TCSR_Y	MSPT8 = 0, HIE = 0 in SYSCR	MSPT8 = 0, HIE = 0 in SYSCR	TMR_Y
H'FFF2	KMPCR	MSTP2 = 0, HIE = 1 in SYSCR	MSTP2 = 0, HIE = 1 in SYSCR	PORT
	TCORA_Y	MSPT8 = 0, HIE = 0 in SYSCR	MSPT8 = 0, HIE = 0 in SYSCR	TMR_Y
H'FFF3	KMIMRA	MSTP2 = 0, HIE = 1 in SYSCR	MSTP2 = 0, HIE = 1 in SYSCR	INT
	TCORB_Y	MSPT8 = 0, HIE = 0 in SYSCR	MSPT8 = 0, HIE = 0 in SYSCR	TMR_Y
H'FFF4	TCNT_Y	MSPT8 = 0, HIE = 0 in SYSCR	MSPT8 = 0, HIE = 0 in SYSCR	
H'FFF5	TISR	MSPT8 = 0, HIE = 0 in SYSCR	MSPT8 = 0, HIE = 0 in SYSCR	
H'FFF8	DADR0	MSTP10 = 0	MSTP10 = 0	D/A
H'FFF9	DADR1			
H'FFFA	DACR			

Section 20 Electrical Characteristics

20.1 Electrical Characteristics of H8S/2144B

20.1.1 Absolute Maximum Ratings

Table 20.1 lists the absolute maximum ratings.

Table 20.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +7.3	V
I/O buffer power supply voltage (port A)	$V_{CC}B$	–0.3 to +7.0	V
Power supply (VCL input)*	V_{CL}	–0.3 to +4.3	V
Input voltage (other than ports 6, 7, and A)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port 6)	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (CIN input not selected for port A)	V_{in}	–0.3 to $V_{CC}B$ +0.3	V
Input voltage (CIN input selected for port 6)	V_{in}	–0.3 V to lower of voltages V_{CC} + 0.3 and AV_{CC} + 0.3	V
Input voltage (CIN input selected for port A)	V_{in}	–0.3 V to lower of voltages $V_{CC}B$ + 0.3 and AV_{CC} + 0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Reference supply voltage	AV_{ref}	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	General specifications: –20 to +75	°C
		Wide temperature range specifications: –40 to +85	
Operating temperature (flash memory programming/erasing)	T_{opr}	General specifications: –20 to +75	°C
		Wide temperature range specifications: –40 to +85	
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Operating this LSI in excess of the absolute maximum ratings may result in permanent damage.
Do not apply a voltage exceeding 7.0 V to input pins for the 5-V/4-V operation products.

Note: * Power supply pin for the internal power supply. Do not apply a power to the VCL pin for the 5-V/4-V operation products. Connect a capacitor for regulating the internal power voltage between the VCL and GND pins.

20.1.2 DC Characteristics

Table 20.2 lists the DC characteristics. Permissible output current values and bus driving characteristics are shown in tables 20.3 and 20.4, respectively.

Table 20.2 DC Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, AV_{CC}*[1] = 5.0 V ±10%,
AV_{ref}*[1] = 4.5 V to AV_{CC}, V_{SS} = AV_{SS}*[1] = 0 V,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60 (KWUL = 00)*[2]*[4], $\overline{KIN15}$ to $\overline{KIN8}$*[5]*[6], $\overline{IRQ2}$ to $\overline{IRQ0}$*[3], $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$ $V_{CC}B \times 0.7$		
			$V_T^+ - V_T^-$	0.4	—	—		
Schmitt trigger input voltage (level switching)*[4]	P67 to P60 (KWUL = 01)		V_T^-	$V_{CC} \times 0.3$	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—		
	P67 to P60 (KWUL = 10)		V_T^-	$V_{CC} \times 0.4$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.8$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.03$	—	—		
	P67 to P60 (KWUL = 11)		V_T^-	$V_{CC} \times 0.45$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.9$		
			$V_T^+ - V_T^-$	0.05	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	EXTAL			$V_{CC} \times 0.7$	—	V_{CC} + 0.3		
	PA7 to PA0*[5]			$V_{CC}B \times 0.7$	—	$V_{CC}B$ + 0.3		
	Port 7			2.0		AV_{CC} + 0.3		
	Input pins except (1) and (2) above			2.0		V_{CC} + 0.3		

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0 (3)	V_{IL}	–0.3	—	0.5	V	
	PA7 to PA0		–0.3	—	1.0		
	NMI, EXTAL, input pins except (1) and (3) above		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5 $V_{CC}B$ – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OL} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3		—	—	1.0	V	I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA

Notes: 1. Do not leave the AV_{CC}, AV_{ref}, and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AV_{CC} and AV_{ref} pins to the power supply (V_{CC}), or some other method. Be sure that $AV_{ref} \leq AV_{CC}$.

2. Characteristics for P67 to P60 also indicate those for multiplexed signals of on-chip peripheral modules.
3. Characteristic for $\overline{IRQ2}$ also indicate that for the multiplexed $\overline{ADTRG}$ signal.
4. The upper limit of the applicable voltage for port 6 is V_{CC} + 0.3 V when CIN input is not selected, and the lower of V_{CC} + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is the applicable voltage.
5. The upper limit of the applicable voltage for port A is $V_{CC}B$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}B$ + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is the applicable voltage.
6. The port A characteristics depend on $V_{CC}B$, and the characteristics for other pins depend on V_{CC}.

Table 20.2 DC Characteristics (2)

Conditions: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, AV_{CC}*[1] = 5.0 V ±10%, AV_{ref}*[1] = 4.5 V to AV_{CC}, V_{SS} = AV_{SS}*[1] = 0 V, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD1, MD0		—	—	1.0		
	Port 7		—	—	1.0		V_{in} = 0.5 to AV_{CC} – 0.5 V
Tri-state leakage current (off state)	Ports 1 to 6, 8, 9, A*[4], B	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V, V_{in} = 0.5 to $V_{CC}B$ – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V
	Ports A*[4], B, 6 (P6PUE = 1)		60	—	600		
	Port 6 (P6PUE = 1)		15	—	200		
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50		
	Input pins except (4) above		—	—	15		
Current consumption*[2]	Normal operation	I_{CC}	—	55	70	mA	f = 20 MHz
	Sleep mode		—	36	55	mA	f = 20 MHz
	Standby mode*[3]		—	1.0	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0		50°C < T_a
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reference power supply current	During A/D conversion	AI_{ref}	—	0.5	1.0	mA	
	During A/D, D/A conversion		—	2.0	5.0		
	Idle		—	0.01	5.0	µA	AV_{ref} = 2.0 V to AV_{CC}
Analog power supply voltage*[1]		AV_{CC}	4.5	—	5.5	V	Operating
			2.0	—	5.5		Idle/not used
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AV_{CC}, AV_{ref}, and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AVcc and AVref pins to the power supply (V_{CC}), or some other method. Be sure that $AV_{ref} \leq AV_{CC}$.

2. Current consumption values are for V_{IH} min. = V_{CC} – 0.2 V, $V_{CC}B$ – 0.2 V, and V_{IL} max. = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs disabled.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, V_{IH} min. = V_{CC}– 0.2 V, $V_{CC}B$ – 0.2 V, and V_{IL} max. = 0.2 V.
4. The port A characteristics depend on $V_{CC}B$, and the characteristics for other pins depend on V_{CC}.

Table 20.2 DC Characteristics (3)

Conditions: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, AV_{CC}*[1] = 4.0 V to 5.5 V, AV_{ref}*[1] = 4.0 V to AV_{CC}, V_{SS} = AV_{SS}*[1] = 0 V, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60 (KWUL = 00)*[2]*[4], $\overline{KIN15}$ to $\overline{KIN8}$*[5]*[6], $\overline{IRQ2}$ to $\overline{IRQ0}$*[3], $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	V_{CC} = 4.5 V to 5.5 V $V_{CC}B$ = 4.5 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$ $V_{CC}B \times 0.7$		
			$V_T^+ - V_T^-$	0.4	—	—		
			V_T^-	0.8	—	—	V	V_{CC} = 4.0 V to 4.5 V $V_{CC}B$ = 4.0 V to 4.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$ $V_{CC}B \times 0.7$		
			$V_T^+ - V_T^-$	0.3	—	—		
Schmitt trigger input voltage (level switching)*[4]	P67 to P60 (KWUL = 01)		V_T^-	$V_{CC} \times 0.3$	—	—	V	V_{CC} = 4.0 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—		
	P67 to P60 (KWUL = 10)		V_T^-	$V_{CC} \times 0.4$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.8$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.03$	—	—		
	P67 to P60 (KWUL = 11)		V_T^-	$V_{CC} \times 0.45$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.9$		
			$V_T^+ - V_T^-$	0.05	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL			$V_{CC} \times 0.7$	—	V_{CC} + 0.3		
	PA7 to PA0*[5]			$V_{CC}B \times 0.7$	—	$V_{CC}B$ + 0.3		
	Port 7			2.0	—	AV_{CC} + 0.3		
	Input pins except (1) and (2) above			2.0	—	V_{CC} + 0.3		

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0 (3)	V_{IL}	–0.3	—	0.5	V	
			–0.3	—	1.0		$V_{CC}B$ = 4.5 V to 5.5 V
	PA7 to PA0		–0.3	—	0.8		$V_{CC}B$ = 4.0 V to 4.5 V
	NMI, EXTAL, input pins except (1) and (3) above		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5 $V_{CC}B$ – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA, V_{CC} = 4.5 V to 5.5 V, $V_{CC}B$ = 4.5 V to 5.5 V
			3.0	—	—	V	I_{OH} = –1 mA, V_{CC} = 4.0 V to 4.5 V, $V_{CC}B$ = 4.0 V to 4.5 V
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3		—	—	1.0	V	I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA

Notes: 1. Do not leave the AV_{CC}, AV_{ref}, and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AV_{CC} and AV_{ref} pins to the power supply (V_{CC}), or some other method. Be sure that $AV_{ref} \leq AV_{CC}$.

2. Characteristics for P67 to P60 also indicate those for multiplexed signals of on-chip peripheral modules.
3. Characteristic for $\overline{IRQ2}$ also indicate that for the multiplexed $\overline{ADTRG}$ signal.
4. The upper limit of the applicable voltage for port 6 is V_{CC} + 0.3 V when CIN input is not selected, and the lower of V_{CC} + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is the applicable voltage.
5. The upper limit of the applicable voltage for port A is $V_{CC}B$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}B$ + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is the applicable voltage.
6. The port A characteristics depend on $V_{CC}B$, and the characteristics for other pins depend on V_{CC}.

Table 20.2 DC Characteristics (4)

Conditions: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, AV_{CC}*[1] = 4.0 V to 5.5 V, AV_{ref}*[1] = 4.0 V to AV_{CC}, V_{SS} = AV_{SS}*[1] = 0 V, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD1, MD0		—	—	1.0		
	Port 7		—	—	1.0		V_{in} = 0.5 to AV_{CC} – 0.5 V
Tri-state leakage current (off state)	Ports 1 to 6, 8, 9, A*[4], B	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V, V_{in} = 0.5 to $V_{CC}B$ – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V, V_{CC} = 4.5 V to 5.5 V $V_{CC}B$ = 4.5 V to 5.5 V
	Ports A*[4], B, 6 (P6PUE = 1)		60	—	600		
	Port 6 (P6PUE = 1)		15	—	200		
	Ports 1 to 3		20	—	200	µA	V_{in} = 0 V, V_{CC} = 4.0 V to 4.5 V $V_{CC}B$ = 4.0 V to 4.5 V
	Ports A*[4], B, 6 (P6PUE = 1)		40	—	500		
	Port 6 (P6PUE = 1)		10		150		
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50		
	Input pins except (4) above		—	—	15		
Current consumption*[2]	Normal operation	I_{CC}	—	45	58	mA	f = 16 MHz
	Sleep mode		—	30	46	mA	f = 16 MHz
	Standby mode*[3]		—	1.0	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0		50°C < T_a

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V
Reference power supply current	During A/D conversion	AI_{ref}	—	0.5	1.0	mA	
	During A/D, D/A conversion		—	2.0	5.0		
	Idle		—	0.01	5.0	µA	AV_{ref} = 2.0 V to AV_{CC}
Analog power supply voltage*[1]		AV_{CC}	4.0	—	5.5	V	Operating
			2.0	—	5.5		Idle/not used
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AV_{CC}, AV_{ref}, and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AVcc and AVref pins to the power supply (V_{CC}), or some other method. Be sure that $AV_{ref} \leq AV_{CC}$.

2. Current consumption values are for V_{IH} min. = V_{CC} – 0.2 V, $V_{CC}B$ – 0.2 V, and V_{IL} max. = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs disabled.
3. The values are for $V_{RAM} \leq V_{CC} < 4.0$ V, V_{IH} min. = V_{CC}– 0.2 V, $V_{CC}B$ – 0.2 V, and V_{IL} max. = 0.2 V.
4. The port A characteristics depend on $V_{CC}B$, and the characteristics for other pins depend on V_{CC}.

Table 20.3 Permissible Output Currents

Conditions: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	PA7 to PA4 (bus driving function selected)	I_{OL}	—	—	20	mA
	Ports 1 to 3		—	—	10	
	$\overline{\text{RESO}}$		—	—	3	
	Other output pins		—	—	2	
Permissible output low current (total)	Total of ports 1 to 3	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Notes: 1. To ensure reliability, do not exceed the output current values in table 20.3.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 20.1 and 20.2.

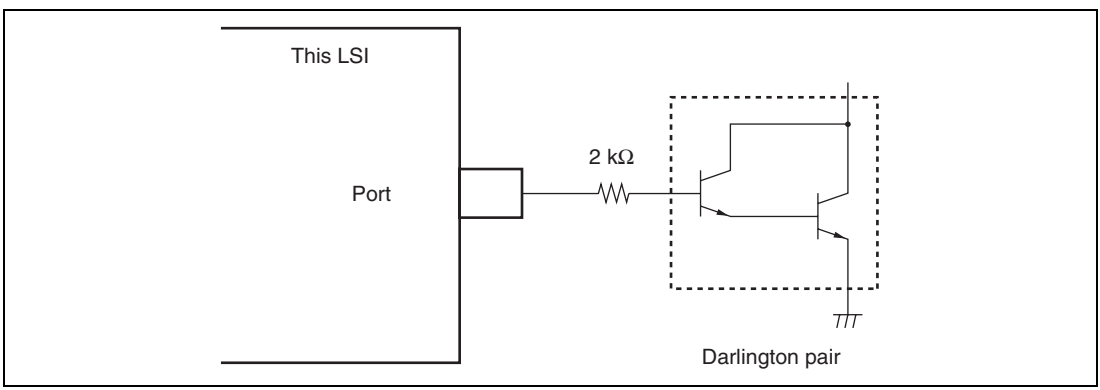


Figure 20.1 Darlington Pair Driving Circuit (Example)

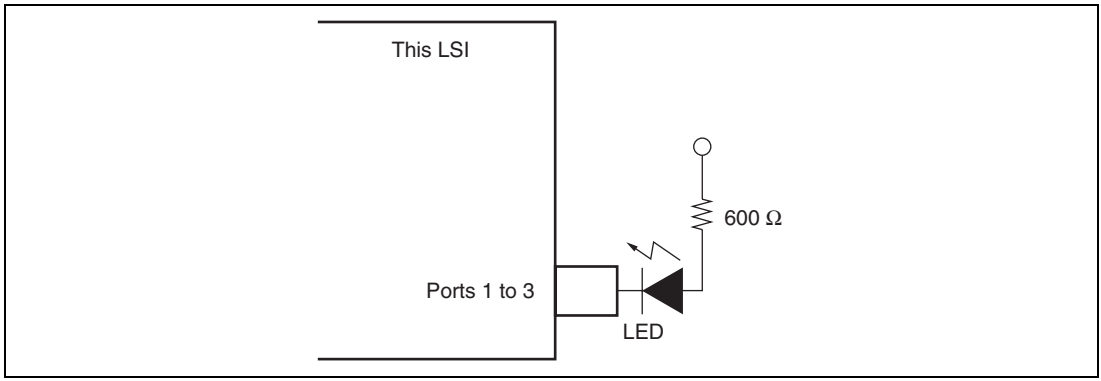


Figure 20.2 LED Driving Circuit (Example)

Table 20.4 Bus Driving Characteristics

Conditions: $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V

Applicable Pins: PA7 to PA4 (bus driving function selected)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output low voltage	V_{OL}	—	—	0.8	V	I_{OL} = 16 mA, $V_{CC}B$ = 4.5 V to 5.5 V
		—	—	0.5		I_{OL} = 8 mA
		—	—	0.4		I_{OL} = 3 mA

20.1.3 AC Characteristics

Figure 20.3 shows the test conditions for the AC characteristics.

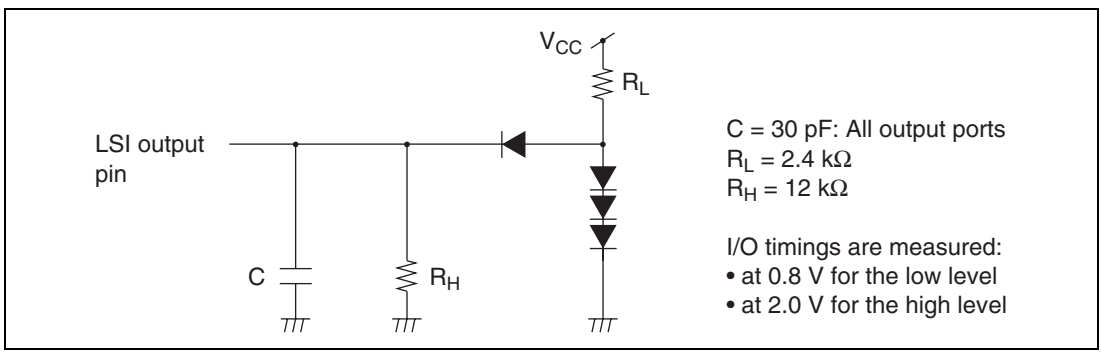


Figure 20.3 Output Load Circuit

Clock Timing: Table 20.5 shows the clock timing. The clock timing specified here covers clock (ϕ) output and oscillation stabilization times of the clock pulse generator (crystal) and external clock input (the EXTAL pin). For details on external clock input (the EXTAL pin and EXCL pin) timing, see section 17, Clock Pulse Generator.

Table 20.5 Clock Timing

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B		Condition A			
		16 MHz		20 MHz			
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Reference**
Clock cycle time	t_{cyc}	62.5	500	50	500	ns	Figure 20.4
Clock high pulse width	t_{CH}	20	—	17	—	ns	Figure 20.4
Clock low pulse width	t_{CL}	20	—	17	—	ns	
Clock rising time	t_{Cr}	—	10	—	8	ns	
Clock falling time	t_{Cf}	—	10	—	8	ns	
Oscillation stabilization time at reset (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 20.5
Oscillation stabilization time at leaving software standby (crystal)	t_{OSC2}	8	—	8	—	ms	Figure 20.6
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	

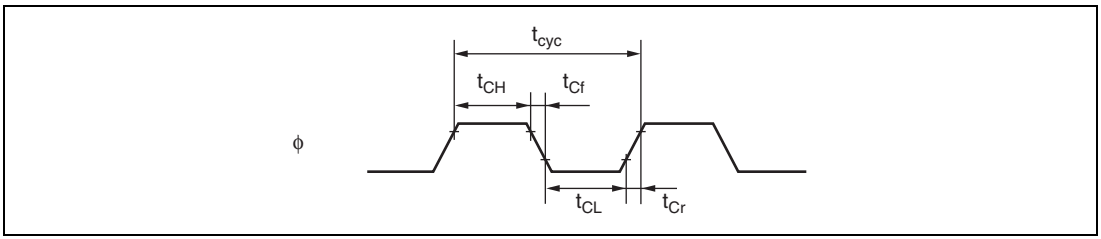


Figure 20.4 System Clock Timing

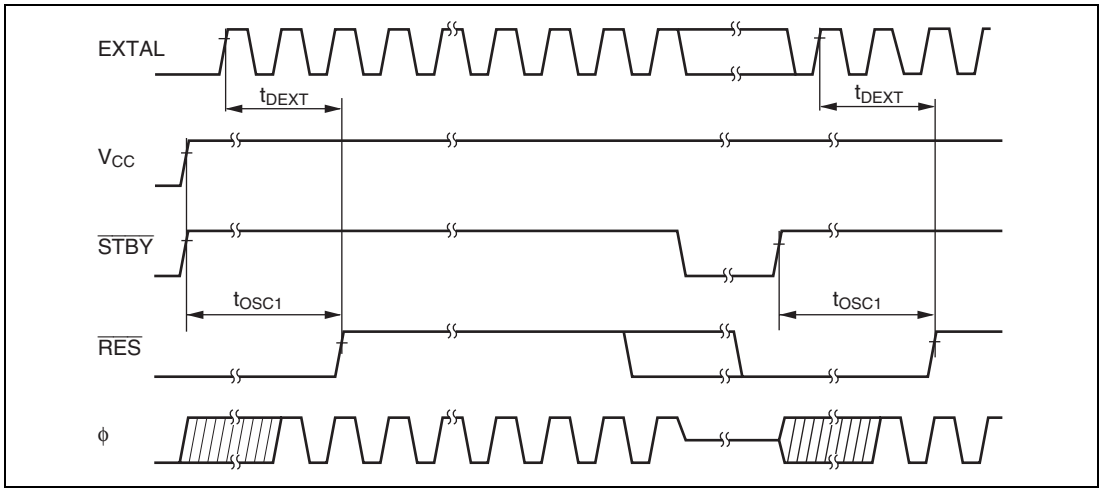


Figure 20.5 Oscillation Stabilization Timing

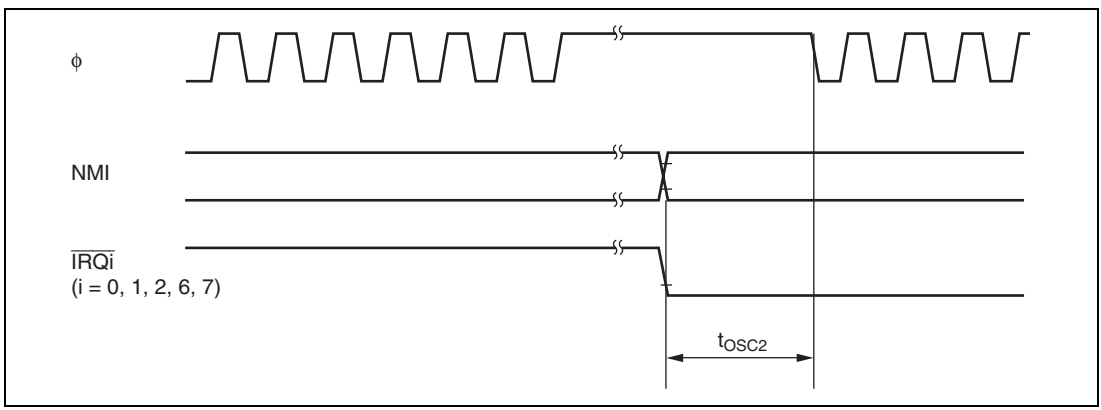


Figure 20.6 Oscillation Stabilization Timing (Leaving Software Standby Mode)

Control Signal Timing: Table 20.6 shows the control signal timing. The only external interrupts that can be received during this LSI operating on the subclock (φ = 32.768 kHz) are NMI, IRQ0, IRQ1, IRQ2, IRQ6, and IRQ7.

Table 20.6 Control Signal Timing

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, φ = 32.768 kHz or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, φ = 32.768 kHz or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B		Condition A			
		16 MHz		20 MHz			
Item	Symbol	Min.	Max.	Min.	Max.	Unit	Test Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 20.7
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time (NMI)	t_{NMIS}	150	—	150	—	ns	Figure 20.8
NMI hold time (NMI)	t_{NMIH}	10	—	10	—	ns	
NMI pulse width (leaving software standby mode)	t_{NMIW}	200	—	200	—	ns	
IRQ setup time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQS}	150	—	150	—	ns	
IRQ hold time($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQH}	10	—	10	—	ns	
IRQ pulse width ($\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ2}$ to $\overline{IRQ0}$) (leaving software standby mode)	t_{IRQW}	200	—	200	—	ns	

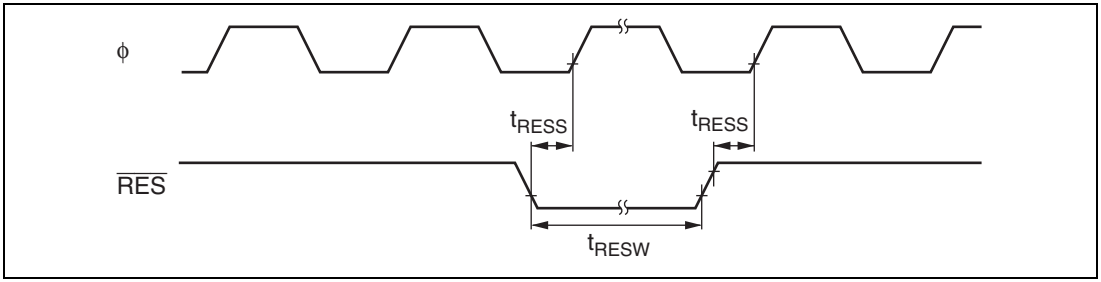


Figure 20.7 Reset Input Timing

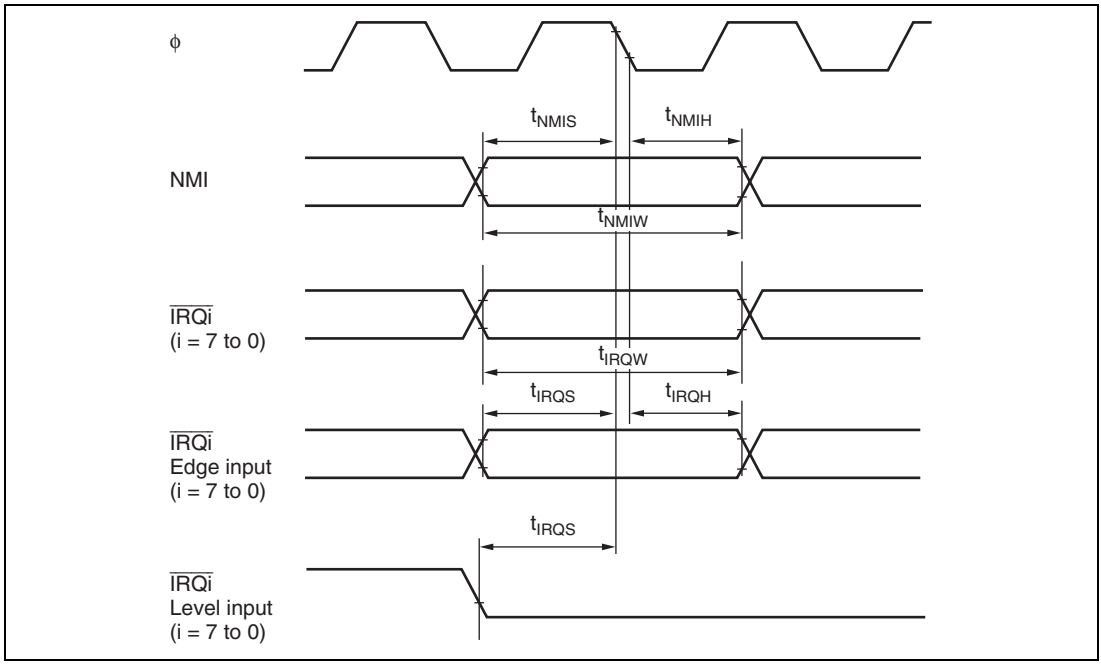


Figure 20.8 Interrupt Input Timing

Bus Timing: Table 20.7 shows the bus timing. Operation in external extended mode is not guaranteed when this LSI is operating on the subclock (φ = 32.768 kHz).

Table 20.7 Bus Timing (1) (Normal Mode)

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B		Condition A			
		16 MHz		20 MHz			Test
Item	Symbol	Min.	Max.	Min.	Max.	Unit	Conditions
Address delay time	t_{AD}	—	30	—	20	ns	Figures 20.9 to 20.13
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 15$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	30	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	45	—	30	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	45	—	30	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	45	—	30	ns	
Read data setup time	t_{RDS}	20	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 40$	—	$1.0 \times t_{cyc} - 30$	ns	
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 35$	—	$1.5 \times t_{cyc} - 25$	ns	
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 40$	—	$2.0 \times t_{cyc} - 30$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 25$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 40$	—	$3.0 \times t_{cyc} - 30$	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 1	t_{WRD1}	—	45	—	30	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 2	t_{WRD2}	—	45	—	30	ns	

Item	Symbol	Condition B 16 MHz Min.	Condition B 16 MHz Max.	Condition A 20 MHz Min.	Condition A 20 MHz Max.	Unit	Test Conditions
$\overline{HWR}$, $\overline{LWR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc}$ – 30	—	$1.0 \times t_{cyc}$ – 20	—	ns	Figures 20.9 to 20.13
$\overline{HWR}$, $\overline{LWR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc}$ – 30	—	$1.5 \times t_{cyc}$ – 20	—	ns	
Write data delay time	t_{WDD}	—	45	—	30	ns	
Write data setup time	t_{WDS}	0	—	0	—	ns	
Write data hold time	t_{WDH}	15	—	10	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	45	—	30	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	

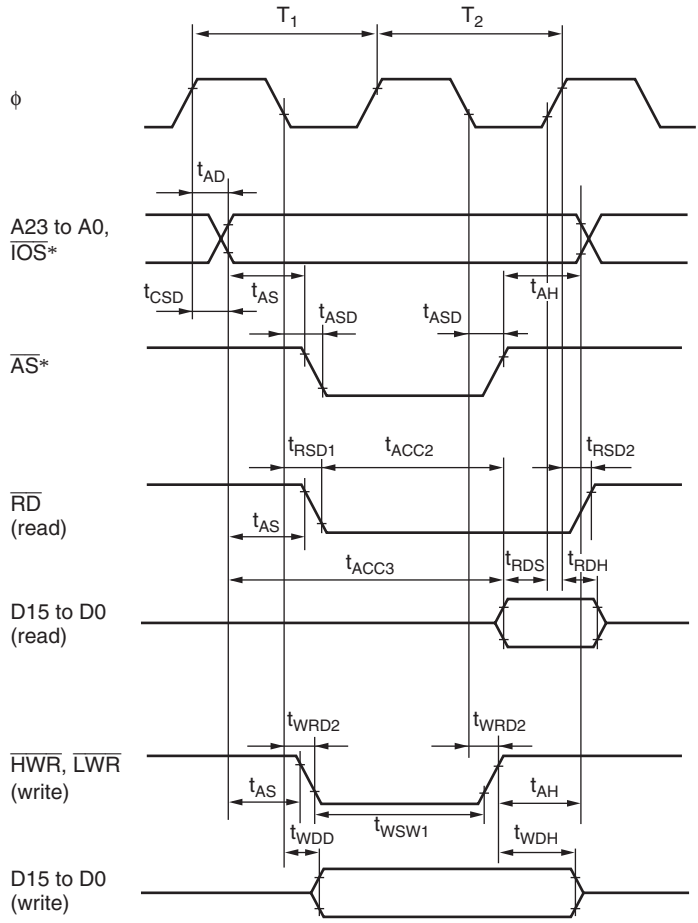
Table 20.7 Bus Timing (2) (Advanced Mode)

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

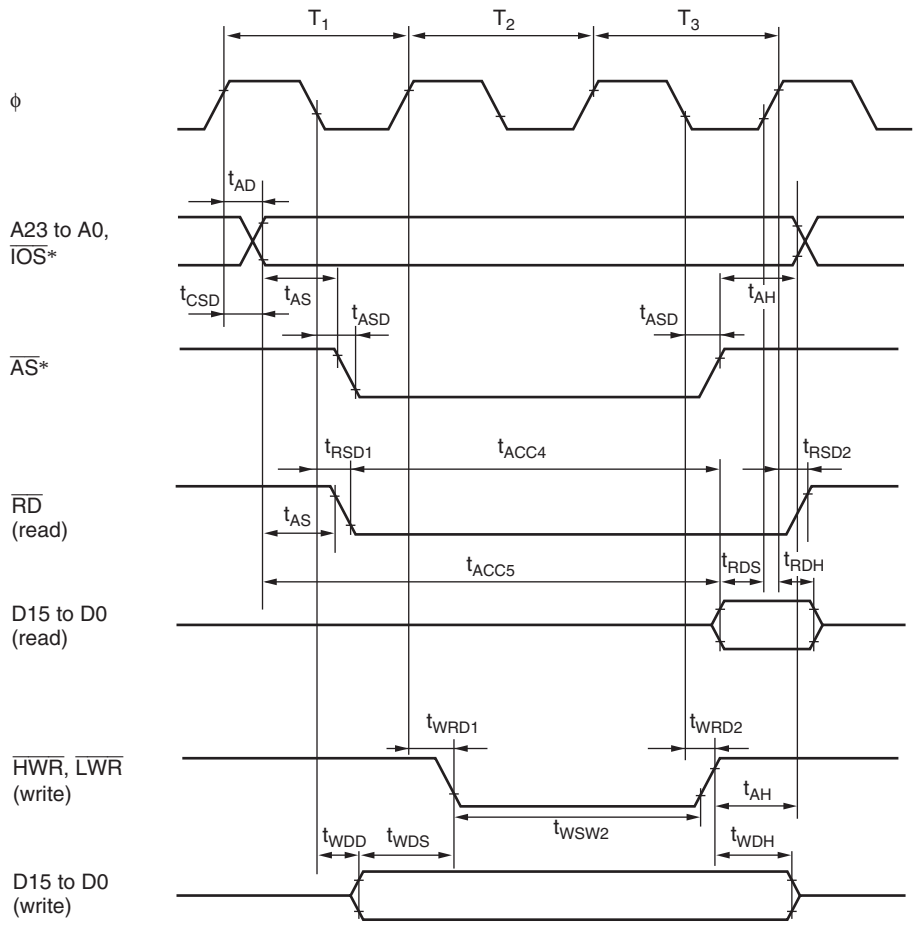
		Condition B		Condition A			
		16 MHz		20 MHz			Test
Item	Symbol	Min.	Max.	Min.	Max.	Unit	Conditions
Address delay time	t_{AD}	—	45	—	30	ns	Figures 20.9 to 20.13
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 35$	—	$0.5 \times t_{cyc} - 25$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	45	—	30	ns	
$\overline{AS}$ delay time	t_{ASD}	—	45	—	30	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	45	—	30	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	45	—	30	ns	
Read data setup time	t_{RDS}	20	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 55$	—	$1.0 \times t_{cyc} - 40$	ns	
Read data access time 2	t_{ACC2}	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 25$	ns	
Read data access time 3	t_{ACC3}	—	$3.0 \times t_{cyc} - 55$	—	$3.0 \times t_{cyc} - 40$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 25$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 55$	—	$3.0 \times t_{cyc} - 40$	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 1	t_{WRD1}	—	45	—	30	ns	
$\overline{HWR}$, $\overline{LWR}$ delay time 2	t_{WRD2}	—	45	—	30	ns	

Item	Symbol	Condition B 16 MHz Min.	Condition B 16 MHz Max.	Condition A 20 MHz Min.	Condition A 20 MHz Max.	Unit	Test Conditions
$\overline{HWR}$, $\overline{LWR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc}$ – 30	—	$1.0 \times t_{cyc}$ – 20	—	ns	
$\overline{HWR}$, $\overline{LWR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc}$ – 30	—	$1.5 \times t_{cyc}$ – 20	—	ns	Figures 20.9 to 20.13
Write data delay time	t_{WDD}	—	45	—	30	ns	
Write data setup time	t_{WDS}	0	—	0	—	ns	
Write data hold time	t_{WDH}	15	—	10	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	45	—	30	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	



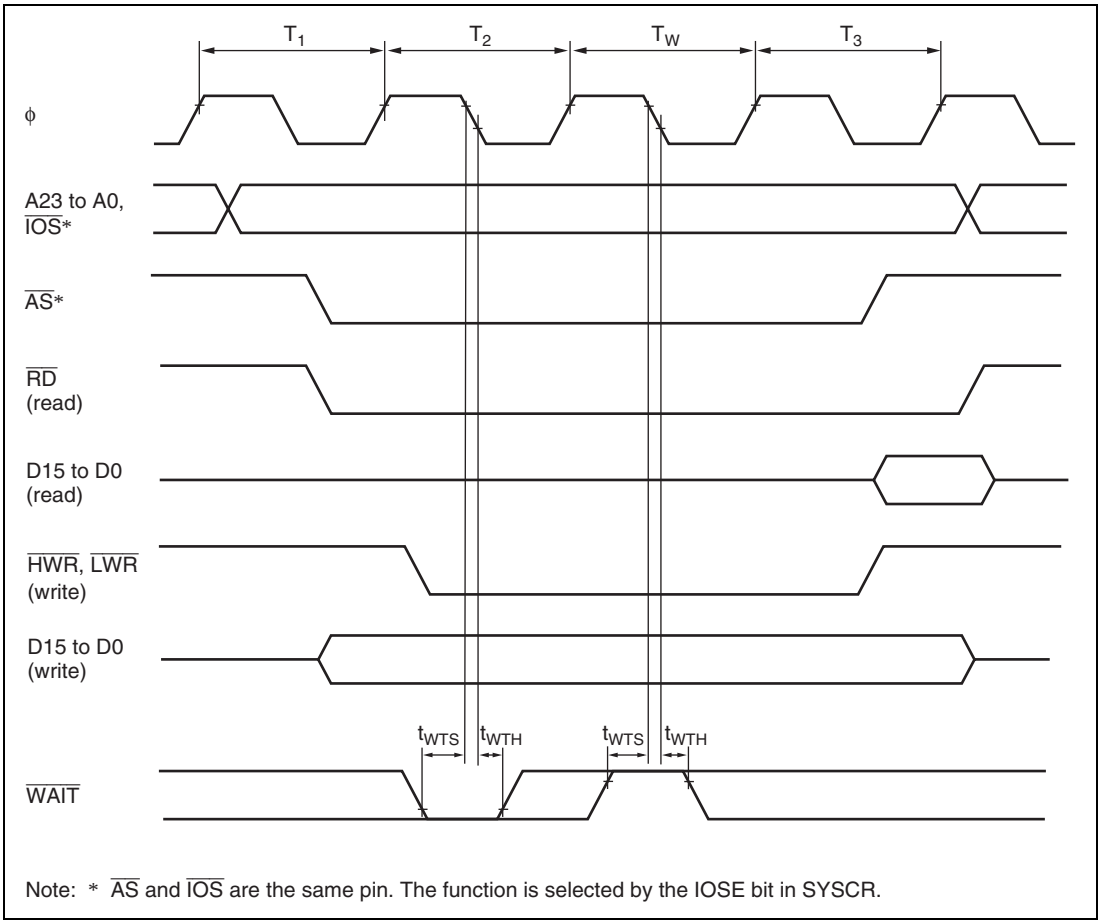
Note:* AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.9 Basic Bus Timing (Two-State Access)



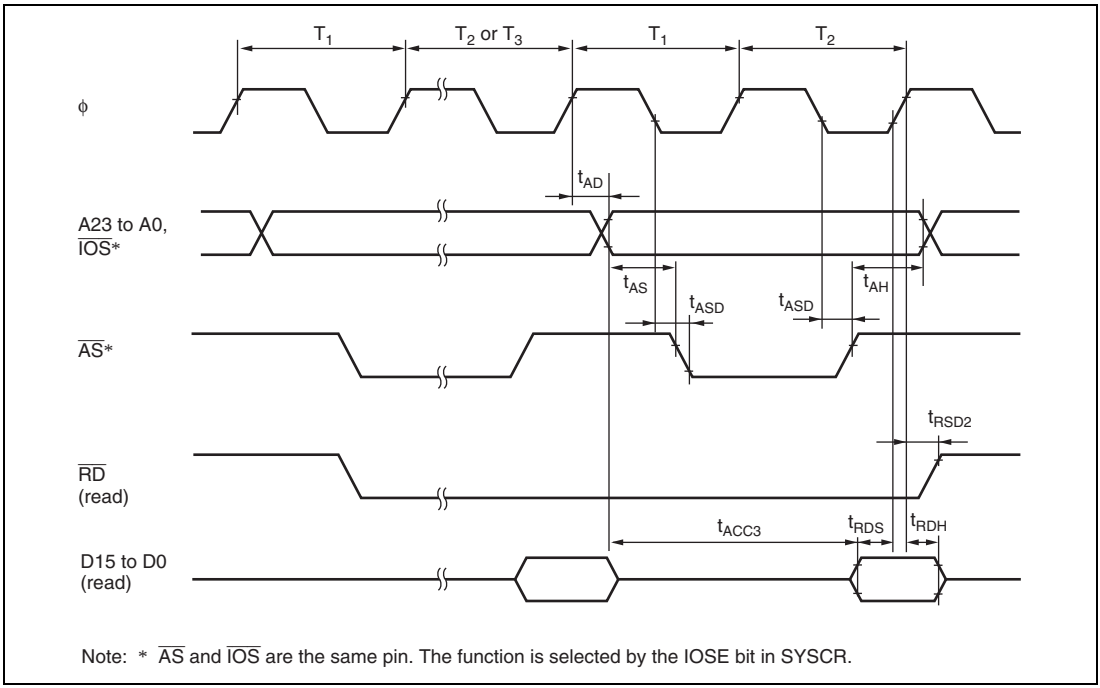
Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.10 Basic Bus Timing (Three-State Access)



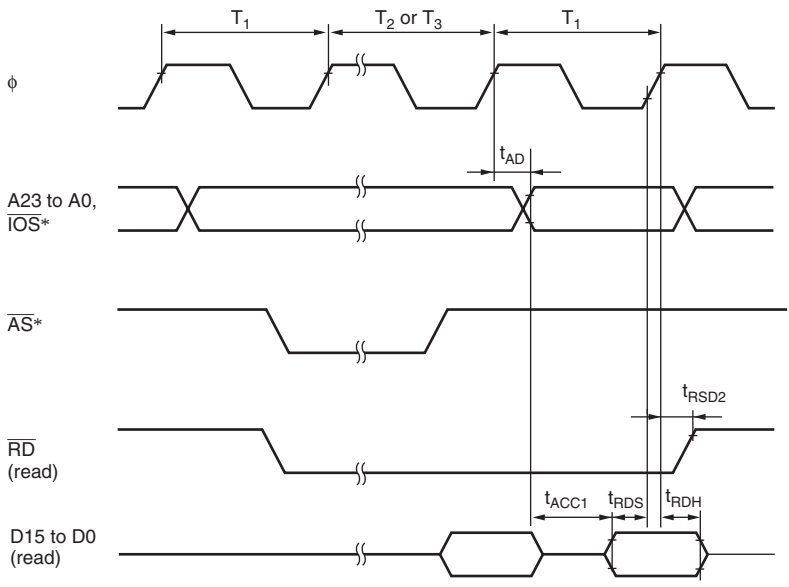
Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.11 Basic Bus Timing (Three-State Access with One Wait Cycle)



Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.12 Burst ROM Access Timing (Two-State Access)



Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.13 Burst ROM Access Timing (One-State Access)

Timing of On-Chip Peripheral Modules: Tables 20.8 shows the on-chip peripheral module timing. The only on-chip peripheral modules that can operate during this LSI operating on the subclock (ϕ = 32.768 kHz) are the I/O ports, external interrupts (NMI, IRQ0, IRQ1, IRQ2, IRQ6, and IRQ7), watchdog timer, and the 8-bit timer (channels 0 and 1).

Table 20.8 Timing of On-Chip Peripheral Modules

Condition A: V_{CC} = 5.0 V ±10%, $V_{CC}B$ = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 32.768 kHz* or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, $V_{CC}B$ = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 32.768 kHz* or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Note: * For modules that can operate during this LSI operating on the subclock

				Condition B		Condition A			
				16 MHz		20 MHz			
Item			Symbol	Min.	Max.	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	50	—	50	ns	Figure 20.14
	Input data setup time		t_{PRS}	30	—	30	—		
	Input data hold time		t_{PRH}	30	—	30	—		
FRT	Timer output delay time		t_{FTOD}	—	50	—	50	ns	Figure 20.15
	Timer input setup time		t_{FTIS}	30	—	30	—		
	Timer clock input setup time		t_{FTCS}	30	—	30	—		Figure 20.16
	Timer clock pulse width	Single edge	t_{FTCWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{FTCWL}	2.5	—	2.5	—		
TMR	Timer output delay time		t_{TMOD}	—	50	—	50	ns	Figure 20.17
	Timer reset input setup time		t_{TMRS}	30	—	30	—		Figure 20.19
	Timer clock input setup time		t_{TMCS}	30	—	30	—		Figure 20.18
	Timer clock pulse width	Single edge	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TMCWL}	2.5	—	2.5	—		
PWMX	Pulse output delay time		t_{PWOD}	—	50	—	50	ns	Figure 20.20

Item			Symbol	Condition B 16 MHz Min.	Condition B 16 MHz Max.	Condition A 20 MHz Min.	Condition A 20 MHz Max.	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 20.21
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock falling time		t_{SCKf}	—	1.5	—	1.5		
SCI	Transmit data delay time (synchronous)		t_{TXD}	—	50	—	50	ns	Figure 20.22
	Receive data setup time (synchronous)		t_{RXS}	50	—	50	—		
	Receive data hold time (synchronous)		t_{RXH}	50	—	50	—		
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 20.23
WDT	$\overline{\text{RESO}}$ output delay time		t_{RESD}	—	120	—	100	ns	Figure 20.24
	$\overline{\text{RESO}}$ output pulse width		t_{RESOW}	132	—	132	—	t_{cyc}	

Note: * Only on-chip peripheral modules that can be used in subclock operation

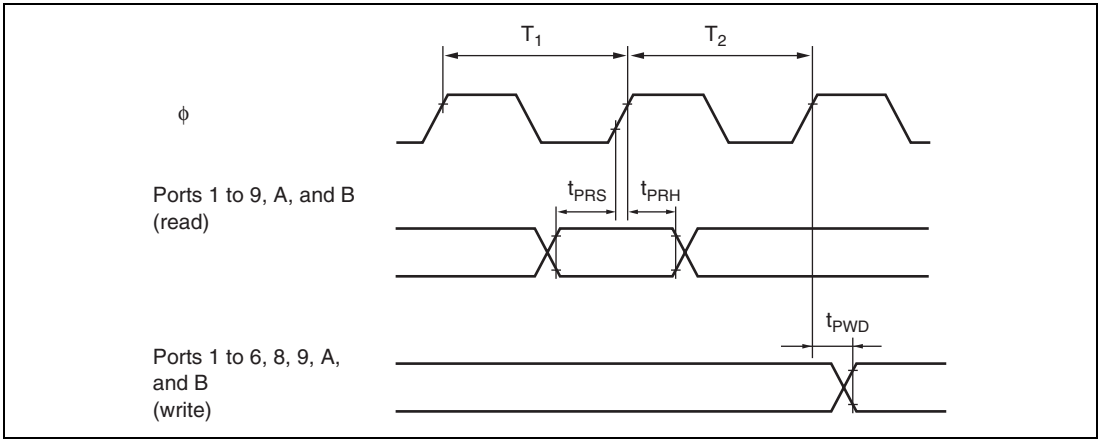


Figure 20.14 I/O Port Input/Output Timing

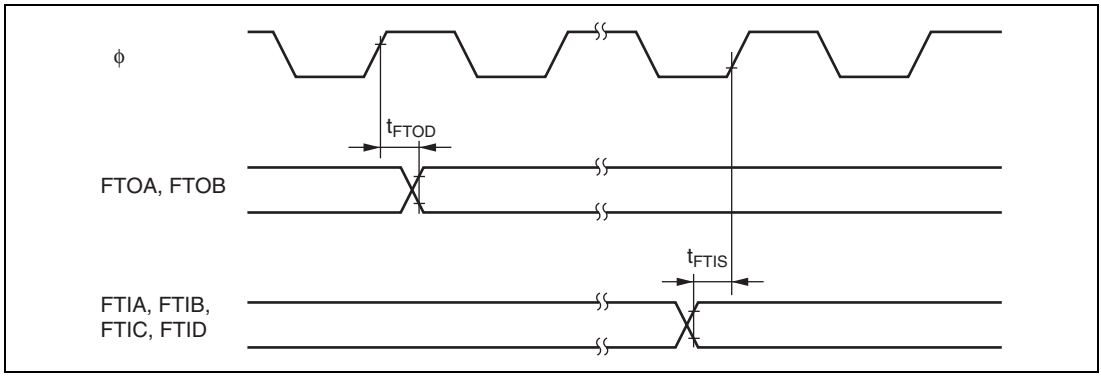


Figure 20.15 FRT Input/Output Timing

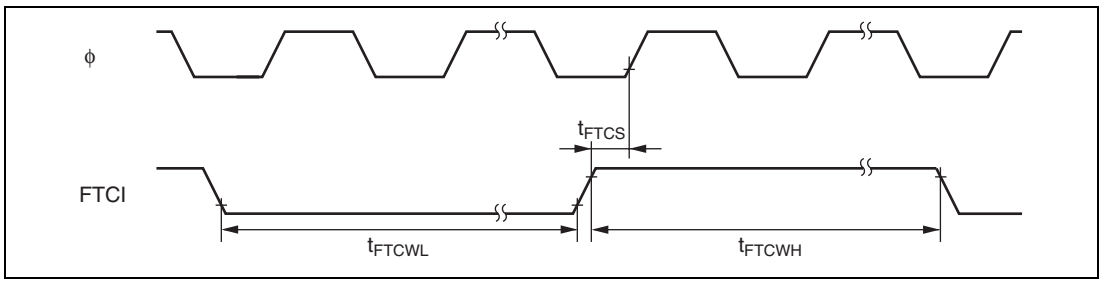


Figure 20.16 FRT Clock Input Timing

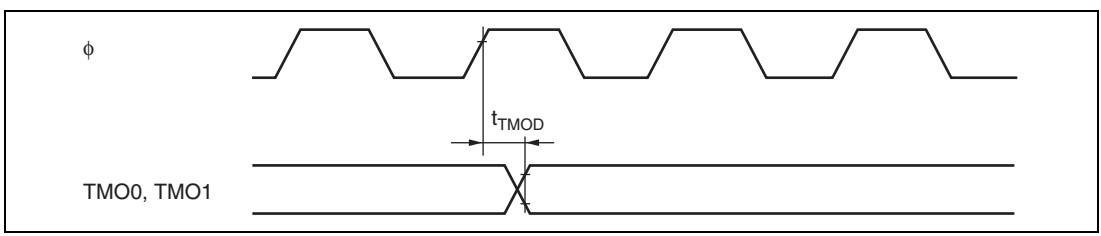


Figure 20.17 8-Bit Timer Output Timing

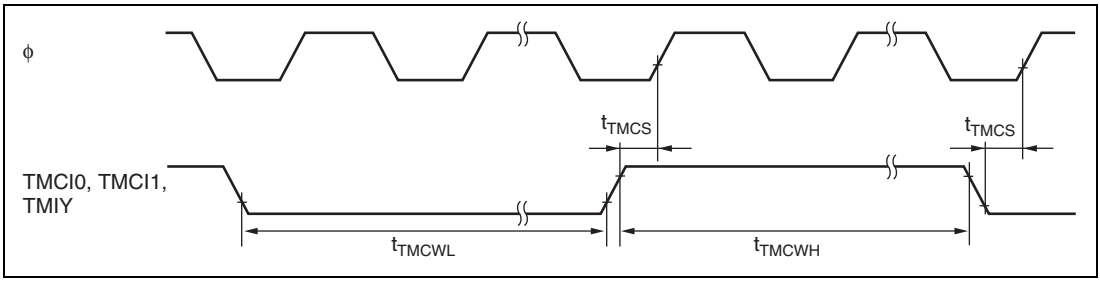


Figure 20.18 8-Bit Timer Clock Input Timing

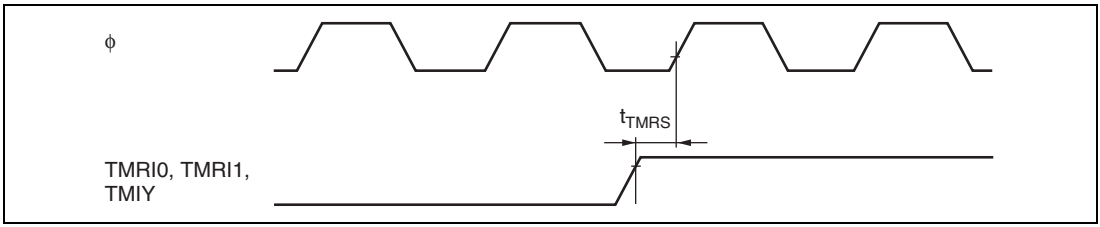


Figure 20.19 8-Bit Timer Reset Input Timing

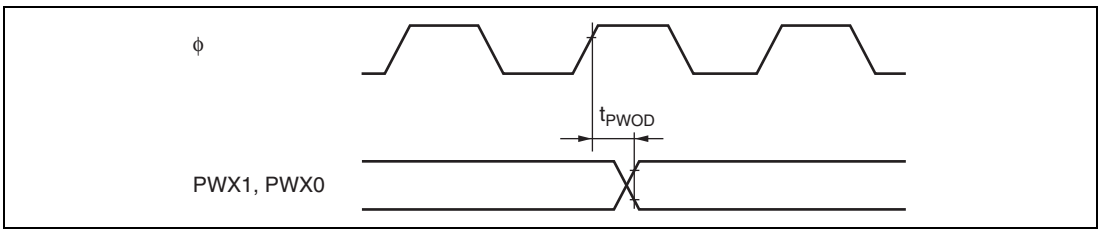


Figure 20.20 PWMX Output Timing

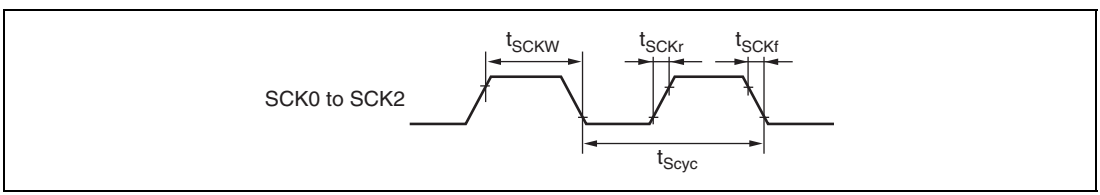


Figure 20.21 SCK Clock Input Timing

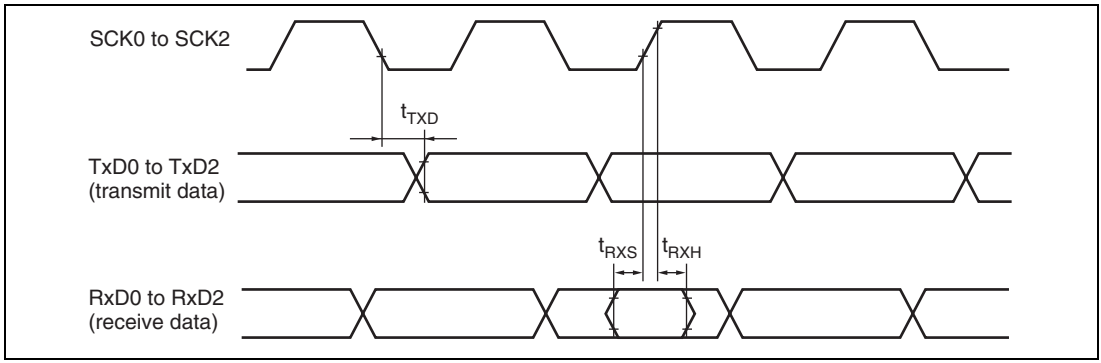


Figure 20.22 SCI Input/Output Timing (Synchronous Mode)

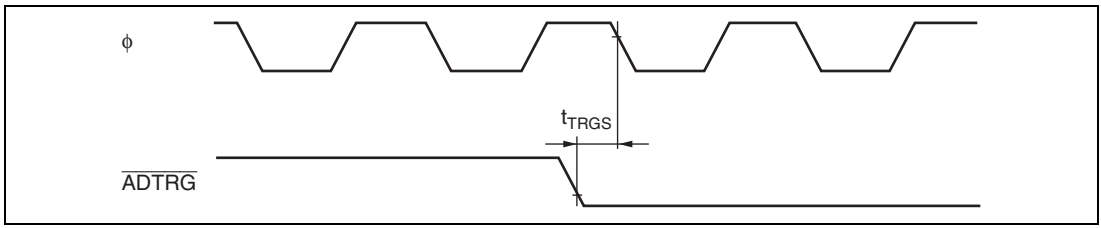


Figure 20.23 A/D Converter External Trigger Input Timing

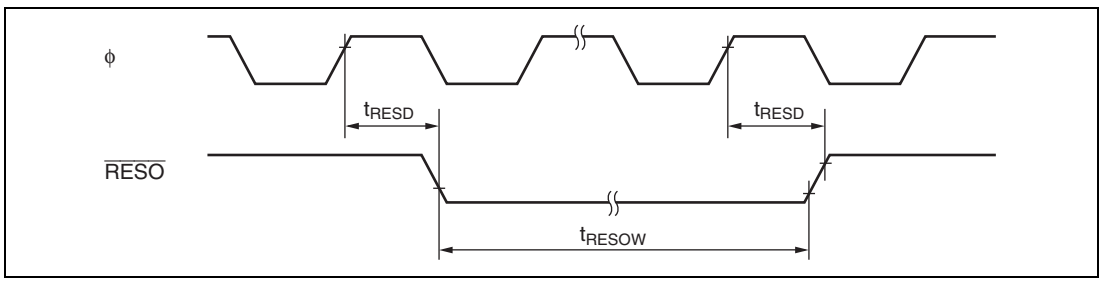


Figure 20.24 WDT Output Timing ($\overline{RESO}$)

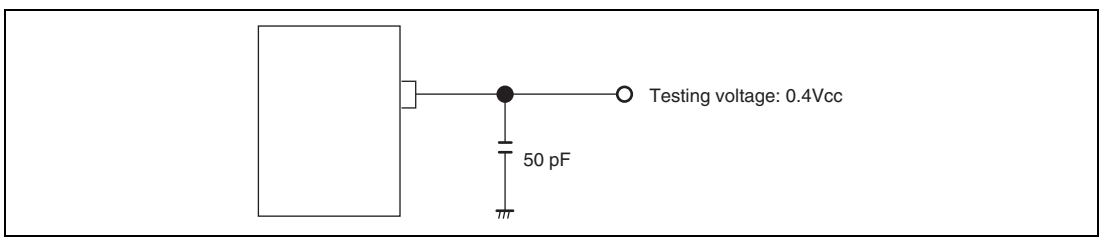


Figure 20.25 Tester Measurement Condition

20.1.4 A/D Conversion Characteristics

Tables 20.9 and 20.10 list the A/D conversion characteristics.

Table 20.9 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

	Condition B			Condition A			
	16 MHz			20 MHz			
Item	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Resolution		10			10		bits
Conversion time*[3]	—	—	8.4	—	—	6.7	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*[1] 5*[2]	—	—	10*[1] 5*[2]	kΩ
Nonlinearity error	—	—	±3.0	—	—	±3.0	LSB
Offset error	—	—	±3.5	—	—	±3.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	LSB

Notes: 1. When conversion time ≥ 11.17 µs (φ ≤ 12 MHz with CKS = 1 or CKS = 0)
2. When conversion time < 11.17 µs (φ > 12 MHz with CKS = 1)
3. When this LSI operates on the maximum operating frequency in single-chip mode

Table 20.10 A/D Conversion Characteristics
(CIN15 to CIN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

	Condition B			Condition A			
	16 MHz			20 MHz			
Item	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Resolution		10			10		bits
Conversion time*[3]	—	—	8.4	—	—	6.7	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*[1]	—	—	10*[1]	kΩ
			5*[2]			5*[2]	
Nonlinearity error	—	—	±5.0	—	—	±5.0	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

Notes: 1. When conversion time ≥ 11.17 µs (ϕ ≤ 12 MHz with CKS = 1 or CKS = 0)
2. When conversion time < 11.17 µs (ϕ > 12 MHz with CKS = 1)
3. When this LSI operates on the maximum operating frequency in single-chip mode

20.1.5 D/A Conversion Characteristics

Table 20.11 lists the D/A conversion characteristics.

Table 20.11 D/A Conversion Characteristics

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{ref} = 4.5 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, AV_{ref} = 4.0 V to AV_{CC},
V_{SS} = AV_{SS} = 0 V, φ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B			Condition A			
		16 MHz			20 MHz			
Item		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Resolution			8			8		bits
Conversion time	With 20 pF load capacitance	—	—	10	—	—	10	µs
Absolute accuracy	With 2 MΩ load resistance	—	±1.0	±1.5	—	±1.0	±1.5	LSB
	With 4 MΩ load resistance	—	—	±1.0	—	—	±1.0	

20.1.6 Flash Memory Characteristics

Table 20.12 shows the flash memory characteristics.

Table 20.12 Flash Memory Characteristics (Programming/Erasure)

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C (General specifications), Ta = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Programming time*[1]*[2]*[4]		t_P	—	10	200	ms/ 128 bytes	
Erasure time*[1]*[3]*[6]		t_E	—	100	1200	ms/ block	
Reprogramming count		N_{WEC}	—	—	100	times	
Programming	Wait time after setting SWE bit*[1]	x	1	—	—	µs	
	Wait time after setting PSU bit*[1]	y	50	—	—	µs	
	Wait time after setting P bit*[1]*[4]	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional write
	Wait time after clearing P bit *[1]	α	5	—	—	µs	
	Wait time after clearing PSU bit *[1]	β	5	—	—	µs	
	Wait time after setting PV bit *[1]	γ	4	—	—	µs	
	Wait time after dummy write*[1]	ε	2	—	—	µs	
	Wait time after clearing PV bit *[1]	η	2	—	—	µs	
	Wait time after clearing SWE bit *[1]	θ	100	—	—	µs	
	Maximum programming count*[1]*[4]*[5]	N	—	—	1000	times	

	Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Erasure	Wait time after setting SWE bit*[1]	x	1	—	—	µs	
	Wait time after setting ESU bit*[1]	y	100	—	—	µs	
	Wait time after setting E bit*[1]*[6]	z	10	—	100	ms	
	Wait time after clearing E bit*[1]	α	10	—	—	µs	
	Wait time after clearing ESU bit*[1]	β	10	—	—	µs	
	Wait time after setting EV bit*[1]	γ	20	—	—	µs	
	Wait time after dummy-writing H'FF*[1]	ε	2	—	—	µs	
	Wait time after clearing EV bit*[1]	η	4	—	—	µs	
	Wait time after clearing SWE bit*[1]	θ	100	—	—	µs	
	Maximum erasure count*[1]*[6]*[7]	N	—	—	120	times	

Notes: 1. Set the times according to the programming/erasing algorithms.

2. Programming time per 128 bytes (Shows the total period for which the P bit in FLMCR1 is set. It does not include the programming-verifying time.)

3. Block erasing time (Shows the total period for which the E bit in FLMCR1 is set. It does not include the erasing-verifying time.)

4. Maximum programming time (t_P (max.))

   t_P (max.) = (wait time after setting P bit (z1) + (z3)) × 6
   + wait time after setting P bit (z2) × ((N) – 6)

5. The maximum programming court (N) should be set according to the actual set value of z1, z2 and z3 to allow programming within the maximum programming time (t_P (max.)).

   The wait time after setting the P bit (z1, z2, and z3) should be alternated according to the programming count (n) as follows:

   $1 \leq n \leq 6$ z1 = 30µs, z3 = 10µs
   $7 \leq n \leq 1000$ z2 = 200µs

6. Maximum erasure time (t_E (max.))

   t_E (max.) = Wait time after setting E bit (z) × maximum erasure count (N)

7. The maximum erasure count (N) should be set according to the actual set value of z to allow erasing within the maximum erasure time (t_E (max.)).

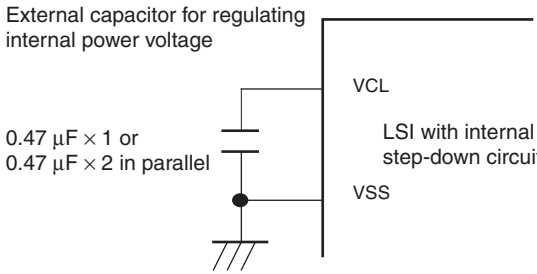
20.1.7 Usage Note

- LSI with Internal Step-Down Circuit

  This LSI includes an internal step-down circuit which automatically step down the internal power voltage to an appropriate level.

  A capacitor or capacitors for regulating the internal power voltage (one 0.47-µF capacitor or two 0.47-µF capacitors in parallel) must be placed between the internal step-down and VSS pins.

  For connection of the capacitor, see figure 20.26.



Do not connect the VCL pin of an LSI with the internal step-down circuit to the Vcc power. A capacitor or capacitors for regulating the internal power voltage must be connected to the VCL pin. The Capacitor should be a laminated ceramic type (0.47 µF × 1 or 0.47 µF × 2 in parallel) and placed close to the pins.

Figure 20.26 Connection of VCL Capacitor

20.2 Electrical Characteristics of H8S/2134B

20.2.1 Absolute Maximum Ratings

Table 20.13 lists the absolute maximum ratings.

Table 20.13 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.3 to +7.3	V
Power supply (VCL input)*	V_{CL}	–0.3 to +4.3	V
Input voltage (other than ports 6 and 7)	V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (CIN input not selected for port 6)	V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (CIN input selected for port 6)	V_{in}	–0.3 V to lower of voltages V_{CC} + 0.3 and AV_{CC} + 0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	General specifications: –20 to +75	°C
		Wide temperature range specifications: –40 to +85	
Operating temperature (flash memory programming/erasing)	T_{opr}	General specifications: –20 to +75	°C
		Wide temperature range specifications: –40 to +85	
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Operating this LSI in excess of the absolute maximum ratings may result in permanent damage.

Do not apply a voltage exceeding 7.0 V to input pins for the 5-V/4-V operation products.

Note: * Power supply pin for the internal power supply. Do not apply a power to the VCL pin for the 5-V/4-V operation products. Connect a capacitor for regulating the internal power voltage between the VCL and GND pins.

20.2.2 DC Characteristics

Table 20.14 lists the DC characteristics. Permissible output current values are shown in table 20.16.

Table 20.14 DC Characteristics (1)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC}*[1] = 5.0 V ±10%, V_{SS} = AV_{SS}*[1] = 0 V,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60 (KWUL = 00)*[2]*[4], $\overline{KIN7}$ to $\overline{KIN0}$, $\overline{IRQ2}$ to $\overline{IRQ0}$*[3], $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	0.4	—	—		
Schmitt trigger input voltage (level switching)*[4]	P67 to P60 (KWUL = 01)		V_T^-	$V_{CC} \times 0.3$	—	—	V	
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—		
	P67 to P60 (KWUL = 10)		V_T^-	$V_{CC} \times 0.4$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.8$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.03$	—	—		
	P67 to P60 (KWUL = 11)		V_T^-	$V_{CC} \times 0.45$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.9$		
			$V_T^+ - V_T^-$	0.05	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	
	EXTAL			$V_{CC} \times 0.7$	—	V_{CC} + 0.3		
	Port 7			2.0		AV_{CC} + 0.3		
	Input pins except (1) and (2) above			2.0		V_{CC} + 0.3		

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0 (3)	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, input pins except (1) and (3) above		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OL} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3		—	—	1.0	V	I_{OL} = 10 mA

Notes: 1. Do not leave the AV_{CC} and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AV_{CC} pin to the power supply (V_{CC}), or some other method.

2. Characteristics for P67 to P60 also indicate those for multiplexed signals of on-chip peripheral modules.
3. Characteristic for $\overline{IRQ2}$ also indicate that for the multiplexed $\overline{ADTRG}$ signal.
4. The upper limit of the applicable voltage for port 6 is V_{CC} + 0.3 V when CIN input is not selected, and the lower of V_{CC} + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is the applicable voltage.

Table 20.14 DC Characteristics (2)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC}*[1] = 5.0 V ±10%, V_{SS} = AV_{SS}*[1] = 0 V,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

	Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD1, MD0		—	—	1.0		
	Port 7		—	—	1.0		V_{in} = 0.5 to AV_{CC} – 0.5 V
Tri-state leakage current (off state)	Ports 1 to 6, 8, 9	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V
	Port 6 (P6PUE = 1)		60	—	600		
	Port 6 (P6PUE = 1)		15	—	200		
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50		
	Input pins except (4) above		—	—	15		
Current consumption*[2]	Normal operation	I_{CC}	—	55	70	mA	f = 20 MHz
	Sleep mode		—	36	55	mA	f = 20 MHz
	Standby mode*[3]		—	1.0	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0		50°C < T_a
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reference power supply current*[4]	During A/D conversion	AI_{ref}	—	0.5	1.0	mA	
	During A/D, D/A conversion		—	2.0	5.0		
	Idle		—	0.01	5.0	µA	
Analog power supply voltage*[1]		AV_{CC}	4.5	—	5.5	V	Operating
			2.0	—	5.5		Idle/not used
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AV_{CC} and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AV_{CC} pin to the power supply (V_{CC}), or some other method.

2. Current consumption values are for V_{IH} min. = V_{CC} – 0.2 V and V_{IL} max. = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs disabled.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, V_{IH} min. = V_{CC}– 0.2 V and V_{IL} max. = 0.2 V.
4. The reference power supply current (AI_{ref}) is added to the analog power supply current (AI_{CC}).

Table 20.14 DC Characteristics (3)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC}*[1] = 4.0 V to 5.5 V, V_{SS} = AV_{SS}*[1] = 0 V, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P67 to P60 (KWUL = 00)*[2]*[4], $\overline{KIN7}$ to $\overline{KIN0}$, $\overline{IRQ2}$ to $\overline{IRQ0}$*[3], $\overline{IRQ5}$ to $\overline{IRQ3}$	(1)	V_T^-	1.0	—	—	V	V_{CC} = 4.5 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	0.4	—	—		
			V_T^-	0.8	—	—	V	V_{CC} = 4.0 V to 4.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	0.3	—	—		
Schmitt trigger input voltage (level switching)	P67 to P60 (KWUL = 01)		V_T^-	$V_{CC} \times 0.3$	—	—	V	V_{CC} = 4.0 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.05$	—	—		
	P67 to P60 (KWUL = 10)		V_T^-	$V_{CC} \times 0.4$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.8$		
			$V_T^+ - V_T^-$	$V_{CC} \times 0.03$	—	—		
	P67 to P60 (KWUL = 11)		V_T^-	$V_{CC} \times 0.45$	—	—		
			V_T^+	—	—	$V_{CC} \times 0.9$		
			$V_T^+ - V_T^-$	0.05	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0	(2)	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL			$V_{CC} \times 0.7$	—	V_{CC} + 0.3		
	Port 7			2.0	—	AV_{CC} + 0.3		
	Input pins except (1) and (2) above			2.0	—	V_{CC} + 0.3		

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD1, MD0 (3)	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, input pins except (1) and (3) above		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA, V_{CC} = 4.5 V to 5.5 V
			3.0	—	—	V	I_{OH} = –1 mA, V_{CC} = 4.0 V to 4.5 V
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1 to 3		—	—	1.0	V	I_{OL} = 10 mA

Notes: 1. Do not leave the AV_{CC} and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AV_{CC} pin to the power supply (V_{CC}), or some other method.

2. Characteristics for P67 to P60 also indicate those for multiplexed signals of on-chip peripheral modules.
3. Characteristic for $\overline{IRQ2}$ also indicate that for the multiplexed $\overline{ADTRG}$ signal.
4. The upper limit of the applicable voltage for port 6 is V_{CC} + 0.3 V when CIN input is not selected, and the lower of V_{CC} + 0.3 V and AV_{CC} + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is the applicable voltage.

Table 20.14 DC Characteristics (4)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC}*[1] = 4.0 V to 5.5 V, V_{SS} = AV_{SS}*[1] = 0 V, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD1, MD0		—	—	1.0		
	Port 7		—	—	1.0		V_{in} = 0.5 to AV_{CC} – 0.5 V
Tri-state leakage current (off state)	Ports 1 to 6, 8, 9	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	300	µA	V_{in} = 0 V, V_{CC} = 4.5 V to 5.5 V
	Port 6 (P6PUE = 1)		60	—	600		
	Port 6 (P6PUE = 1)		15	—	200		
	Ports 1 to 3		20	—	200	µA	V_{in} = 0 V, V_{CC} = 4.0 V to 4.5 V
	Port 6 (P6PUE = 1)		40	—	500		
	Port 6 (P6PUE = 1)		10		150		
Input capacitance	$\overline{RES}$ (4)	C_{in}	—	—	80	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	NMI		—	—	50		
	Input pins except (4) above		—	—	15		
Current consumption*[2]	Normal operation	I_{CC}	—	45	58	mA	f = 16 MHz
	Sleep mode		—	30	46	mA	f = 16 MHz
	Standby mode*[3]		—	1.0	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0		50°C < T_a

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D, D/A conversion	AI_{CC}	—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	AV_{CC} = 2.0 V to 5.5 V
Reference power supply current*[4]	During A/D conversion	AI_{ref}	—	0.5	1.0	mA	
	During A/D, D/A conversion		—	2.0	5.0		
	Idle		—	0.01	5.0	µA	
Analog power supply voltage*[1]		AV_{CC}	4.0	—	5.5	V	Operating
			2.0	—	5.5		Idle/not used
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. Do not leave the AV_{CC} and AV_{SS} pins open even if the A/D converter and D/A converter are not used.

Even if the A/D converter and D/A converter are not used, apply a voltage in the range from 2.0 V to 5.5 V by connecting the AV_{CC} pin to the power supply (V_{CC}), or some other method.

2. Current consumption values are for V_{IH} min. = V_{CC} – 0.2 V and V_{IL} max. = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs disabled.
3. The values are for $V_{RAM} \leq V_{CC} < 4.0$ V, V_{IH} min. = V_{CC}– 0.2 V and V_{IL} max. = 0.2 V.
4. The reference power supply current (AI_{ref}) is added to the analog power supply current (AI_{CC}).

Table 20.15 Permissible Output Currents

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	Ports 1 to 3	I_{OL}	—	—	10	mA
	Other output pins		—	—	2	
Permissible output low current (total)	Total of ports 1 to 3	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Notes: 1. To ensure reliability, do not exceed the output current values in table 20.3.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 20.27 and 20.28.

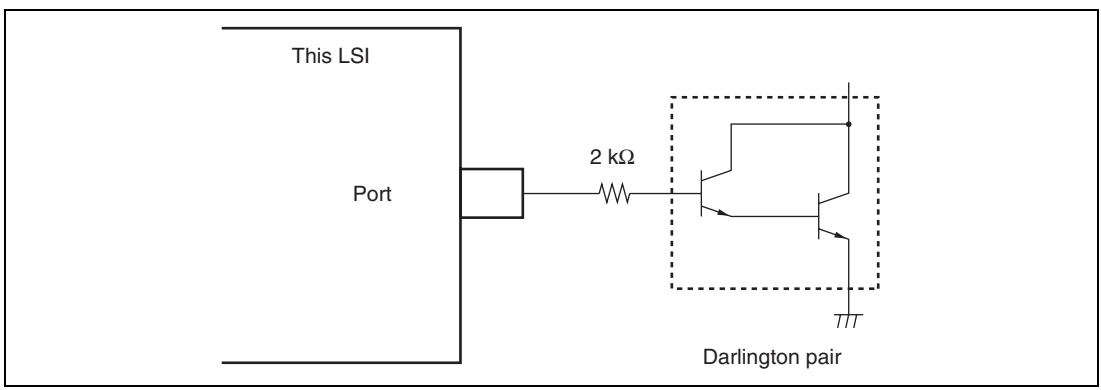


Figure 20.27 Darlington Pair Driving Circuit (Example)

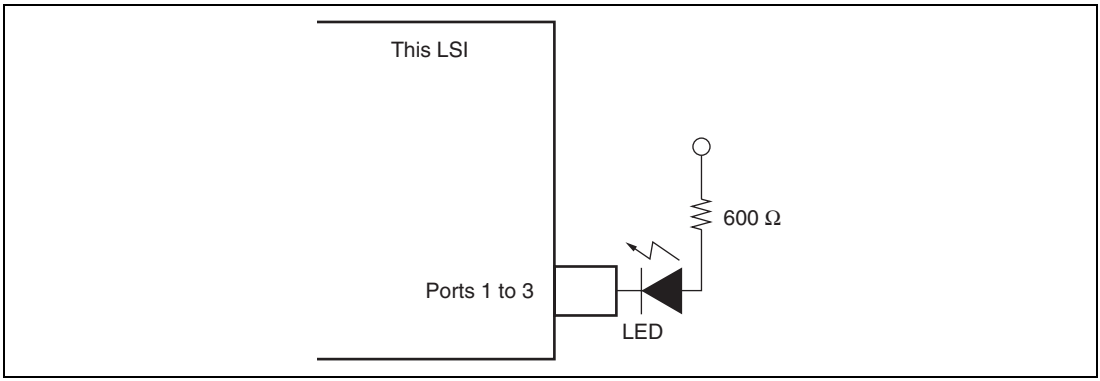


Figure 20.28 LED Driving Circuit (Example)

20.2.3 AC Characteristics

Figure 20.29 shows the test conditions for the AC characteristics.

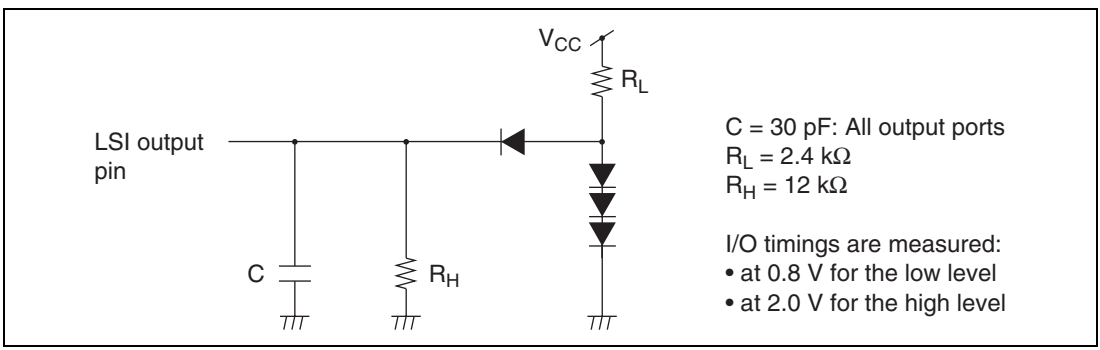


Figure 20.29 Output Load Circuit

Clock Timing: Table 20.16 shows the clock timing. The clock timing specified here covers clock (ϕ) output and oscillation stabilization times of the clock pulse generator (crystal) and external clock input (the EXTAL pin). For details on external clock input (the EXTAL pin and EXCL pin) timing, see section 17, Clock Pulse Generator.

Table 20.16 Clock Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B		Condition A			
		16 MHz		20 MHz			
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Reference**
Clock cycle time	t_{cyc}	62.5	500	50	500	ns	Figure 20.30
Clock high pulse width	t_{CH}	20	—	17	—	ns	Figure 20.30
Clock low pulse width	t_{CL}	20	—	17	—	ns	
Clock rising time	t_{Cr}	—	10	—	8	ns	
Clock falling time	t_{Cf}	—	10	—	8	ns	
Oscillation stabilization time at reset (crystal)	t_{OSC1}	10	—	10	—	ms	Figure 20.31
Oscillation stabilization time at leaving software standby (crystal)	t_{OSC2}	8	—	8	—	ms	Figure 20.32
External clock output stabilization delay time	t_{DEXT}	500	—	500	—	µs	

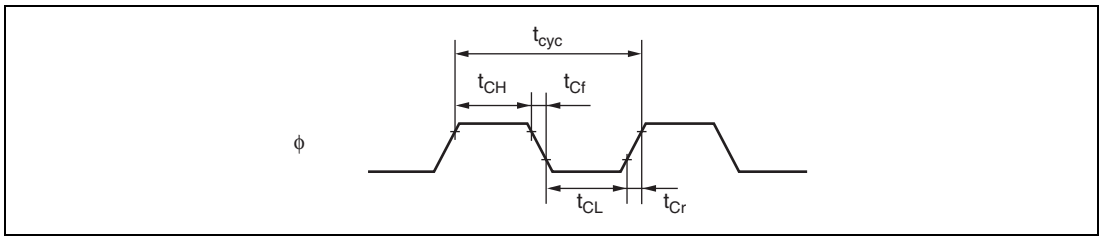


Figure 20.30 System Clock Timing

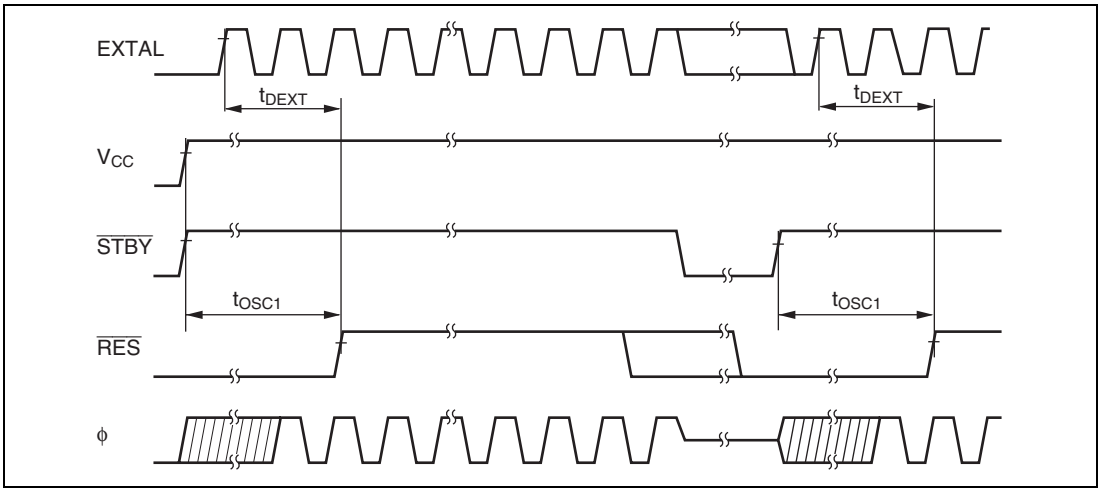


Figure 20.31 Oscillation Stabilization Timing

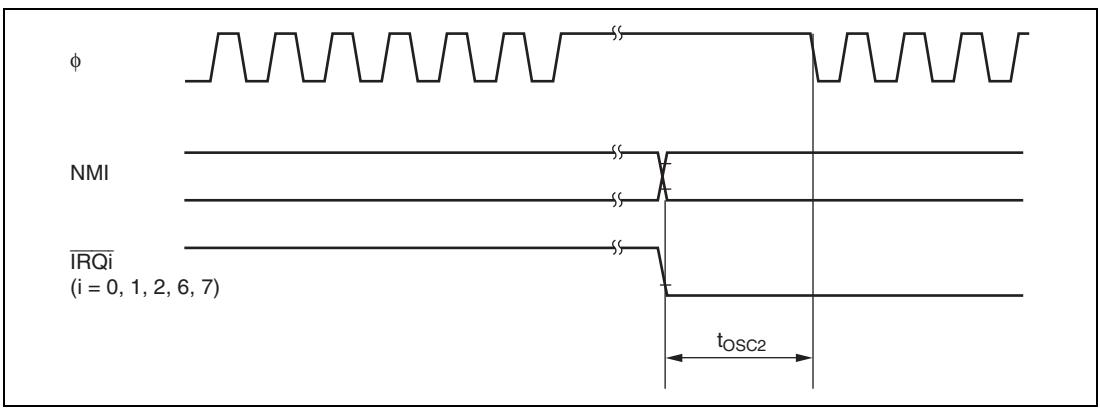


Figure 20.32 Oscillation Stabilization Timing (Leaving Software Standby Mode)

Control Signal Timing: Table 20.17 shows the control signal timing. The only external interrupts that can be received during this LSI operating on the subclock (ϕ = 32.768 kHz) are NMI, IRQ0, IRQ1, IRQ2, IRQ6, and IRQ7.

Table 20.17 Control Signal Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 32.768 kHz or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 32.768 kHz or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B		Condition A			
		16 MHz		20 MHz			Test
Item	Symbol	Min.	Max.	Min.	Max.	Unit	Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 20.33
$\overline{RES}$ pulse width	t_{RESW}	20	—	20	—	t_{cyc}	
NMI setup time (NMI)	t_{NMIS}	150	—	150	—	ns	Figure 20.34
NMI hold time (NMI)	t_{NMIH}	10	—	10	—	ns	
NMI pulse width (leaving software standby mode)	t_{NMIW}	200	—	200	—	ns	
IRQ setup time ($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQS}	150	—	150	—	ns	
IRQ hold time($\overline{IRQ7}$ to $\overline{IRQ0}$)	t_{IRQH}	10	—	10	—	ns	
IRQ pulse width ($\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ2}$ to $\overline{IRQ0}$) (leaving software standby mode)	t_{IRQW}	200	—	200	—	ns	

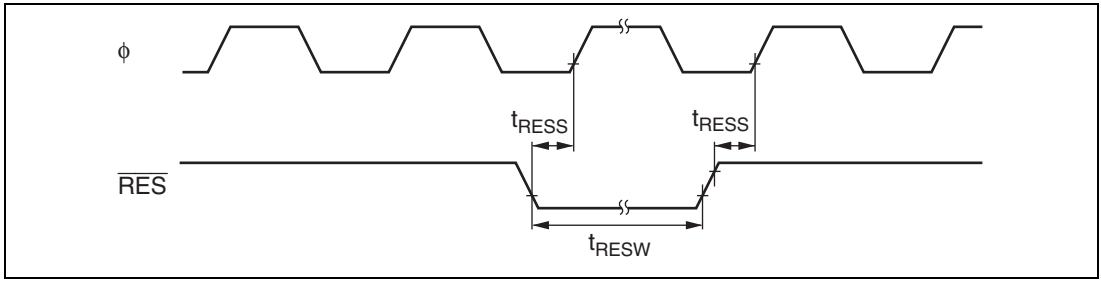


Figure 20.33 Reset Input Timing

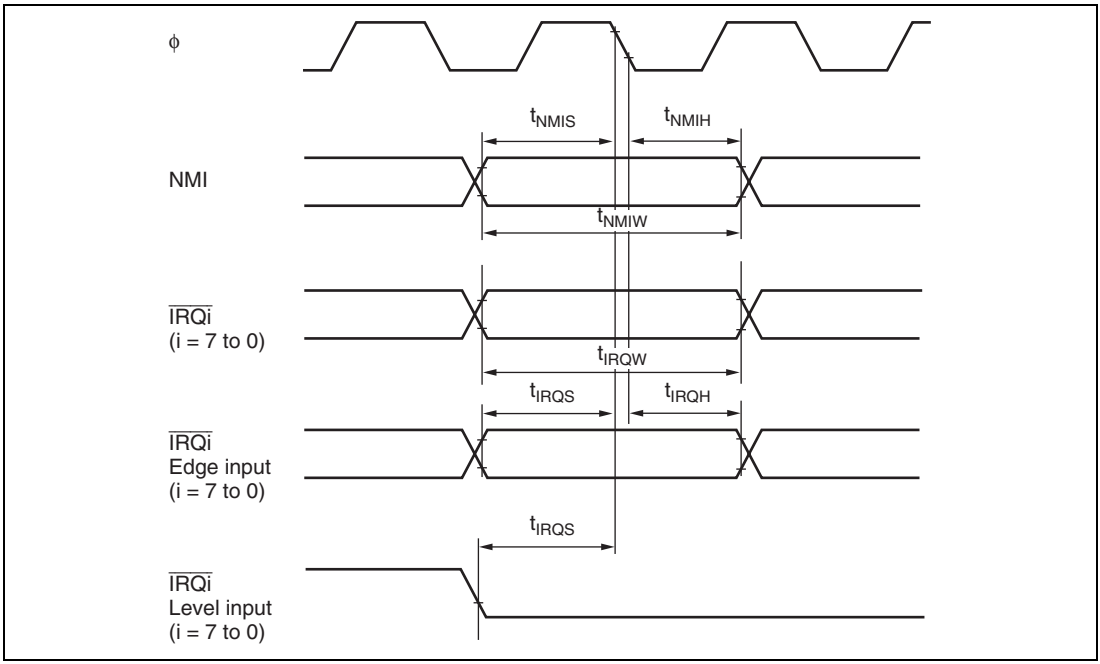


Figure 20.34 Interrupt Input Timing

Bus Timing: Table 20.18 shows the bus timing. Operation in external extended mode is not guaranteed when this LSI is operating on the subclock (ϕ = 32.768 kHz).

Bus Timing: Table 20.18 shows the bus timing. Operation in external expansion mode is not guaranteed when operating on the subclock (φ = 32.768 kHz).

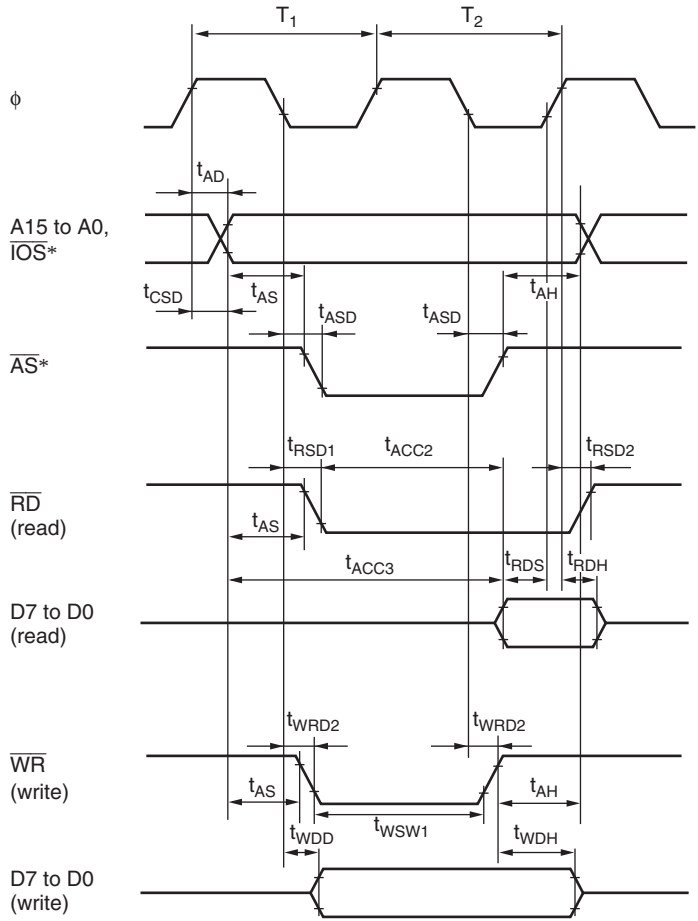
Table 20.18 Bus Timing

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, φ = 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

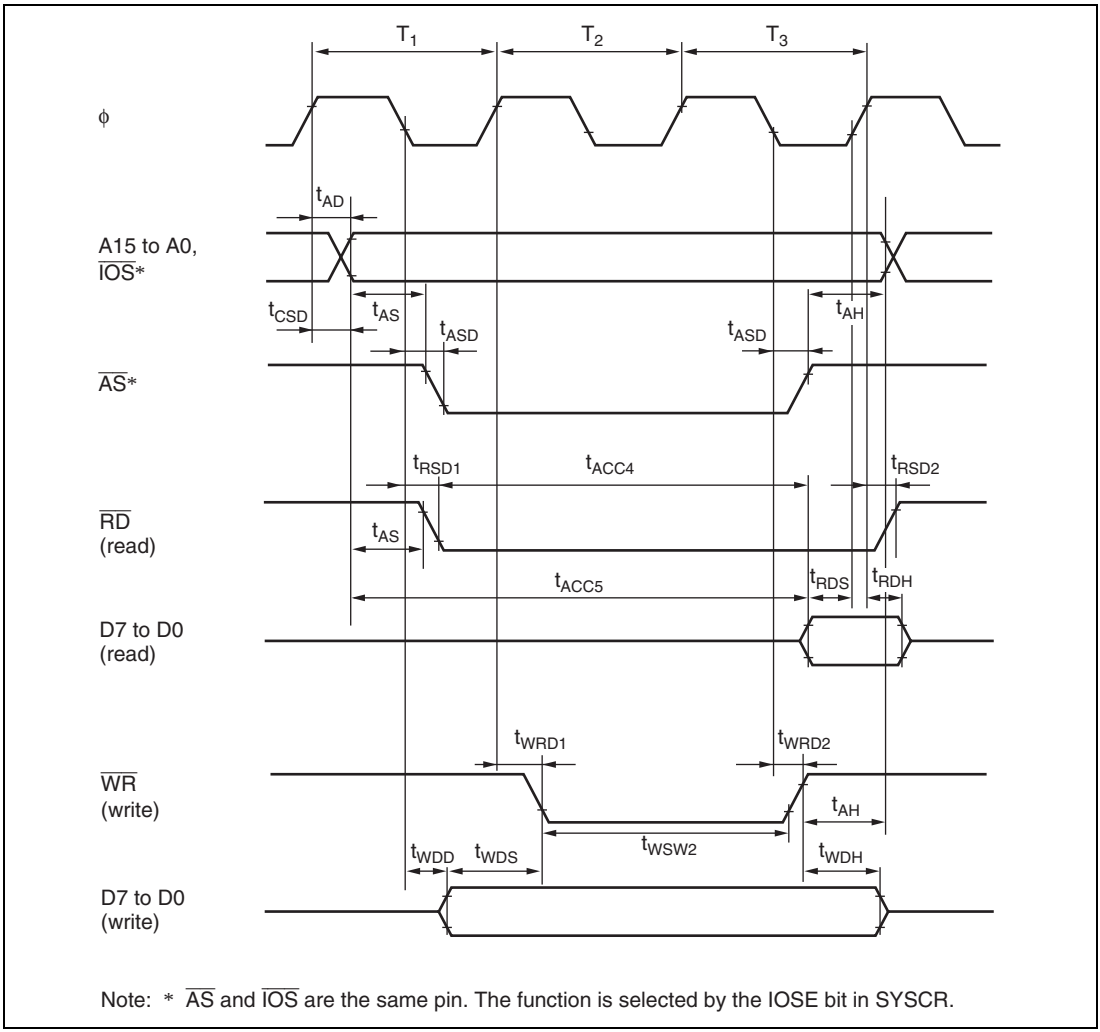
		Condition B		Condition A			
		16 MHz		20 MHz			Test
Item	Symbol	Min.	Max.	Min.	Max.	Unit	Conditions
Address delay time	t_{AD}	—	30	—	20	ns	Figures 20.35 to 20.39
Address setup time	t_{AS}	$0.5 \times t_{cyc} - 20$	—	$0.5 \times t_{cyc} - 15$	—	ns	
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 15$	—	$0.5 \times t_{cyc} - 10$	—	ns	
$\overline{CS}$ delay time ($\overline{IOS}$)	t_{CSD}	—	30	—	20	ns	
$\overline{AS}$ delay time	t_{ASD}	—	45	—	30	ns	
$\overline{RD}$ delay time 1	t_{RSD1}	—	45	—	30	ns	
$\overline{RD}$ delay time 2	t_{RSD2}	—	45	—	30	ns	
Read data setup time	t_{RDS}	20	—	15	—	ns	
Read data hold time	t_{RDH}	0	—	0	—	ns	
Read data access time 1	t_{ACC1}	—	$1.0 \times t_{cyc} - 40$	—	$1.0 \times t_{cyc} - 30$	ns	
Read data access time 2	t_{ACC2}	—	$1.5 \times t_{cyc} - 35$	—	$1.5 \times t_{cyc} - 25$	ns	
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 40$	—	$2.0 \times t_{cyc} - 30$	ns	
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 35$	—	$2.5 \times t_{cyc} - 25$	ns	
Read data access time 5	t_{ACC5}	—	$3.0 \times t_{cyc} - 40$	—	$3.0 \times t_{cyc} - 30$	ns	

Item	Symbol	Condition B 16 MHz Min.	Condition B 16 MHz Max.	Condition A 20 MHz Min.	Condition A 20 MHz Max.	Unit	Test Conditions
$\overline{WR}$ delay time 1	t_{WRD1}	—	45	—	30	ns	Figures 20.35 to 20.39
$\overline{WR}$ delay time 2	t_{WRD2}	—	45	—	30	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc} - 30$	—	$1.0 \times t_{cyc} - 20$	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc} - 30$	—	$1.5 \times t_{cyc} - 20$	—	ns	
Write data delay time	t_{WDD}	—	45	—	30	ns	
Write data setup time	t_{WDS}	0	—	0	—	ns	
Write data hold time	t_{WDH}	15	—	10	—	ns	
$\overline{WAIT}$ setup time	t_{WTS}	45	—	30	—	ns	
$\overline{WAIT}$ hold time	t_{WTH}	5	—	5	—	ns	



Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.35 Basic Bus Timing (Two-State Access)



Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.36 Basic Bus Timing (Three-State Access)

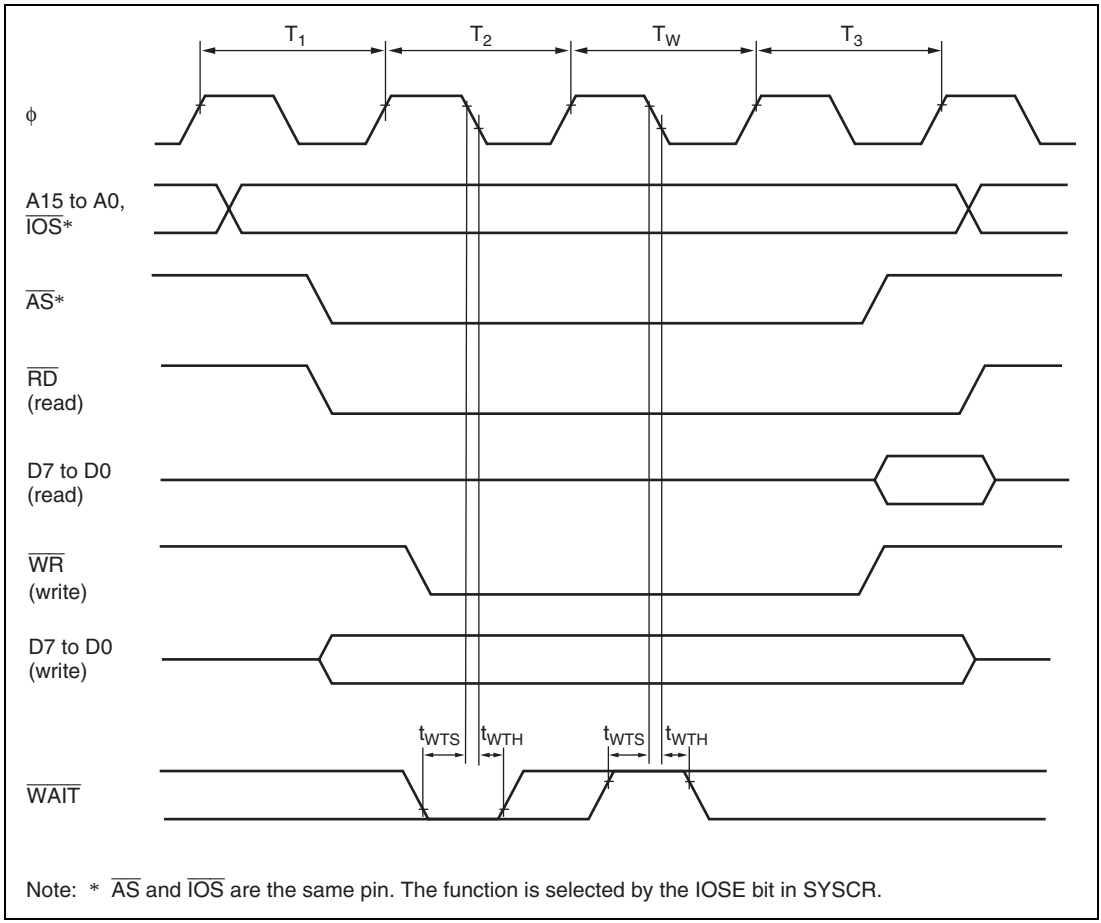
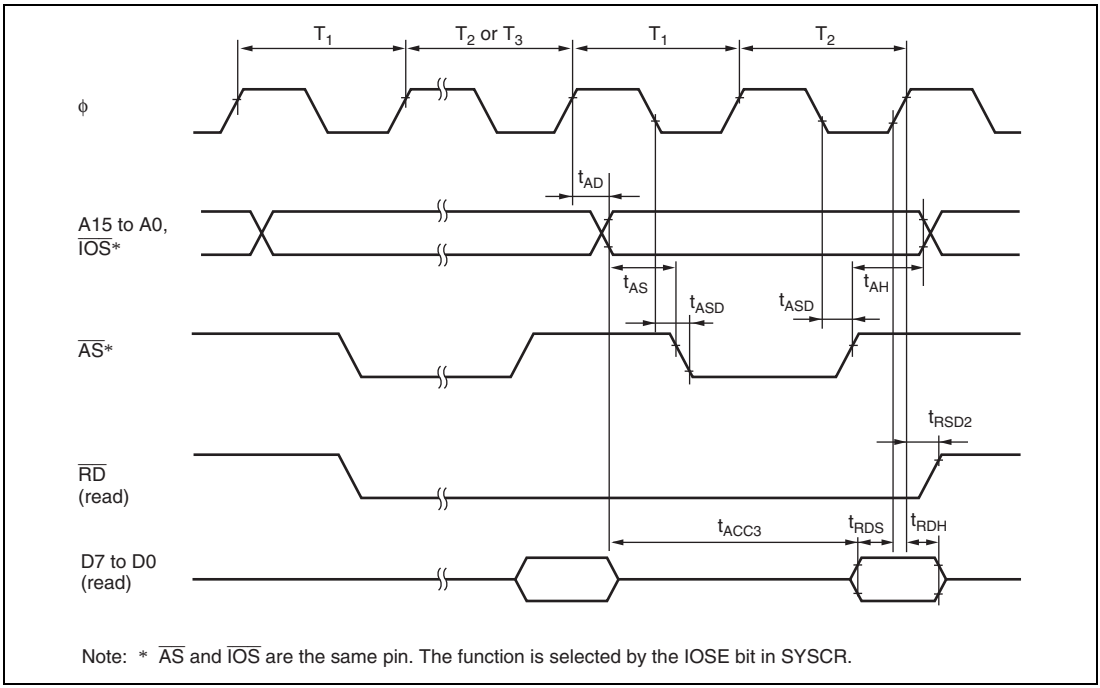
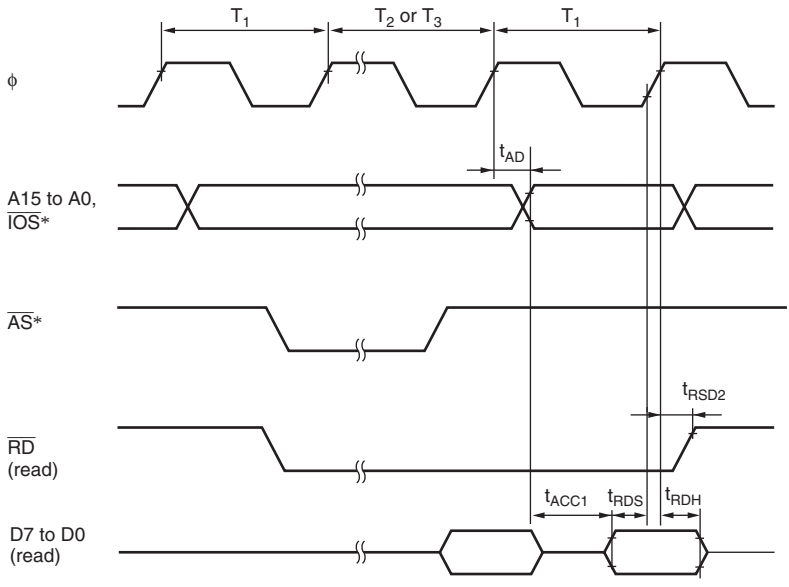


Figure 20.37 Basic Bus Timing (Three-State Access with One Wait Cycle)



Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.38 Burst ROM Access Timing (Two-State Access)



Note: * $\overline{AS}$ and $\overline{IOS}$ are the same pin. The function is selected by the IOSE bit in SYSCR.

Figure 20.39 Burst ROM Access Timing (One-State Access)

Timing of On-Chip Peripheral Modules: Tables 20.19 shows the on-chip peripheral module timing. The only on-chip peripheral modules that can operate during this LSI operating on the subclock (ϕ = 32.768 kHz) are the I/O ports, external interrupts (NMI, IRQ0, IRQ1, IRQ2, IRQ6, and IRQ7), watchdog timer, and the 8-bit timer (channels 0 and 1).

Table 20.19 Timing of On-Chip Peripheral Modules

Condition A: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 32.768 kHz* or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, ϕ = 32.768 kHz* or 2 MHz to maximum operating frequency, T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Note: * For modules that can operate during this LSI operating on the subclock

				Condition B		Condition A			
				16 MHz		20 MHz			
Item			Symbol	Min.	Max.	Min.	Max.	Unit	Test Conditions
I/O ports	Output data delay time		t_{PWD}	—	50	—	50	ns	Figure 20.40
	Input data setup time		t_{PRS}	30	—	30	—		
	Input data hold time		t_{PRH}	30	—	30	—		
FRT	Timer output delay time		t_{FTOD}	—	50	—	50	ns	Figure 20.41
	Timer input setup time		t_{FTIS}	30	—	30	—		
	Timer clock input setup time		t_{FTCS}	30	—	30	—		Figure 20.42
	Timer clock pulse width	Single edge	t_{FTCWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{FTCWL}	2.5	—	2.5	—		
TMR	Timer output delay time		t_{TMOD}	—	50	—	50	ns	Figure 20.43
	Timer reset input setup time		t_{TMRS}	30	—	30	—		Figure 20.45
	Timer clock input setup time		t_{TMCS}	30	—	30	—		Figure 20.44
	Timer clock pulse width	Single edge	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TMCWL}	2.5	—	2.5	—		
PWMX	Pulse output delay time		t_{PWOD}	—	50	—	50	ns	Figure 20.46

Item			Symbol	Condition B 16 MHz Min.	Condition B 16 MHz Max.	Condition A 20 MHz Min.	Condition A 20 MHz Max.	Unit	Test Conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 20.47
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock falling time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time (synchronous)		t_{TXD}	—	50	—	50	ns	Figure 20.48
	Receive data setup time (synchronous)		t_{RXS}	50	—	50	—		
	Receive data hold time (synchronous)		t_{RXH}	50	—	50	—		
A/D converter	Trigger input setup time		t_{TRGS}	30	—	30	—	ns	Figure 20.49

Note: * Only on-chip peripheral modules that can be used in subclock operation

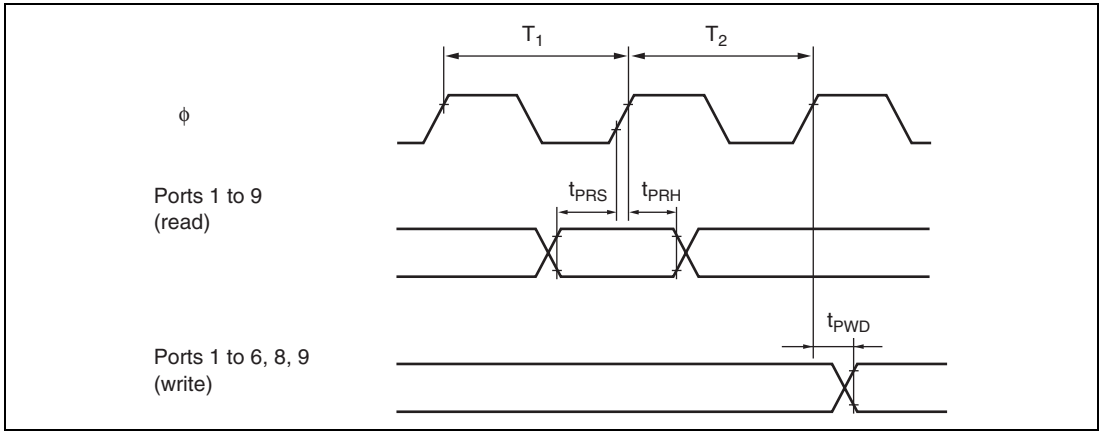


Figure 20.40 I/O Port Input/Output Timing

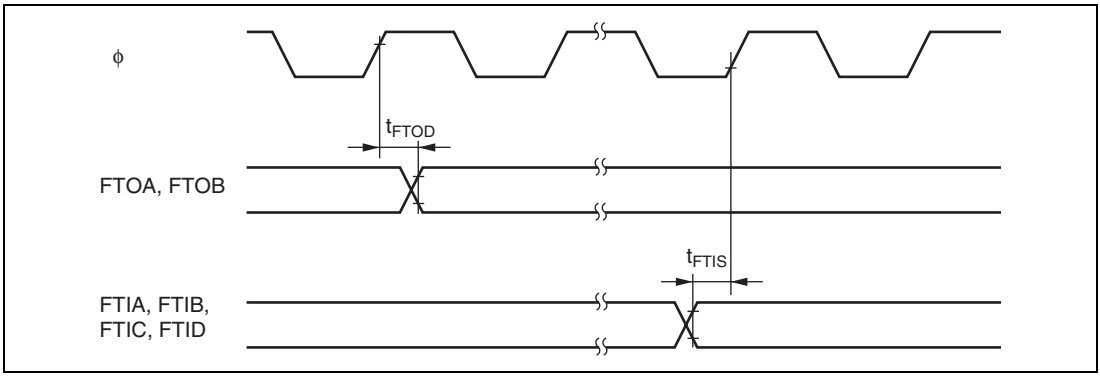


Figure 20.41 FRT Input/Output Timing

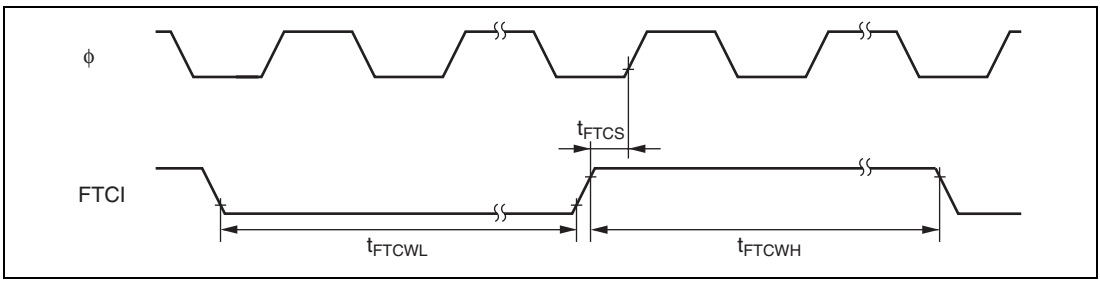


Figure 20.42 FRT Clock Input Timing

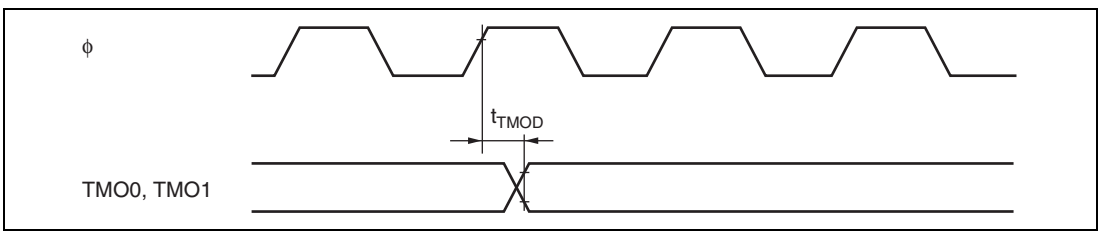


Figure 20.43 8-Bit Timer Output Timing

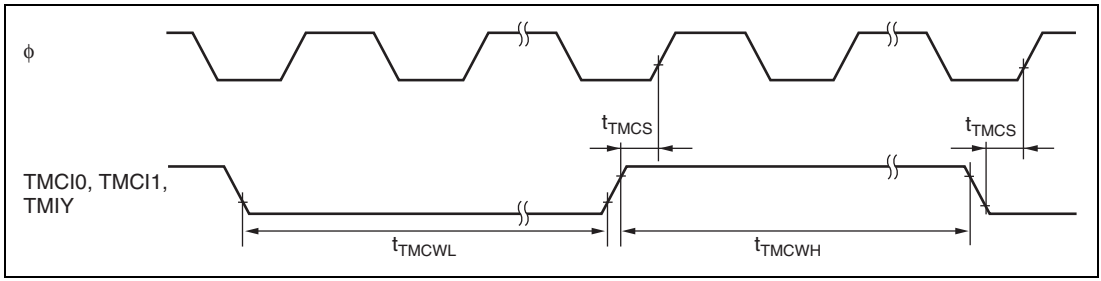


Figure 20.44 8-Bit Timer Clock Input Timing

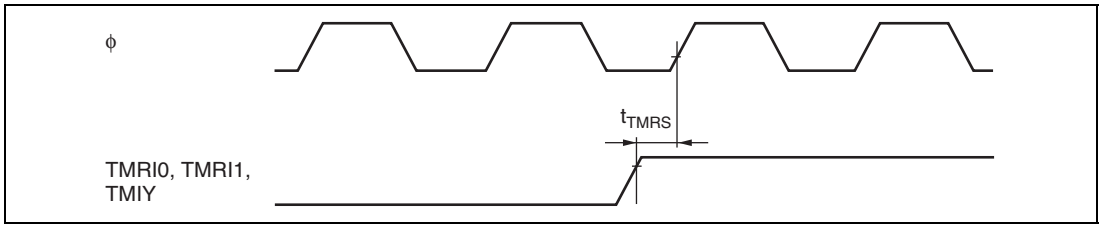


Figure 20.45 8-Bit Timer Reset Input Timing

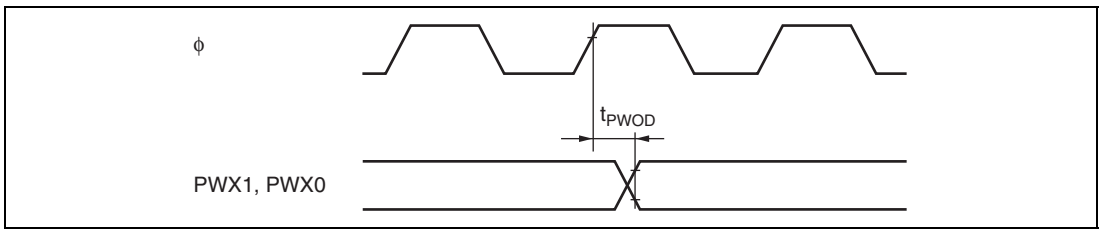


Figure 20.46 PWMX Output Timing

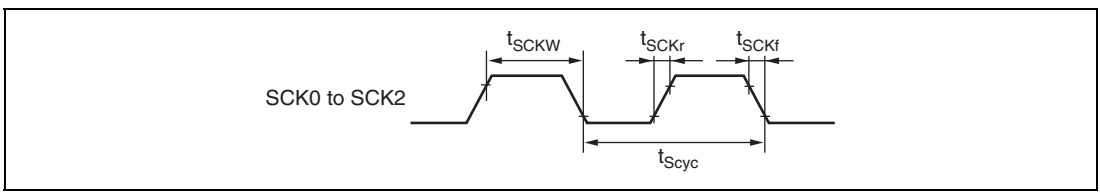


Figure 20.47 SCK Clock Input Timing

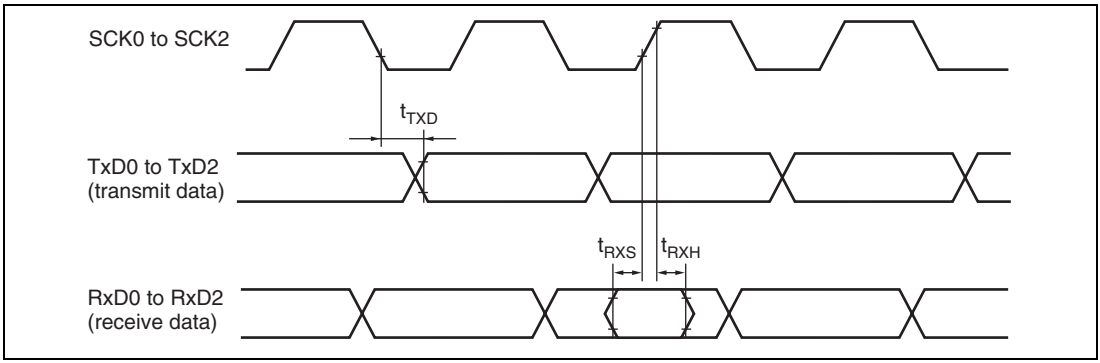


Figure 20.48 SCI Input/Output Timing (Synchronous Mode)

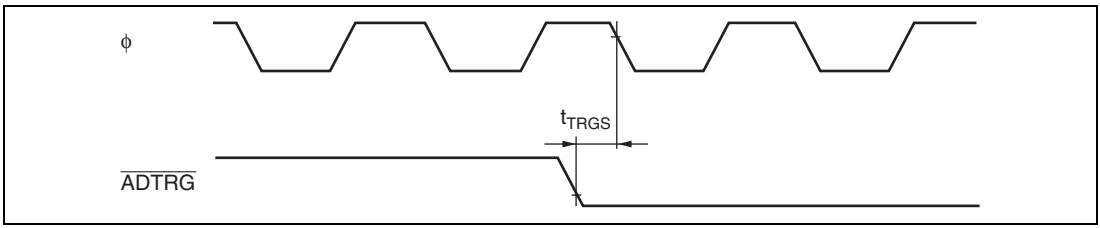


Figure 20.49 A/D Converter External Trigger Input Timing

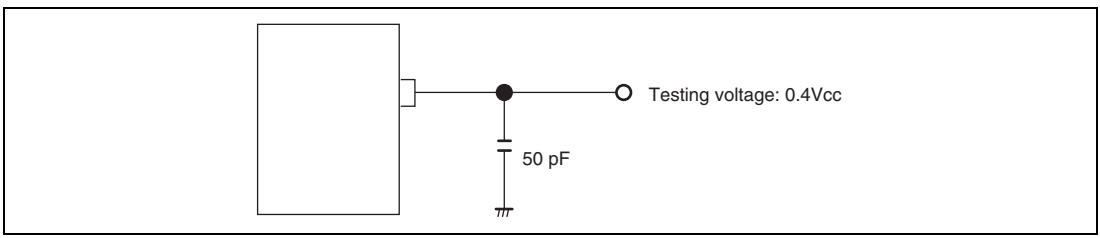


Figure 20.50 Tester Measurement Condition

20.2.4 A/D Conversion Characteristics

Tables 20.20 and 20.21 list the A/D conversion characteristics.

Table 20.20 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

	Condition B			Condition A			
	16 MHz			20 MHz			
Item	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Resolution		10			10		bits
Conversion time*[3]	—	—	8.4	—	—	6.7	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*[1]	—	—	10*[1]	kΩ
			5*[2]			5*[2]	
Nonlinearity error	—	—	±3.0	—	—	±3.0	LSB
Offset error	—	—	±3.5	—	—	±3.5	LSB
Full-scale error	—	—	±3.5	—	—	±3.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	—	—	±4.0	LSB

Notes: 1. When conversion time ≥ 11.17 µs (ϕ ≤ 12 MHz with CKS = 1 or CKS = 0)
2. When conversion time < 11.17 µs (ϕ > 12 MHz with CKS = 1)
3. When this LSI operates on the maximum operating frequency in single-chip mode

Table 20.21 A/D Conversion Characteristics
(CIN7 to CIN0 Input: 134/266-State Conversion)

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

	Condition B			Condition A			
	16 MHz			20 MHz			
Item	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Resolution		10			10		bits
Conversion time*[3]	—	—	8.4	—	—	6.7	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*[1]	—	—	10*[1]	kΩ
			5*[2]			5*[2]	
Nonlinearity error	—	—	±5.0	—	—	±5.0	LSB
Offset error	—	—	±5.5	—	—	±5.5	LSB
Full-scale error	—	—	±5.5	—	—	±5.5	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±6.0	—	—	±6.0	LSB

Notes: 1. When conversion time ≥ 11.17 µs (ϕ ≤ 12 MHz with CKS = 1 or CKS = 0)
2. When conversion time < 11.17 µs (ϕ > 12 MHz with CKS = 1)
3. When this LSI operates on the maximum operating frequency in single-chip mode

20.2.5 D/A Conversion Characteristics

Table 20.22 lists the D/A conversion characteristics.

Table 20.22 D/A Conversion Characteristics

Condition A: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

Condition B: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V,
ϕ = 2 MHz to maximum operating frequency,
T_a = –20 to +75°C (General specifications), T_a = –40 to +85°C (Wide temperature range specifications)

		Condition B			Condition A			
		16 MHz			20 MHz			
Item		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Resolution			8			8		bits
Conversion time	With 20 pF load capacitance	—	—	10	—	—	10	µs
Absolute accuracy	With 2 MΩ load resistance	—	±1.0	±1.5	—	±1.0	±1.5	LSB
	With 4 MΩ load resistance	—	—	±1.0	—	—	±1.0	

20.2.6 Flash Memory Characteristics

Table 20.23 shows the flash memory characteristics.

Table 20.23 Flash Memory Characteristics (Programming/Erasure)

Conditions: V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0 V, Ta = –20 to +75°C (General specifications),
Ta = –40 to +85°C (Wide temperature range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Programming time*[1]*[2]*[4]		t_P	—	10	200	ms/ 128 bytes	
Erasure time*[1]*[3]*[6]		t_E	—	100	1200	ms/ block	
Reprogramming count		N_{WEC}	—	—	100	times	
Programming	Wait time after setting SWE bit*[1]	x	1	—	—	µs	
	Wait time after setting PSU bit*[1]	y	50	—	—	µs	
	Wait time after setting P bit*[1]*[4]	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional write
	Wait time after clearing P bit *[1]	α	5	—	—	µs	
	Wait time after clearing PSU bit *[1]	β	5	—	—	µs	
	Wait time after setting PV bit *[1]	γ	4	—	—	µs	
	Wait time after dummy write*[1]	ε	2	—	—	µs	
	Wait time after clearing PV bit *[1]	η	2	—	—	µs	
	Wait time after clearing SWE bit *[1]	θ	100	—	—	µs	
	Maximum programming count*[1]*[4]*[5]	N	—	—	1000	times	

	Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Erasure	Wait time after setting SWE bit*[1]	x	1	—	—	µs	
	Wait time after setting ESU bit*[1]	y	100	—	—	µs	
	Wait time after setting E bit*[1]*[6]	z	10	—	100	ms	
	Wait time after clearing E bit*[1]	α	10	—	—	µs	
	Wait time after clearing ESU bit*[1]	β	10	—	—	µs	
	Wait time after setting EV bit*[1]	γ	20	—	—	µs	
	Wait time after dummy-writing H'FF*[1]	ε	2	—	—	µs	
	Wait time after clearing EV bit*[1]	η	4	—	—	µs	
	Wait time after clearing SWE bit*[1]	θ	100	—	—	µs	
	Maximum erasure count*[1]*[6]*[7]	N	—	—	120	times	

Notes:
1. Set the times according to the programming/erasing algorithms.
2. Programming time per 128 bytes (Shows the total period for which the P bit in FLMCR1 is set. It does not include the programming-verifying time.)
3. Block erasing time (Shows the total period for which the E bit in FLMCR1 is set. It does not include the erasing-verifying time.)
4. Maximum programming time (t_P (max.))
   t_P (max.) = (wait time after setting P bit (z1) + (z3)) $\times$ 6
   + wait time after setting P bit (z2) $\times$ ((N) – 6)
5. The maximum programming court (N) should be set according to the actual set value of z1, z2 and z3 to allow programming within the maximum programming time (t_P (max.)).
   The wait time after setting the P bit (z1, z2, and z3) should be alternated according to the programming count (n) as follows:
   $1 \leq n \leq 6$ z1 = 30µs, z3 = 10µs
   $7 \leq n \leq 1000$ z2 = 200µs
6. Maximum erasure time (t_E (max.))
   t_E (max.) = Wait time after setting E bit (z) $\times$ maximum erasure count (N)
7. The maximum erasure count (N) should be set according to the actual set value of z to allow erasing within the maximum erasure time (t_E (max.)).

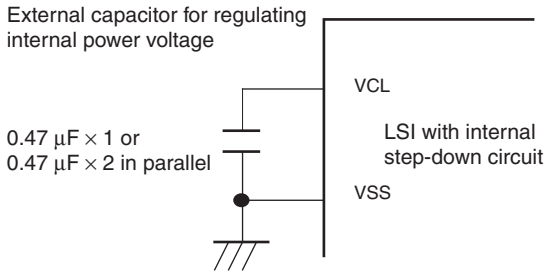
20.2.7 Usage Note

- LSI with Internal Step-Down Circuit

  This LSI includes an internal step-down circuit which automatically step down the internal power voltage to an appropriate level.

  A capacitor or capacitors for regulating the internal power voltage (one 0.47-µF capacitor or two 0.47-µF capacitors in parallel) must be placed between the internal step-down and VSS pins.

  For connection of the capacitor, see figure 20.51.



Do not connect the VCL pin of an LSI with the internal step-down circuit to the Vcc power. A capacitor or capacitors for regulating the internal power voltage must be connected to the VCL pin. The Capacitor should be a laminated ceramic type (0.47 µF × 1 or 0.47 µF × 2 in parallel) and placed close to the pins.

Figure 20.51 Connection of VCL Capacitor

Appendix A I/O Port States in Each Processing State

Table A.1 I/O Port States in Each Processing State

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Sleep Mode	Sub-sleep Mode	Subactive Mode	Program Execution State
Port 1 A7 to A0	1	L	T	kept*[1]	kept*[1]	kept*[1]	kept*[1]	A7 to A0	A7 to A0
	2, 3 (EXPE = 1)	T						Address output/ input port	Address output/ input port
	2, 3 (EXPE = 0)							I/O port	I/O port
Port 2 A15 to A8	1	L	T	kept*[1]	kept*[1]	kept*[1]	kept*[1]	A15 to A8	A15 to A8
	2, 3 (EXPE = 1)	T						Address output/ input port	Address output/ input port
	2, 3 (EXPE = 0)							I/O port	I/O port
Port 3 D15 to D8*[3]	1	T	T	T	T	T	T	D15 to D8*[3]	D15 to D8*[3]
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port
Port 4	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 5	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 6	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 7	1	T	T	T	T	T	T	Input port	Input port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 8	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 97 $\overline{\text{WAIT}}$	1	T	T	T/kept	T/kept	T/kept	T/kept	$\overline{\text{WAIT}}$/ I/O port	$\overline{\text{WAIT}}$/ I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port

Port Name Pin Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Sleep Mode	Sub-sleep Mode	Subactive Mode	Program Execution State
Port 96 ϕ EXCL	1	Clock output	T	[DDR = 1] H [DDR = 0] T	EXCL input	[DDR = 1] clock output [DDR = 0] T	EXCL input	EXCL input	Clock output/ EXCL input/ input port
	2, 3 (EXPE = 1)	T							
	2, 3 (EXPE = 0)								
Ports 95 to 93 $\overline{AS}$, $\overline{HWR}$*4, $\overline{RD}$	1	H	T	H	H	H	H	$\overline{AS}$, $\overline{HWR}$*4, $\overline{RD}$	$\overline{AS}$, $\overline{HWR}$*4, $\overline{RD}$
	2, 3 (EXPE = 1)	T							
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port
Ports 92 to 91	1	T	T	kept	kept	kept	kept	I/O port	I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)								
Port 90 $\overline{LWR}$*2	1	T	T	H/kept	H/kept	H/kept	H/kept	$\overline{LWR}$/ I/O port	$\overline{LWR}$/ I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port
Port A*2 A23 to A16	1	T	T	kept*1	kept*1	kept*1	kept*1	I/O port	I/O port
	2, 3 (EXPE = 1)							A23 to A16/ I/O port	A23 to A16/ I/O port
	2, 3 (EXPE = 0)							I/O port	I/O port
Port B*2 D7 to D0	1	T	T	T/kept	T/kept	T/kept	T/kept	D7 to D0/ I/O port	D7 to D0/ I/O port
	2, 3 (EXPE = 1)								
	2, 3 (EXPE = 0)			kept	kept	kept	kept	I/O port	I/O port

[Legend]

H: High

L: Low

T: High-impedance state

kept: Input ports are in the high-impedance state (when DDR = 0 and PCR = 1, input pull-up MOSs remain on).

Output ports maintain their previous state.

Depending on the pins, the on-chip peripheral modules may be initialized and the I/O port function determined by DDR and DR used.

DDR: Data direction register

Notes: 1. When the address output is selected, the previous address accessed is retained.

2. This signal is for the H8S/2144B and is not available for the H8S/2134B.

3. These signal names are for the H8S/2144B. D7 to D0 are used for the H8S/2134B.

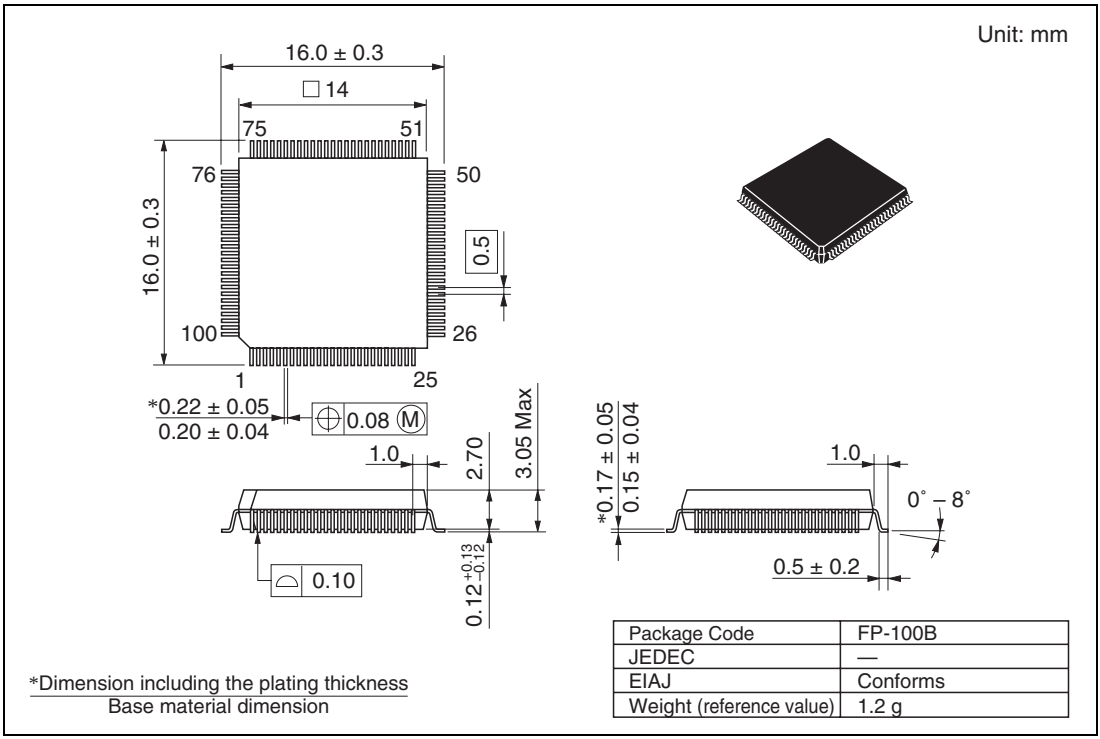
4. This signal name is for the H8S/2144B. $\overline{WR}$ is used for the H8S/2134B.

Appendix B Product Codes

Product Type		Product Code	Mark Code	Package (Code)
H8S/2144B	Flash memory version	HD64F2144B	F2144BFA20	100-pin QFP (FP-100B)
			F2144BTE20	100-pin TQFP (TFP-100B)
H8S/2134B	Flash memory version	HD64F2134B	F2134BFA20	80-pin QFP (FP-80B)
			F2134BTE20	80-pin TQFP (TFP-80B)

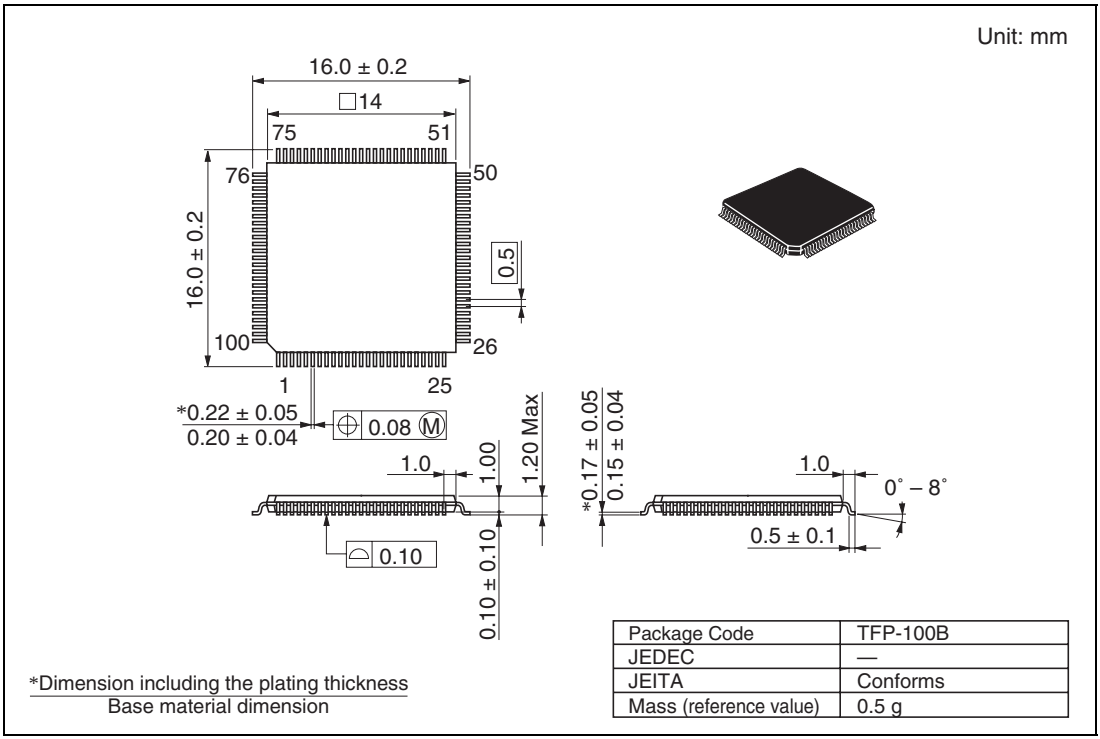
Note: * Some products above are in the developing or planning stage. Please contact Renesas agency to conform the present status of each product.

Appendix C Package Dimensions



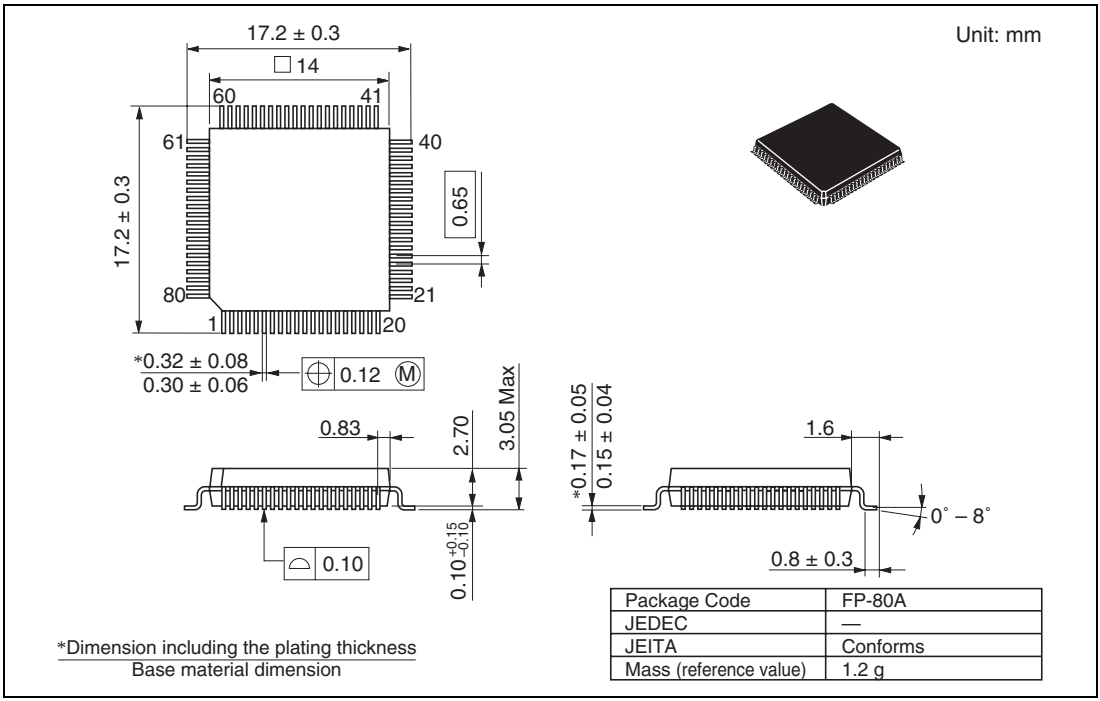
Package Code	FP-100B
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.2 g

Figure C.1 Package Dimensions (FP-100B)



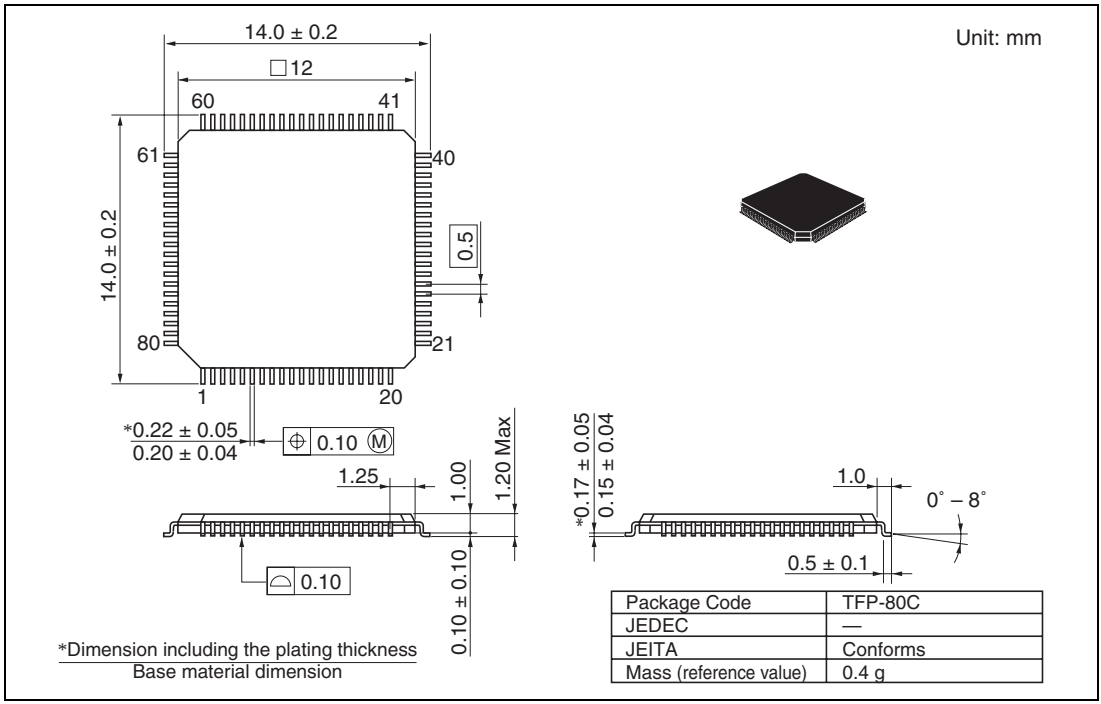
Package Code	TFP-100B
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.5 g

Figure C.2 Package Dimensions (TFP-100B)



Package Code	FP-80A
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.2 g

Figure C.3 Package Dimensions (FP-80A)



Package Code	TFP-80C
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.4 g

Figure C.4 Package Dimensions (TFP-80C)

Index

S

T

U

W

Renesas 16-Bit Single-Chip Microcomputer
Hardware Manual
H8S/2144B, H8S/2134B

Publication Date:	Rev.1.00, Jun. 24, 2005
Published by:	Sales Strategic Planning Div. Renesas Technology Corp.
Edited by:	Technical Documentation & Information Department Renesas Kodaira Semiconductor Co., Ltd.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

H8S/2144B, H8S/2134B
Hardware Manual

Renesas Technology Corp.
2-6-2, Ote-machi, Chiyoda-ku, Tokyo, 100-0004, Japan