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# **HD74HC164**

## 8-bit Parallel-out Shift Register

REJ03D0580-0400 Rev.4.00 Mar 25, 2009

### **Description**

This 8-bit shift register has gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on the input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input.

#### **Features**

• High Speed Operation:  $t_{pd}$  (Clock to Q) = 14.5 ns typ ( $C_L = 50$  pF)

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage:  $V_{CC} = 2$  to 6 V

• Low Input Current: 1 μA max

• Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	
HD74HC164P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	Р	_	
HD74HC164FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)	
HD74HC164RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)	

Note: Please consult the sales office for the above package availability.

### **Function Table**

	Inp	uts		Outputs				
Clear	Clock	Α	В	$Q_A$	Q <sub>B</sub>		Q <sub>H</sub>	
L	Х	X	Х	L	L		L	
Н		X	Х	$Q_Ao$	Q <sub>Bo</sub>		$Q_{Ho}$	
Н		L	Х	L	$Q_{An}$		$Q_{Gn}$	
Н		Х	L	L	$Q_{An}$		$Q_{Gn}$	
Н	$\int$	Н	Н	Н	$Q_{An}$		$Q_{Gn}$	

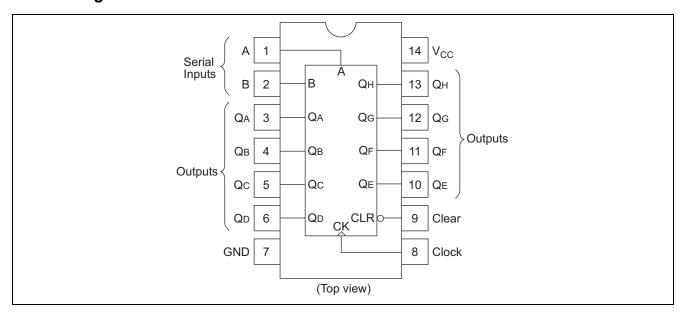
 $Q_{Ao}$  to  $Q_{Ho}$  = Outputs remain unchanged.

 $Q_{An}$  to  $Q_{Gn}$  = Data shifted from the previous stage on a positive edge at the clock input.

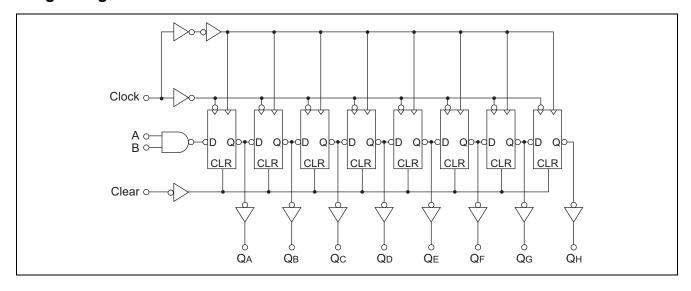
H: High levelL: Low levelX: Irrelevant



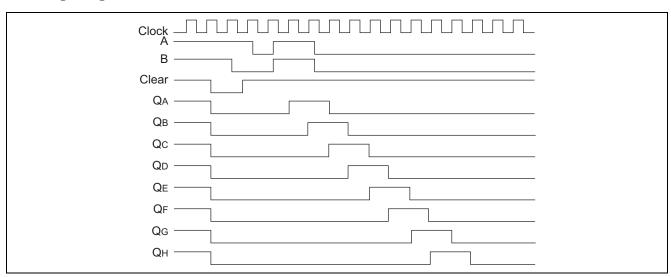
## **Pin Arrangement**



## **Logic Diagram**



## **Timing Diagram**



## **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
Input / Output voltage	Vin, Vout	-0.5 to V <sub>CC</sub> +0.5	V
Input / Output diode current	I <sub>IK</sub> , I <sub>OK</sub>	±20	mA
Output current	I <sub>0</sub>	±25	mA
V <sub>CC</sub> , GND current	I <sub>CC</sub> or I <sub>GND</sub>	±50	mA
Power dissipation	P <sub>T</sub>	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## **Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to V <sub>CC</sub>	V	
Operating temperature	Та	-40 to 85	°C	
		0 to 1000		V <sub>CC</sub> = 2.0 V
Input rise / fall time*1	t <sub>r</sub> , t <sub>f</sub>	0 to 500	ns	V <sub>CC</sub> = 4.5 V
		0 to 400		$V_{CC} = 6.0 \text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

### **Electrical Characteristics**

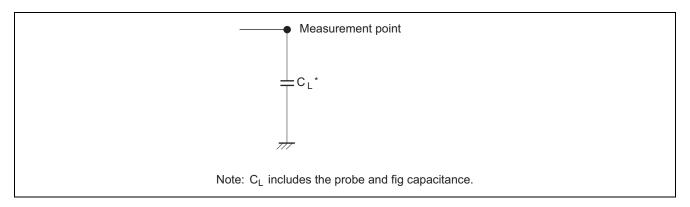
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C		$Ta = -40 \text{ to} + 85^{\circ}\text{C}$		Unit	Test Conditions		
			Min	Тур	Max	Min	Max	5	rest Conditions	
		2.0	1.5	_	_	1.5	_			
	$V_{IH}$	4.5	3.15		_	3.15	_	V		
Input voltage		6.0	4.2	1	_	4.2	_			
input voltage		2.0			0.5		0.5			
	V <sub>IL</sub>	4.5			1.35	_	1.35	V		
		6.0			1.8	_	1.8			
		2.0	1.9	2.0	_	1.9	_			
	V <sub>OH</sub>	4.5	4.4	4.5	_	4.4	_	٧		$I_{OH} = -20 \mu A$
		6.0	5.9	6.0	_	5.9	_		$Vin = V_{IH} \text{ or } V_{IL}$	
		4.5	4.18		_	4.13	_			$I_{OH} = -4 \text{ mA}$
Output voltage		6.0	5.68	_	_	5.63	_			$I_{OH} = -5.2 \text{ mA}$
Output voltage	V <sub>OL</sub>	2.0	-	0.0	0.1	_	0.1		$Vin = V_{IH} \text{ or } V_{IL}$	
		4.5	_	0.0	0.1		0.1			$I_{OL} = 20 \mu A$
		6.0	-	0.0	0.1	_	0.1	V		
		4.5			0.26	_	0.33			$I_{OL} = 4 \text{ mA}$
		6.0		1	0.26	_	0.33			$I_{OL} = 5.2 \text{ mA}$
Input current	lin	6.0	_	_	±0.1	_	±1.0	μΑ	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	Icc	6.0	_	_	4.0	_	40	μΑ	Vin = V <sub>CC</sub> or GN	D, lout = $0 \mu A$

## **Switching Characteristics**

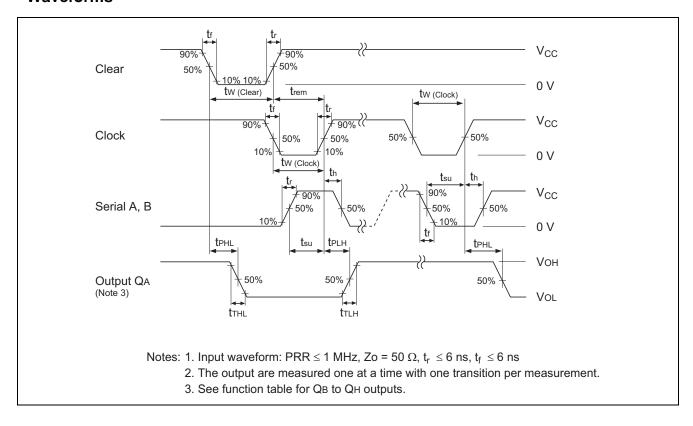
 $(C_L = 50 \text{ pF}, \text{Input } t_r = t_f = 6 \text{ ns})$ 

11	Symbol	V <sub>CC</sub> (V)	Ta = 25°C		$Ta = -40 \text{ to } +85^{\circ}\text{C}$		11!1	Test Conditions		
Item			Min	Тур	Max	Min	Max	Unit	rest Conditions	
		2.0	_	_	5	_	4			
Maximum clock frequency	f <sub>max</sub>	4.5	_	_	25	_	20	MHz		
rrequericy		6.0	_	_	29	_	24			
		2.0	_	_	160	_	200			
	t <sub>PHL</sub>	4.5	_	14	32	_	40	ns		
		6.0	_	_	27	_	34		Clock to O	
Dana and in a dalam		2.0	_	_	160	_	200		Clock to Q	
Propagation delay time	t <sub>PLH</sub>	4.5	_	15	32	_	40	ns		
une		6.0	_	_	27	_	34			
		2.0	_	_	175	_	220			
	t <sub>PHL</sub>	4.5	_	17	35	_	44	ns	Clear to Q	
		6.0	_	_	30	_	37			
	t <sub>su</sub>	2.0	100	_	_	125	_		A, B to Clock	
Setup time		4.5	20	1	_	25	_	ns		
		6.0	17	_	_	21	_			
	t <sub>h</sub>	2.0	5	_	_	5	_	ns	Clock to A, B	
Hold time		4.5	5	0	_	5	_			
		6.0	5	_	_	5	_			
		2.0	5	_	_	5	_			
Removal time	t <sub>rem</sub>	4.5	5	0	_	5	_	ns	Clear to Clock	
		6.0	5	_	_	5	_			
		2.0	80	_	_	100	_			
		4.5	16	8	_	20	_	ns	Clock	
Pulse width	4	6.0	14	_	_	17	_			
Puise width	t <sub>w</sub>	2.0	80	_	_	100	_			
		4.5	16	5	_	20	_	ns	Clear	
		6.0	14	_	_	17	_			
Output rice/fell		2.0	_	_	75	_	95			
Output rise/fall time	$t_{TLH}, t_{THL}$	4.5	_	5	15	_	19	ns		
ume		6.0	_	_	13	_	16			
Input capacitance	Cin			5	10		10	pF		

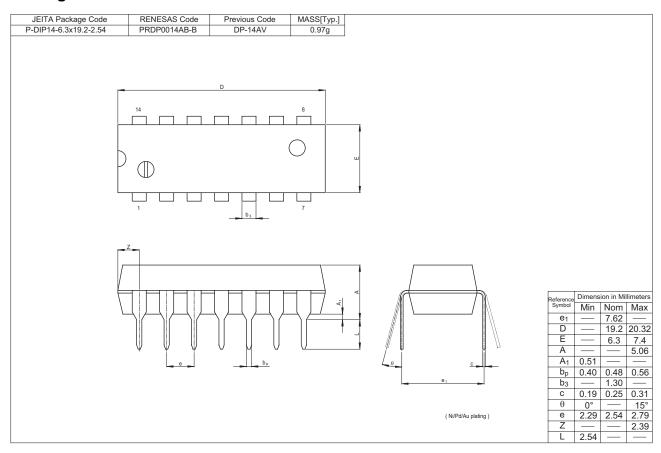
### **Test Circuit**

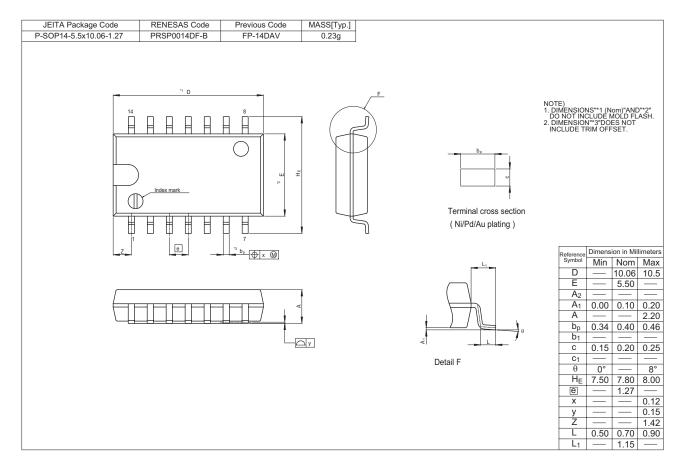


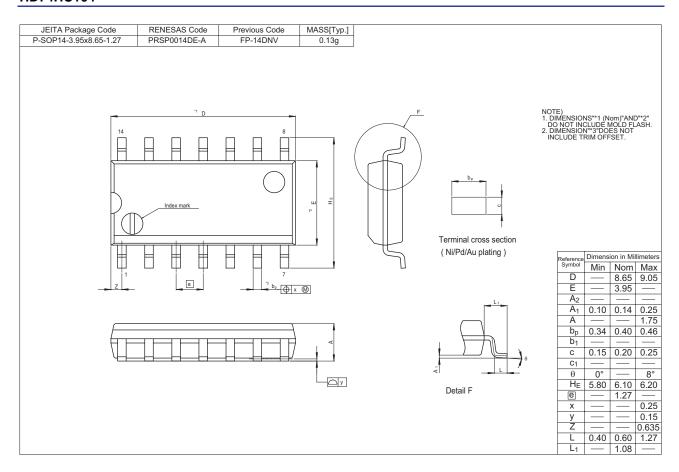
### **Waveforms**



### **Package Dimensions**







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