

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HD74LV393A

Dual 4-bit Binary Counters

REJ03D0333-0300Z
(Previous ADE-205-276A (Z))
Rev.3.00
Jun. 28, 2004

Description

The HD74LV393A contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

The HD74LV393A is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter is set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 6\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV393AFPEL	SOP-14 pin(JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74LV393ARPEL	SOP-14 pin(JEDEC)	FP-14DNV	RP	EL (2,500 pcs/reel)
HD74LV393ATELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

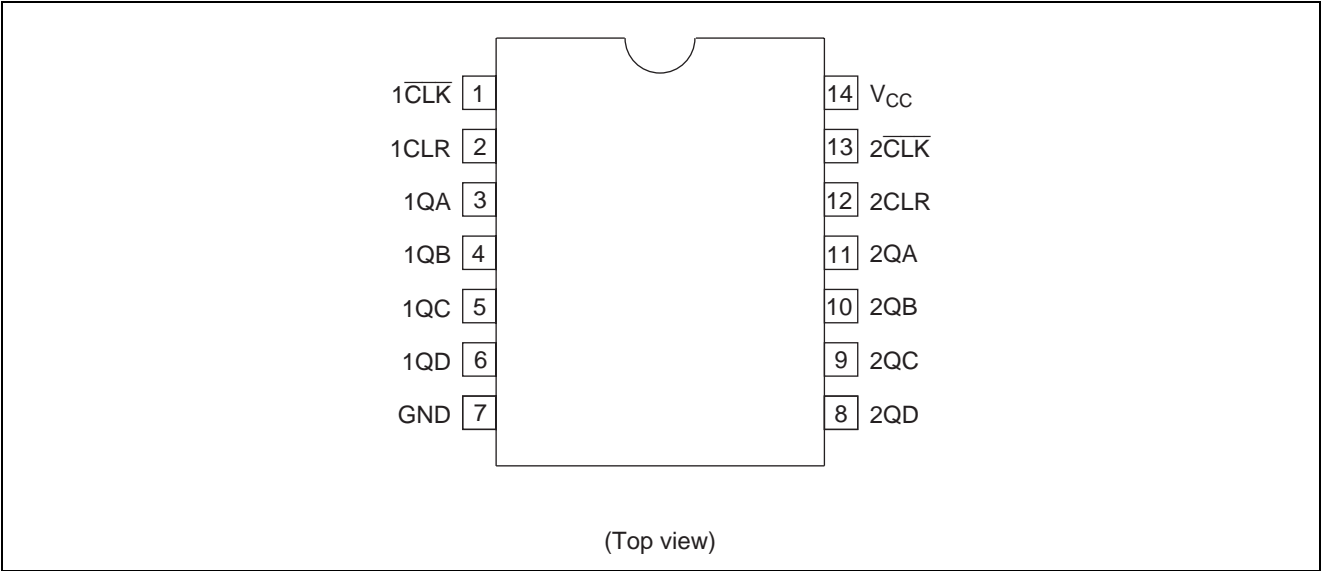
Note: Please consult the sales office for the above package availability.

Function Table

Inputs		Output
CLK	CLR	
X	H	L
H	L	No change
L	L	No change
↑	L	No change
↓	L	Count up

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785 500	mW	SOP TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

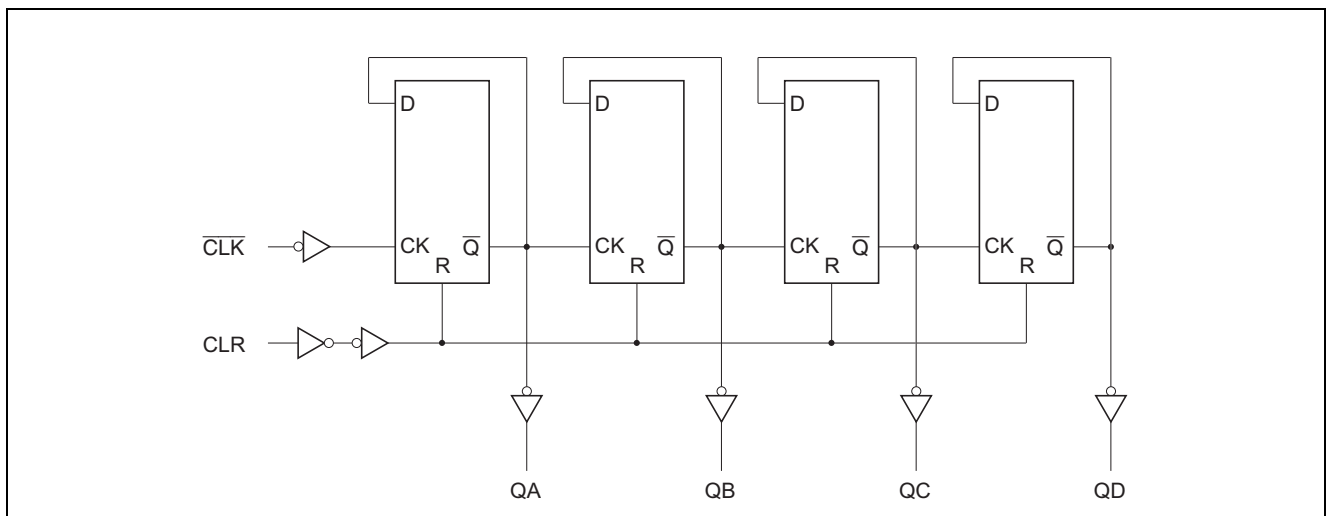
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

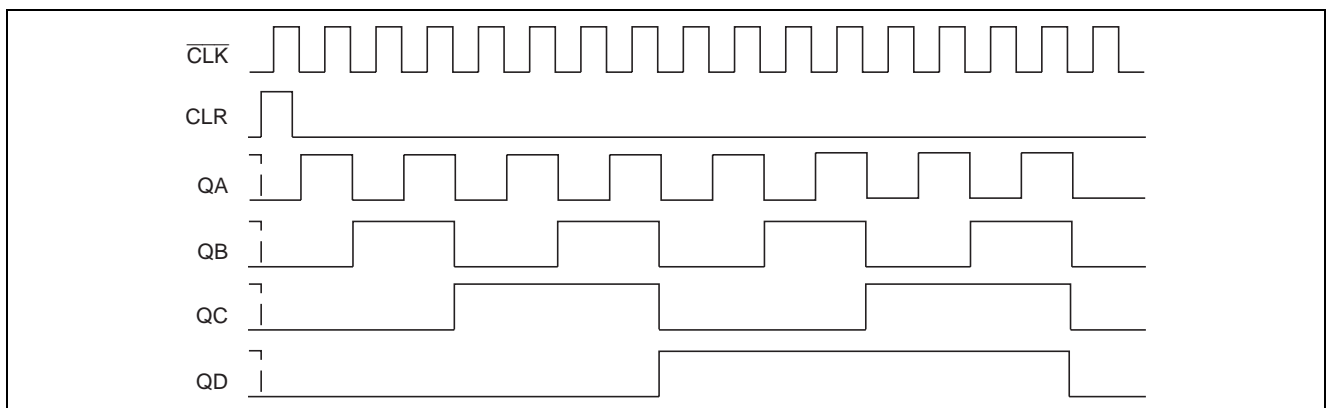
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0\text{ V}$
		—	-2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	-6		$V_{CC} = 3.0$ to 3.6 V
		—	-12		$V_{CC} = 4.5$ to 5.5 V
	I_{OL}	—	50	μA	$V_{CC} = 2.0\text{ V}$
		—	2	mA	$V_{CC} = 2.3$ to 2.7 V
		—	6		$V_{CC} = 3.0$ to 3.6 V
		—	12		$V_{CC} = 4.5$ to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3$ to 2.7 V
		0	100		$V_{CC} = 3.0$ to 3.6 V
		0	20		$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	V _{CC} × 0.7	—	—		
		3.0 to 3.6	V _{CC} × 0.7	—	—		
		4.5 to 5.5	V _{CC} × 0.7	—	—		
	V _{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V _{CC} × 0.3		
		3.0 to 3.6	—	—	V _{CC} × 0.3		
		4.5 to 5.5	—	—	V _{CC} × 0.3		
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 μA
		2.3	2.0	—	—		I _{OH} = -2 mA
		3.0	2.48	—	—		I _{OH} = -6 mA
		4.5	3.8	—	—		I _{OH} = -12 mA
	V _{OL}	Min to Max	—	—	0.1	V	I _{OL} = 50 μA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 6 mA
		4.5	—	—	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	μA	V _{IN} = 5.5 V or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 V to 5.5 V
Input capacitance	C _{IN}	3.3	—	1.7	—	pF	V _I = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	50	90	—	40	—	MHz	C _L = 15 pF		
		30	60	—	25	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	11.8	17.7	1.0	20.5	ns	C _L = 15 pF	CLK	Q _A
		—	15.1	21.3	1.0	24.5		C _L = 50 pF		
		—	13.4	20.3	1.0	23.5		C _L = 15 pF		Q _B
		—	16.7	23.9	1.0	27.5		C _L = 50 pF		
		—	14.9	22.5	1.0	26.0		C _L = 15 pF		Q _C
		—	18.2	26.1	1.0	30.0		C _L = 50 pF		
		—	16.2	24.2	1.0	28.0		C _L = 15 pF		Q _D
		—	19.5	27.8	1.0	32.0		C _L = 50 pF		
	t _{PHL}	—	10.8	14.8	1.0	17.0		C _L = 15 pF	CLR	Q _n
		—	14.2	17.4	1.0	20.0		C _L = 50 pF		
Setup time	t _{su}	6.0	—	—	6.0	—	ns		CLR L before CLK ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLR H	
		5.0	—	—	5.0	—			CLK H or L	

Switching Characteristics (cont)

 $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	75	120	—	65	—	MHz	C _L = 15 pF		
		45	65	—	35	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	8.6	13.2	1.0	15.5	ns	C _L = 15 pF	CLK	Q _A
		—	11.1	16.7	1.0	19.0		C _L = 50 pF		
		—	10.2	15.8	1.0	18.5		C _L = 15 pF		Q _B
		—	12.7	19.3	1.0	22.0		C _L = 50 pF		
		—	11.7	18.0	1.0	21.0		C _L = 15 pF		Q _C
		—	14.2	21.5	1.0	24.5		C _L = 50 pF		
		—	13.0	19.7	1.0	23.0		C _L = 15 pF		Q _D
		—	15.5	23.2	1.0	26.5		C _L = 50 pF		
	t _{PHL}	—	7.9	12.3	1.0	14.5		C _L = 15 pF	CLR	Q _n
		—	10.4	15.8	1.0	18.0		C _L = 50 pF		
Setup time	t _{su}	5.0	—	—	5.0	—	ns		CLR L before CLK ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLR H	
		5.0	—	—	5.0	—			CLK H or L	

 $V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f _{max}	125	170	—	105	—	MHz	C _L = 15 pF		
		85	115	—	75	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	5.8	8.5	1.0	10.0	ns	C _L = 15 pF	CLK	Q _A
		—	7.3	10.5	1.0	12.0		C _L = 50 pF		
		—	6.8	9.8	1.0	11.5		C _L = 15 pF		Q _B
		—	8.3	11.8	1.0	13.5		C _L = 50 pF		
		—	7.7	11.2	1.0	13.0		C _L = 15 pF		Q _C
		—	9.2	13.2	1.0	15.0		C _L = 50 pF		
		—	8.5	12.5	1.0	14.5		C _L = 15 pF		Q _D
		—	10.0	14.5	1.0	16.5		C _L = 50 pF		
	t _{PHL}	—	5.4	8.1	1.0	9.5		C _L = 15 pF	CLR	Q _n
		—	6.9	10.1	1.0	11.5		C _L = 50 pF		
Setup time	t _{su}	4.0	—	—	4.0	—	ns		CLR L before CLK ↓	
Pulse width	t _w	5.0	—	—	5.0	—	ns		CLR H	
		5.0	—	—	5.0	—			CLK H or L	

Operating Characteristics

C_L = 50 pF

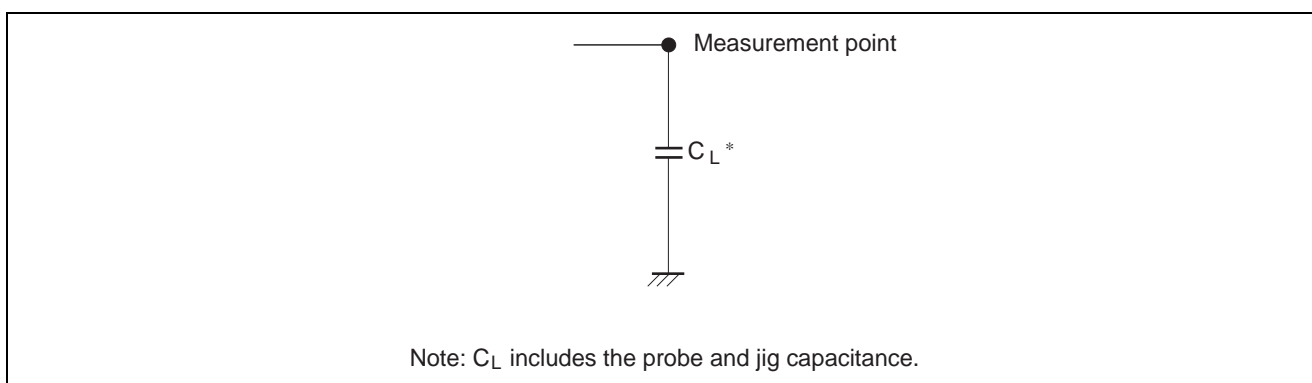
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	—	12.0	—	pF	f = 10 MHz
		5.0	—	15.0	—		

Noise Characteristics

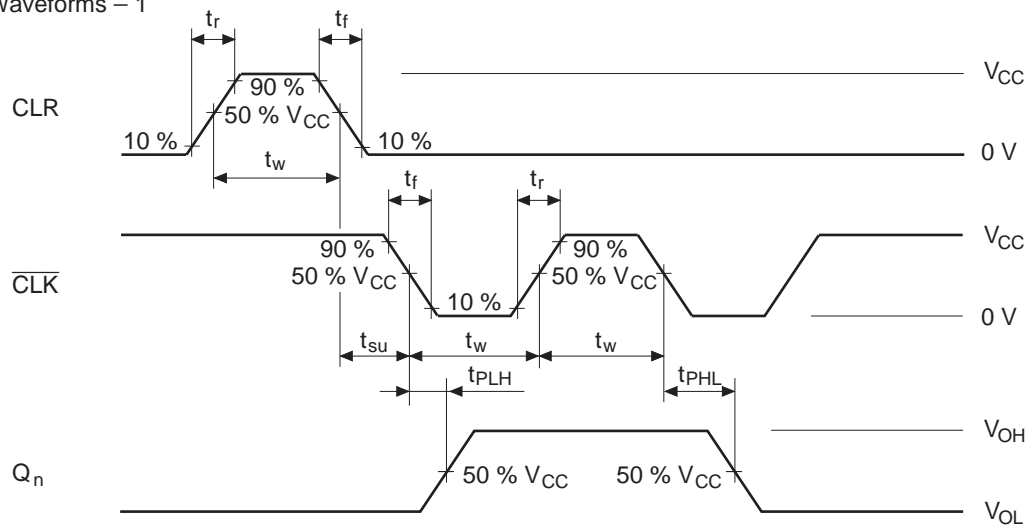
$C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.4	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	−0.4	−0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	3.2	—	V	
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99	V	

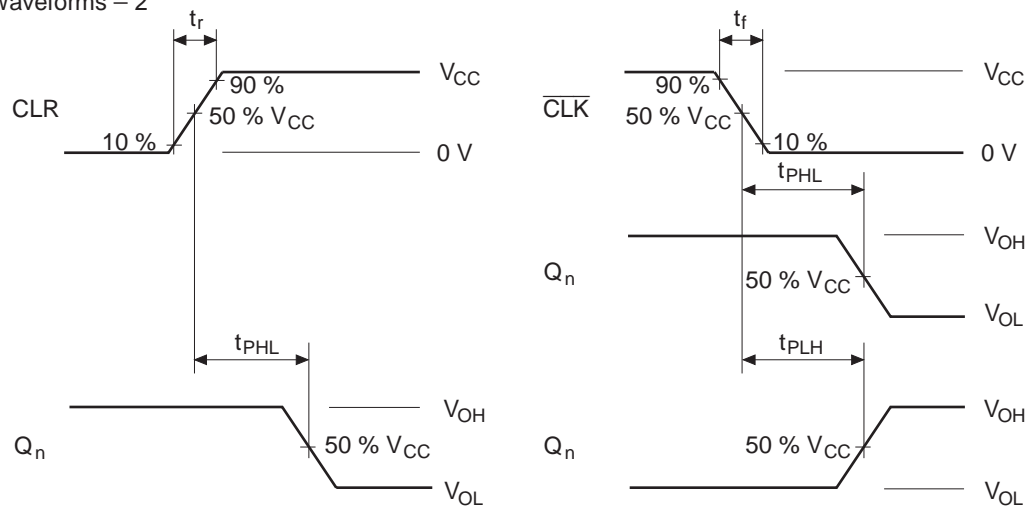
Test Circuit



• Waveforms – 1



• Waveforms – 2

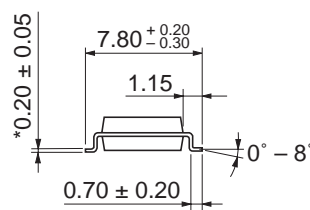
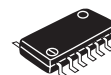
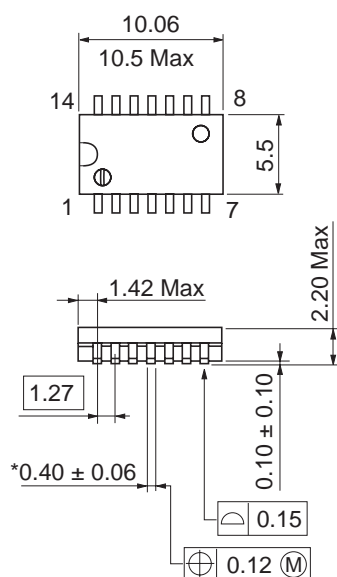


Notes: 1. Input waveform: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of January, 2003

Unit: mm

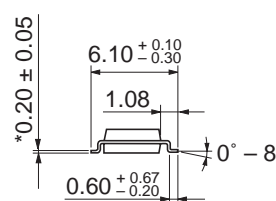
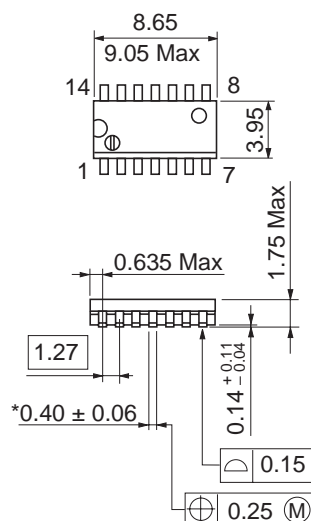


*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003

Unit: mm

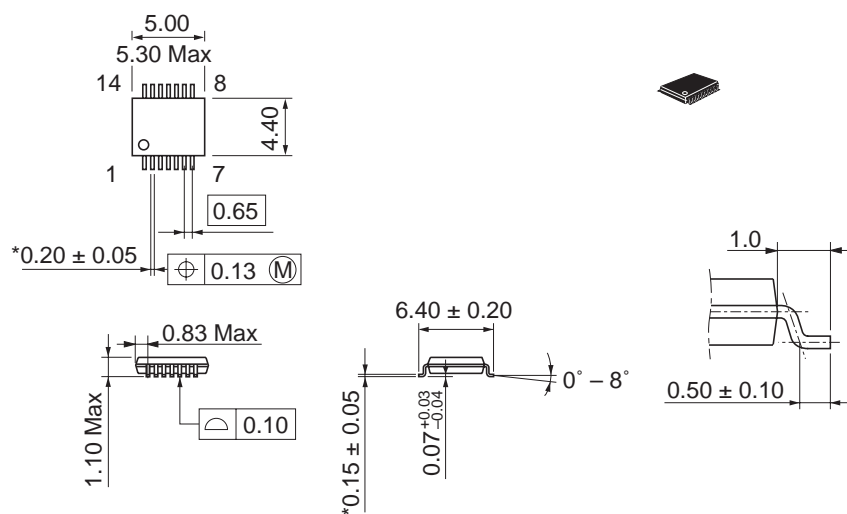


*Ni/Pd/Au plating

Package Code	FP-14DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.13 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

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Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001