General Description

The 810001-22 is a PLL based synchronous clock generator that is optimized for digital video clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation, and to support the complex PLL multiplication ratios needed for video rate conversion.

The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency video output clock.

Preset multiplication ratios are selected from internal lookup tables using device input selection pins. The multiplication ratios are optimized to support common video rates used in professional video system applications. The VCXO requires the use of an external, inexpensive pullable crystal. Two crystal connections are provided (pin selectable) so that both 60 and 59.94Hz base frame rates can be supported. The VCXO requires external passive loop filter components which are used to set the PLL loop bandwidth and damping characteristics.

Features

- Jitter attenuation and frequency translation of video clock signals
- Supports SMTPE 292M, ITU-R Rec. 601/656 and MPEG-transport clocks
- Support of High-Definition (HD) and Standard-Definition (SD) pixel rates
- Dual VCXO-PLL supports both 60 and 59.94Hz base frame rates in one device
- Dual PLL mode for high-frequency clock generation (32.967MHz to 162MHz)
- VCXO-PLL mode for low-frequency clock generation (27MHz and 26.973MHz)
- One LVCMOS/LVTTL PLL clock output
- Two selectable LVCMOS/LVTTL input clocks
- LVCMOS/LVTTL compatible control signals
- RMS phase jitter @148.5MHz, using a 27MHz crystal (12kHz – 20MHz): 1.01ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in a lead-free (RoHS 6) 32-VFQFN package
- **Use replacement part: 8T49N241-dddNLGI**

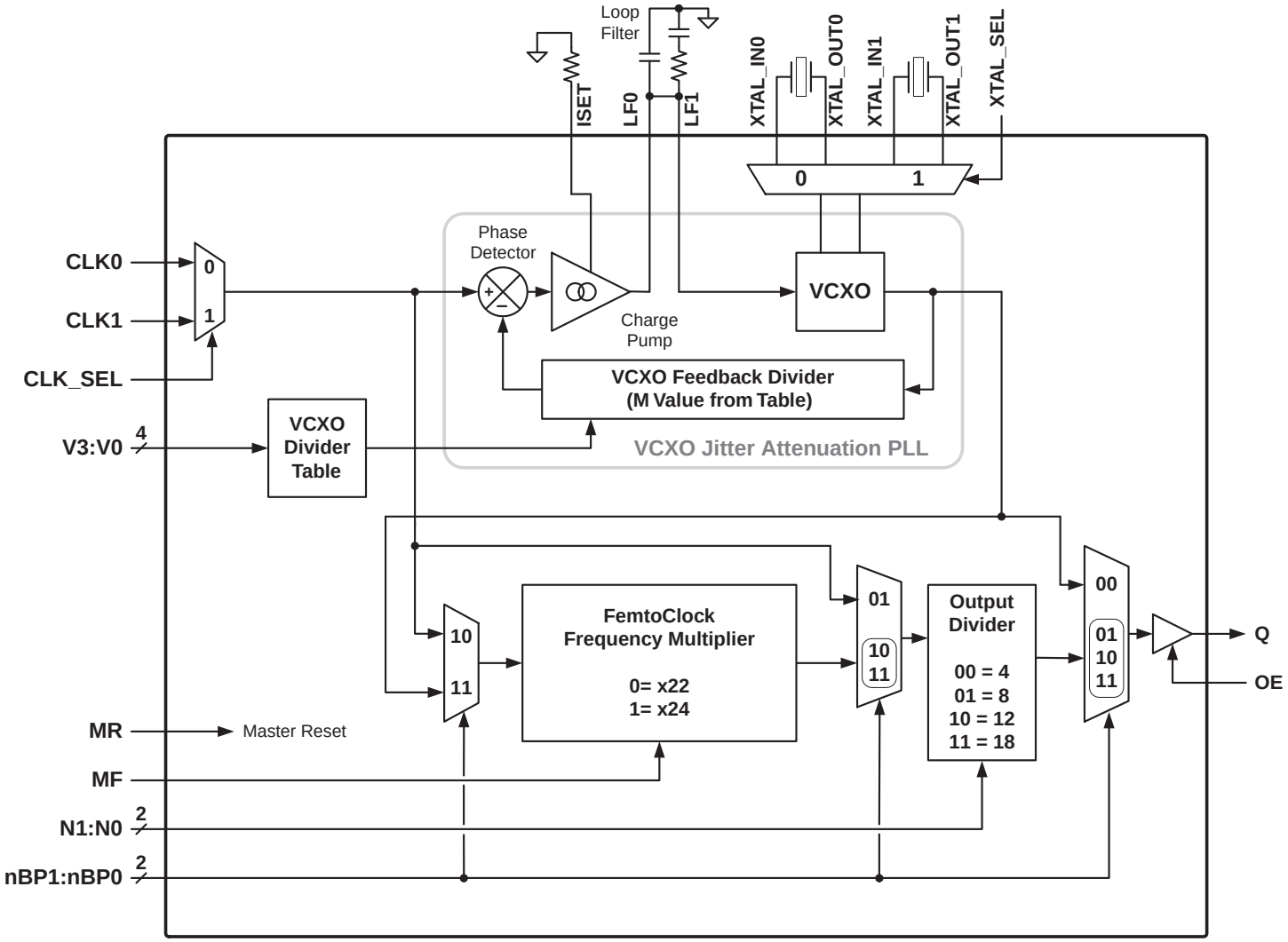
Supported Input Frequencies

f_{VCXO} = 27MHz	f_{VCXO} = 26.973MHz
67.5kHz	67.4326
56.25kHz	56.1938
45.0kHz	44.955
37.5kHz	37.4625
33.75kHz	33.7163
31.4685kHz	31.4371
31.25kHz	31.2188
28.125kHz	28.0969
27.0kHz	26.973
22.5kHz	22.4775
18.75kHz	18.7313
18kHz	17.982
15.7343kHz	15.7185
15.625kHz	15.6094

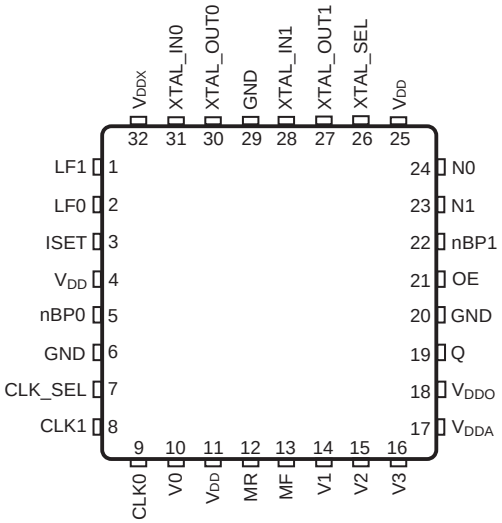
Supported Output Frequencies

f_{VCXO} = 27MHz	f_{VCXO} = 26.973MHz
148.5	148.3516
74.25	74.1758
49.5	49.4505
33	32.967
162	161.8382
81	80.9191
54	53.9461
36	35.9640
27	26.973

Block Diagram



Pin Assignment



810001-22
32 Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 11, 25	V_{DD}	Power		Core supply pins.
5, 22	nBP0, nBP1	Input	Pullup	PLL Bypass control pins. See block diagram.
6, 20, 29	GND	Power		Power supply ground.
7	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
8, 9	CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
10, 14, 15, 16	V0, V1, V2, V3	Input	Pulldown	VCXO PLL divider selection pins. LVCMOS/LVTTL interface levels.
12	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the output to go low. When logic LOW, the internal dividers and the output is enabled. LVCMOS/LVTTL interface levels.
13	MF	Input	Pulldown	FemtoClock multiplication factor select pin. LVCMOS/LVTTL interface levels.
17	V_{DDA}	Power		Analog supply pin.
18	V_{DDO}	Power		Output supply pin.
19	Q	Output		Single-ended VCXO PLL clock output. LVCMOS/LVTTL interface levels.
21	OE	Input	Pullup	Output enable. When logic LOW, the clock output is in high-impedance. When logic HIGH, the output is enabled. LVCMOS/LVTTL interface levels.
23, 24	N1, N0	Input	Pulldown	FemtoClock output divide select pins. LVCMOS/LVTTL interface levels.
26	XTAL_SEL	Input	Pulldown	Crystal select. When HIGH, selects XTAL1. When LOW, selects XTAL0. LVCMOS/LVTTL interface levels.
27, 28	XTAL_OUT1, XTAL_IN1	Input		Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output.
30, 31	XTAL_OUT0, XTAL_IN0	Input		Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output.
32	V_{DDX}	Power		Power supply pin for VCXO charge pump.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	$V_{DD} = V_{DDO} = 3.465V$		8.5		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			22.5		Ω

Function Tables

Table 3A. VCXO PLL Feedback Divider and Input Frequency Function Table

Input				VCXO PLL Configuration Feedback-Divider M	Input frequency for crystal frequency (f_{VCXO}) in kHz	
V3	V2	V1	V0		f_{VCXO} = 27MHz	f_{VCXO} = 26.973MHz
0 (default)	0 (default)	0 (default)	0 (default)	400	67.5	67.4326
0	0	0	1	480	56.25	56.1938
0	0	1	0	600	45.00	44.9550
0	0	1	1	720	37.50	37.4625
0	1	0	0	800	33.75	33.7163
0	1	0	1	858	31.4685	31.4371
0	1	1	0	864	31.25	31.2188
0	1	1	1	960	28.125	28.0969
1	0	0	0	1000	27.00	26.973
1	0	0	1	1200	22.50	22.4775
1	0	1	0	1440	18.75	18.7313
1	0	1	1	1500	18.00	17.9820
1	1	0	0	1716	15.7343	15.7185
1	1	0	1	1728	15.6250	15.6094
1	1	1	0	1716	15.7343	15.7185
1	1	1	1	960	28.125	28.0969

Table 3B. Output Frequency Table (Dual PLL Mode)

f_{VCXO}	FemtoClock Look-up Table			Output Frequency f_Q (MHz)
	MF	N1	N0	
27MHz	0	0	0	148.5000
	0	0	1	74.2500
	0	1	0	49.5000
	0	1	1	33.0000
	1	0	0	162.0000
	1	0	1	81.0000
	1	1	0	54.0000
	1	1	1	36.0000
26.973MHz	0	0	0	148.3515
	0	0	1	74.1758
	0	1	0	49.4505
	0	1	1	32.9670
	1	0	0	161.8382
	1	0	1	80.9191
	1	1	0	53.9461
	1	1	1	35.9640

NOTE: Use the VCXO-PLL mode to achieve output frequencies of 27MHz or 26.973MHz. See Table 3G.

Table 3C. CLK_SEL Function Table

Input	
CLK_SEL	Operation
0 (default)	Selects CLK0 as PLL reference input.
1	Selects CLK1 as PLL reference input.

Table 3D. MR Master Reset Function Table

Input	
MR	Operation
0 (default)	Normal operation, internal dividers and the output Q are enabled.
1	Internal dividers are reset. Q output is in logic low state (with OE = 1).

Table 3E. FemtoCLock PLL Feedback Divider Function Table

Input	
MF	Operation
0 (default)	Selects MF = 22. The 2nd stage PLL (FemtoClock. multiplies the output frequency of the VCXO-PLL by 22.
1	Selects MF = 24. The 2nd stage PLL (FemtoClock. multiplies the output frequency of the VCXO-PLL by 24.

Table 3F. PLL Output Divider Function Table

Input		
N1	**N0**	**Operation**
0 (default)	0 (default)	Output divider N = 4.
0	1	Output divider N = 8.
1	0	Output divider N = 12.
1	1	Output divider N = 18.

Table 3G. PLL BYPASS Logic Function Table

Input		
nBP1	**nBP0**	**Operation**
0	0	VCXO-PLL mode: The input reference frequency is multiplied by the VCXO-PLL. $f_{OUT} = f_{REF} * M$.
0	1	Test mode: The input reference frequency is divided by the output divider N and bypasses both PLLs. $f_{OUT} = f_{REF} \div N$.
1	0	FemtoClock Mode: The input reference frequency is multiplied by the 2nd PLL (FemtoClock, MF). The 1st PLL (VCXO-PLL, M) is bypassed. This mode does not support jitter attenuatiion. $f_{OUT} = f_{REF} * MF \div N$.
1 (default)	1 (default)	Dual PLL Mode: both PLLs are cascaded for jitter attenuation and frequency multiplication. $f_{OUT} = f_{REF} * M * MF \div N$.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = V_{DDX}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{DDX}	Charge Pump Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				187	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current	No Load			4	mA
I_{DDX}	Charge Pump Supply Current				4	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = V_{DDX}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK[0:1], CLK_SEL, P[1:0], V[3:0], N[1:0], MR, MF, XTAL_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		OE, nBP0, nBP1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK[0:1], CLK_SEL, P[1:0], V[3:0], N[1:0], MR, MF, XTAL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OE, nBP0, nBP1	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -24mA	2.6			V
V_{OL}	Output Low Voltage		I_{OL} = 24mA			0.5	V

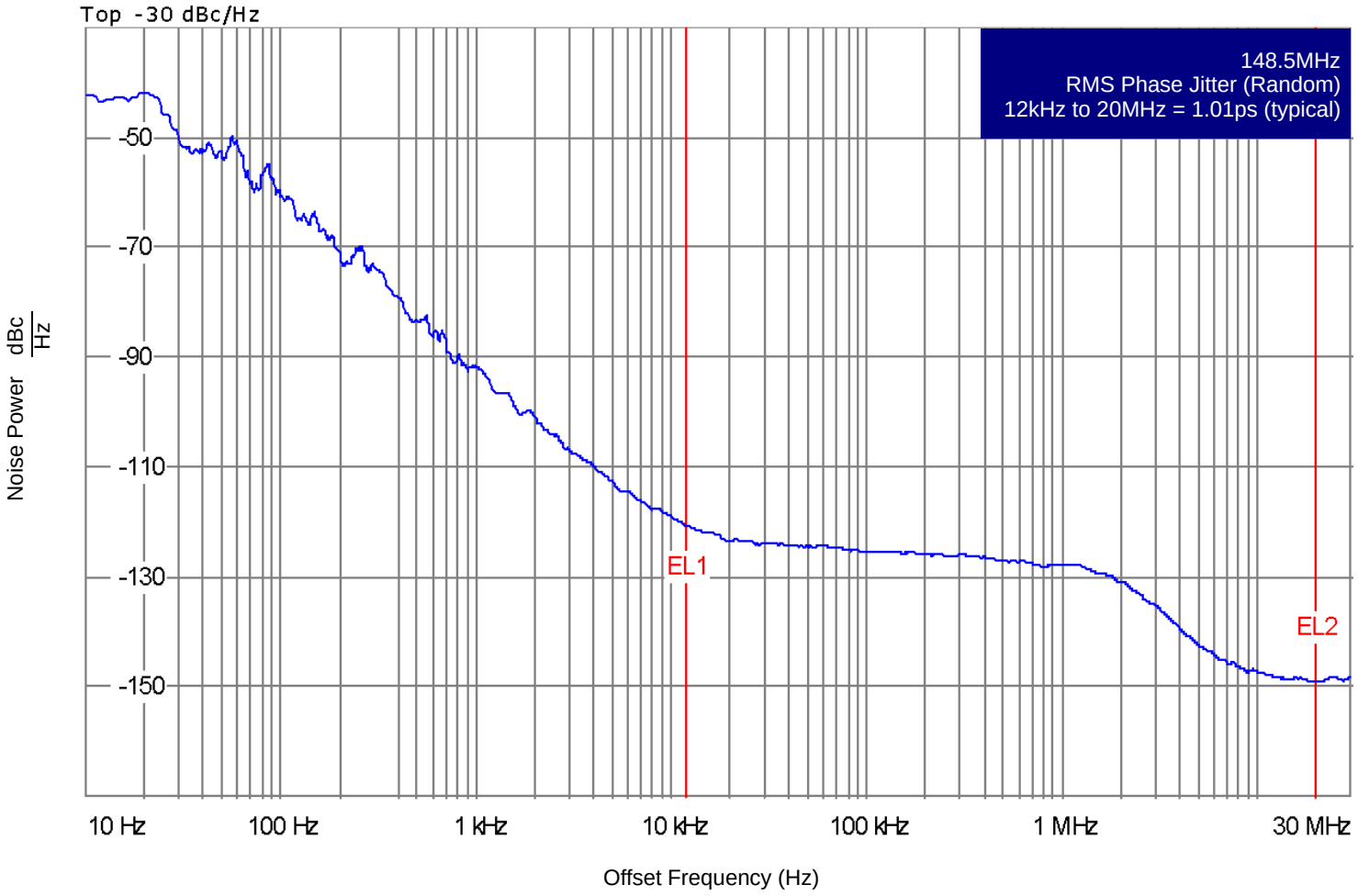
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = V_{DDO} = V_{DDX} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

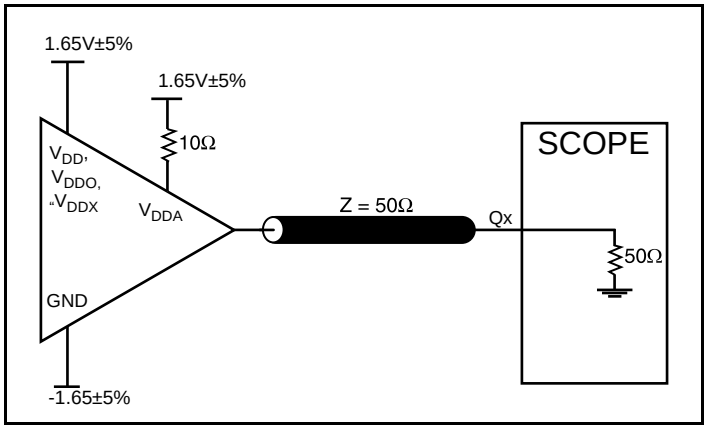
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	nBP0, nBP1 = 00	26		28	MHz
		nBP1 = 1	31		175	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	148.5MHz, Integration Range: 12kHz – 20MHz		1.01		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		750	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	VCXO & FemtoClock PLL Lock Time; NOTE 2				5	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
See Parameter Measurement Information Section.
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: Lock Time measured from power-up to stable output frequency.

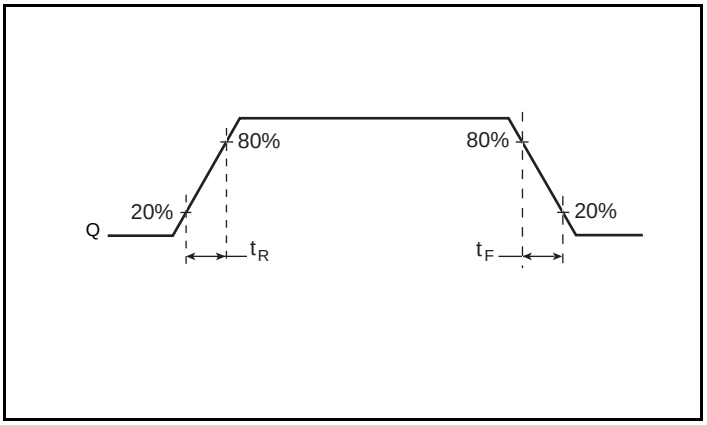
Typical Phase Noise at 148.3516MHz



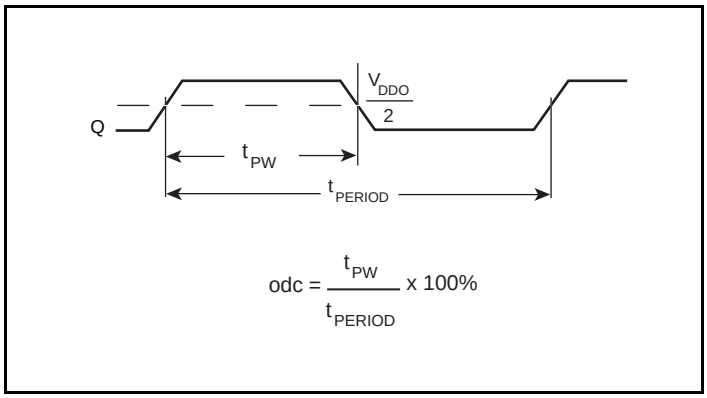
Parameter Measurement Information



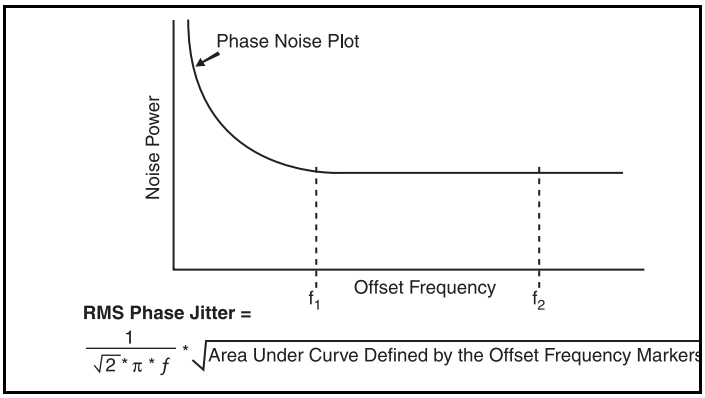
3.3V Output Load AC Test Circuit



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Phase Jitter

Application Information

Recommendations for Unused Input Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 810001-22 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO} and V_{DDX} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

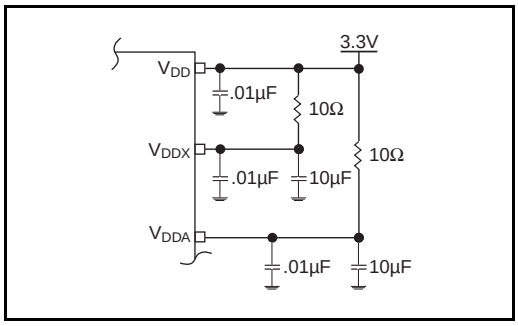


Figure 1. Power Supply Filtering

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

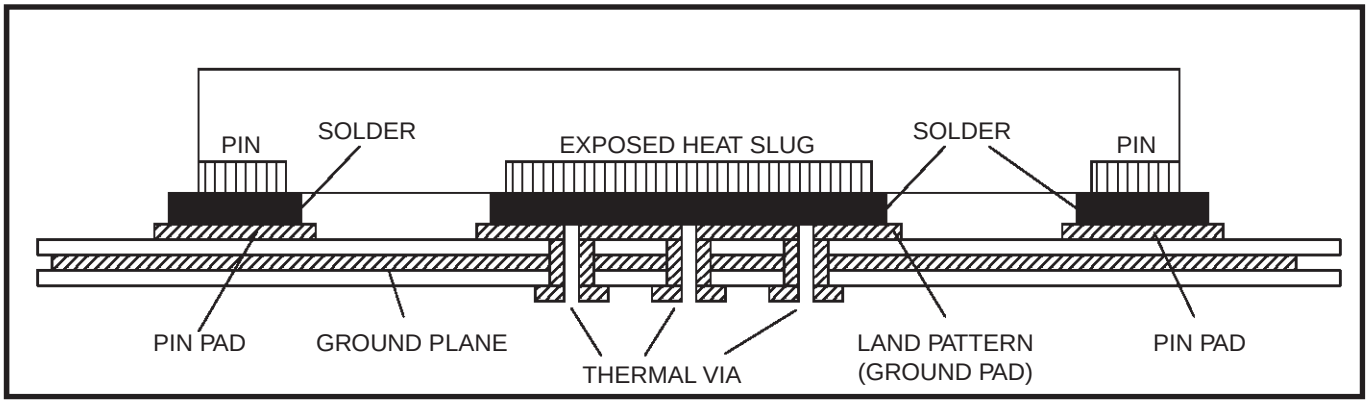


Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 3 shows an example of the 810001-22 application schematic. In this example, the device is operated at $V_{DD} = V_{DDO} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. An optional 3-pole filter can also be used for additional spur reduction. It is recommended that the loop filter components be laid out for the 3-pole option. This will also allow the 2-pole filter to be used.

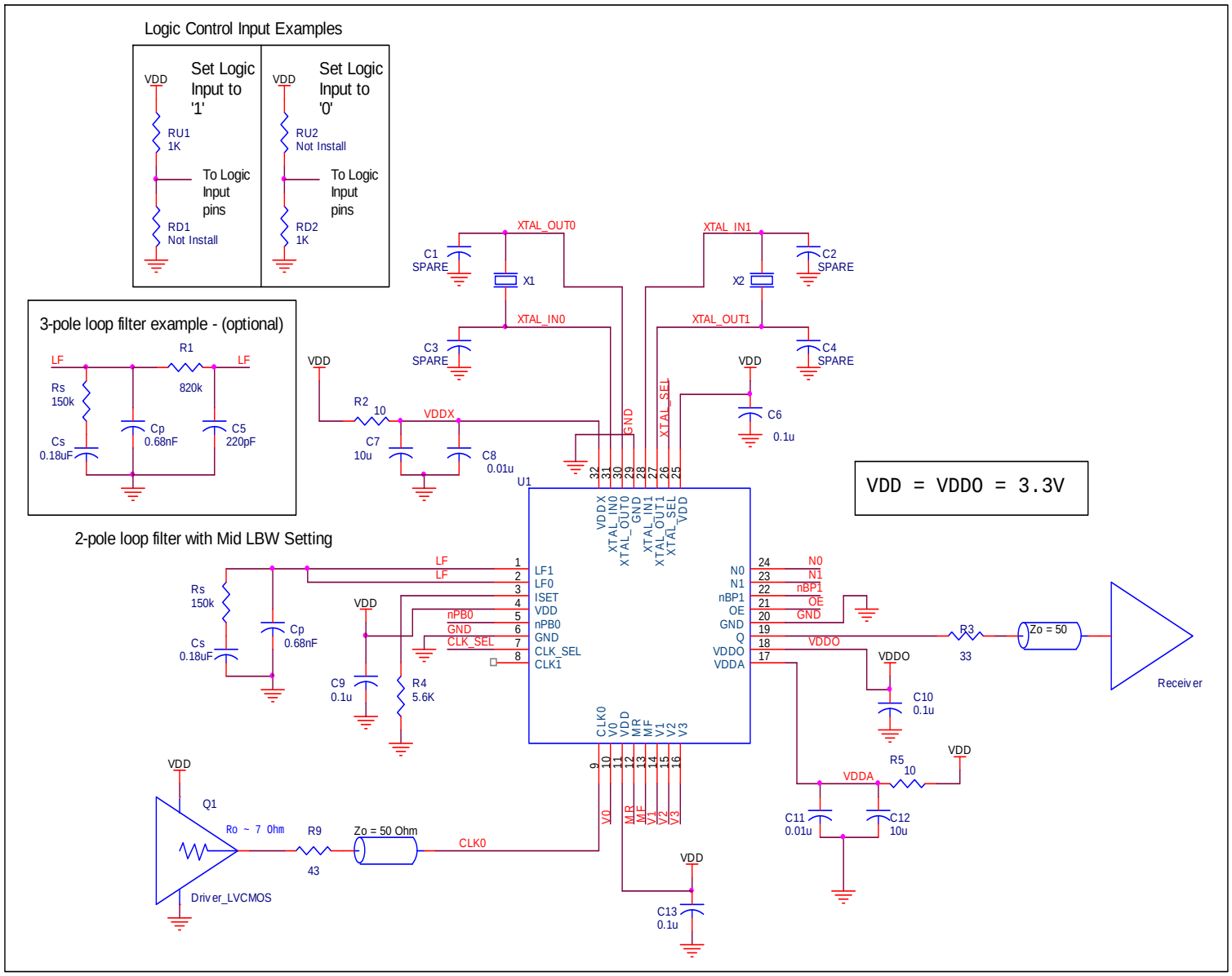


Figure 3. 810001-22 Schematic Example

VCXO-PLL External Components

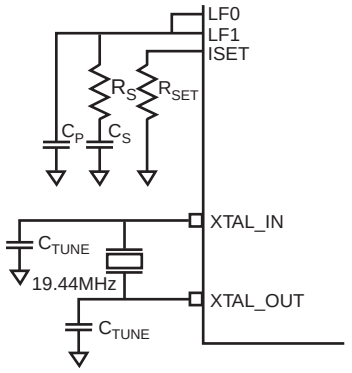
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal's C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal's C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependent on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The frequency of oscillation in the third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental. The oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the tuning curve. This potential problem is why VCXO crystals are required to be tested for absence of any activity inside a +/-200 ppm window at three times the fundamental frequency. Refer to F_{L_3OVT} and $F_{L\_3OVT\_spurs}$ in the crystal Characteristics table.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Units
k_{VCXO}	VCXO Gain	13.65	kHz/V
C_{V_LOW}	Low Varactor Capacitance	16	pF
C_{V_HIGH}	High Varactor Capacitance	33	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	MF	R_S (kΩ)	C_S (µF)	C_P (nF)	R_{SET} (kΩ)
11Hz (Low)	27, 26.973	1728	150	1	10	18
64Hz (Mid)	27, 26.973	1000	150	0.18	0.68	5.6
597Hz (High)	27, 26.973	400	220	0.022	0.12	2.2

Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			27		MHz
				26.973		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		0		70	^{0}C
C_L	Load Capacitance			12		pF
C_O	Shunt Capacitance			4		pF
C_O / C_1	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				20	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C				±3 per year	ppm

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

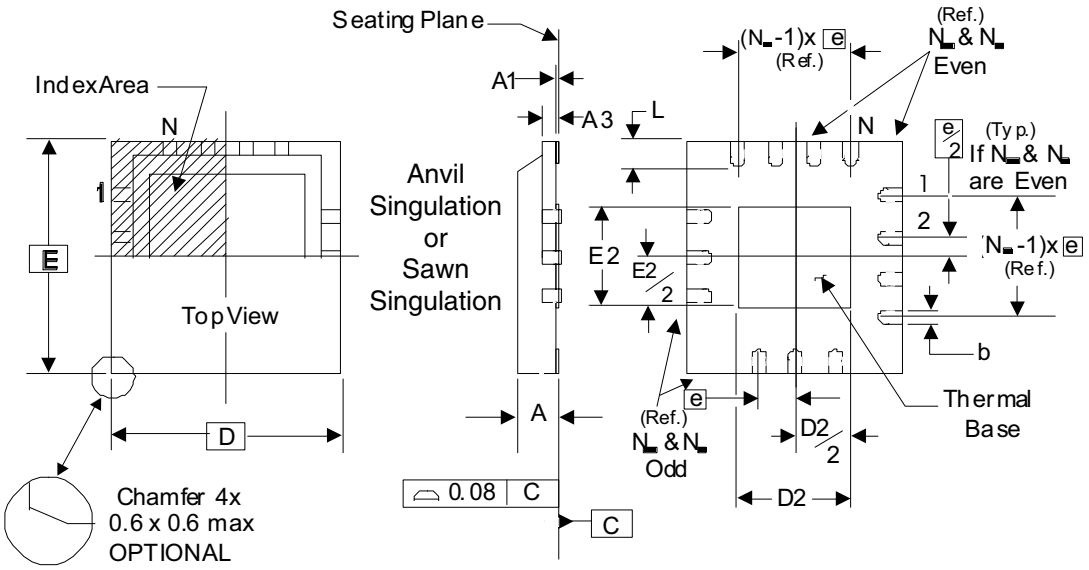
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29°C/W

Transistor Count

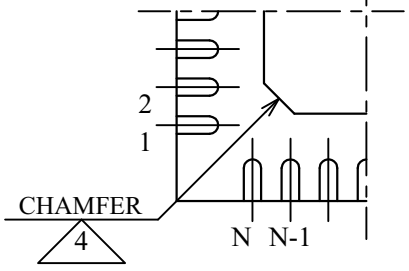
The transistor count for 810001-22 is: 7283

Package Outline and Package Dimensions

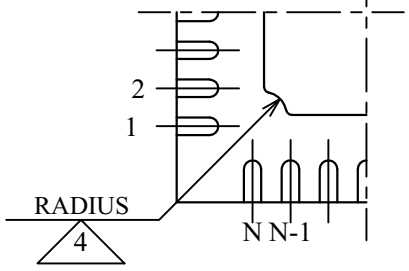
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 7. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 7 below.

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
810001BK-22LF	ICS0001B22L	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
810001BK-22LFT	ICS0001B22L	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Product Discontinuation Notice - Last time buy expires August 14, 2016 PDN# CQ-15-04	8/14/15

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