# Low Skew, 1-to-4, Crystal Oscillator/LVCMOS-to-3.3V, 2.5V LVPECL/LVCMOS Fanout Buffer

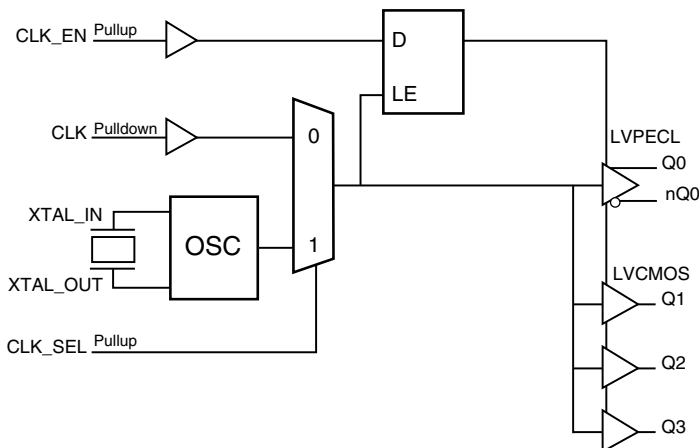# ICS8534I-13

## General Description

The ICS8534I-13 is a low skew, high performance 1-to-4 Crystal Oscillator/LVCMOS-to-3.3V, 2.5V LVPECL/LVCMOS fanout buffer. The ICS8534I-13 has selectable single-ended clock or crystal inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8534I-13 ideal for those applications demanding well defined performance and repeatability.

## Features

- One differential LVPECL output, and three single-ended LVCMOS outputs

- Selectable LVCMOS/LVTTL CLK or crystal inputs

- CLK can accept the following input levels: LVCMOS, LVTTL

- Crystal frequency range: 12MHz – 40MHz

- Maximum output frequency: 266MHz

- Propagation delay: 2.1ns (maximum), 3.3V LVPECL output

- Additive phase jitter, RMS: 0.221ps (typical), 3.3V LVPECL output

- Full 3.3V or 2.5V operating supply

- -40°C to 85°C ambient operating temperature

- Lead-free (RoHS 6) packaging

## Block Diagram



## Pin Assignment



**ICS8534I-13**

**16-Lead SOIC, 150MIL**

3.9mm x 9.9mm x 1.375mm package body

**M Package**

**Top View**

# Pin Description and Pin Characteristic Tables

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ0 output is forced high. LVCMOS / LVTTL interface levels. |
| 2, 3 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 4 | $V_{CC}$ | Power | | Positive supply pin. |
| 5 | CLK | Input | Pulldown | Clock input. LVCMOS / LVTTL interface levels. |
| 6 | CLK_SEL | Input | Pullup | Clock select input. When HIGH, selects XTAL inputs. When LOW, selects CLK input. LVCMOS / LVTTL interface levels. |
| 7, 12 | $V_{EE}$ | Power | | Negative supply pins. |
| 8 | $V_{CCO\_LVPECL}$ | Power | | Output power supply mode for LVPECL clock outputs. |
| 9, 10 | Q0, nQ0 | Output | | Differential clock outputs. LVPECL interface levels. |
| 11 | nc | Unused | | No connect. |
| 13, 15, 16 | Q1, Q2, Q3 | Output | | Single ended clock outputs. LVCMOS / LVTTL interface levels. |
| 14 | $V_{CCO\_LVCMOS}$ | Power | | Output power supply mode for LVCMOS / LVTTL clock outputs. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Crystal Not Included | | | 4 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance (per output) | Q[1:3] | $V_{CC}$, $V_{CC\_LVCMOS}$ = 3.465V | | 8 | | pF |
| | | | $V_{CC}$, $V_{CC\_LVCMOS}$ = 2.625V | | 5 | | pF |
| $R_{PULUP}$ | Input Pullup Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | Q[1:3] | $V_{CC}$, $V_{CC\_LVCMOS}$ = 3.465V | | 15 | | Ω |
| | | | $V_{CC}$, $V_{CC\_LVCMOS}$ = 2.625V | | 20 | | Ω |

# Function Tables

## Table 3A. Control Input Function Table

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| **CLK_EN** | **CLK_SEL** | **Selected Source** | **Q0** | **nQ0** | **Q[1:3]** |
| 0 | 0 | CLK | Disabled; LOW | Disabled; HIGH | Disabled; LOW |
| 0 | 1 | XTAL_IN, XTAL_OUT | Disabled; LOW | Disabled; HIGH | Disabled; LOW |
| 1 | 0 | CLK | Enabled | Enabled | Enabled |
| 1 | 1 | XTAL_IN, XTAL_OUT | Enabled | Enabled | Enabled |

NOTE: After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 1.

NOTE: In the active mode, the state of the outputs are a function of the CLK input as described in Table 3B.
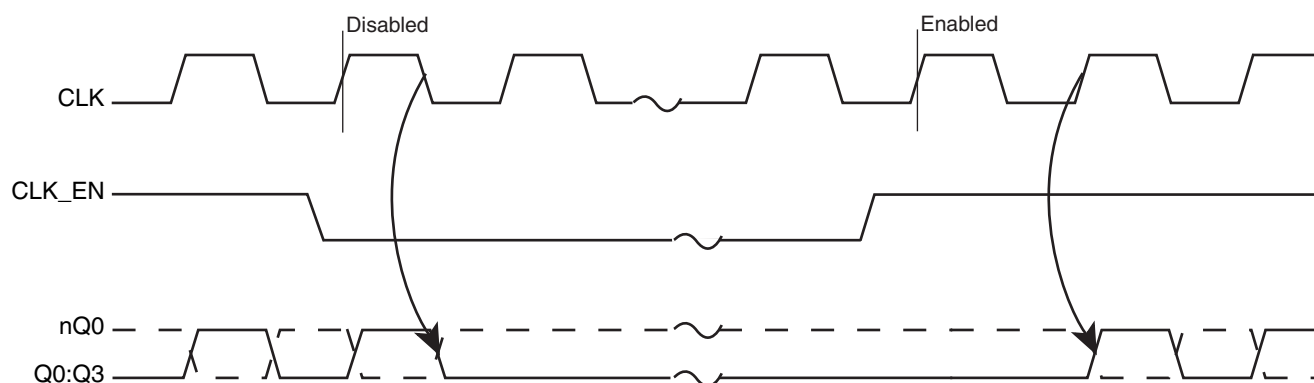


**Figure 1. CLK_EN Timing Diagram**

## Table 3B. Control Input Function Table

| Inputs | Outputs | | |
|---|---|---|---|
| **CLK** | **Q0** | **nQ0** | **Q[1:3]** |
| 0 (default) | LOW | HIGH | LOW |
| 1 | HIGH | LOW | HIGH |

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|------|--------|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ (LVCMOS) | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{CCO\_LVCMOS}$ + 0.5V |
| Inputs, $V_I$ (LVPECL) | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 76°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC} = V_{CCO\_LVPECL} = V_{CCO\_LVCMOS} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO\_LVPECL}$<br>$V_{CCO\_LVCMOS}$ | Power Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 65 | mA |
| $I_{CCO\_LVPECL}$ | Power Supply Current | No Load | | | 25 | mA |
| $I_{CCO\_LVCMOS}$ | Power Supply Current | No Load | | | 5 | mA |

**Table 4B. Power Supply DC Characteristics,** $V_{CC} = V_{CCO\_LVPECL} = V_{CCO\_LVCMOS} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{CCO\_LVPECL}$<br>$V_{CCO\_LVCMOS}$ | Power Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | | 60 | mA |
| $I_{CCO\_LVPECL}$ | Power Supply Current | No Load | | | 22 | mA |
| $I_{CCO\_LVCMOS}$ | Power Supply Current | No Load | | | 4 | mA |

**Table 4C. LVCMOS/LVTTL DC Characteristics,** $V_{CC} = V_{CCO\_LVCMOS} = 2.5V \pm 5\%$, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|---|-----------------|---------|---------|---------|-------|
| $V_{IH}$ | Input High Voltage | | $V_{CC}$ = 3.3V | 2 | | $V_{CC}$ + 0.3 | V |
| | | | $V_{CC}$ = 2.5V | 1.7 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{CC}$ = 3.3V | -0.3 | | 0.8 | V |
| | | | $V_{CC}$ = 2.5V | -0.3 | | 0.7 | V |
| $V_{HYS}$ | Input Hysteresis | CLK_EN, CLK_SEL | | 100 | | | mV |
| $I_{IH}$ | Input High Current | CLK | $V_{CC} = V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| | | CLK_EN, CLK_SEL | $V_{CC} = V_{IN}$ = 3.465V or 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | CLK_EN, CLK_SEL | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO\_LVCMOS}$ = 3.465V | 2.6 | | | V |
| | | | $V_{CCO\_LVCMOS}$ = 2.625V | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO\_LVCMOS}$ = 3.465V or 2.625V | | | 0.55 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_LVCMOS}$/2. See Parameter Measurement Information Section, *LVCMOS Output Load Test Circuit Diagram.*

**Table 4D. LVPECL DC Characteristics,** $V_{CC} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{OH}$ | Output High Voltage: NOTE 1 | | $V_{CCO\_LVPECL} - 1.4$ | | $V_{CCO\_LVPECL} - 0.9$ | V |
| $V_{OL}$ | Output Low Voltage: NOTE 1 | | $V_{CCO\_LVPECL} - 2.1$ | | $V_{CCO\_LVPECL} - 1.7$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CCO\_LVPECL} - 2V$.

**Table 4E. LVPECL DC Characteristics,** $V_{CC} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$, $V_{EE}$ = 0V, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{OH}$ | Output High Voltage: NOTE 1 | | $V_{CCO\_LVPECL} - 1.4$ | | $V_{CCO\_LVPECL} - 0.9$ | V |
| $V_{OL}$ | Output Low Voltage: NOTE 1 | | $V_{CCO\_LVPECL} - 2.1$ | | $V_{CCO\_LVPECL} - 1.5$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.4 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CCO\_LVPECL} - 2V$.

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | 12 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | $\Omega$ |
| Shunt Capacitance ($C_O$) | | | | 7 | pF |
| Drive Level | | | | 1 | mW |
| Load Capacitance ($C_L$) | | 12 | | 18 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

# AC Electrical Characteristics

**Table 6A. LVPECL AC Characteristics,** $V_{CC} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | | | 266 | MHz |
| $t_{PD}$ | Propagation Delay: Note 1 | | | 1.5 | | 2.1 | ns |
| $fjit$ | Buffer Additive Phase Jitter, RMS | | 155.52MHz, Integration Range: 12kHz - 20MHz | | 0.221 | | ps |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 2, 3 | | | | 150 | 600 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% - 80% | 200 | | 1050 | ps |
| odc | Output Duty Cycle | XTAL | | 46 | | 54 | % |
| | | CLK | | 45 | | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq 266MHz$ unless noted otherwise.
NOTE 1: Measured from the $V_{CC}/2$ of the input to the differential output crosspoint.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the LVPECL output differential crosspoint.
NOTE 3: This parameter is defined in accordance with JDEC Standard 65.

**Table 6B. LVPECL AC Characteristics,** $V_{CC} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | | | 266 | MHz |
| $t_{PD}$ | Propagation Delay: Note 1 | | | 1.4 | | 2.2 | ns |
| $fjit$ | Buffer Additive Phase Jitter, RMS | | 155.52MHz, Integration Range: 12kHz - 20MHz | | 0.178 | | ps |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 2, 3 | | | | 100 | 450 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% - 80% | 115 | | 1115 | ps |
| odc | Output Duty Cycle | XTAL | | 46 | | 54 | % |
| | | CLK | | 44 | | 56 | % |

For NOTES, see Table 6A above.

**Table 6C. LVCMOS AC Characteristics,** $V_{CC}$ = $V_{CCO\_LVCMOS}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|--|-----------------|---------|---------|---------|-------|
| $f_{OUT}$ | Output Frequency | | | | | 266 | MHz |
| $t_{PD}$ | Propagation Delay: Note 1 | | | 2.7 | | 3.85 | ns |
| $f$jit | Buffer Additive Phase Jitter, RMS | | 155.52MHz, Integration Range: 12kHz - 20MHz | | 0.273 | | ps |
| $t$sk(b) | Bank Skew; NOTE 2, 4 | | | | | 75 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 150 | 500 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% - 80% | 450 | | 1000 | ps |
| odc | Output Duty Cycle | XTAL | | 47 | | 53 | % |
| | | CLK | | 35 | | 65 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from the $V_{CC}$/2 of the input to $V_{CCO\_LVCMOS}$/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the $V_{CCO\_LVCMOS}$/2.
NOTE 4: This parameter is defined in accordance with JDEC Standard 65.

**Table 6D. LVCMOS AC Characteristics,** $V_{CC}$ = $V_{CCO\_LVCMOS}$ = 2.5V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|--|-----------------|---------|---------|---------|-------|
| $f_{OUT}$ | Output Frequency | | | | | 266 | MHz |
| $t_{PD}$ | Propagation Delay: Note 1 | | | 2.75 | | 4.10 | ns |
| $f$jit | Buffer Additive Phase Jitter, RMS | | 155.52MHz, Integration Range: 12kHz - 20MHz | | 0.181 | | ps |
| $t$sk(b) | Bank Skew; NOTE 2, 4 | | | | | 75 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 210 | 800 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | | 20% - 80% | 250 | | 1700 | ps |
| odc | Output Duty Cycle | XTAL | | 47 | | 53 | % |
| | | CLK | | 30 | | 70 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE 1: Measured from the $V_{CC}$/2 of the input to $V_{CCO\_LVCMOS}$/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the $V_{CCO\_LVCMOS}$/2.
NOTE 4: This parameter is defined in accordance with JDEC Standard 65.
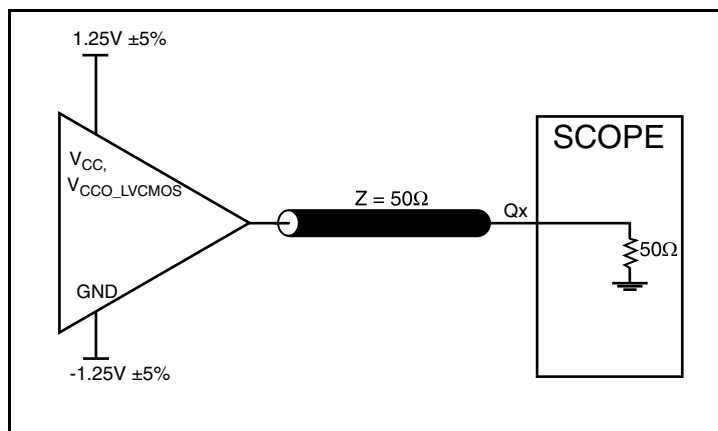
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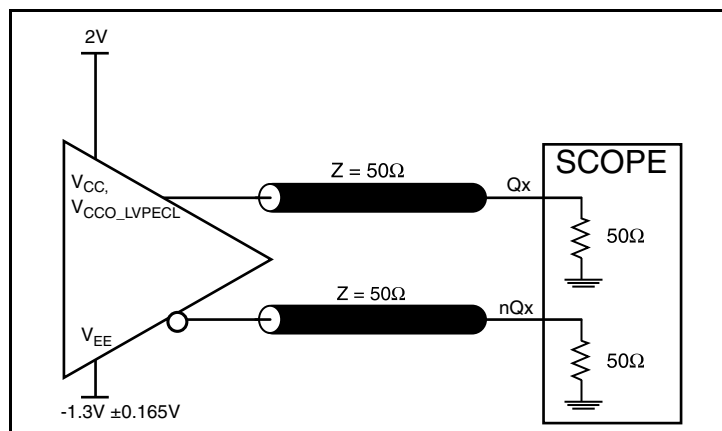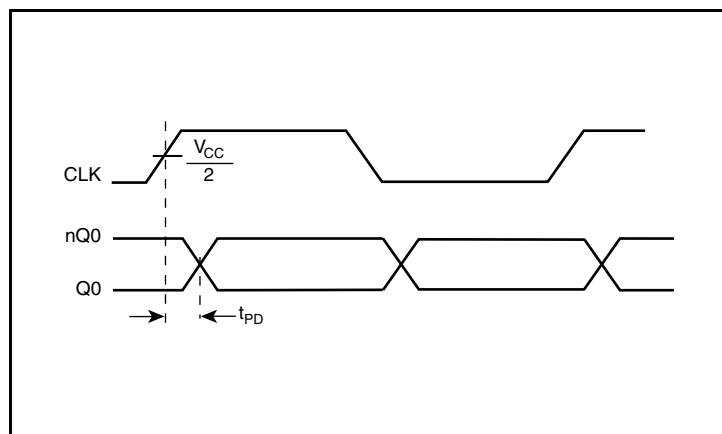


**3.3V LVPECL Output Load Test Circuit**
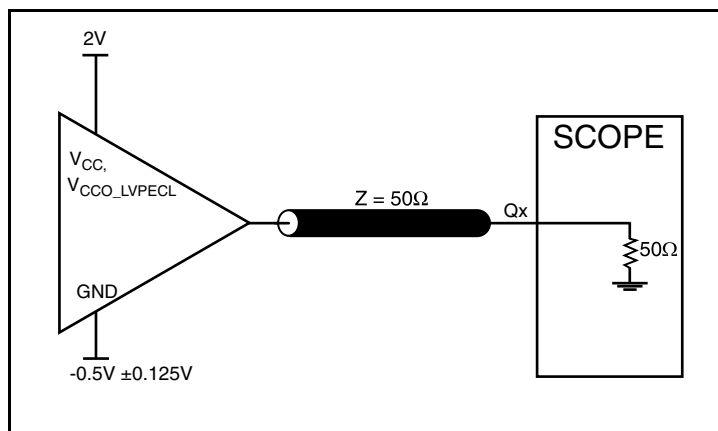


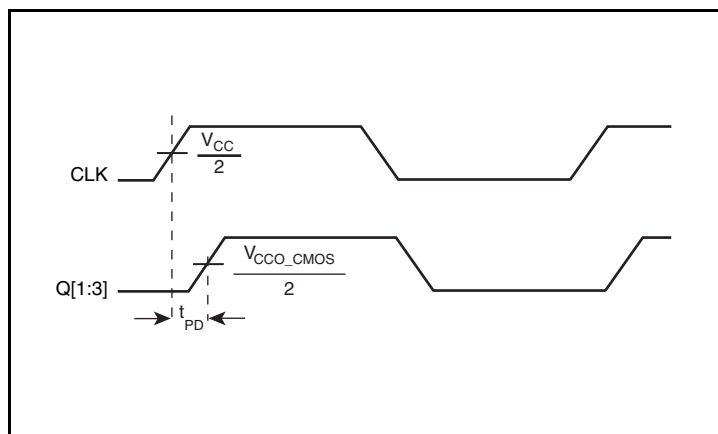**2.5V LVPECL Output Load Test Circuit**
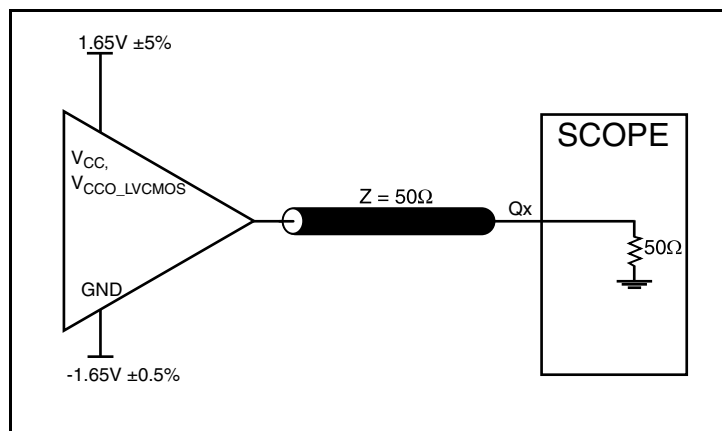


**3.3V LVCMOS Output Load Test Circuit**
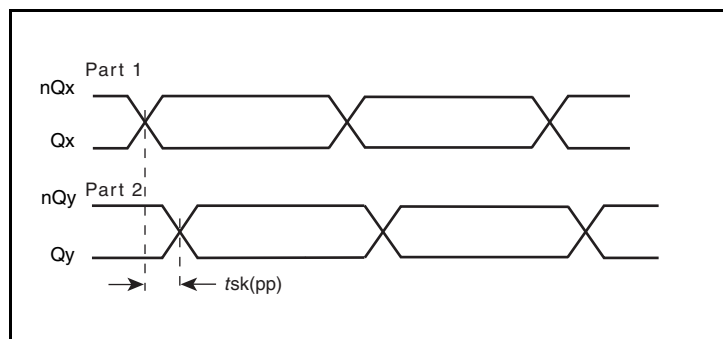


**2.5V LVCMOS Output Load Test Circuit**



**LVPECL Propagation Delay**



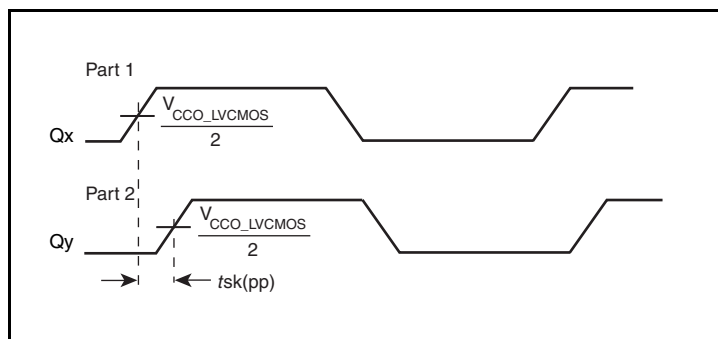**LVCMOS Propagation Delay**
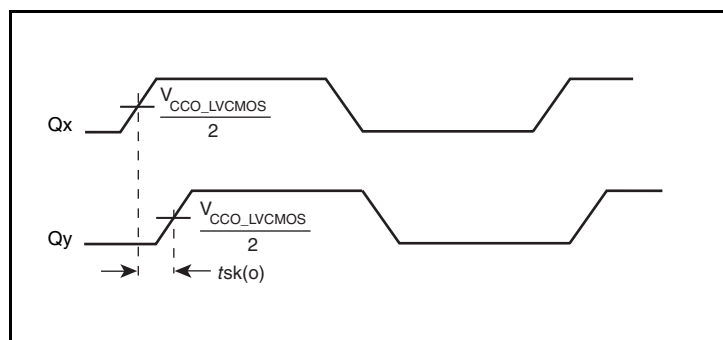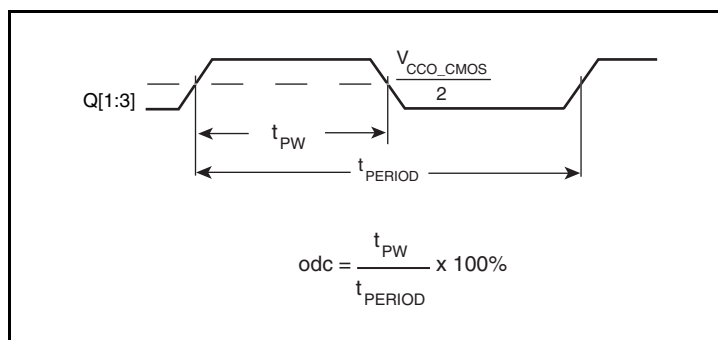
# Parameter Measurement Information (continued)



**LVPECL Part-to-Part Skew**


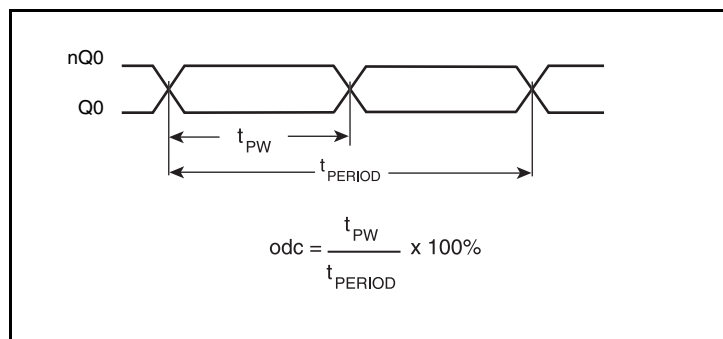
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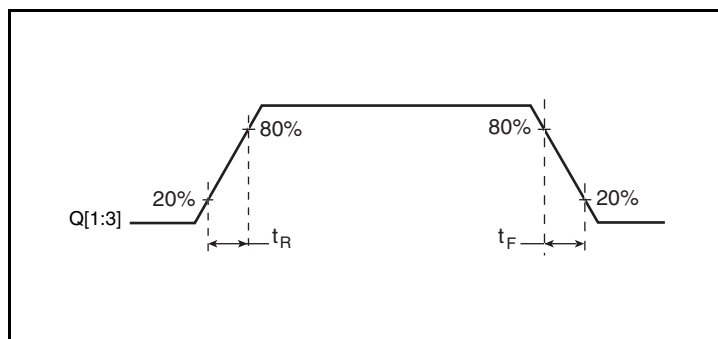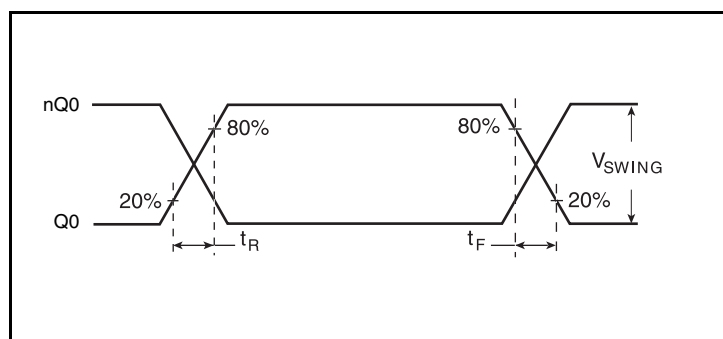


**LVCMOS Bank Skew**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**LVCMOS Output Duty Cycle/Pulse Width/Period**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**LVPECL Output Duty Cycle/Pulse Width/Period**



**LVCMOS Output Rise/Fall Time**



**LVPECL Output Rise/Fall Time**

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### CLK Inputs

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pullup resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

#### LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The ICS8534I-13 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
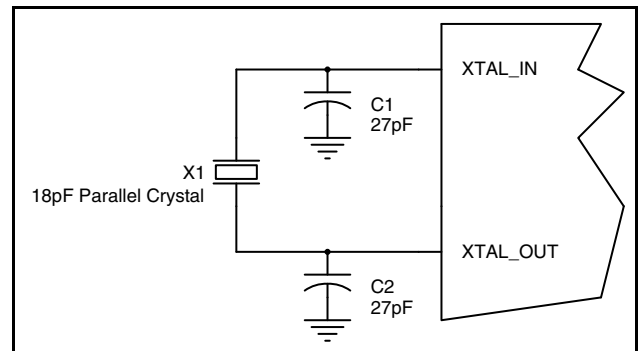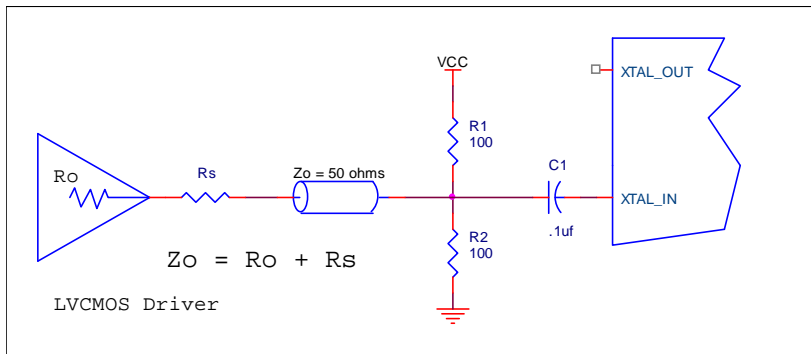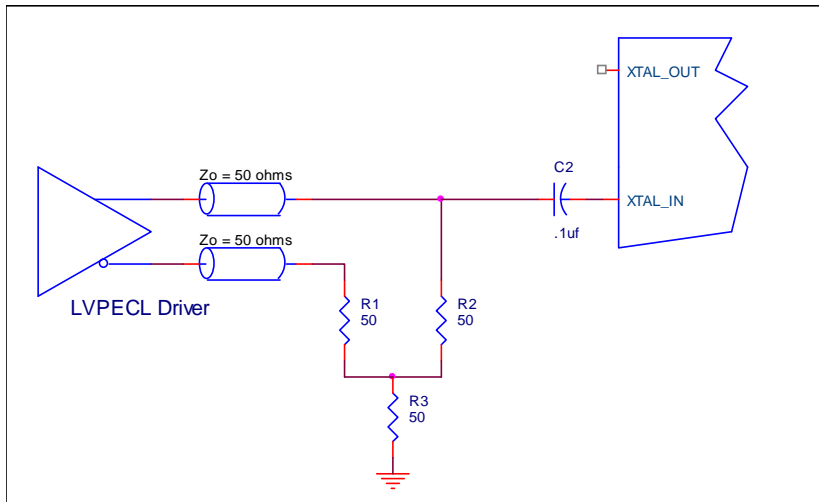


Figure 2. Crystal Input Interface

## Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
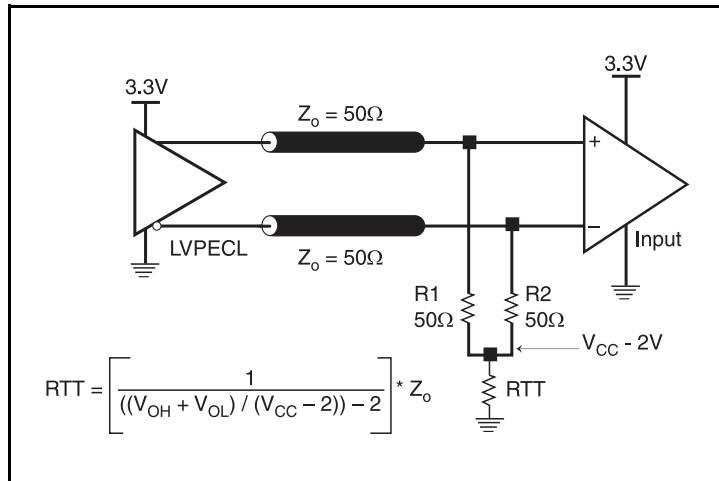


$$RTT = \left[ \frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2} \right] * Z_o$$

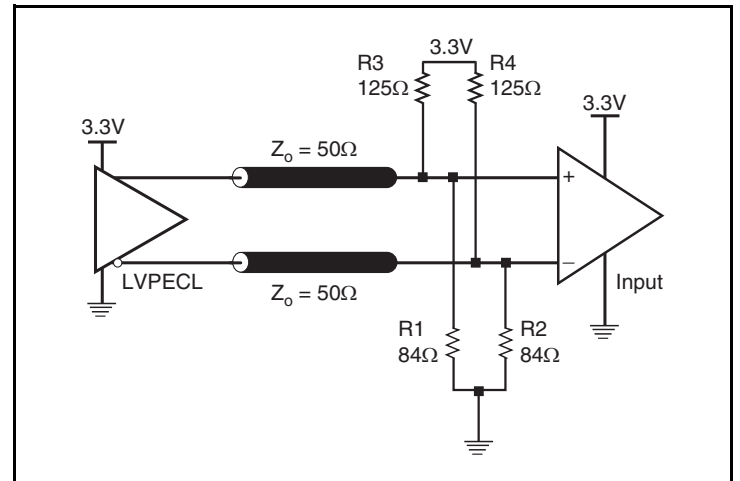**Figure 4A. 3.3V LVPECL Output Termination**



**Figure 4B. 3.3V LVPECL Output Termination**

## Termination for 2.5V LVPECL Outputs

*Figure 5A* and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50$\Omega$ to $V_{CCO}$ – 2V. For $V_{CCO}$ = 2.5V, the $V_{CCO}$ – 2V is very close to -LVCMOS ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*
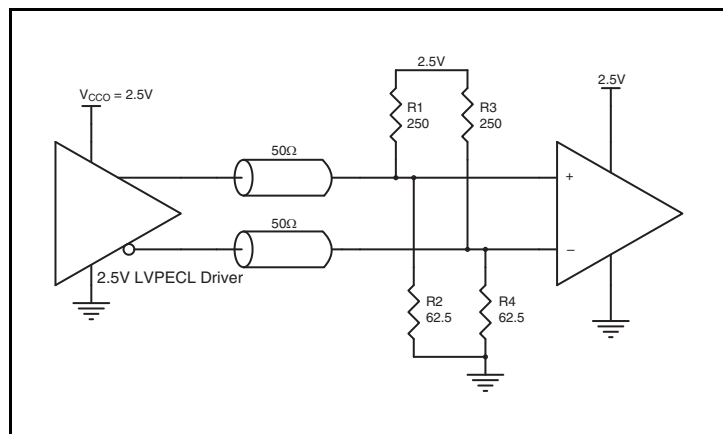
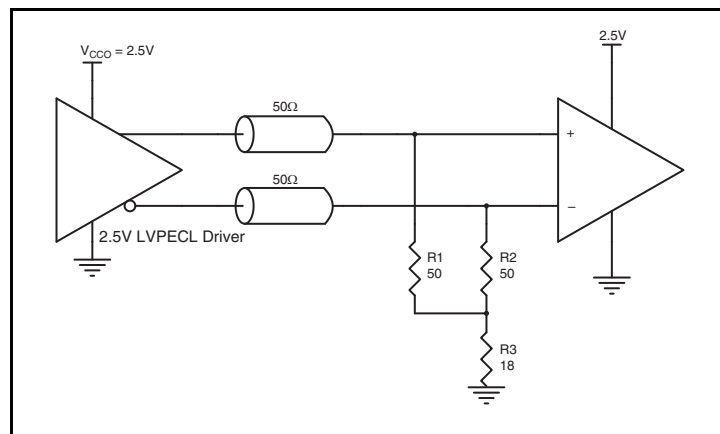**Figure 5A. 2.5V LVPECL Driver Termination Example**

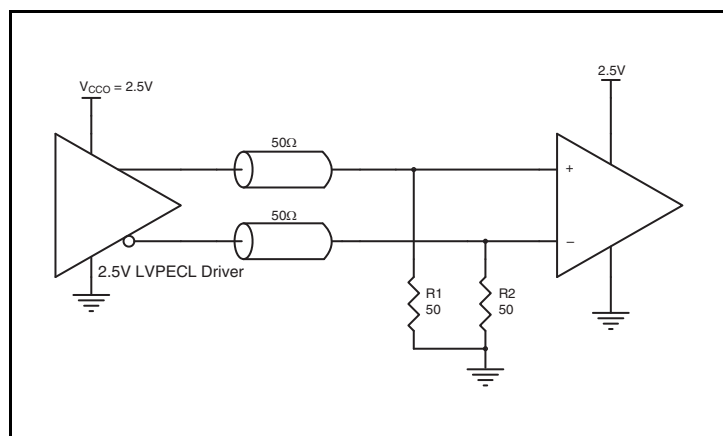**Figure 5B. 2.5V LVPECL Driver Termination Example**

**Figure 5C. 2.5V LVPECL Driver Termination Example**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8534I-13.
Equations and example calculations are also provided.

### 1. Power Dissipation

The total power dissipation for the ICS8534i-13 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

Core and LVPECL Output Power Dissipation

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 65mA = **225.225mW**

- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 1 * 30mW = **30mW**

**LVCMOS Output Power Dissipation**

- Output Impedance $R_{OUT}$ Power Dissipation due to Loading 50Ω to $V_{CCO\_LVCMOS}$/2
  Output Current $I_{OUT}$ = $V_{CCO\_MAX}$/ [2 * (50Ω + $R_{OUT}$)] = 3.465V / [2 * (50Ω + 15Ω] = **26.7mA**

- Power Dissipation on the $R_{OUT}$ per LVCMOS output
  Power ($R_{OUT}$) = $R_{OUT}$ * $(I_{OUT})^2$ = 15Ω * $(26.7mA)^2$ = **10.7mW per output**

- Total Power Dissipation on the $R_{OUT}$
      **Total Power ($R_{OUT}$)** = 10.7mW * 3 = **32.1mW**

**Total Power Dissipation**

- **Total Power**

  = LVPECL Power (core)$_{MAX}$ + LVPECL Power (outputs)$_{MAX}$ + Total Power ($R_{OUT}$)

  = 225.225mW + 30mW + 32.1mW

  = 287.325mW

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

   The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

   Tj = Junction Temperature

   $\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

   Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

   $T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 76°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

   85°C + 0.287W * 76°C/W = 106.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).
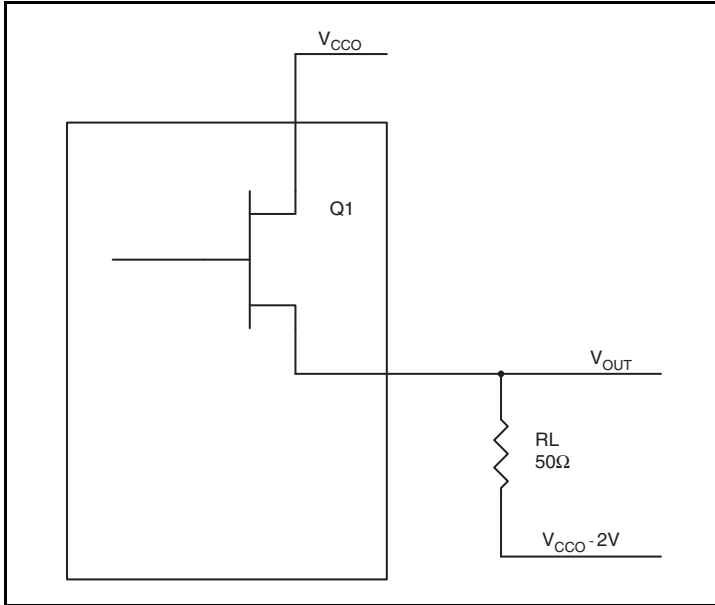
### Table 7. Thermal Resistance $\theta_{JA}$ for 16 Lead SOIC, Forced Convection

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters Per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 76.0°C/W | 69.78°C/W | 67.49°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6.*



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$
$\qquad (V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$
$\qquad (V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L]$ * $(V_{CCO\_MAX} - V_{OH\_MAX})$ = $[(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L]$ * $(V_{CCO\_MAX} - V_{OH\_MAX})$ = $[(2V - 0.9V)/50W]$ * 0.9V = **19.8mW**

Pd_L = $[(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L]$ * $(V_{CCO\_MAX} - V_{OL\_MAX})$ = $[(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L]$ * $(V_{CCO\_MAX} - V_{OL\_MAX})$ = $[(2V - 1.7V)/50W]$ * 1.7V = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

## Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 16 Lead SOIC**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters Per Second | **0** | **1** | **2** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 76.0°C/W | 69.78°C/W | 67.49°C/W |

## Transistor Count

The transistor count for ICS8534I-13 is: 550

## Package Outline and Package Dimensions
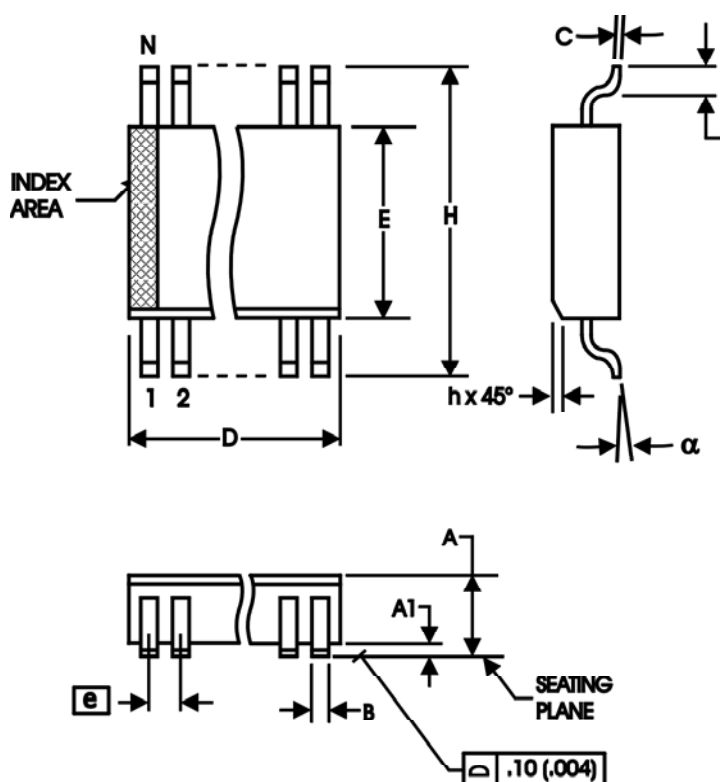
**Package Outline - G Suffix for 16 Lead SOIC**



**Table 9. Package Dimensions**

| Symbol | Millimeters | |
|---|---|---|
| | **Minimum** | **Maximum** |
| **N** | 16 | |
| **A** | 1.35 | 1.75 |
| **A1** | 0.10 | 0.25 |
| **B** | 0.33 | 0.51 |
| **C** | 0.19 | 0.25 |
| **D** | 0.80 | 10.00 |
| **E** | 3.80 | 4.00 |
| **e** | 1.27 BASIC | |
| **H** | 5.80 | 6.20 |
| **h** | 0.25 | 0.50 |
| **L** | 0.40 | 1.27 |
| $\alpha$ | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012

# Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8534BMI-13LF | 8534BMI-13L | 16 Lead, "Lead-Free" SOIC | Tube | -40°C to 85°C |
| 8534BMI-13LFT | 8534BMI-13L | 16 Lead, "Lead-Free" SOIC | Tape & Reel | -40°C to 85°C |

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## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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