Description

The 87016I is a low skew, 1:16 LVCMOS/LVTTL Clock Generator. The device has four banks of four outputs and each bank can be independently selected for ÷1 or ÷2 frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

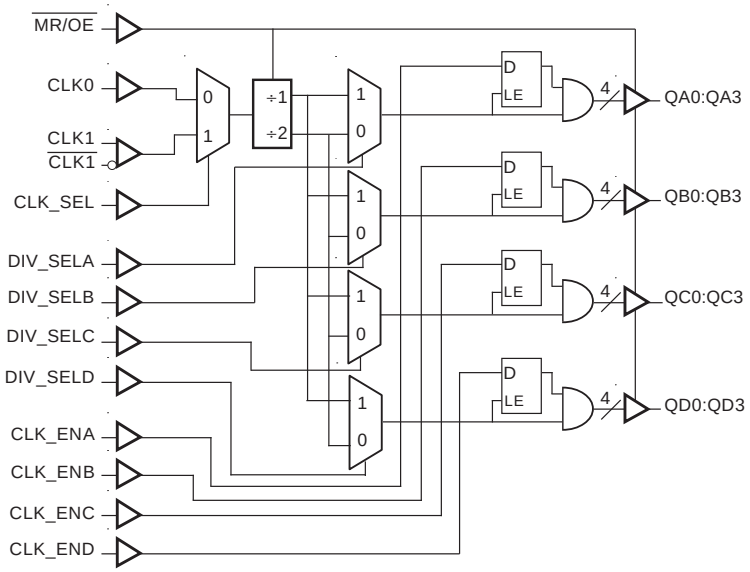
The divide select inputs, DIV_SELA:DIV_SELD, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The bank enable inputs, CLK_ENA:CLK_END, support enabling and disabling each bank of outputs individually. The CLK_ENA:CLK_END circuitry has a synchronizer to prevent runt pulses when enabling or disabling the clock outputs. The master reset input, MR/OE, resets the ÷1/÷2 flip flops and also controls the active and high impedance states of all outputs. This pin has an internal pull-up resistor and is normally used only for test purposes or in systems which use low power modes.

The 87016I is characterized to operate with the core at 3.3V or 2.5V and the banks at 3.3V, 2.5V, or 1.8V. Guaranteed bank, output, and part-to-part skew characteristics make the 87016I ideal for those clock applications demanding well-defined performance and repeatability.

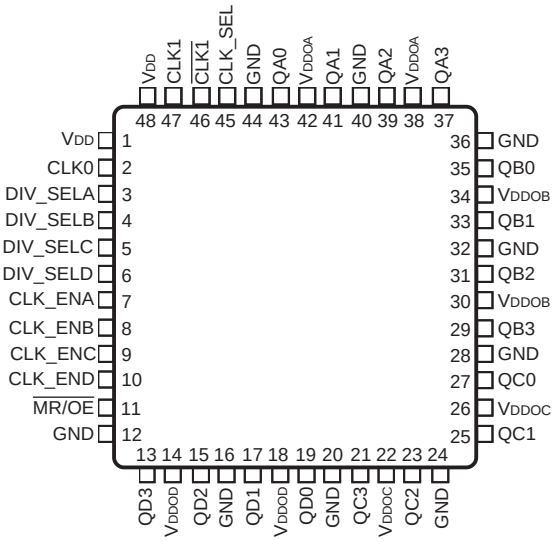
Features

- Sixteen LVCMOS/LVTTL outputs (4 banks of 4 outputs)
- Selectable differential CLK1/$\overline{CLK1}$ or LVCMOS/LVTTL clock input
- CLK1, $\overline{CLK1}$ pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Independent bank control for ÷1 or ÷2 operation
- Independent output bank voltage settings for 3.3V, 2.5V, or 1.8V operation
- Asynchronous clock enable/disable
- Output skew: 170ps (maximum)
- Bank skew: 50ps (maximum
- Part-to-Part Skew: 800ps (maximum)
- Supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Lead-free packaging

Block Diagram



Pin Assignment



87016I

48-LQFP
7 × 7 × 1.4 mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 48	V_{DD}	Power		Positive supply pins.
2	CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
3	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. See Table 3. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs. See Table 3. LVCMOS / LVTTL interface levels.
5	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. See Table 3. LVCMOS / LVTTL interface levels.
6	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. See Table 3. LVCMOS / LVTTL interface levels.
7	CLK_ENA	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
8	CLK_ENB	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
9	CLK_ENC	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
10	CLK_END	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
11	$\overline{MR/OE}$	Input	Pullup	Master reset. When LOW, resets the ÷1/÷2 flip flops and sets the outputs to high impedance. LVCMOS / LVTTL interface levels.
12, 16, 20, 24, 28, 32, 36, 40, 44	GND	Power		Power supply ground
13, 15, 17, 19	QD3, QD2, QD1, QD0	Output		Bank D single-ended clock outputs. LVCMOS/LVTTL interface levels.
14, 18	V_{DDOD}	Power		Bank D output supply pins.
21, 23, 25, 27	QC3, QC2, QC1, QC0	Output		Bank C single-ended clock outputs. LVCMOS/LVTTL interface levels.
22, 26	V_{DDOC}	Power		Bank C output supply pins.
29, 31, 33, 35	QB3, QB2, QB1, QB0	Output		Bank C single-ended clock outputs. LVCMOS/LVTTL interface levels.
30, 34	V_{DDOB}	Power		Bank B output supply pins.
37, 39, 41, 43	QA3, QA2, QA1, QA0	Output		Bank A single-ended clock outputs. LVCMOS/LVTTL interface levels.
38, 42	V_{DDOA}	Power		Bank B output supply pins.
45	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, $\overline{CLK1}$ inputs. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
46	$\overline{CLK1}$	Input	Pullup	Inverting differential clock input.
47	CLK1	Input	Pulldown	Non-inverting differential clock input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pull-up Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pull-down Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDOx} = 3.465V			18	pF
		V_{DD}, V_{DDOx} = 2.625V			12	pF
		V_{DD} = 3.465V, V_{DDOx} = 2.625V			20	pF
		V_{DD} = 3.465V, V_{DDOx} = 1.89V			30	pF
		V_{DD} = 2.625V, V_{DDOx} = 1.89V			14	pF
R_{OUT}	Output Impedance		5	7	12	Ω

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

Function Tables

Table 3. Function Table

Inputs			Outputs	
$\overline{MR/OE}$	CLK_ENx	DIV_SELx	Bank [A:D]	Qx Frequency
0	X	X	Hi-Z	N/A
1	1	0	Active	fIN/2
1	1	1	Active	fIN
1	0	X	LOW	N/A

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to $V_{DD\ Ox}$+ 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDOx} = 3.3V ± 5%, 2.5V ± 5%, 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current				100	mA
I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}	Output Supply Current				15	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDOx} = 2.5V ± 5%, 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}	Output Supply Voltage		2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current				95	mA
I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}	Output Supply Current				8	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		CLK_EN[A:D], DIV_SEL[A:D], MR/OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		CLK_EN[A:D], DIV_SEL[A:D], MR/OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOx} = 3.3V ± 5%	2.6			V
			V_{DDOx} = 2.5V ± 5%	1.8			V
			V_{DDOx} = 1.8V ± 5%; I_{OH} = -2mA	V_{DDOx} – 0.45			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOx} = 3.3V ± 5%			0.5	V
			V_{DDOx} = 2.5V ± 5%			0.5	V
			V_{DDOx} = 1.8V ± 5%; I_{OH} = 2mA			0.45	V
I_{OZL}	Output Hi-Z Current Low			-5			µA
I_{OZH}	Output Hi-Z Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOX}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 4D. Differential DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	$\overline{CLK1}$	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
		CLK1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	$\overline{CLK1}$	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for CLK1, $\overline{CLK1}$ is V_{DD} + 0.3V.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDOx} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.8	3.4	3.9	ns
		CLK1/$\overline{CLK1}$; NOTE 1B		2.75	3.4	4.1	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			50	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	200		700	ps
odc	Output Duty Cycle		f < 175MHz	45		55	%
			$f \geq$ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDOX}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDOx} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.9	3.8	4.7	ns
		CLK1/$\overline{CLK1}$; NOTE 1B		3.0	3.6	4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			70	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			210	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	150		700	ps
odc	Output Duty Cycle		$f \leq$ 125MHz	40		60	%
t_{pw}	Output Pulse Width		f > 125MHz	$t_{Period}/2 - 800$		$t_{Period}/2$ + 800	ps
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

For NOTES, please see above, Table 5A.

Table 5C. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDOx} = 2.5V ± 5%, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		2.9	3.5	4.0	ns
		CLK1/$\overline{CLK1}$; NOTE 1B		3.0	3.5	4.0	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			50	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	200		700	ps
odc	Output Duty Cycle		*f* < 175MHz	45		55	%
			f ≥ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

Table 5D. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDOx} = 1.8V ± 5%, T_A = -40°C to 85°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		3.0	3.9	4.7	ns
		CLK1/$\overline{CLK1}$; NOTE 1B		3.0	3.9	4.7	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			50	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			170	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	200		700	ps
odc	Output Duty Cycle		*f* < 175MHz	45		55	%
			f ≥ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

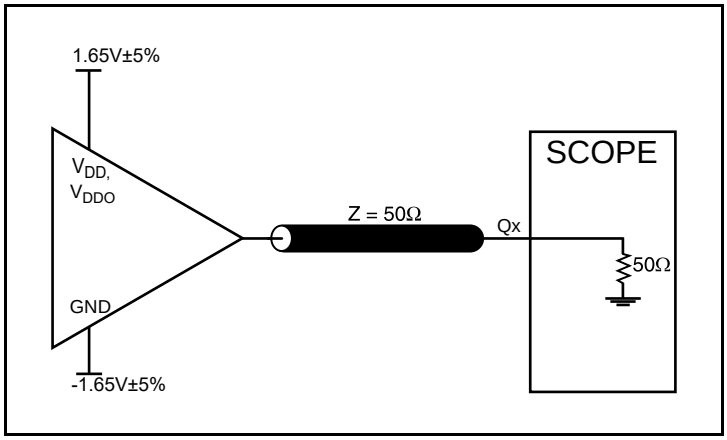
For NOTES, please see above, Table 5C.

Table 5E. AC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDOx} = 1.8V ± 5%, T_A = -40°C to 85°C

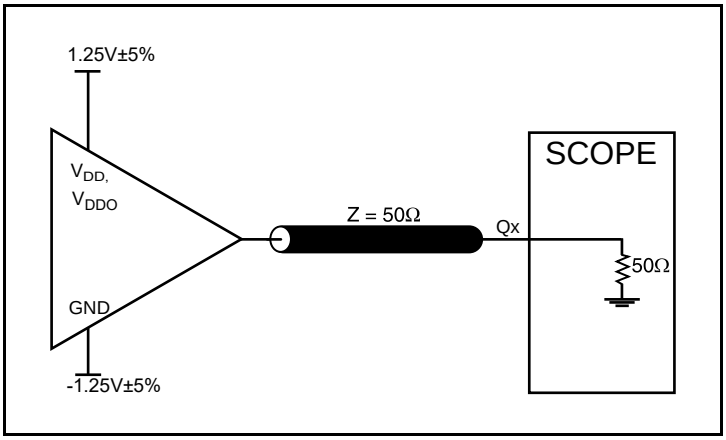
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High	CLK0; NOTE 1A		3.1	4.1	5.2	ns
		CLK1/$\overline{CLK1}$; NOTE 1B		3.0	3.9	4.7	ns
*t*sk(b)	Bank Skew; NOTE 2, 6		Measured on the Rising Edge			70	ps
*t*sk(o)	Output Skew; NOTE 3, 6		Measured on the Rising Edge			210	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6					800	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5		20% to 80%	150		700	ps
odc	Output Duty Cycle		*f* < 175MHz	45		55	%
			f ≥ 175MHz	40		60	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

All parameters measured at 250MHz unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDOX}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDOX}/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDOX}/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDOX}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

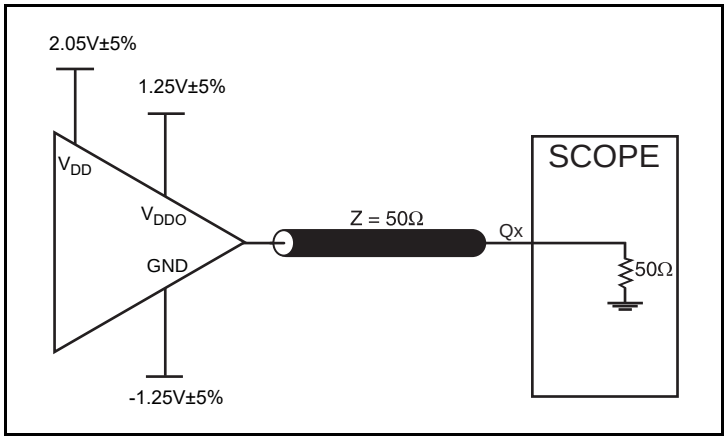
Parameter Measurement Information



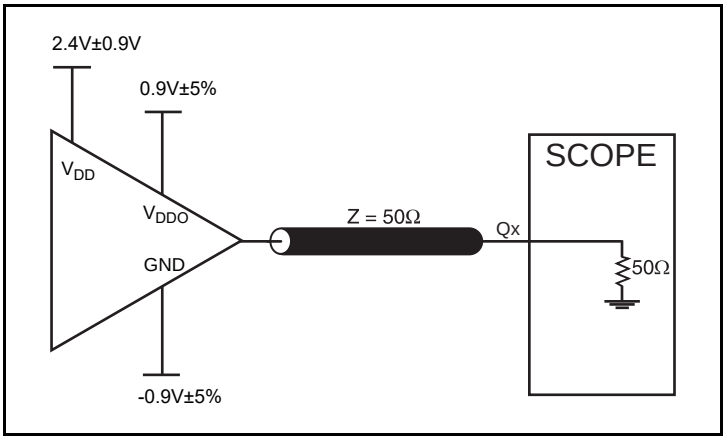
3.3V Core/3.3V LVCMOS Output Load Test Circuit



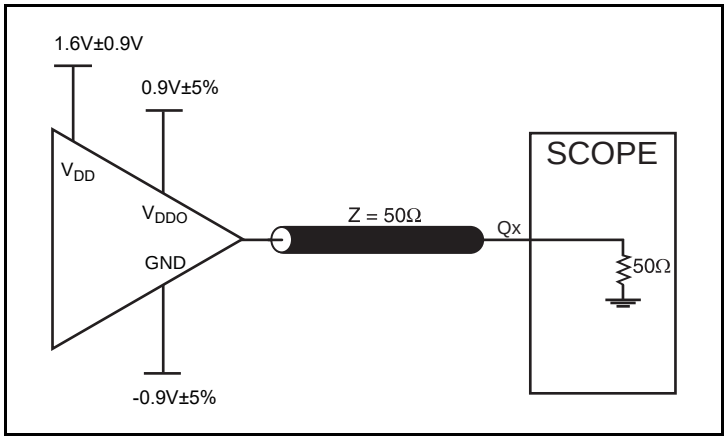
2.5V Core/2.5V LVCMOS Output Load Test Circuit



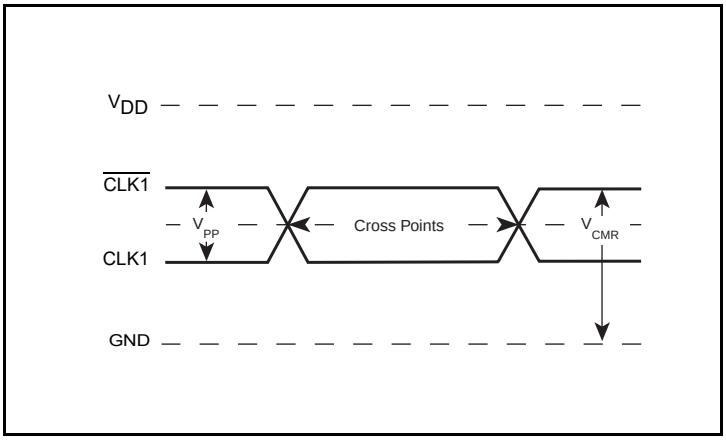
3.3V Core/2.5V LVCMOS Output Load Test Circuit



3.3V Core/1.8V LVCMOS Output Load Test Circuit

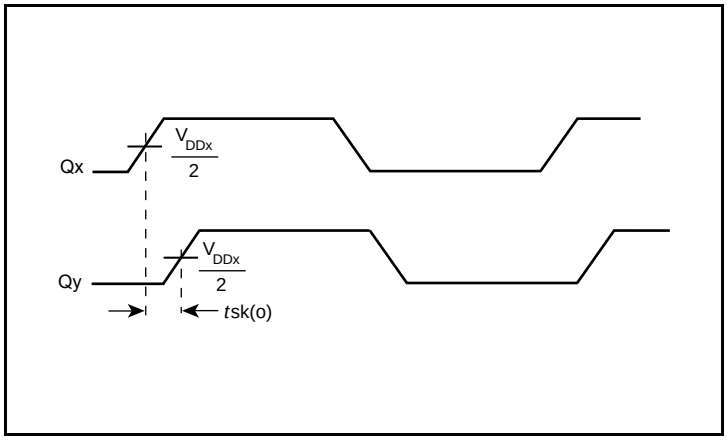


2.5V Core/1.8V LVCMOS Output Load Test Circuit

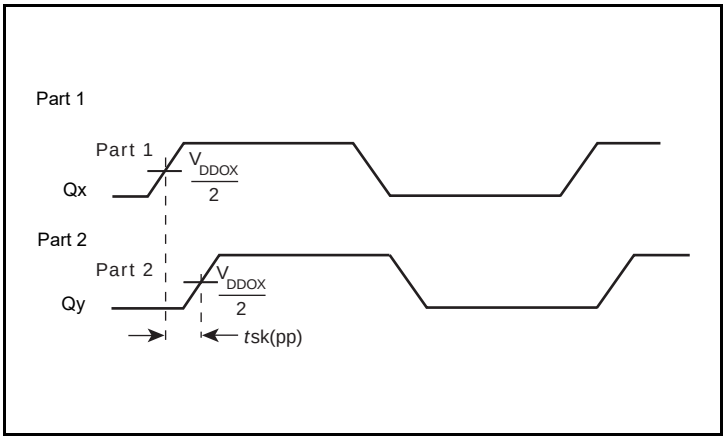


Differential Input Level

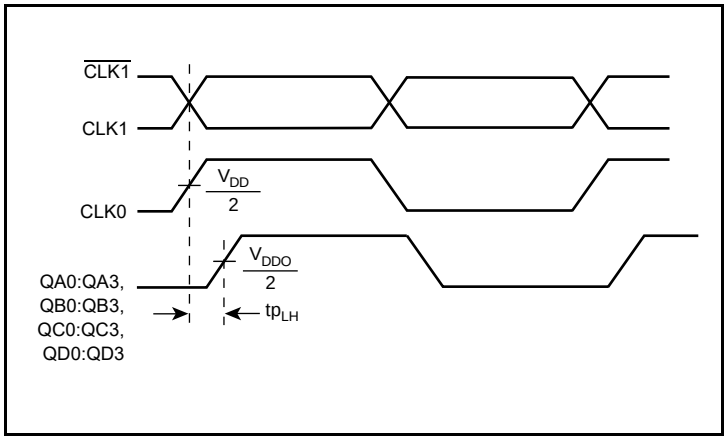
Parameter Measurement Information, continued



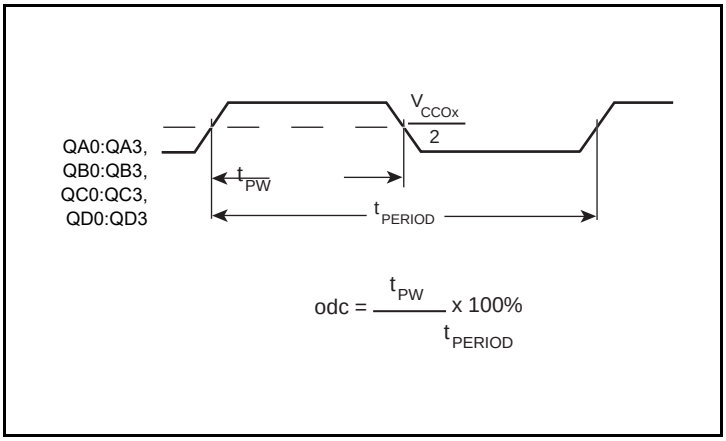
Output Skew



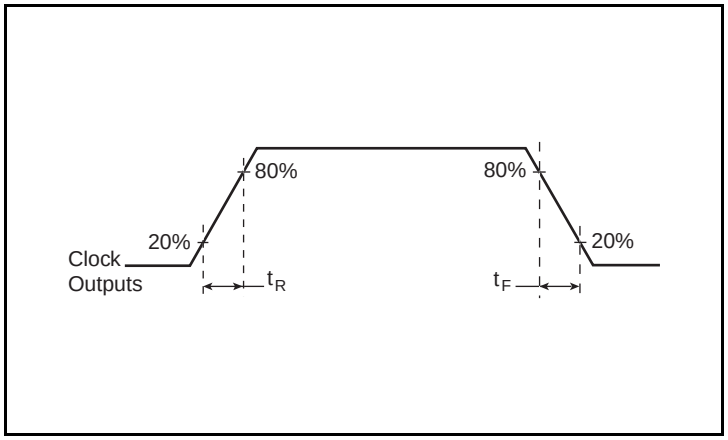
Part-to-Part Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

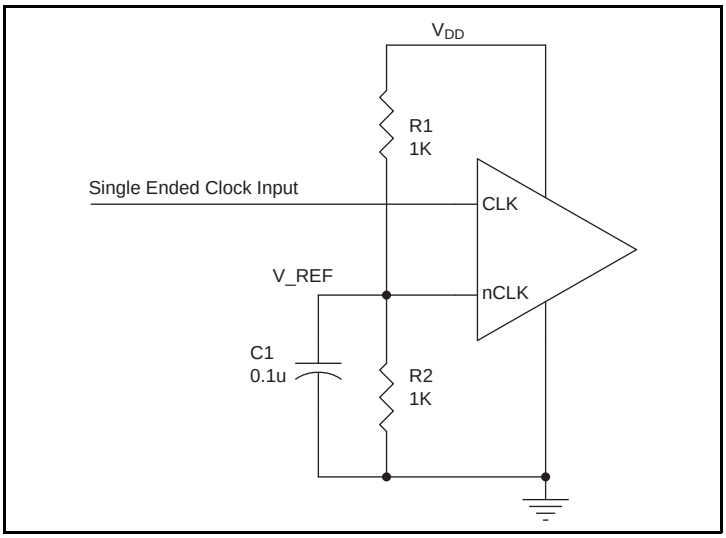


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs

CLK/$\overline{CLK}$ Inputs

For applications not requiring the use of the differential input, both CLK and $\overline{CLK}$ can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /$\overline{CLK}$ accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/$\overline{CLK}$ input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for Renesas LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

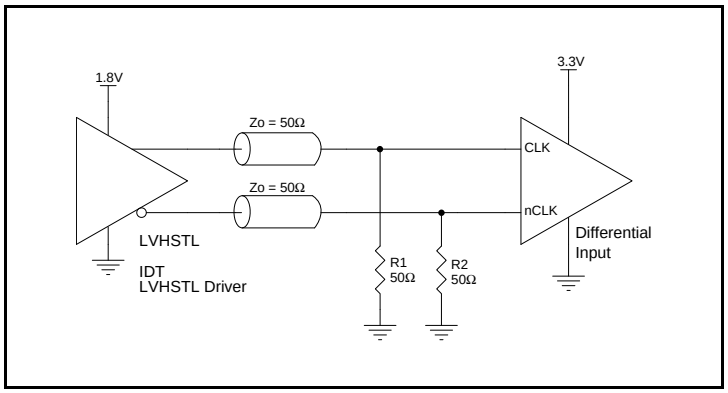


Figure 2A. CLK/$\overline{CLK}$ Input Driven by a Renesas LVHSTL Driver

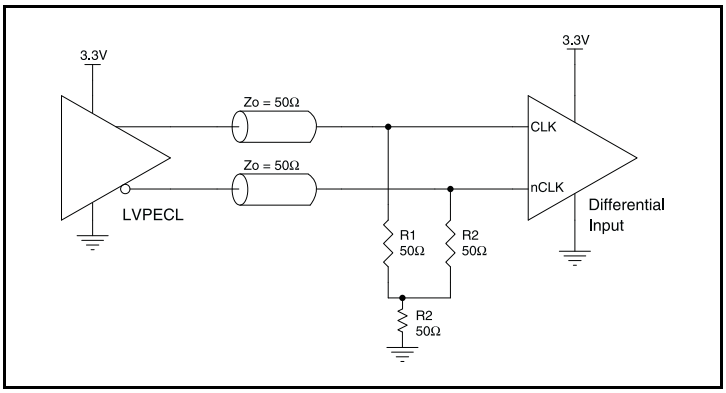


Figure 2B. CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

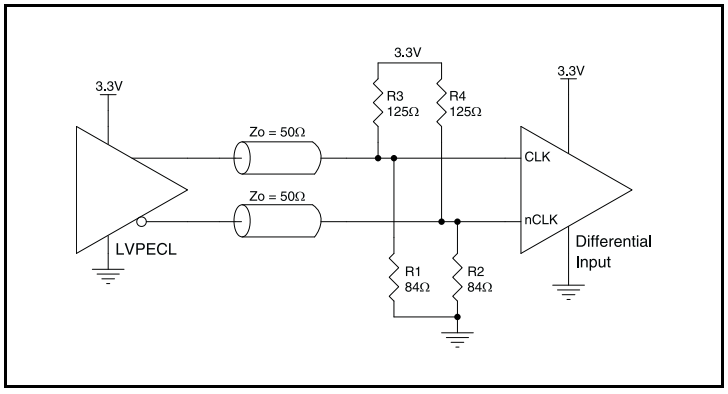


Figure 2C. CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

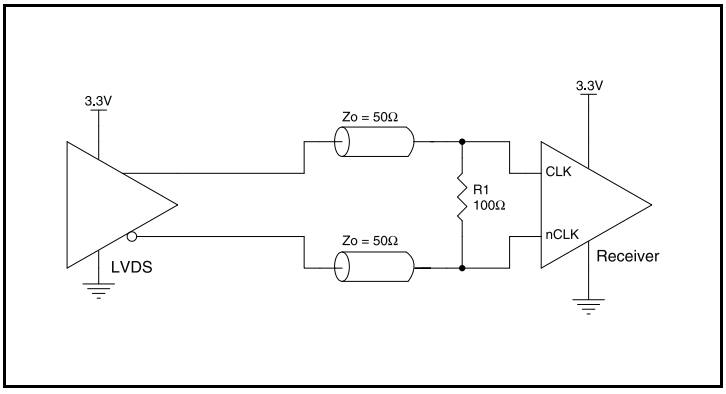


Figure 2D. CLK/$\overline{CLK}$ Input Driven by a 3.3V LVDS Driver

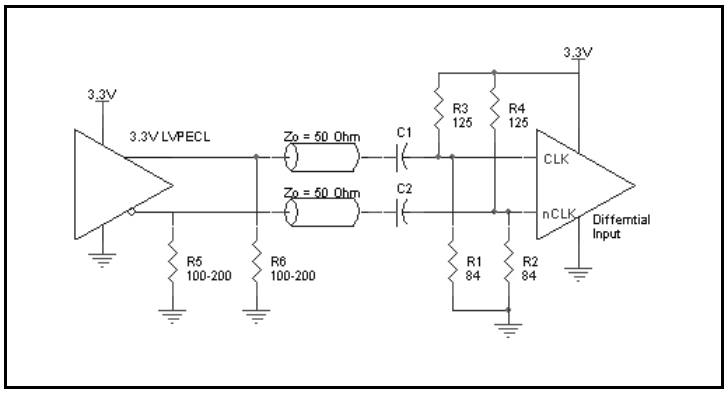


Figure 2E. CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver with AC Couple

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 48-LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 87016I is: 2034

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/cpt/prprg-package-outline-70-x-70-x-14-mm-tqfp-10010-form

Ordering Information

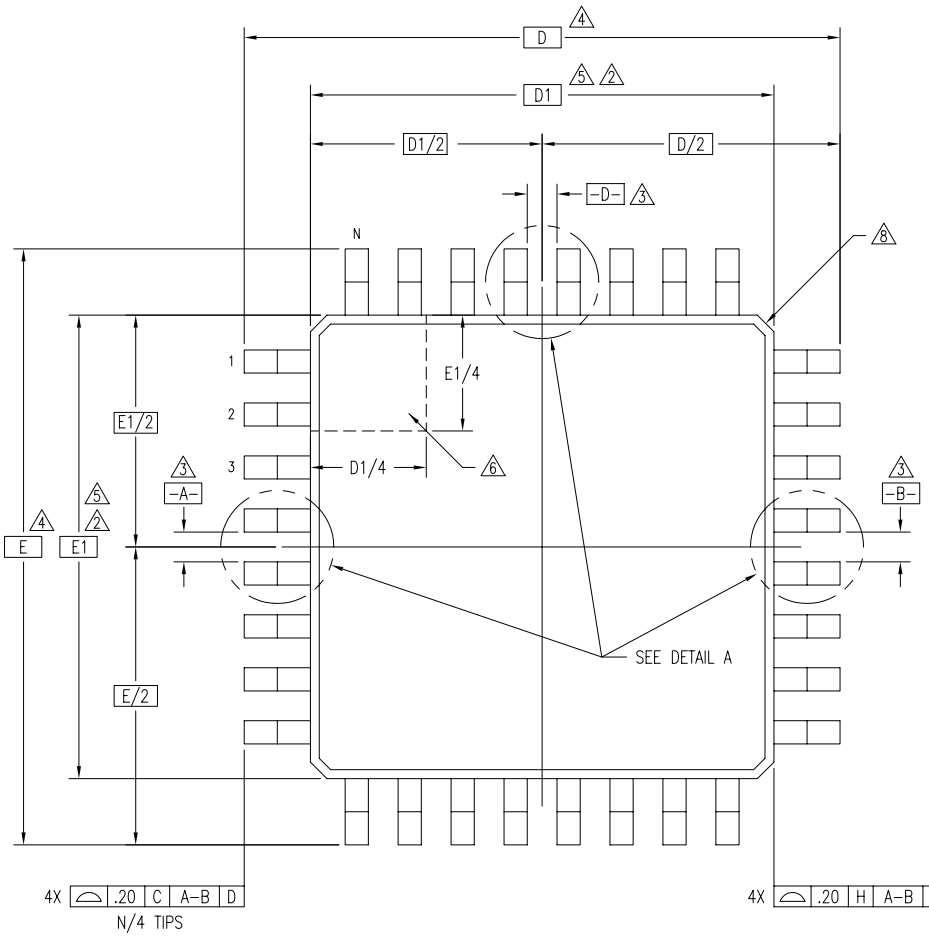
Table 8. Ordering Information

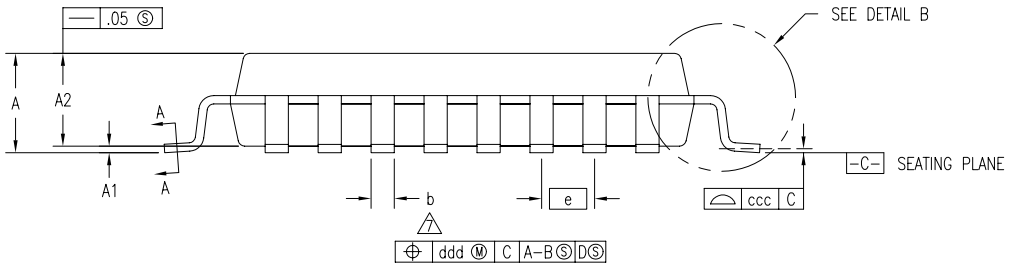
Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87016AYILF	ICS87016AYIL	“Lead-Free” 48 Lead LQFP	Tray	-40°C to 85°C
ICS87016AYILFT	ICS87016AYIL	“Lead-Free” 48 Lead LQFP	Tape & Reel	-40°C to 85°C

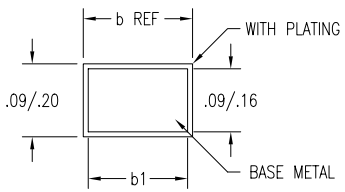
Revision History

Date	Description of Change
January 22, 2020	• Updated package outline drawings section; added link. • Updated logos and footer information.
March 23, 2015	Ordering Information - updated part marking. Updated datasheet format.
March 28, 2013	Corrected typo, VOH: V_{DD} – 0.45 to V_{DDOx} – 0.45
November 15, 2012	Remove leaded parts from Ordering Information table.
May 25, 2007	2.5V AC Characteristics Table - changed *Output Duty Cycle* test condition and limits. Added Output Pulse Width.
March 30, 2007	Features Section - added 2.5V/2.5V and 2.5V/1.8V to supply mode bullet. Added lead-free bullet. Pin Characteristics Table - added 2.5V/2.5V and 2.5V/1.8V to C_{PD}. Added 2.5V Power Supply DC Characteristics Table. LVCMOS DC Characteristics Table - added 2.5V to V_{IH}/V_{IL}. Differential DC Characteristics Table - added 2.5V to I_{IH}/I_{IL}. Added 2.5V Power Supply DC Characteristics Table. Added 2.5V/1.8V Power Supply DC Characteristics Table. Parameter Measurement Information - added *2.5V Core/2.5V Output Load Test Circuit* and *2.5V Core/1.8V Output Load Test Circuit diagrams.* Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free Order/Part Number.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/15/95	TU VU
01	ADD "GREEN" PRG NOMENCLATURE	10/08/04	TU VU
02	ADDED 48 LEAD	10/13/06	PKP
03	ADDED PACKAGE CODE	12/12/12	RC

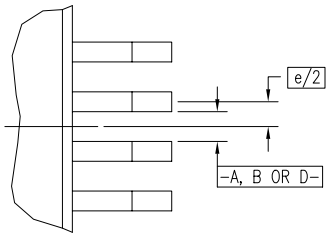




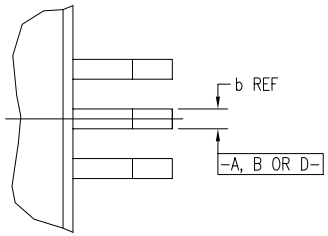


SECTION A-A

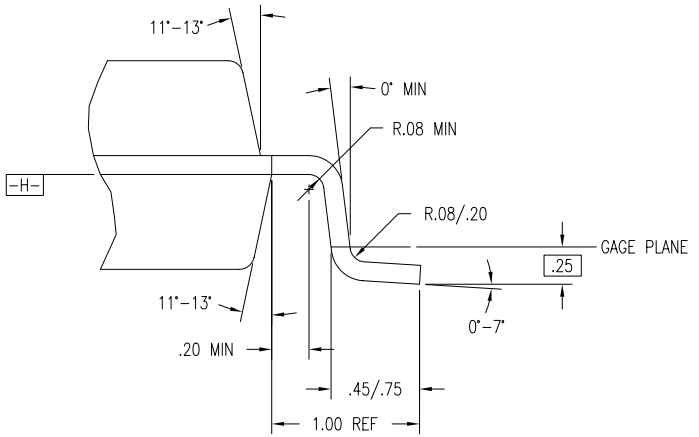
EVEN LEAD SIDES



ODD LEAD SIDES



DETAIL A



DETAIL B

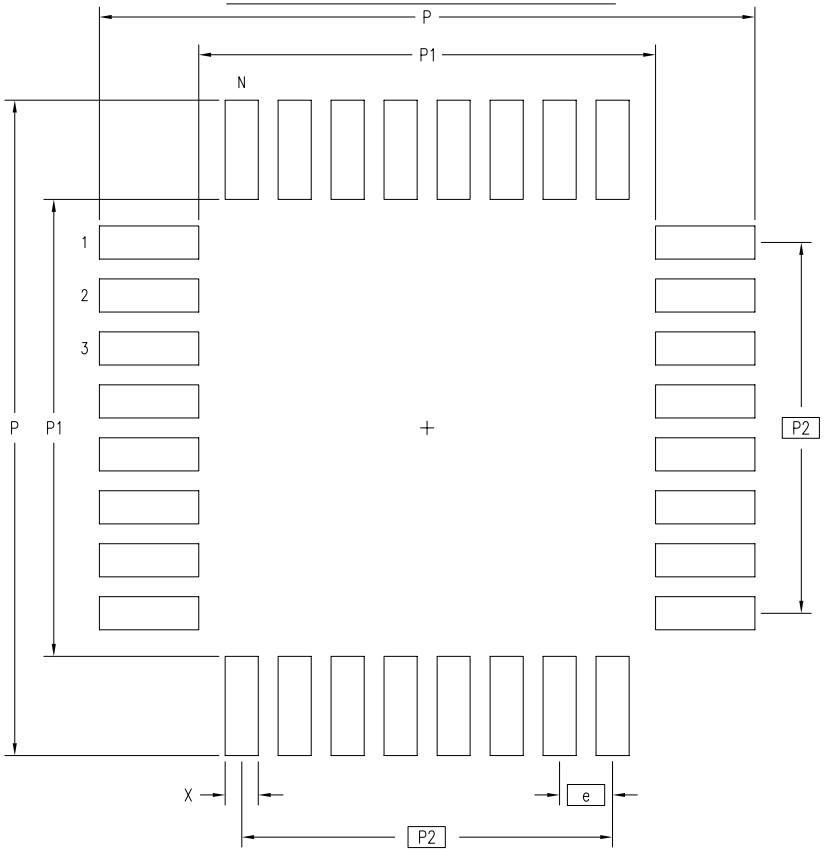
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572	
APPROVALS	DATE	TITLE: PR/PRG PACKAGE OUTLINE 7.0 X 7.0 X 1.4 mm TQFP 1.00/.10 FORM	
DRAWN TU	10/15/95		
CHECKED			
		SIZE: C	DRAWING No.: PSC-4052
		REV: 03	
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/15/95	TU VU
01	ADD "GREEN" PRG NOMENCLATURE	10/08/04	TU VU
02	ADDED 48 LEAD	10/13/06	PKP
03	ADDED PACKAGE CODE	12/12/12	RC

PR/PRG32				
SYMBOL	JEDEC VARIATION BBA			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	32			
e	.80 BSC			
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	–	–	.10	
ddd	–	–	.20	

PR/PRG48				
SYMBOL	JEDEC VARIATION BBC			NOTE
	MIN	NOM	MAX	
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	9.00 BSC			4
D1	7.00 BSC			5,2
E	9.00 BSC			4
E1	7.00 BSC			5,2
N	48			
e	.50 BSC			
b	.17	.22	.27	7
b1	.17	.20	.23	
ccc	–	–	.08	
ddd	–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.60 BSC	
X	.40	.60
e	.80 BSC	
N	32	

	MIN	MAX
P	9.80	10.00
P1	6.80	7.00
P2	5.50 BSC	
X	.25	.35
e	.50 BSC	
N	48	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026, VARIATIONS BBA & BBC.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

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San Jose, CA 95138
PHONE: (408) 284–8200
FAX: (408) 284–3572

APPROVALS	DATE
DRAWN TU	10/15/95
CHECKED	

TITLE: PR/PRG PACKAGE OUTLINE 7.0 X 7.0 X 1.4 mm TQFP 1.00/.10 FORM

SIZE	DRAWING No.	REV
C	PSC–4052	03

DO NOT SCALE DRAWING | SHEET 2 OF 2

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(Rev.1.0 Mar 2020)

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